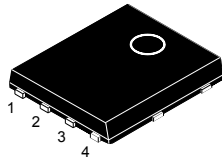
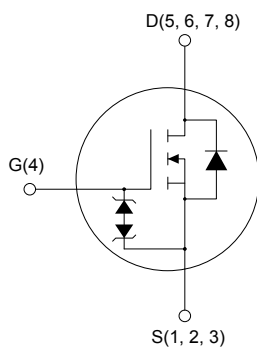


## N-channel 600 V, 330 mΩ typ., 7 A, MDmesh M6 Power MOSFET in a PowerFLAT 5x6 HV package


**PowerFLAT 5x6 HV**


AM15540v7


**Product status link**
[STL13N60M6](#)
**Product summary**

<b>Order code</b>	STL13N60M6
<b>Marking</b>	13N60M6
<b>Package</b>	PowerFLAT™ 5x6 HV
<b>Packing</b>	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL13N60M6	600 V	415 mΩ	7 A	52 W

- Reduced switching losses
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters
- Boost PFC converters

### Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	7	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	4.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total power dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	52	W
$I_{AR}^{(2)}$	Avalanche current, repetitive or not repetitive	2	A
$E_{AS}^{(3)}$	Single pulse avalanche energy	140	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(5)}$	MOSFET $dv/dt$ ruggedness	100	
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. Pulse width limited by  $T_{jmax}$ .
3. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .
4.  $I_{SD} \leq 7\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
5.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.4	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup>			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 3.5\text{ A}$		330	415	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance		-	509	-	$\text{pF}$
$C_{\text{oss}}$	Output capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	34.4	-	
$C_{\text{riss}}$	Reverse transfer capacitance		-	4.2	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	94	-	$\text{pF}$
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	5.6	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 480\text{ V}$ , $I_{\text{D}} = 10\text{ A}$ , $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	13	-	$\text{nC}$
$Q_{\text{gs}}$	Gate-source charge		-	3.4	-	
$Q_{\text{gd}}$	Gate-drain charge		-	6.4	-	

1.  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 5\text{ A}$ , $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$	-	15.8	-	$\text{ns}$
$t_{\text{r}}$	Rise time		-	6.5	-	
$t_{\text{d(off)}}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	25.5	-	
$t_{\text{f}}$	Fall time		-	9.4	-	

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 7\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$	-	182		ns
$Q_{rr}$	Reverse recovery charge		-	1.35		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	14.8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	253		ns
$Q_{rr}$	Reverse recovery charge		-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	16	

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

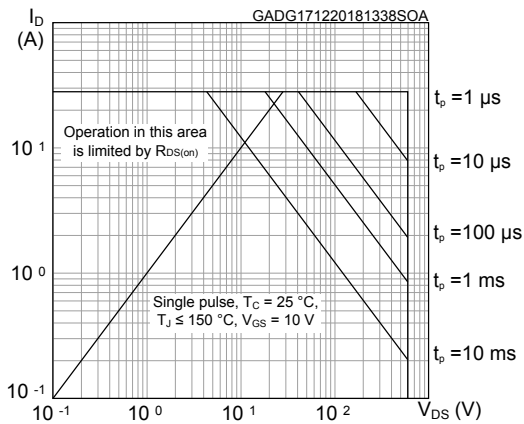


Figure 2. Thermal impedance

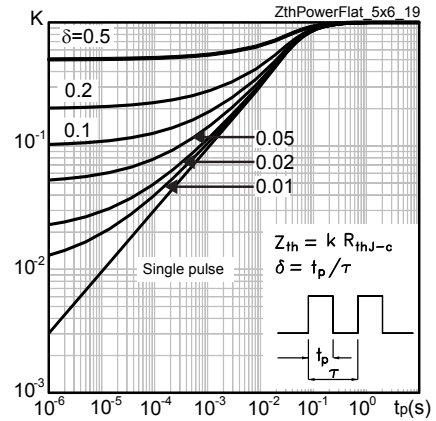


Figure 3. Output characteristics

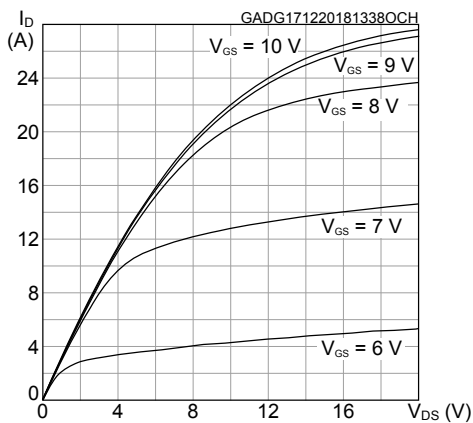


Figure 4. Transfer characteristics

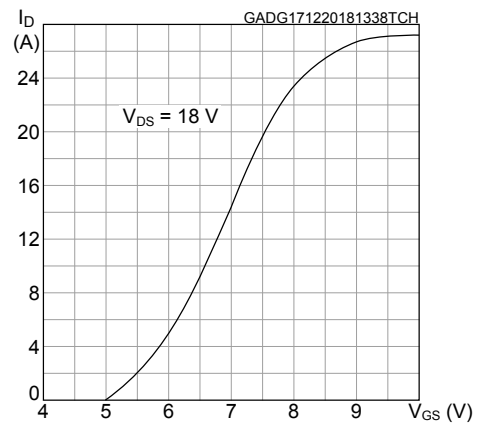


Figure 5. Gate charge vs gate-source voltage

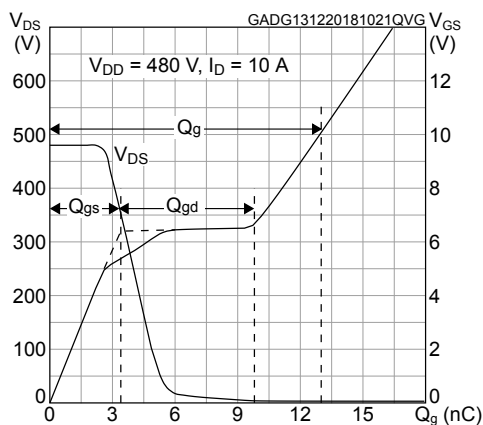


Figure 6. Static drain-source on-resistance

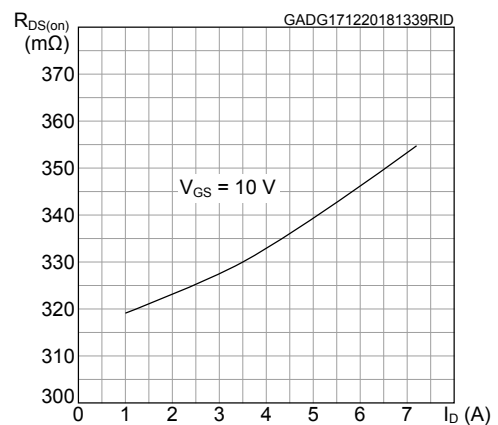


Figure 7. Capacitance variations

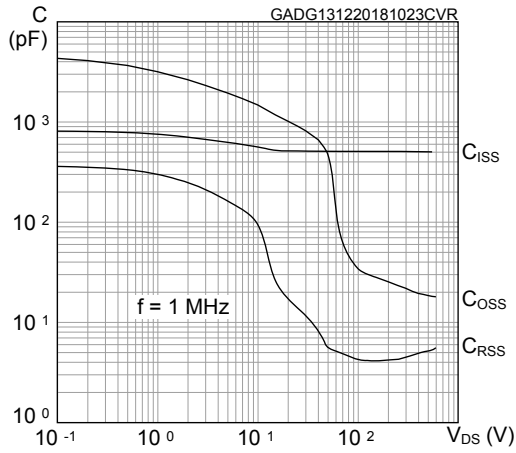


Figure 8. Output capacitance stored energy

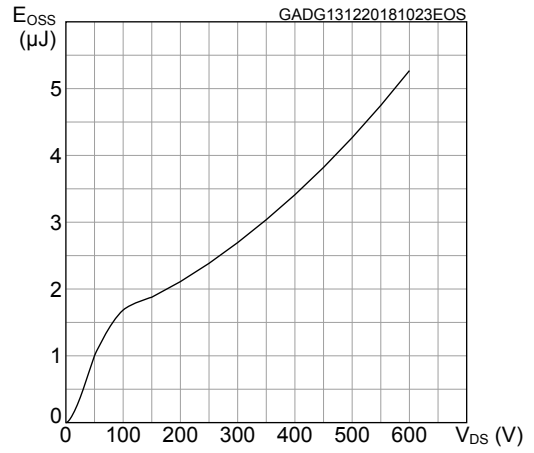


Figure 9. Normalized gate threshold voltage vs temperature

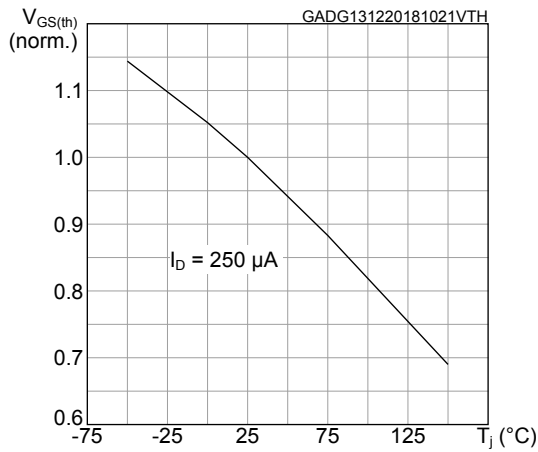


Figure 10. Normalized on-resistance vs temperature

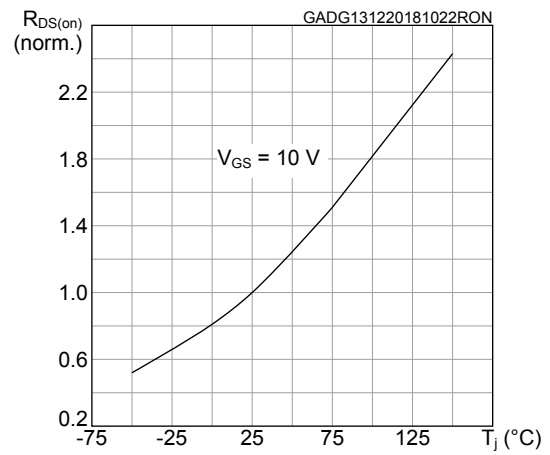


Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature

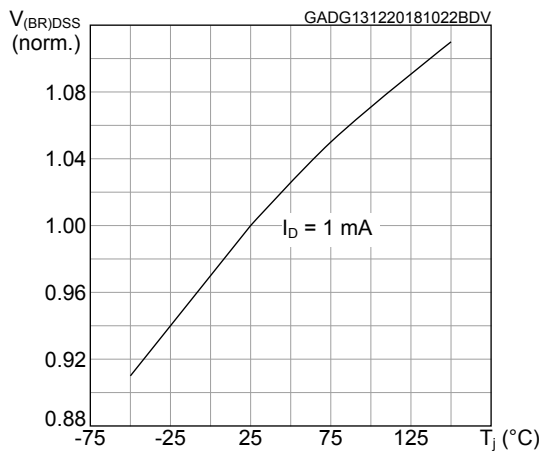
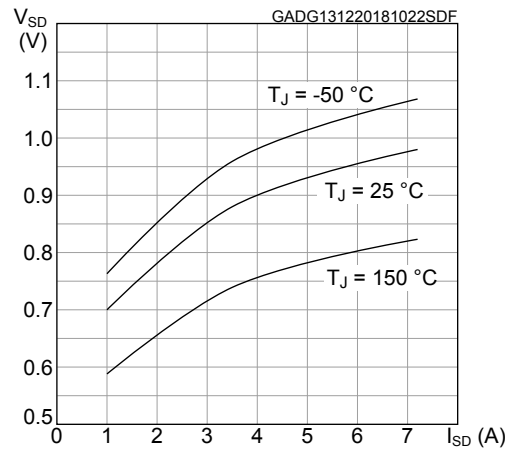


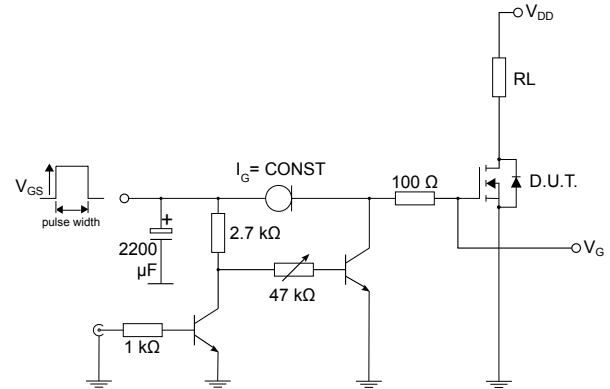
Figure 12. Source-drain diode forward characteristics



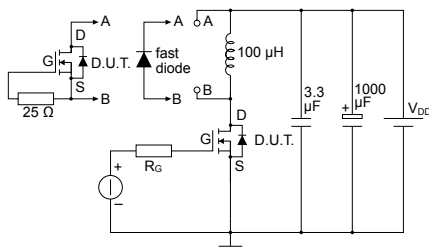
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

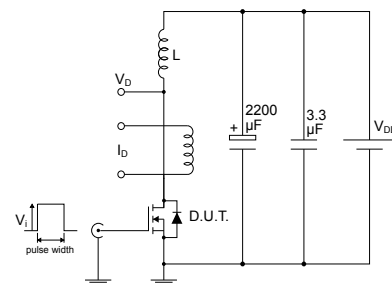

AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


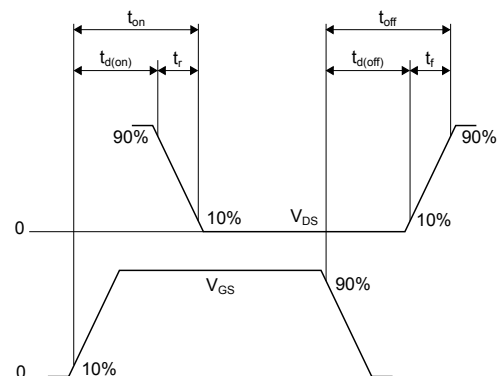
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

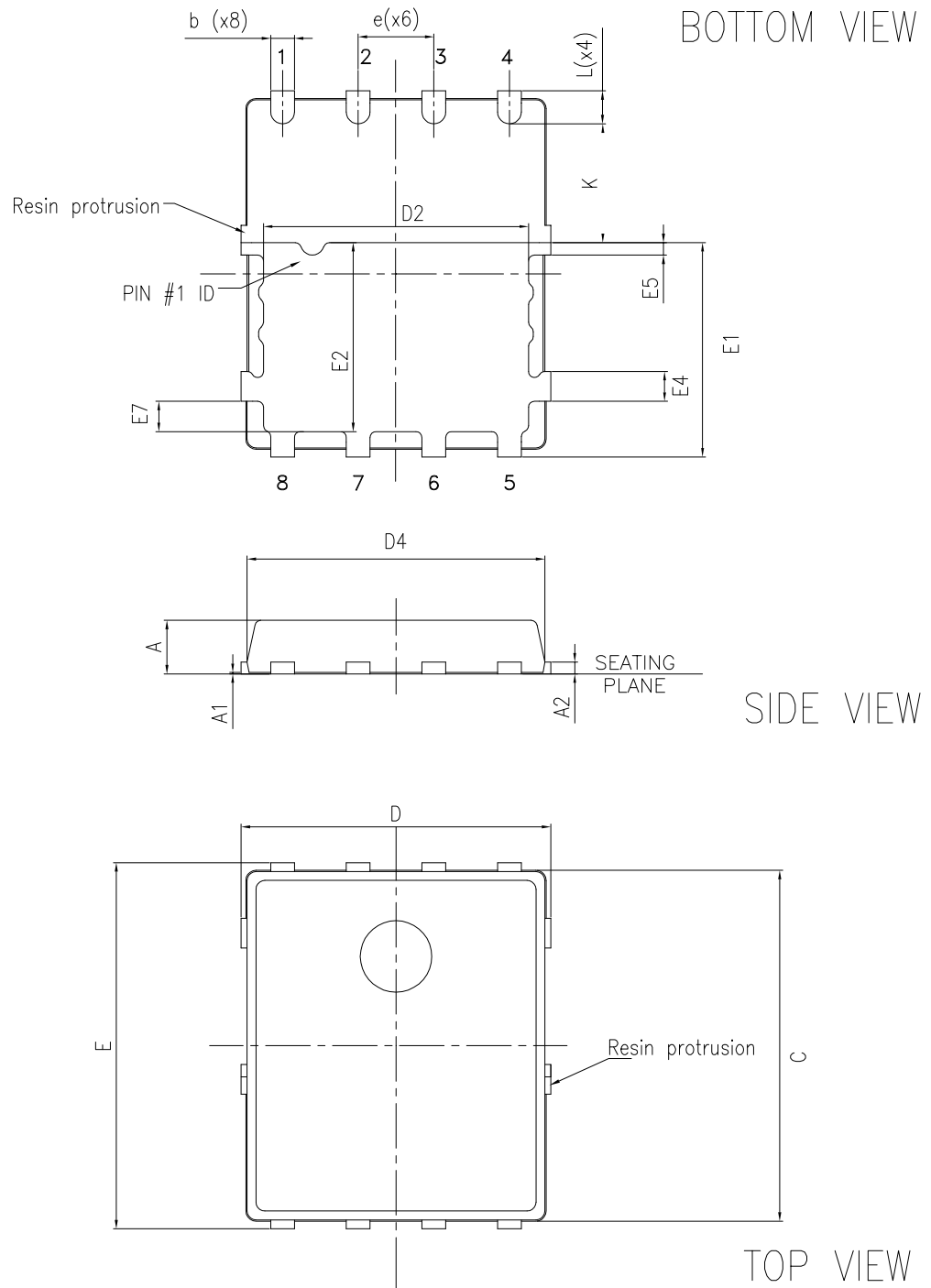
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 PowerFLAT 5x6 HV package information

Figure 19. PowerFLAT 5x6 HV package outline

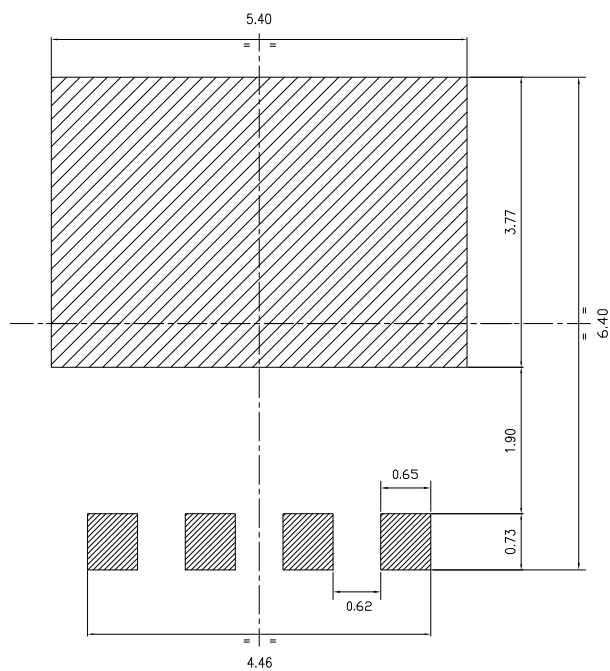


8368143\_Rev\_4

**Table 7. PowerFLAT 5x6 HV mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

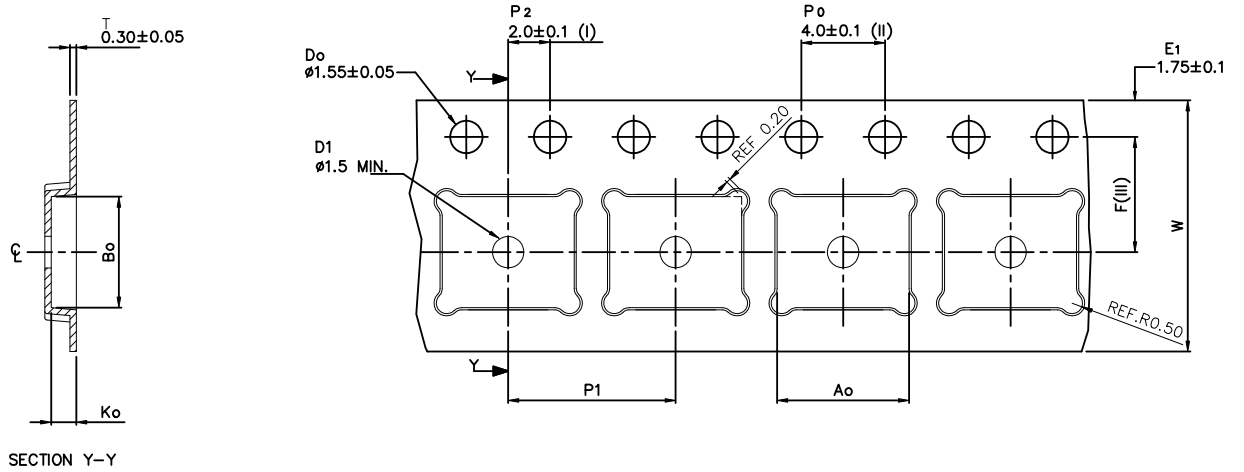
**Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)**



8368143\_Rev\_4\_footprint

## 4.2 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



$A_0$	$6.30 \pm 0.1$
$B_0$	$5.30 \pm 0.1$
$K_0$	$1.20 \pm 0.1$
$F$	$5.50 \pm 0.1$
$P_1$	$8.00 \pm 0.1$
$W$	$12.00 \pm 0.3$

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

8234350\_Tape\_rev\_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

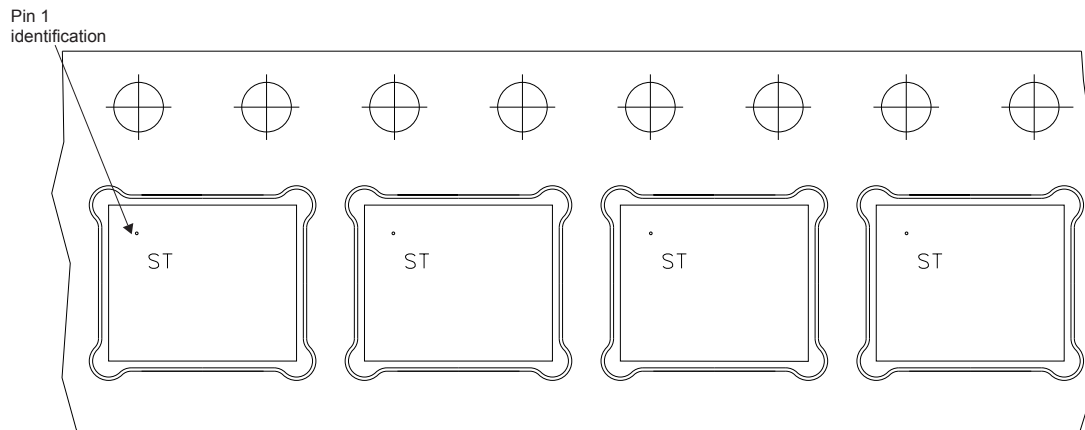
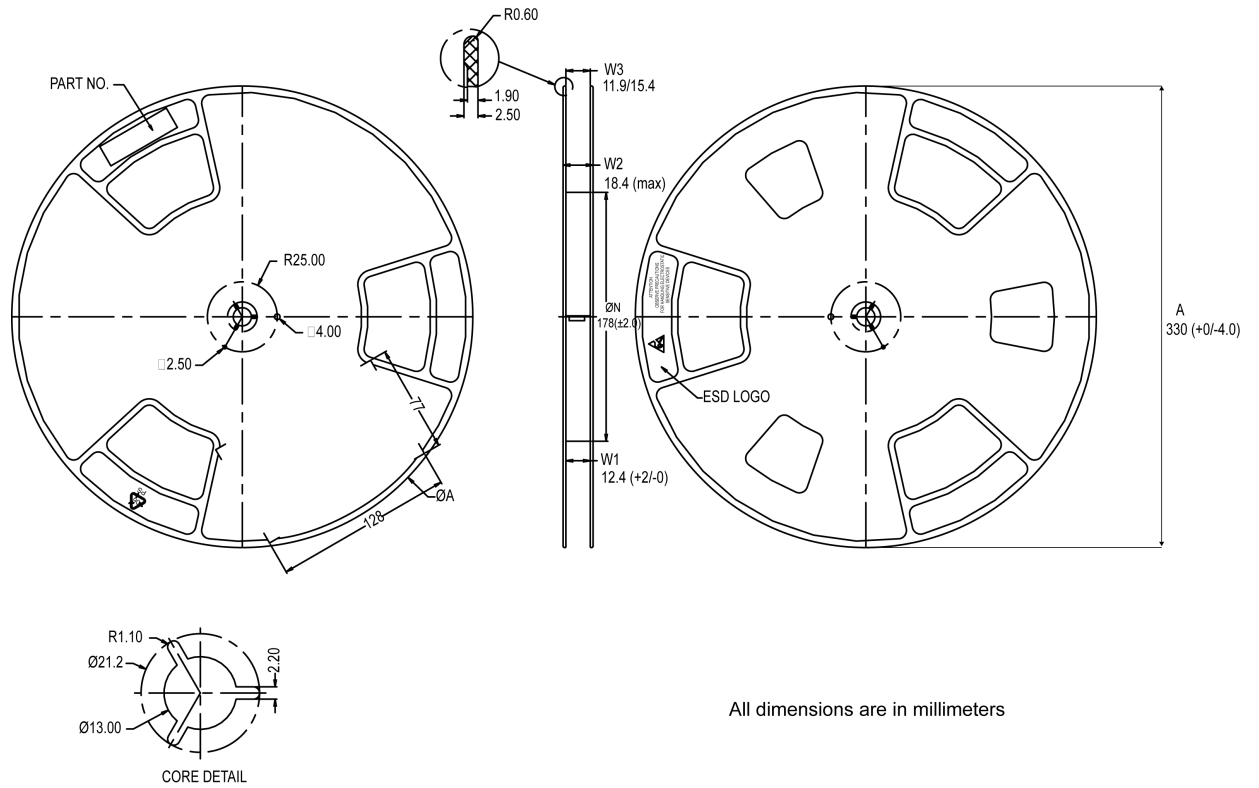


Figure 23. PowerFLAT 5x6 reel



All dimensions are in millimeters

8234350\_Reel\_rev\_C

## Revision history

**Table 8. Document revision history**

Date	Version	Changes
18-Dec-2018	1	First release.
20-May-2019	2	Updated <a href="#">Table 3. Static</a> . Updated <a href="#">Figure 14. Test circuit for gate charge behavior</a> . Minor text changes.

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