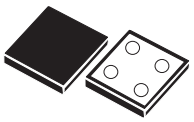
LD39115J

150 mA low quiescent current low noise voltage regulator

Datasheet - production data



Flip-chip 4

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low dropout voltage (80 mV typ. at 100 mA load)
- Very low quiescent current (20 µA typ. at no load, 35 µA typ. at 150 mA load, 1 µA max in off mode)
- Very low noise (33 μV_{RMS} from 1 kHz to 100 kHz at V_{OUT} = 1.8 V)
- Output voltage tolerance: ± 2.0 % @ 25 °C
- 150 mA guaranteed output current
- Wide range of output voltages available on request: 0.8 V to 4.5 V with 100 mV step
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor C_{OUT} = 1 µF
- Internal current and thermal limit
- Flip-chip 4 bumps 0.8 x 0.8 mm. pitch 0.4 mm
- Temperature range: -40 °C to 125 °C

Applications

- Mobile phones
- Personal digital assistants (PDAs)
- Cordless phones and similar battery-powered systems

Description

The LD39115J provides 150 mA maximum current from an input voltage ranging from 1.5 V to 5.5 V with a typical dropout voltage of 80 mV. It is stabilized with a ceramic capacitor. The ultra low drop voltage, low quiescent current and low noise features make it suitable for low power battery-powered applications. Power supply rejection is 65 dB at low frequencies and starts to roll off at 10 kHz. An enable logic control function puts the LD39115J in shutdown mode allowing a total current consumption lower than 1 µA. The device also includes a short-circuit constant current limiting and thermal protection.

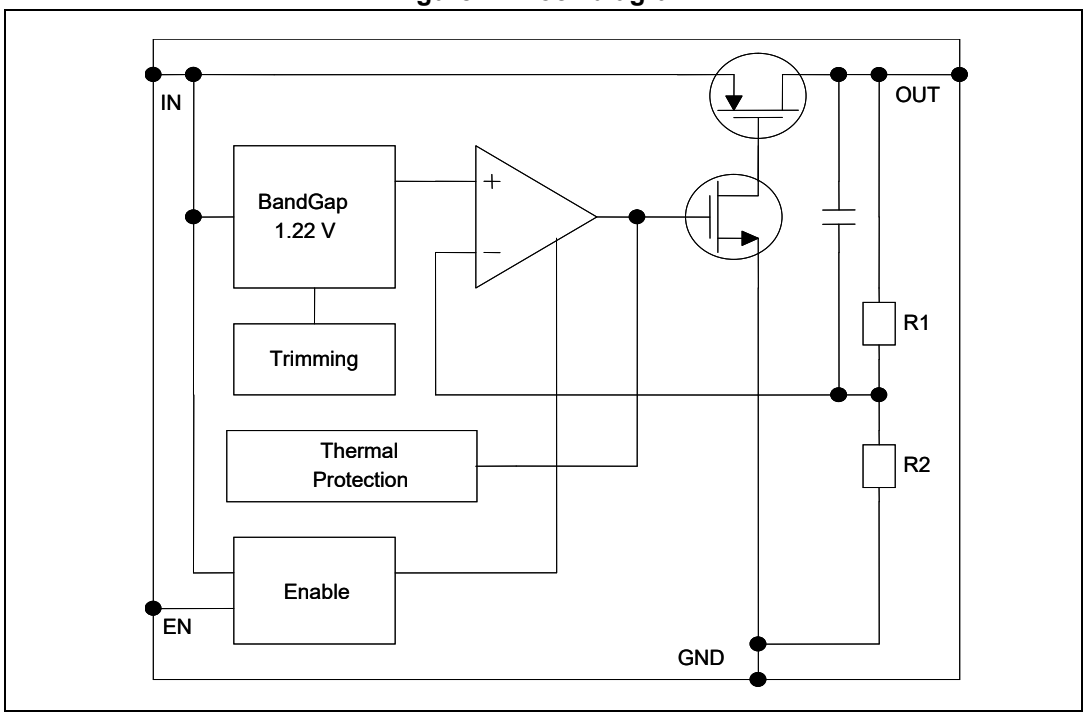
Table 1. Device summary

Order codes	Output voltages
LD39115J12R	1.2 V
LD39115J14R	1.4 V
LD39115J15R	1.5 V
LD39115J18R	1.8 V
LD39115J25R	2.5 V
LD39115J28R	2.8 V
LD39115J30R	3.0 V
LD39115J33R	3.3 V

Contents

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connection (top view)

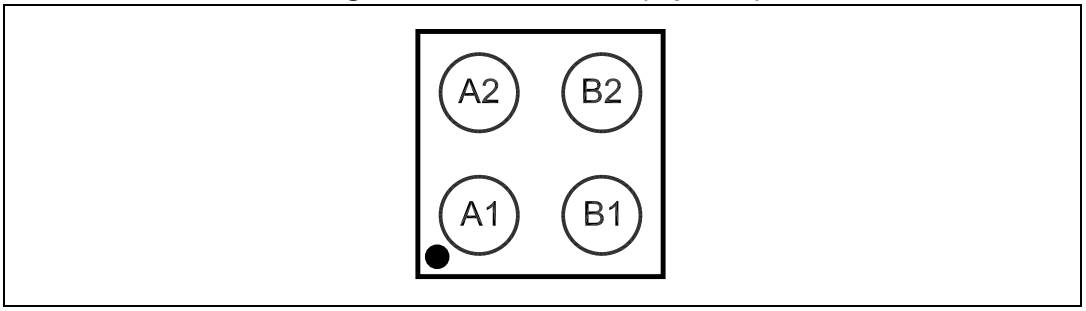
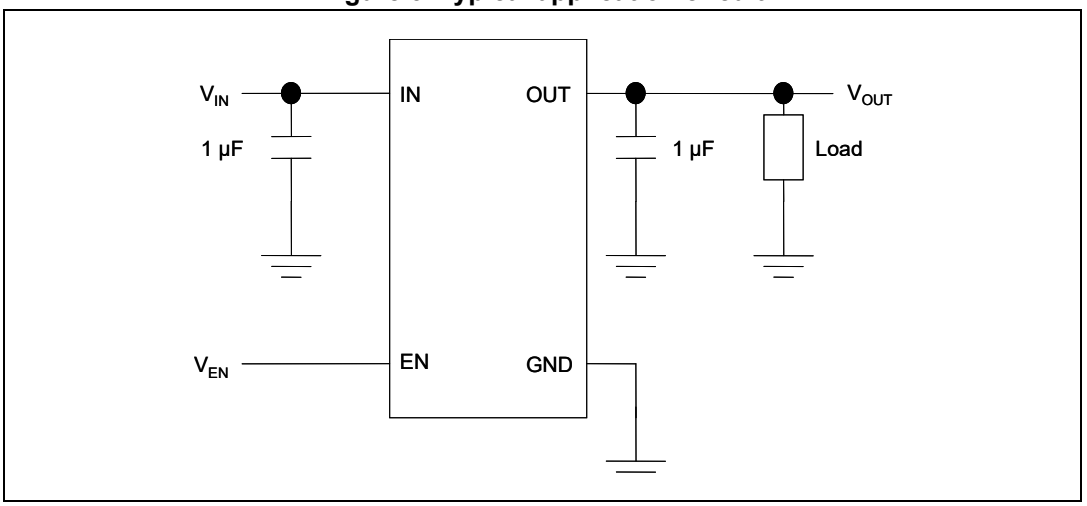


Table 2. Pin description

Pin n°	Symbol	Function
A2	EN	Enable pin logic input: Low = shutdown, High = active
A1	GND	Common ground
B2	IN	Input voltage of the LDO
B1	OUT	Output voltage

3 Typical application

Figure 3. Typical application circuit



4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 6	V
V_{OUT}	DC output voltage	- 0.3 to V_I + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to V_I + 0.3	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	180	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	4	kV

5 Electrical characteristics

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 6. Electrical characteristics for LD39115J (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{UVLO}	Turn-on threshold			1.45	1.48	V
	Turn-off threshold		1.30	1.35		mV
V_{OUT}	V_{OUT} accuracy	V_{OUT} > 1.5 V, I_{OUT} = 1 mA, T_J = 25 °C	-2.0		2.0	%
		V_{OUT} > 1.5 V, I_{OUT} = 1 mA, -40 °C < T_J < 125 °C	-3.0		3.0	%
		V_{OUT} ≤ 1.5 V, I_{OUT} = 1 mA		±10		mV
		V_{OUT} ≤ 1.5 V, I_{OUT} = 1 mA, -40 °C < T_J < 125 °C		±30		mV
ΔV_{OUT}	Static line regulation	V_{OUT} +1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (2)	ΔV_{IN} = +500 mV, I_{OUT} = 1 mA, T_R = T_F = 5 µs		10		mVpp
ΔV_{OUT}	Static load regulation	I_{OUT} = 1 mA to 150 mA		0.002		%/mA
ΔV_{OUT}	Transient load regulation (2)	I_{OUT} = 1 mA to 150 mA, t_R = t_F = 5 µs		40		mVpp
V_{DROP}	Dropout voltage (3)	I_{OUT} = 100 mA, V_{OUT} > 1.5 V -40 °C < T_J < 125 °C		80	110	mV
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 10 mA		30		$\mu V_{RMS}/V$
SVR	Supply voltage rejection V_{OUT} = 1.5 V	V_{IN} = V_{OUTNOM} +1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.1 V Freq. = 1 kHz I_{OUT} = 10 mA		74		dB
		V_{IN} = V_{OUTNOM} + 0.5 V +/- V_{RIPPLE} V_{RIPPLE} = 0.1 V Freq. = 10 kHz I_{OUT} = 10 mA		67		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA, -40 °C < T_J < 125 °C			50	
		I_{OUT} = 0 to 150 mA		35		
		I_{OUT} = 0 to 150 mA, -40 °C < T_J < 125 °C			70	
		V_{IN} input current in OFF MODE: V_{EN} = GND		0.001	1	

Table 6. Electrical characteristics for LD39115J (continued)(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SC}	Short circuit current	R_L = 0	200			mA
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V, -40 °C < T_J < 125 °C			0.4	V
	Enable input logic high	V_{IN} = 1.5 V to 5.5 V, -40 °C < T_J < 125 °C	0.9			
I_{EN}	Enable pin input current	V_{SHDN} = V_{IN}		0.1	100	nA
T_{ON}	Turn on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see *Section 6: Typical performance characteristics*)	1		22	µF

1. For $V_{OUT(NOM)}$ < 1.2 V, V_{IN} = 1.5 V.
2. All transient values are guaranteed by design, not production tested.
3. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V.
4. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95 % of its nominal value.

6 Typical performance characteristics

$C_{IN} = C_{OUT} = 1\ \mu F$, V_{EN} to V_{IN}.

Figure 4. Output voltage vs. temperature (V_{OUT} = 1.2 V)

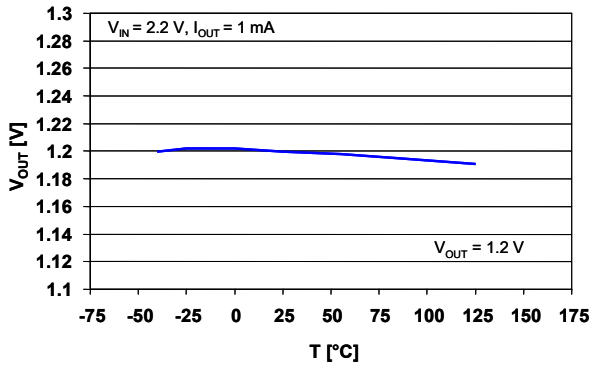


Figure 5. Output voltage vs. temperature (V_{OUT} = 2.8 V)

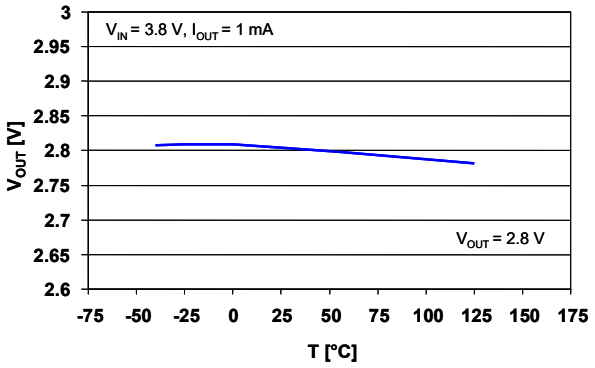


Figure 6. Line regulation vs. temperature

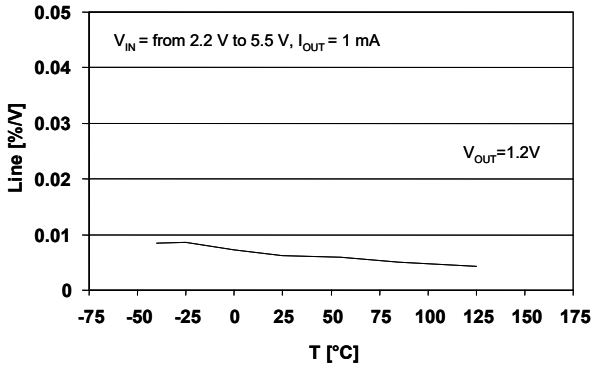


Figure 7. Load regulation vs. temperature

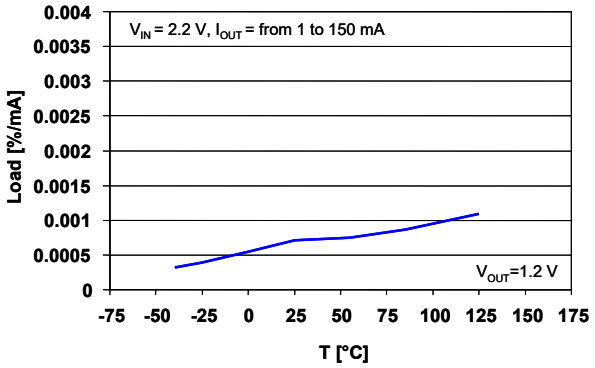


Figure 8. Short-circuit current vs. drop voltage

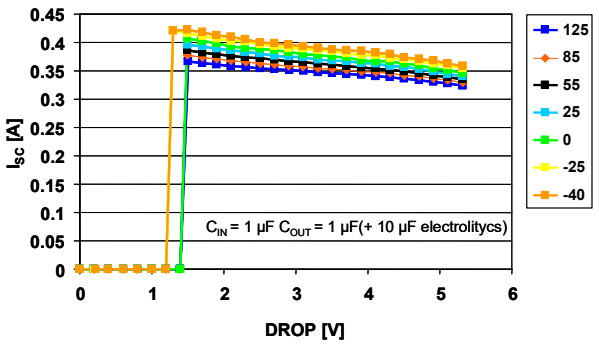


Figure 9. Dropout voltage vs. temperature

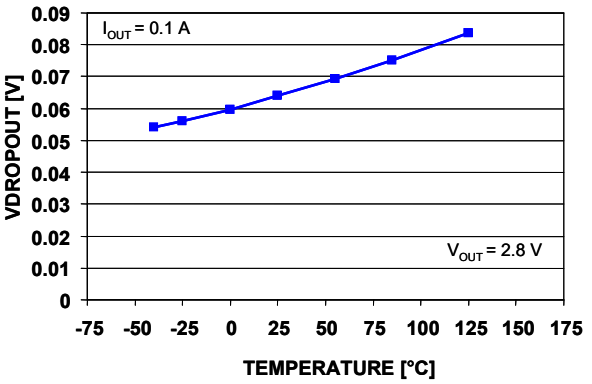


Figure 10. Dropout voltage vs. output current

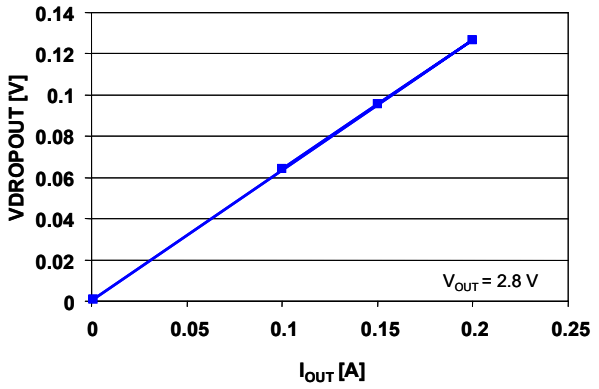


Figure 11. Output voltage vs. input voltage (V_{OUT} = 1.3 V)

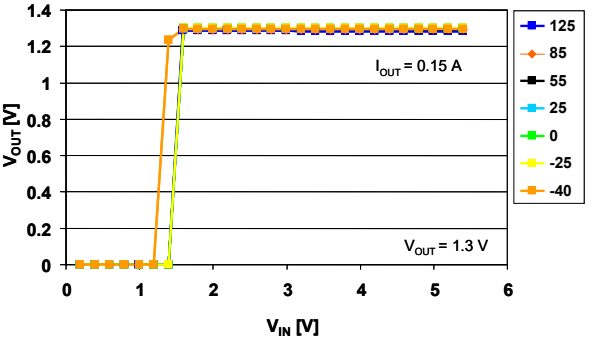


Figure 12. Output voltage vs. input voltage (V_{OUT} = 2.8 V)

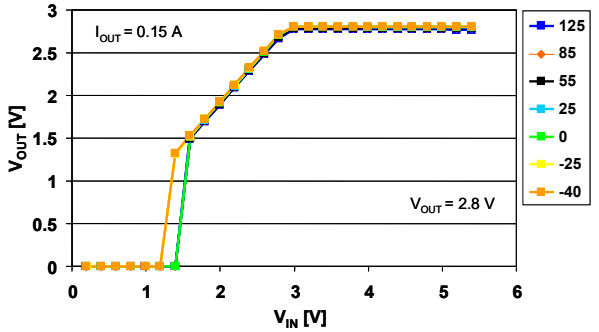


Figure 13. Enable threshold vs. temperature

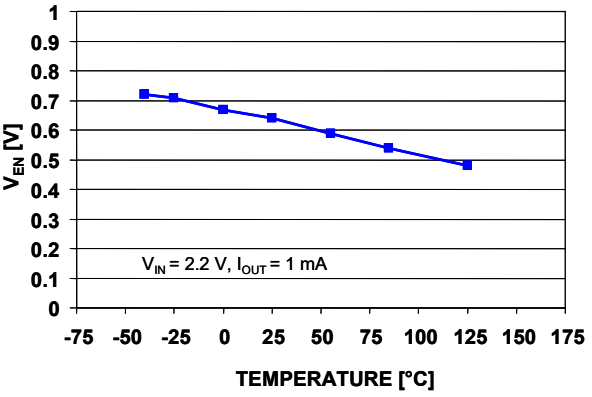


Figure 14. Quiescent current vs. temperature (V_{OUT} = 1.2 V, I_{OUT} = 0 mA)

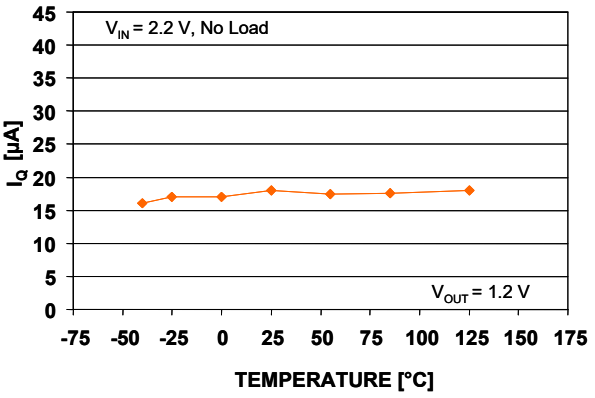


Figure 15. Quiescent current vs. temperature (V_{OUT} = 1.2 V, I_{OUT} = 0.15 A)

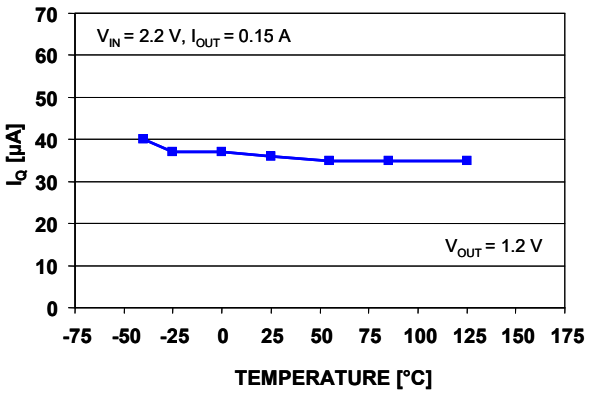


Figure 16. Quiescent current vs. temperature (V_{OUT} = 2.8 V, I_{OUT} = 0.15 A)

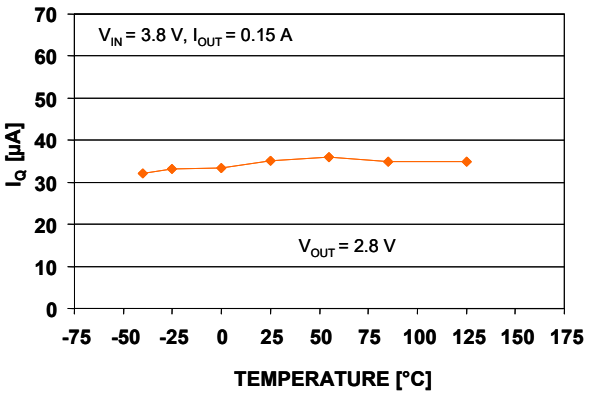


Figure 17. Quiescent current vs. input voltage

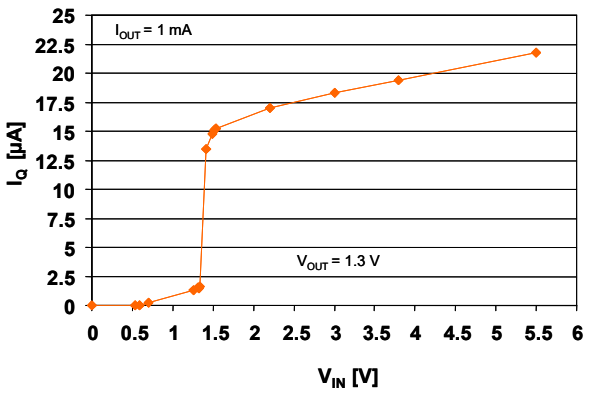


Figure 18. Quiescent current vs. output current

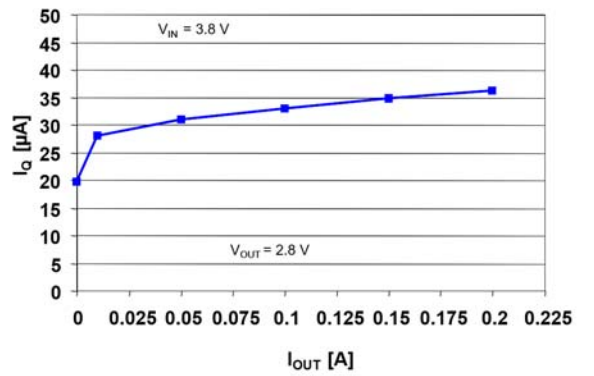


Figure 19. Supply voltage rejection vs. temperature (V_{OUT} = 1.2 V)

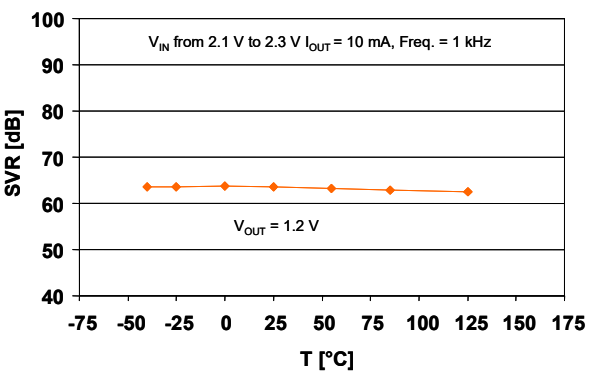


Figure 20. Supply voltage rejection vs. temperature (V_{OUT} = 1.3 V)

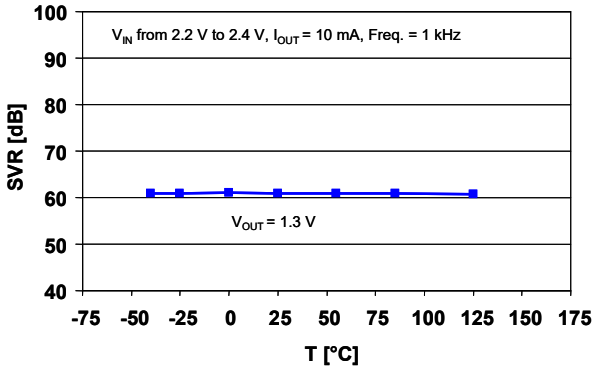


Figure 21. Supply voltage rejection vs. temperature (Freq. = 1 kHz)

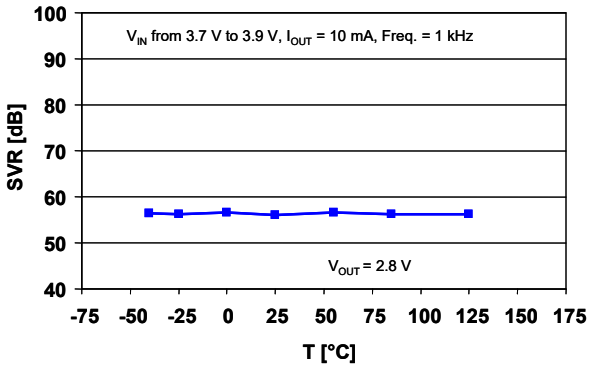


Figure 22. Supply voltage rejection vs. temperature (Freq. = 10 kHz)

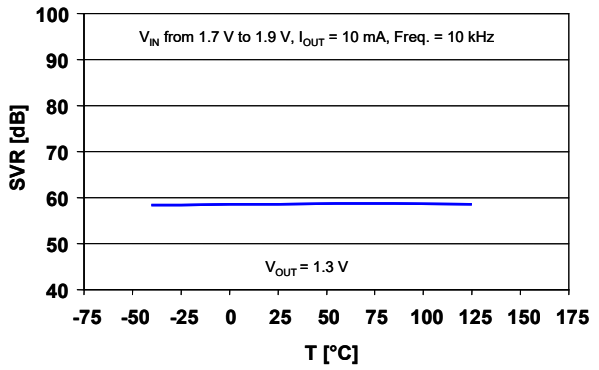


Figure 23. Supply voltage rejection vs. temperature (V_{OUT} = 2.8 V)

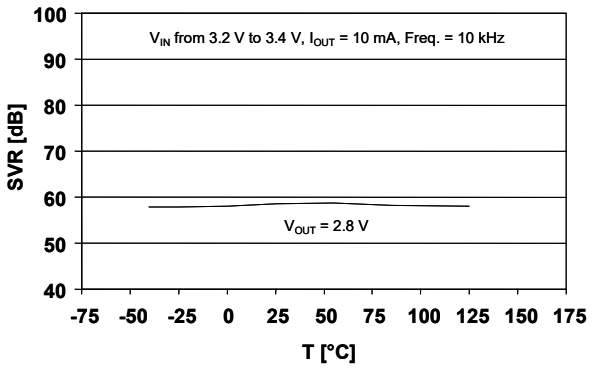


Figure 24. Supply voltage rejection vs. frequency (V_{OUT} = 1.2 V)

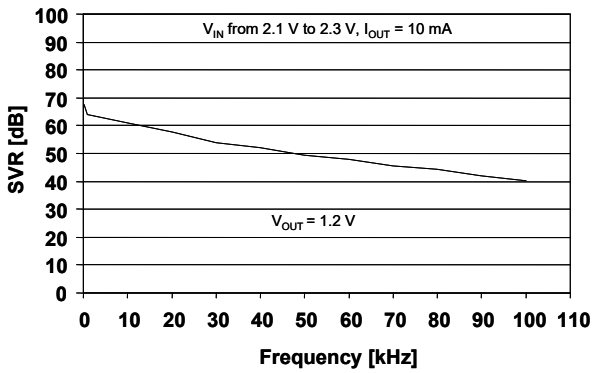


Figure 25. Supply voltage rejection vs. frequency (V_{OUT} = 1.3 V)

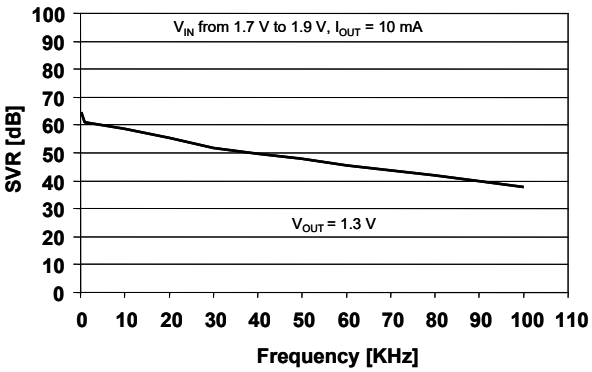


Figure 26. Supply voltage rejection vs. frequency (V_{OUT} = 2.8 V)

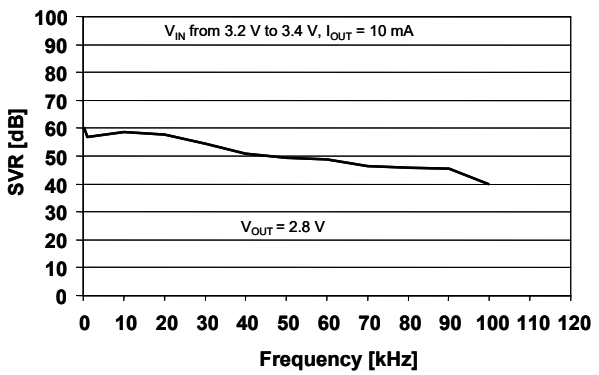


Figure 27. Supply voltage rejection vs. output current

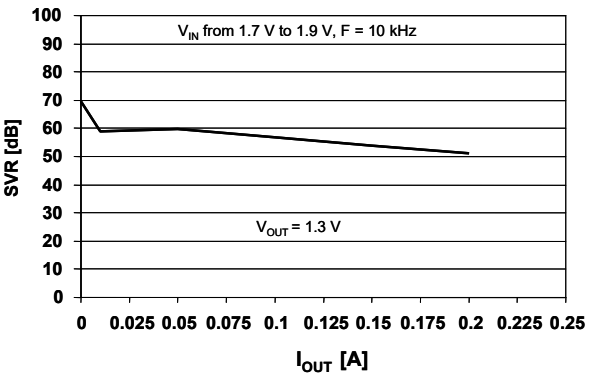


Figure 28. LD39115J noise

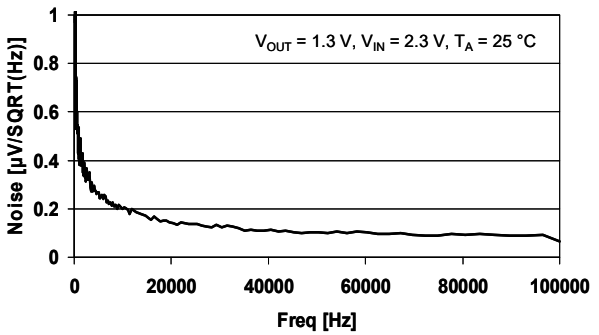
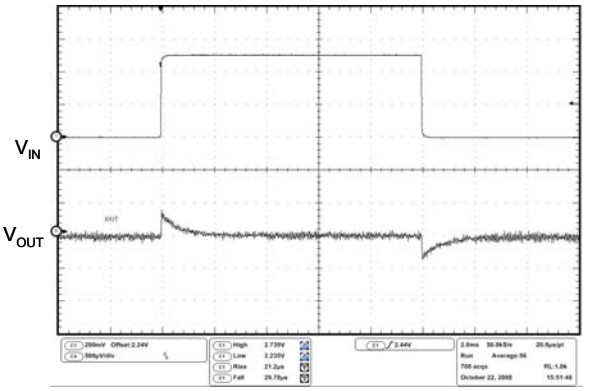
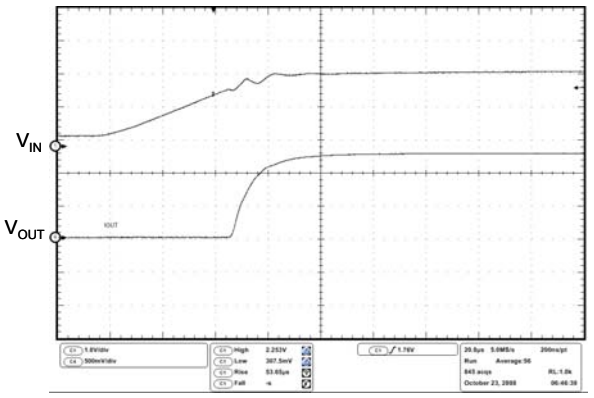


Figure 29. Line regulation transient



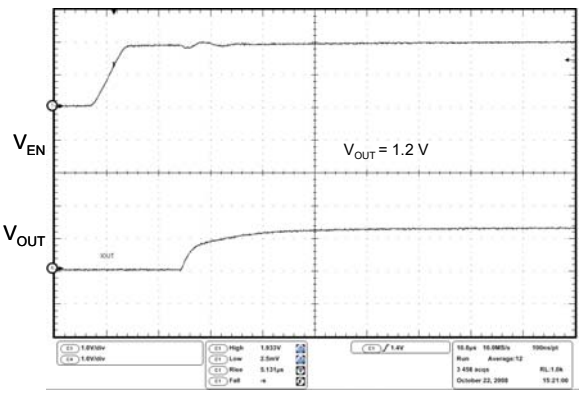
V_{IN} from 2.2 V to 2.7 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF, No C_{IN}
$t_{RISE/FALL}$ = 5 µs

Figure 30. Start up transient



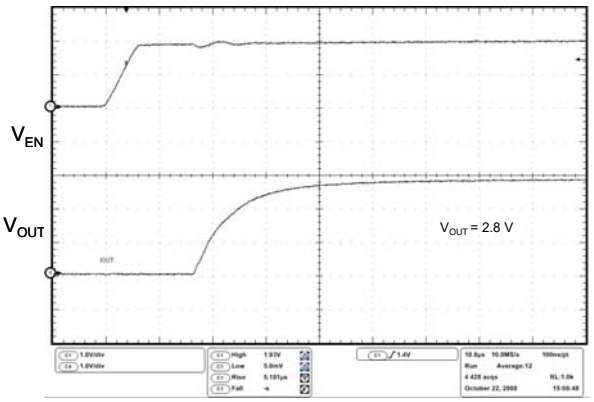
V_{IN} from 0 to 2.3 V, I_{OUT} = 1 mA C_{OUT} = 1 µF No C_{IN},
t_{RISE} = 60 µs

Figure 31. Enable transient (V_{OUT} = 1.2 V)



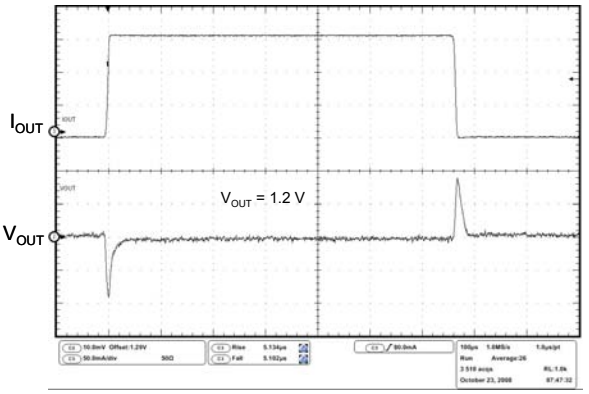
V_{IN} = 2.3 V, V_{EN} from 0 to 2 V, I_{OUT} = 1 mA, Trise = 5 µs

Figure 32. Enable transient (V_{OUT} = 2.8 V)



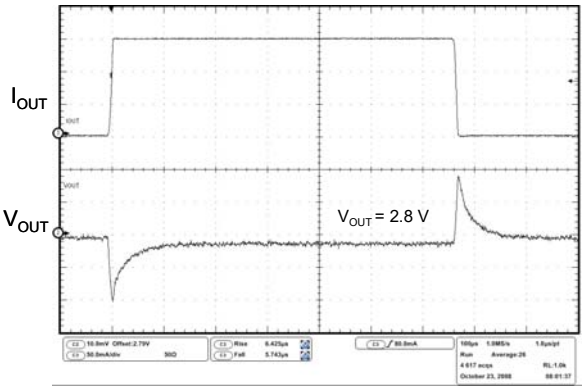
V_{IN} = 3.8 V, V_{EN} from 0 to 2 V, I_{OUT} = 1 mA, t_{RISE} = 5 µs

Figure 33. Load transient (V_{OUT} = 1.2 V)



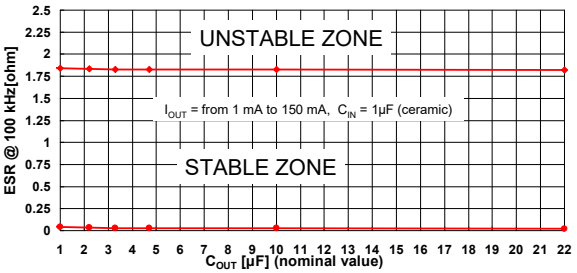
V_{IN} = 2. 2 V, I_{OUT} = from 1 to 150 mA, $t_{RISE/FALL}$ = 5 µs

Figure 34. Load transient (V_{OUT} = 2.8 V)



V_{in} = 3.8 V, I_{OUT} = from 1 to 150 mA, $t_{RISE/FALL}$ = 5 µs

Figure 35. ESR required for stability with ceramics capacitors



V_{IN} = 2. 2 V, I_{OUT} = from 1 to 150 mA, $t_{RISE/FALL}$ = 5 µs

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 36. Flip-chip 4 drawings

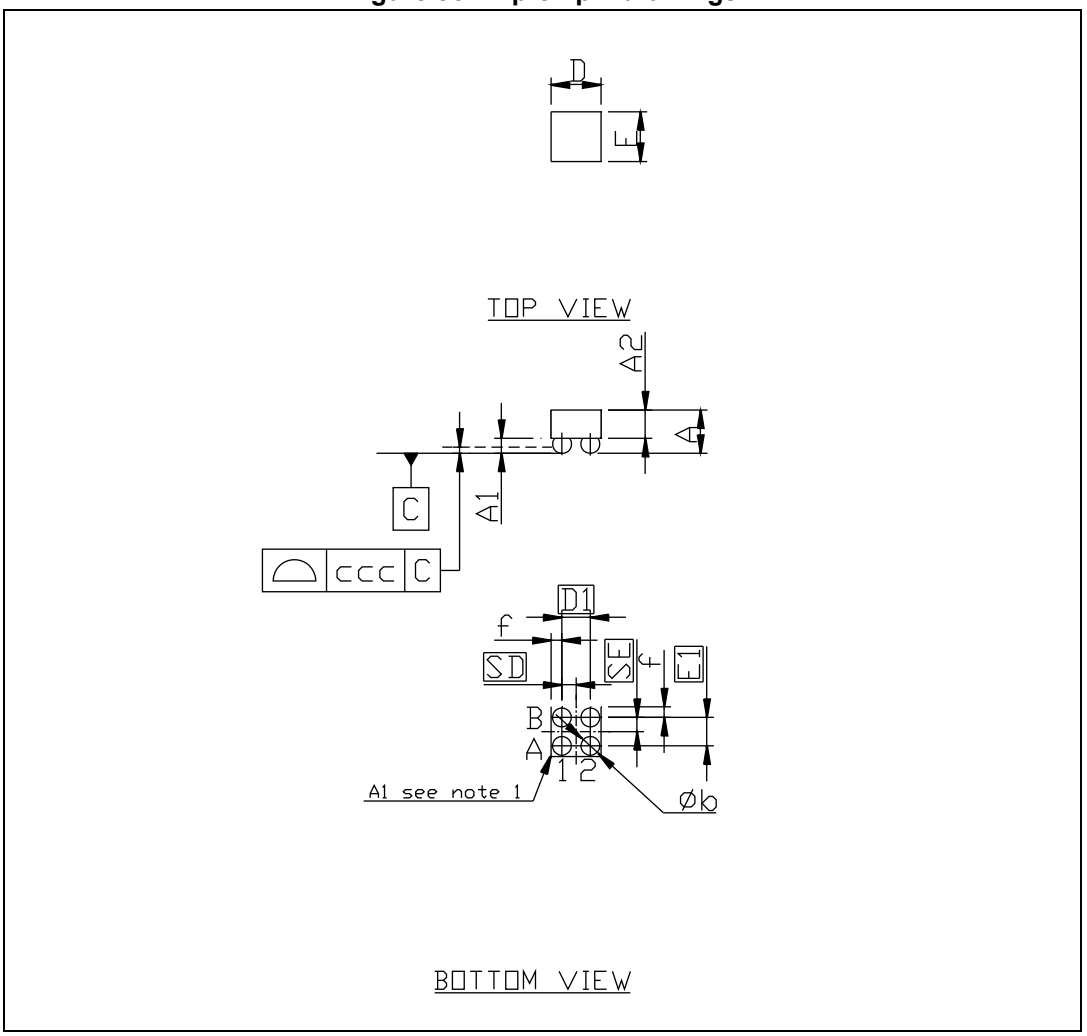
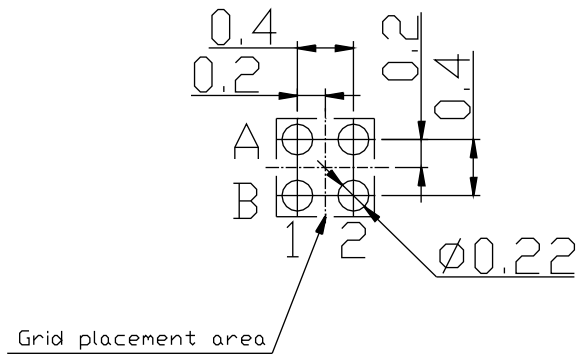


Table 7. Flip-chip 4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.52	0.56	0.60
A1	0.17	0.20	0.23
A2	0.35	0.36	0.37
b	0.23	0.25	0.29
D	0.758	0.788	0.818
D1		0.4	
E	0.758	0.788	0.818
E1		0.4	
SD	0.18	0.2	0.22
SE	0.18	0.2	0.22
f		0.199	
ccc		0.075	

Figure 37. Flip-chip 4 footprint



8 Packaging mechanical data

Figure 38. Flip-chip 4 tape and reel drawing

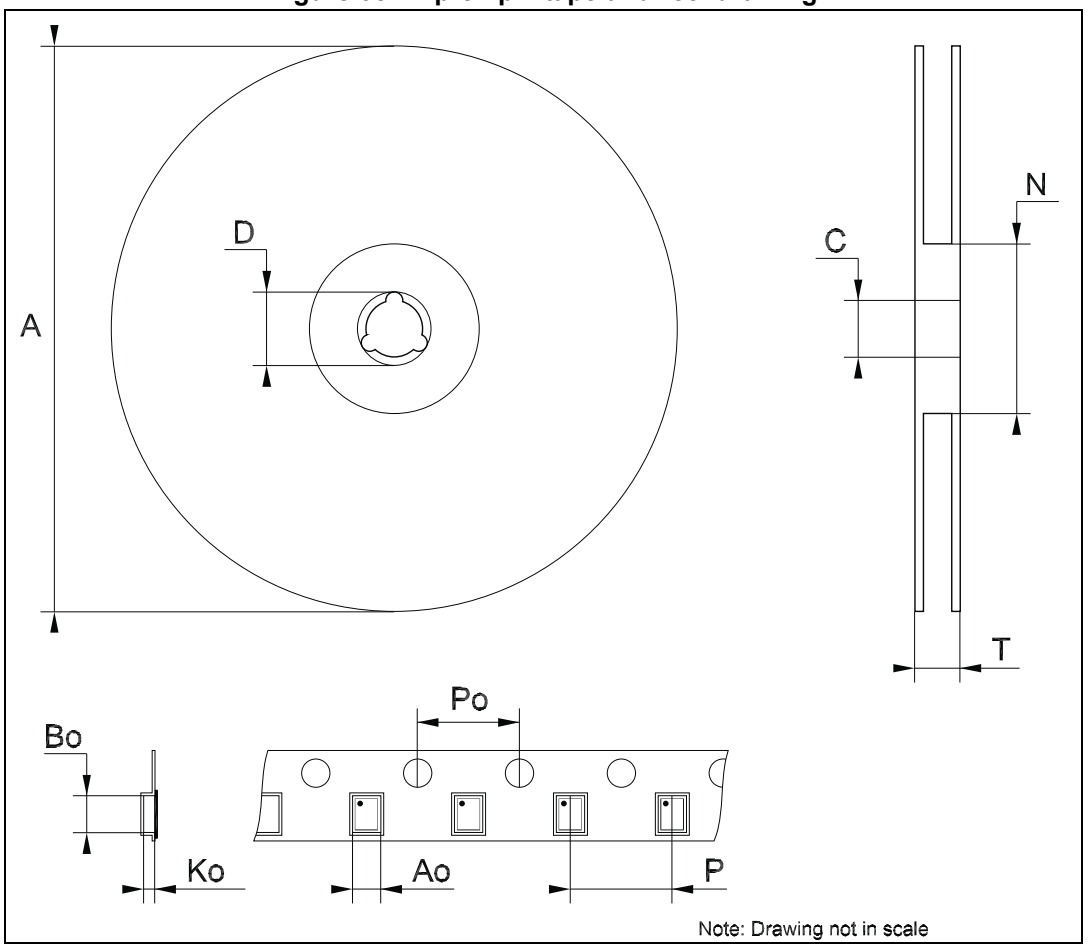


Table 8. Flip-chip 4 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			178
C	12.8		13.2
D	20.2		
N	59	60	61
T			8.4
Ao	0.82	0.87	0.92
Bo	0.82	0.87	0.92
Ko	0.64	0.69	0.74
Po	3.9	4.0	4.1
P	3.9	4.0	4.1

9 Different output voltage versions of the LD39115J available on request

Table 9. Options available on request

Order codes	Output voltages
LD39115J08R	0.8 V
LD39115J10R	1.0 V

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Mar-2009	1	Initial release.
12-Jun-2009	2	Modified: Table 1 on page 1 and Table 8 on page 19.
05-Aug-2009	3	Modified: tape and reel mechanical data on page 18.
17-May-2011	4	Modified: Table 1 on page 1 and Table 8 on page 19.
20-Dec-2011	5	Added: new order code LD39115J25R Table 1 on page 1.
16-Jan-2014	6	Part number LD39115Jxx changed to LD39115J. Updated the Description in cover page, Section 7: Package mechanical data. Added Section 8: Packaging mechanical data. Minor text changes.
12-Sep-2018	7	Added Table 5: ESD performance.
23-Feb-2021	8	Updated *Figure 18* and *Figure 28*.

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