

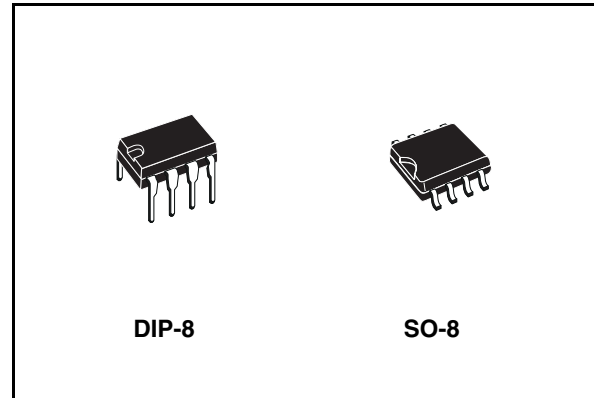


# ST485AB

## Very high speed low power RS-485/RS-422 transceiver

### Features

- Low supply current: 5 mA max
- High data rate > 30 Mbps
- Designed for RS 485 interface applications
- -7 to 12 common mode input voltage range
- Driver maintains high impedance in 3-state or with the power off
- 70mV typical input hysteresis
- Operate from single 5 supply
- $\pm 4$  kV ESD protection
- Current limiting and thermal shutdown for driver overload protection
- Latch-up free up to 500 mA



The ST485A is designed for bi-directional data communications or multipoint bus transmission lines.

### Description

The ST485A is a low power, high speed transceiver for RS-485 and RS-422 communications. The device contains one driver and one receiver in half duplex configuration. The ST485A draws 3 mA (typ.) of supply current when unloaded or fully loaded with disabled drivers. It operates from a single 5 V supply.

Driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that place the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic high output if both inputs are open circuit.

**Table 1. Device summary**

Order code	Temperature range	Package	Packaging
ST485ABN	-40 to 85 °C	DIP-8	50parts per tube / 40tube per box
ST485ABDR	-40 to 85 °C	SO-8 (Tape & reel)	2500 parts per reel

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# 1 Pin configuration

Figure 1. Pin configuration

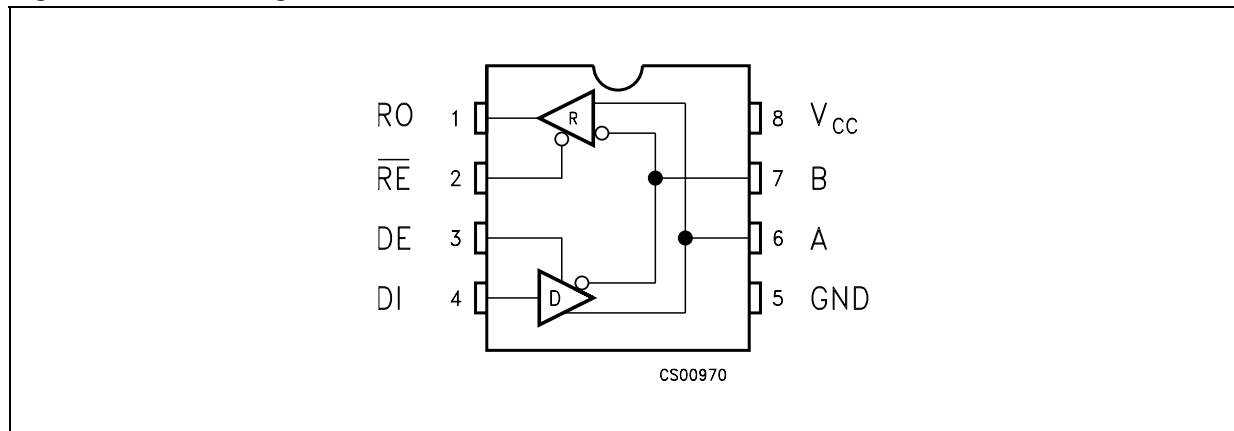


Table 2. Pin description

Pin n°	Symbol	Name and function
1	RO	Receiver output. If $A > B$ by 200 mV, RO will be high; if $A < B$ by 200 mV, RO will be low
2	$\overline{RE}$	Receiver output enable. RO is enabled when RE is low; RO is high impedance when RE is high. If RE is high and DE is low, the device will enter a low power shutdown mode.
3	DE	Driver output enable. The driver outputs are enabled by bringing DE high. They are high impedance when DE is low. If RE is high DE is low, the device will enter a low-power shutdown mode. If the driver outputs are enabled, the part functions as line driver, while they are high impedance, it functions as line receivers if RE is low.
4	DI	Driver input. A low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low
5	GND	Ground
6	A	Non-inverting receiver input and non-inverting driver output
7	B	Inverting receiver input and inverting driver output
8	$V_{CC}$	Supply voltage: $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$

## 2 Truth tables

**Table 3. Truth table (driver)**

Inputs			Outputs		Mode
$\overline{RE}$	DE	DI	B	A	A
X	H	H	L	H	Normal
X	H	L	H	L	Normal
L	L	X	Z	Z	Normal

Note: X = Don't care; Z = High impedance

**Table 4. Truth table (receiver)**

Inputs			Outputs	Mode
$\overline{RE}$	DE	A-B	RO	
L	L	$\geq -0.2\text{ V}$	H	Normal
L	L	$\leq -0.2\text{ V}$	L	Normal
L	L	Inputs open	H	Normal

Note: X = Don't care; Z = High impedance

### 3 Maximum ratings

**Table 5. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	7	V
$V_I$	Control input voltage ( $\overline{RE}$ , DE)	-0.3 to 7	V
$V_{DI}$	Driver input voltage (DI)	-0.3 to 7	V
$V_{DO}$	Driver output voltage (A, B)	-7.5 to 12.5	V
$V_{RI}$	Receiver input voltage (A, B)	-7.5 to 12.5	V
$V_{RO}$	Receiver output voltage (RO)	-0.3 to ( $V_{CC} + 0.3$ )	V

*Note:* Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

## 4 Electrical characteristics

**Table 6. DC electrical characteristics** ( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$ , unless otherwise specified. Typical values are referred to  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ) (*Note: 1*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$I_{SUPPLY}$	$V_{CC}$ Power supply current	No load, $V_{RE}=0\text{ V}$ or $V_{CC}$	$V_{DE} = V_{CC}$		2.3	5	mA
			$V_{DE} = 0\text{ V}$		2.6	5	mA
$C_{I/O}$	Input/output capacitance			10		pF	
$C_{AB}$	Driver output capacity			10		pF	

**Table 7. Logic input electrical characteristics** ( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$ , unless otherwise specified. Typical values are referred to  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ) (*Note: 1*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input logic threshold low	DE, DI, RE			0.8	V
$V_{IH}$	Input logic threshold high	DE, DI, RE	2			V
$I_{IN1}$	Logic input current	DE, DI, RE			$\pm 2.0$	$\mu\text{A}$
$I_{IN2}$	Input current (A, B)	$V_{DE}=0\text{ V}$ , $V_{CC}= 0\text{ or }5.25\text{ V}$	$V_{IN}=12\text{ V}$		1	mA
			$V_{IN}=-7\text{ V}$		-0.8	mA

**Table 8. Transmitter electrical characteristics** ( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$ , unless otherwise specified. Typical values are referred to  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ) (*Note: 1*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OD1}$	Differential driver output (No load)				5	V
$V_{OD2}$	Differential driver output (with load)	$R_L = 54\ \Omega$ (RS-422) $V_{CM} = -7\text{ V to }12\text{ V}$	1.5	2.7	5	V
$\Delta V_{OD}$	Change in magnitude of driver differential output voltage for complementary output states ( <i>Note: 1</i> )	$R_L = 27\ \Omega$ or $50\ \Omega$		0	0.2	V
$V_{OC}$	Driver common mode output voltage	$R_L = 27\ \Omega$ or $50\ \Omega$	1		3	V
$\Delta V_{OC}$	Change in magnitude of driver common mode output voltage ( <i>Note: 1</i> )	$R_L = 54\ \Omega$ or $100\ \Omega$		0	0.2	V
$I_{OSD}$	Driver short circuit output current	$V_O = -7\text{ V to }12\text{ V}$			$\pm 250$	mA

**Table 9. Receiver electrical characteristics** ( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$ , unless otherwise specified. Typical values are referred to  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ) (*Note: 1*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{TH}$	Receiver Differential Threshold Voltage	$V_{CM} = -7\text{ V to }12\text{ V}$	-0.2		0.2	V
$\Delta V_{TH}$	Receiver Input Hysteresis	$V_{CM} = 0\text{ V}$		70		mV
$V_{OH}$	Receiver Output High Voltage	$I_{OUT} = -4\text{ mA}$ , $V_{ID} = 200\text{ mV}$	3.5	4.7		V
$V_{OL}$	Receiver Output Low Voltage	$I_{OUT} = 4\text{ mA}$ , $V_{ID} = -200\text{ mV}$		0.2	0.4	V
$I_{OZR}$	3-State (High Impedance) Output Current at Receiver	$V_O = 0.4\text{ V to }2.4\text{ V}$			$\pm 1$	$\mu\text{A}$
$R_{RIN}$	Receiver Input Resistance	$V_{CM} = -7\text{ V to }12\text{ V}$	12	24		$\text{K}\Omega$
$I_{OSR}$	Receiver Short-Circuit Current	$V_O = 0\text{ V to }V_{CC}$	7		95	mA

**Table 10. Driver switching characteristics** ( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$ , unless otherwise specified. Typical values are referred to  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ) (See *Note: 1*, *Note 3*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$D_R$	Maximum data rate	Jitter < 5%	30	50		Mbps
$t_{PLH}$ $t_{PHL}$	Propagation delay input to output	$R_L = 54\ \Omega$ , $C_{L1} = C_{L2} = 50\ \text{pF}$ , ( <i>Figure 8.</i> )		18	30	ns
$t_{SKEW}$	Differential output delay skew	$R_L = 54\ \Omega$ , $C_{L1} = C_{L2} = 50\ \text{pF}$ , ( <i>Figure 6.</i> )		0.5	2	ns
$t_{TLH}$ $t_{THL}$	Rise or fall differential time	$R_L = 54\ \Omega$ , $C_{L1} = C_{L2} = 50\ \text{pF}$ , ( <i>Figure 6.</i> )		8	12	ns
$t_{PZL}$	Output enable time	$C_L = 50\ \text{pF}$ , S1 Closed			30	ns
$t_{PZH}$	Output enable time	$C_L = 50\ \text{pF}$ , S2 Closed			30	ns
$t_{PHZ}$	Output disable time	$C_L = 15\ \text{pF}$ , S2 Closed			30	ns
$t_{PLZ}$	Output disable time	$C_L = 15\ \text{pF}$ , S1 Closed			30	ns
$t_{SK(EN)}$	Synchronous driver operation a-b at enable				2	ns
$t_{SK(DS)}$	Synchronous driver operation A-B at disable			4	6	ns

**Table 11. Driver switching characteristics** ( $V_{CC} = 4.5V$  to  $5.5V$ ,  $T_A = -40$  to  $85^\circ C$ , unless otherwise specified. Typical values are referred to  $T_A = 25^\circ C$ ,  $V_{CC} = 5V$ ) (See [Note: 1](#), [Note 3](#))

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{PLH}$ $t_{PHL}$	Propagation Delay	$C_L = 15$ pF		18	30	ns
$t_{RPDS}$	$ t_{PLH} - t_{PHL} $ Propagation delay skew	$C_L = 15$ pF		0.5	2	ns
$t_{PZL}$	Output enable time	$C_{RL} = 15$ pF, S1 Closed		7	12	ns
$t_{PZH}$	Output enable time	$C_{RL} = 15$ pF, S2 Closed		7	12	ns
$t_{PHZ}$	Output disable time	$C_{RL} = 15$ pF, S2 Closed		7	12	ns
$t_{PLZ}$	Output disable time	$C_{RL} = 15$ pF, S1 Closed		7	12	ns

- Note:*
- 1 All currents into device pins are positive; all currents out of device pins are negative; all voltages are referenced to device ground unless specified.
  - 2 Applies to peak current. See typical Operating Characteristics.
  - 3  $t_r = t_f \leq 6$  ms.



## 5 Test circuit and typical characteristics

Figure 2. Driver DC test load

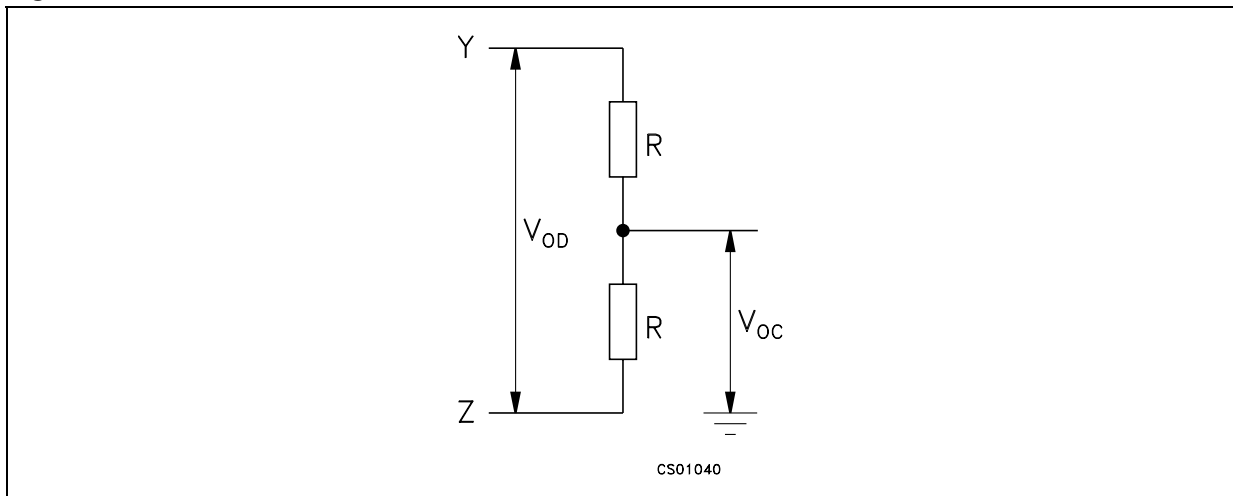


Figure 3. Receiver timing test load

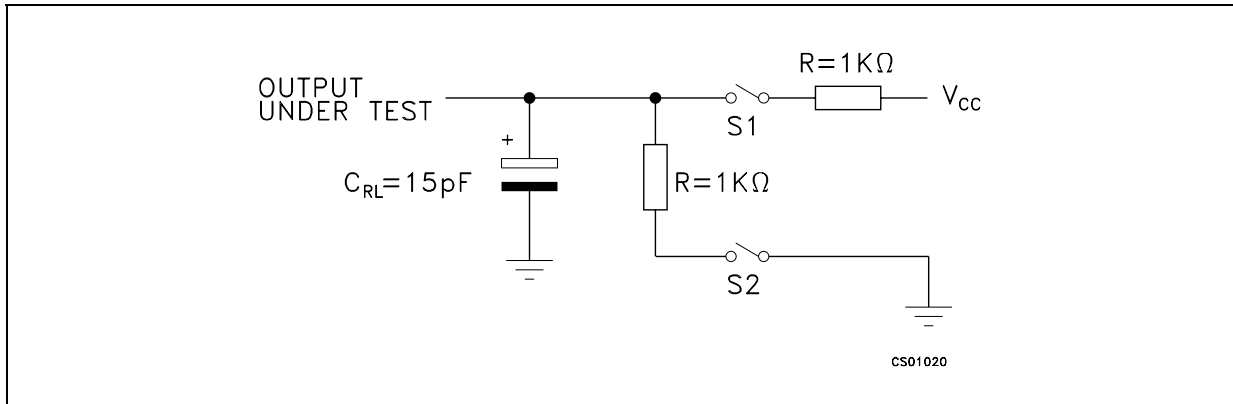


Figure 4. Driver/receiver timing test circuit

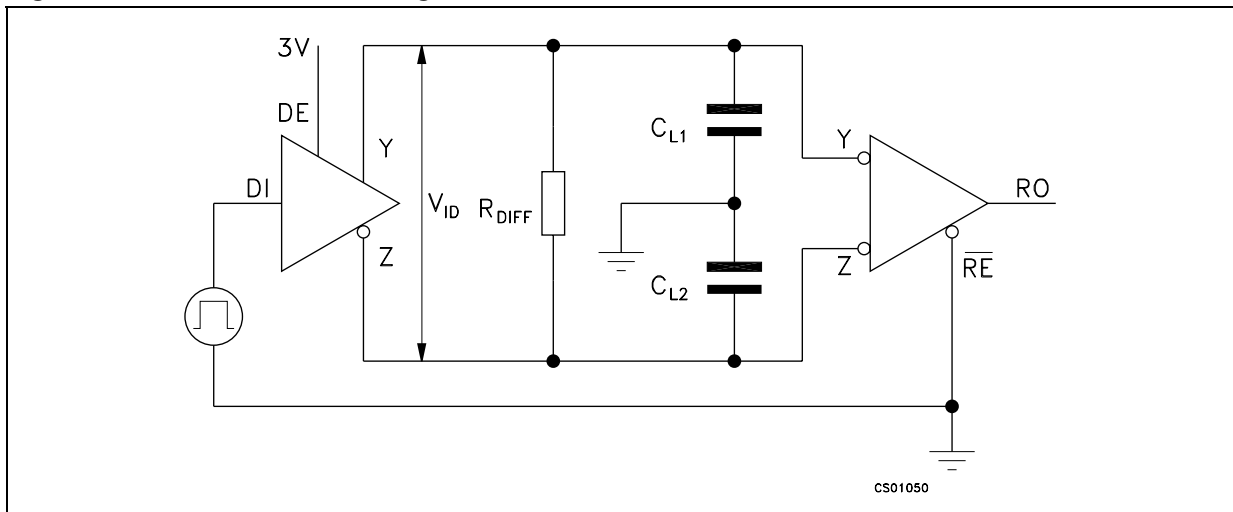


Figure 5. Driver timing test load

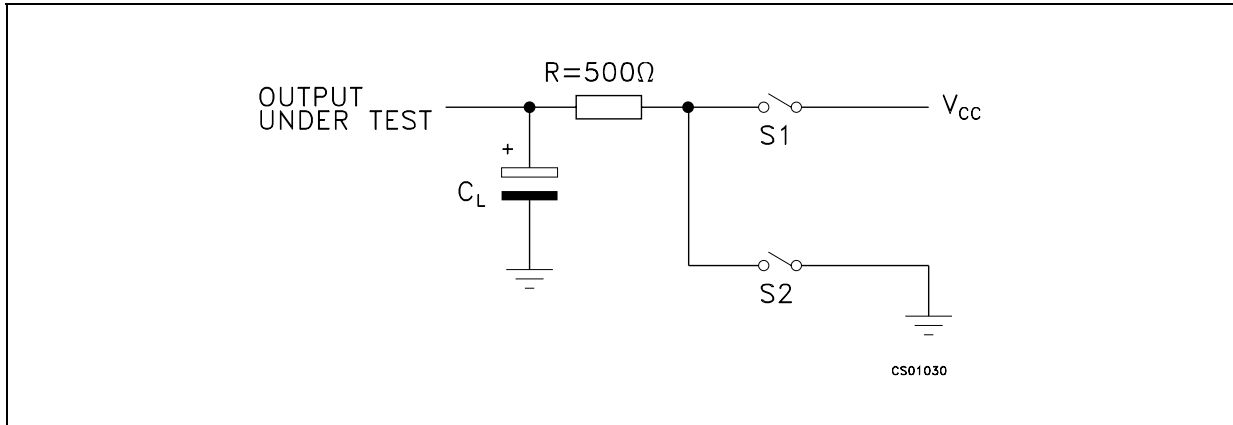


Figure 6. Driver timing test load

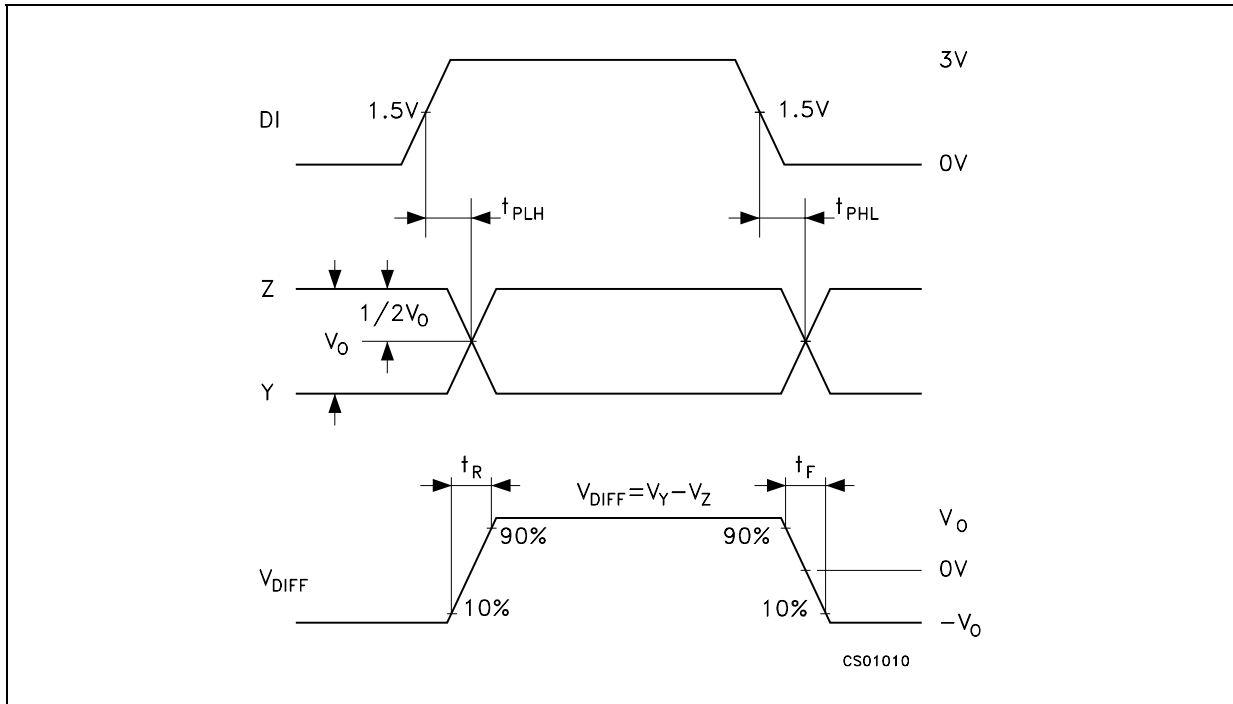


Figure 7. Driver enable and disable time

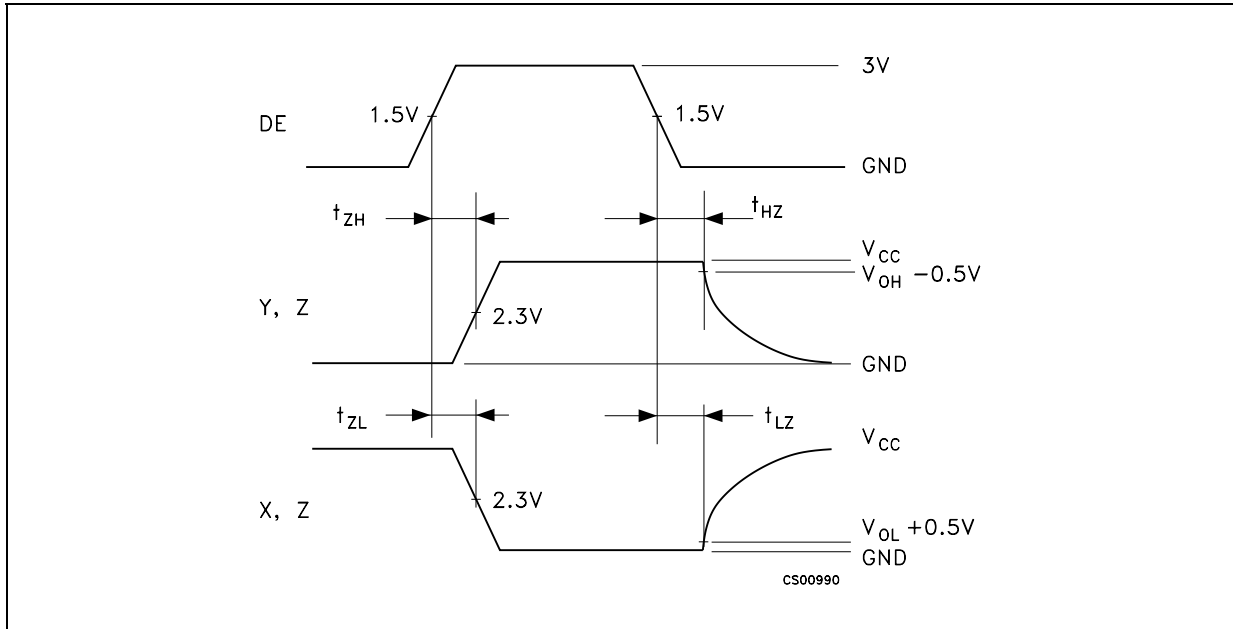


Figure 8. Receiver propagation delay

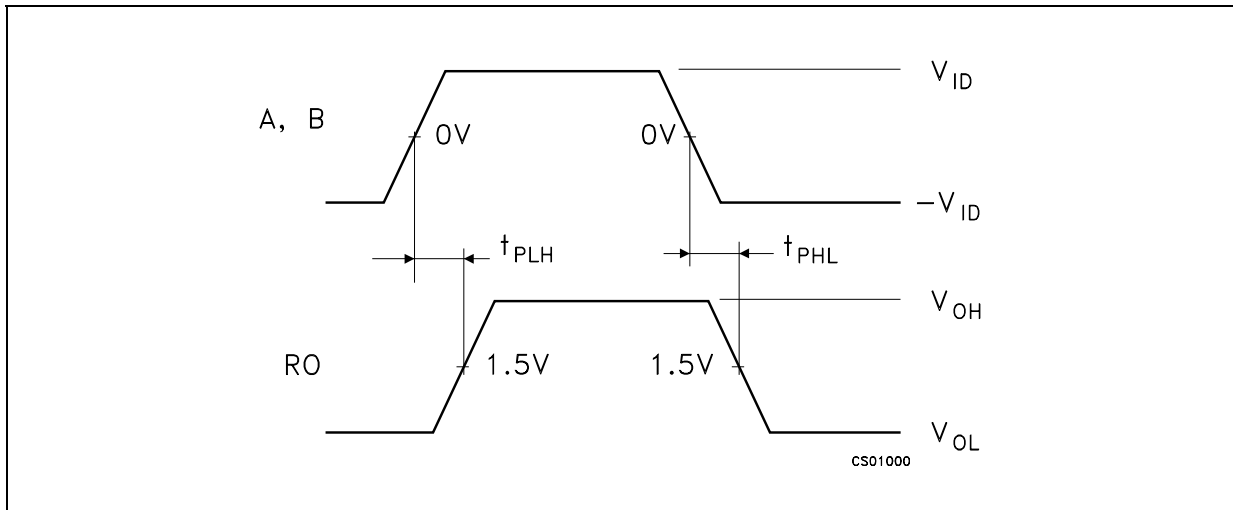


Figure 9. Receiver enable and disable time

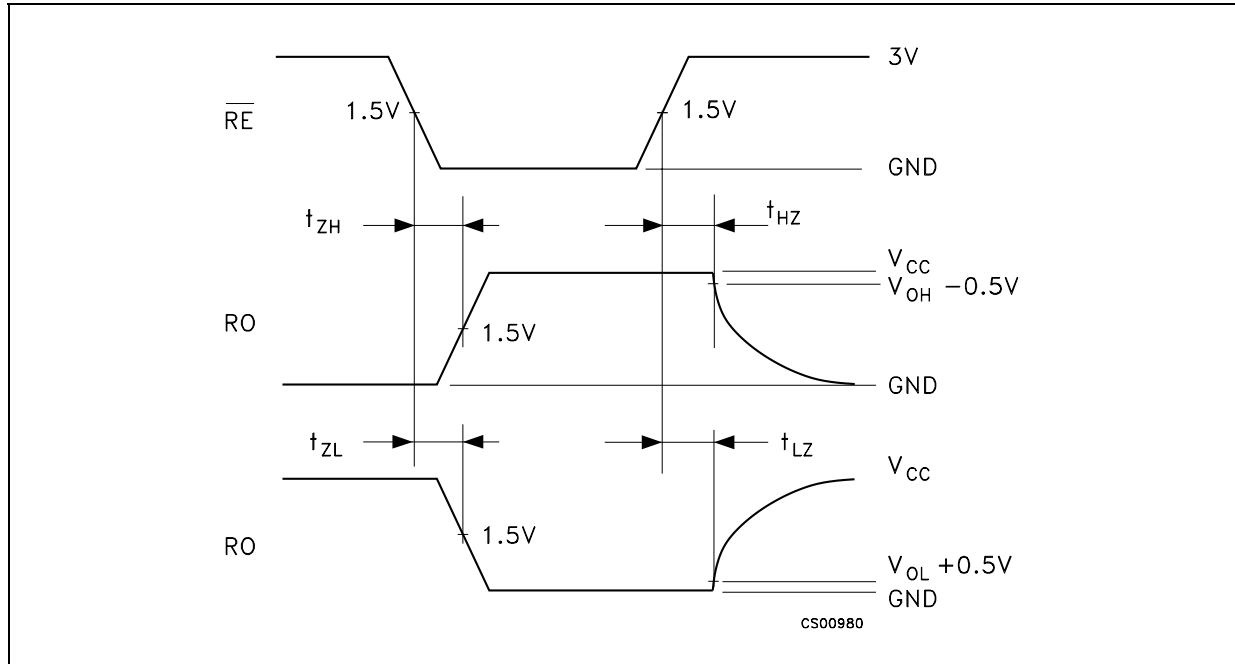


Figure 10. Receiver output current vs. output voltage (output low)

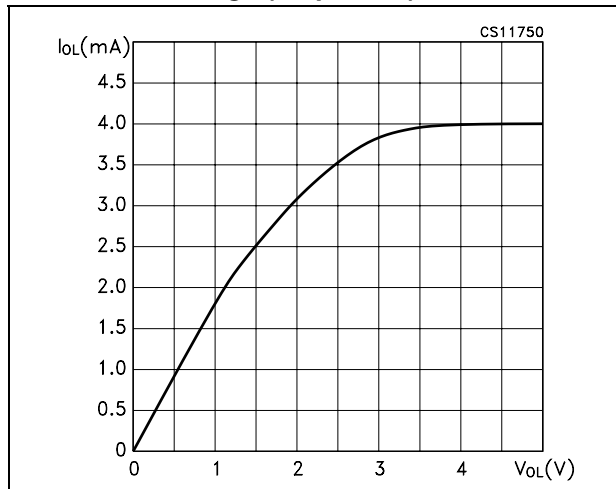
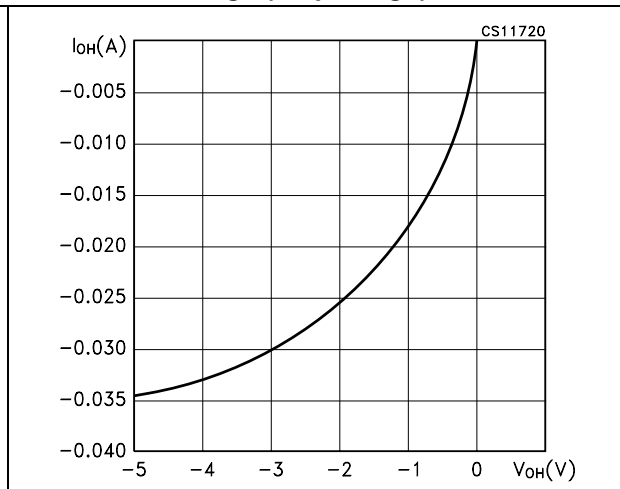
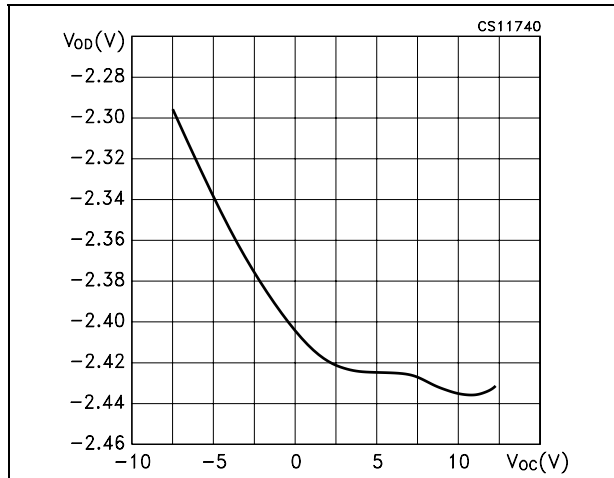


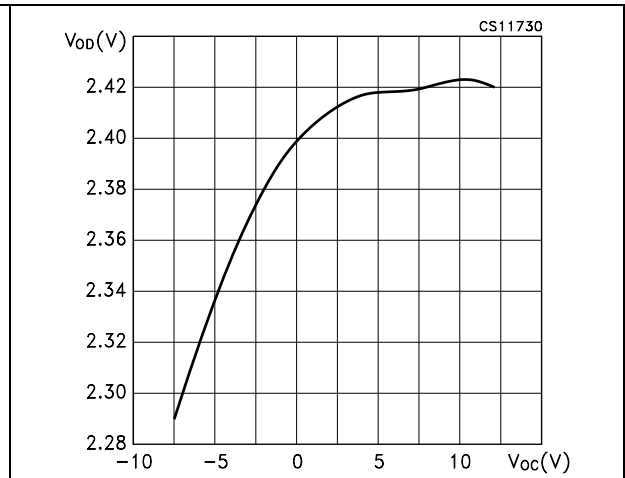
Figure 11. Receiver output current vs. output voltage (output high)



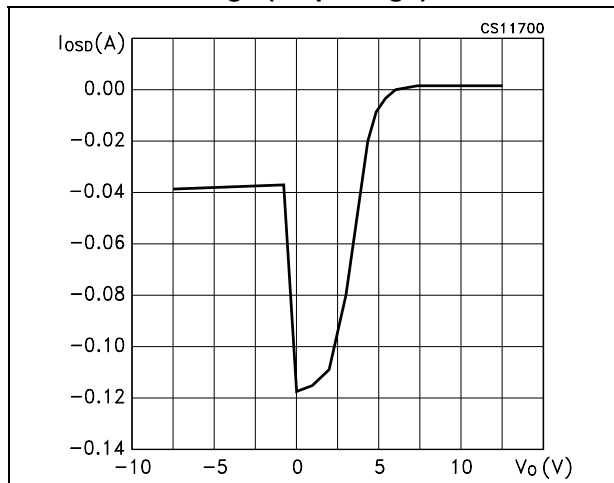
**Figure 12. Driver diff. output voltage vs common mode voltage (diff. output low)**



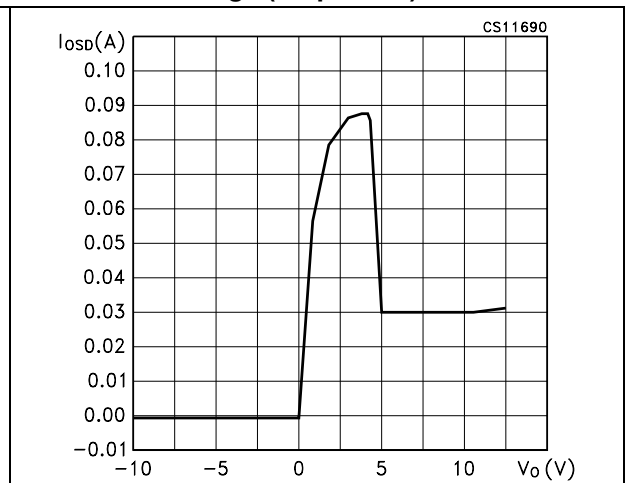
**Figure 13. Driver diff. output voltage vs common mode voltage (diff. output low)**



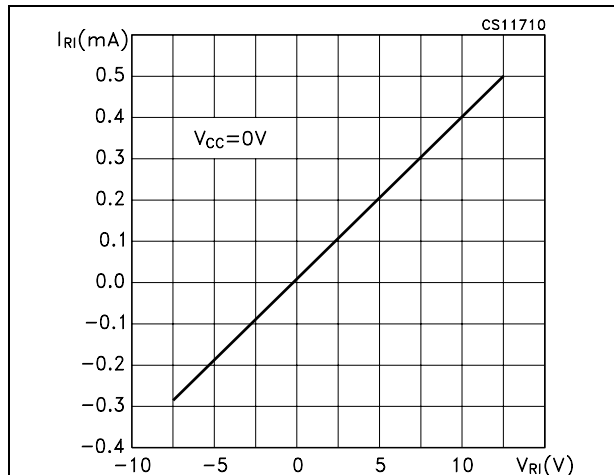
**Figure 14. Driver short circuit current vs line voltage (output high)**



**Figure 15. Driver short circuit current vs. line voltage (output low)**



**Figure 16. Receiver input current vs input voltage**

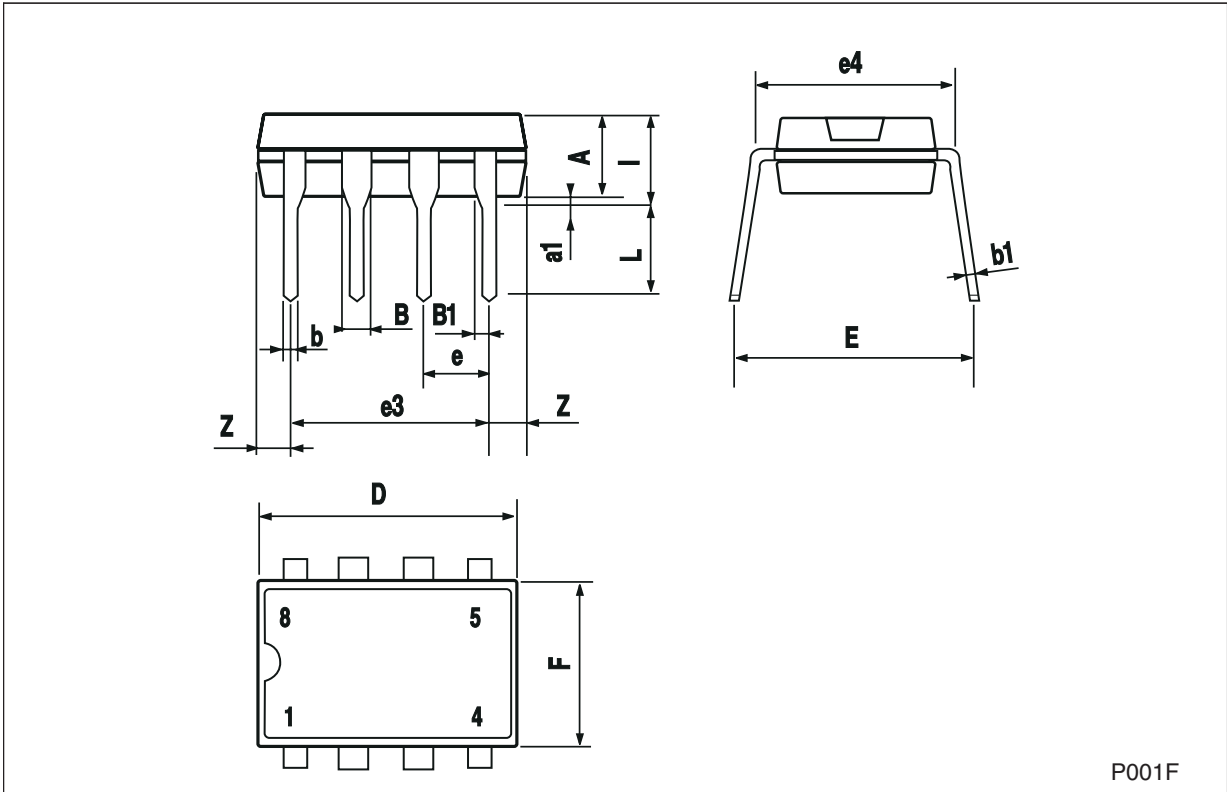


## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**Plastic DIP-8 mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
l			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

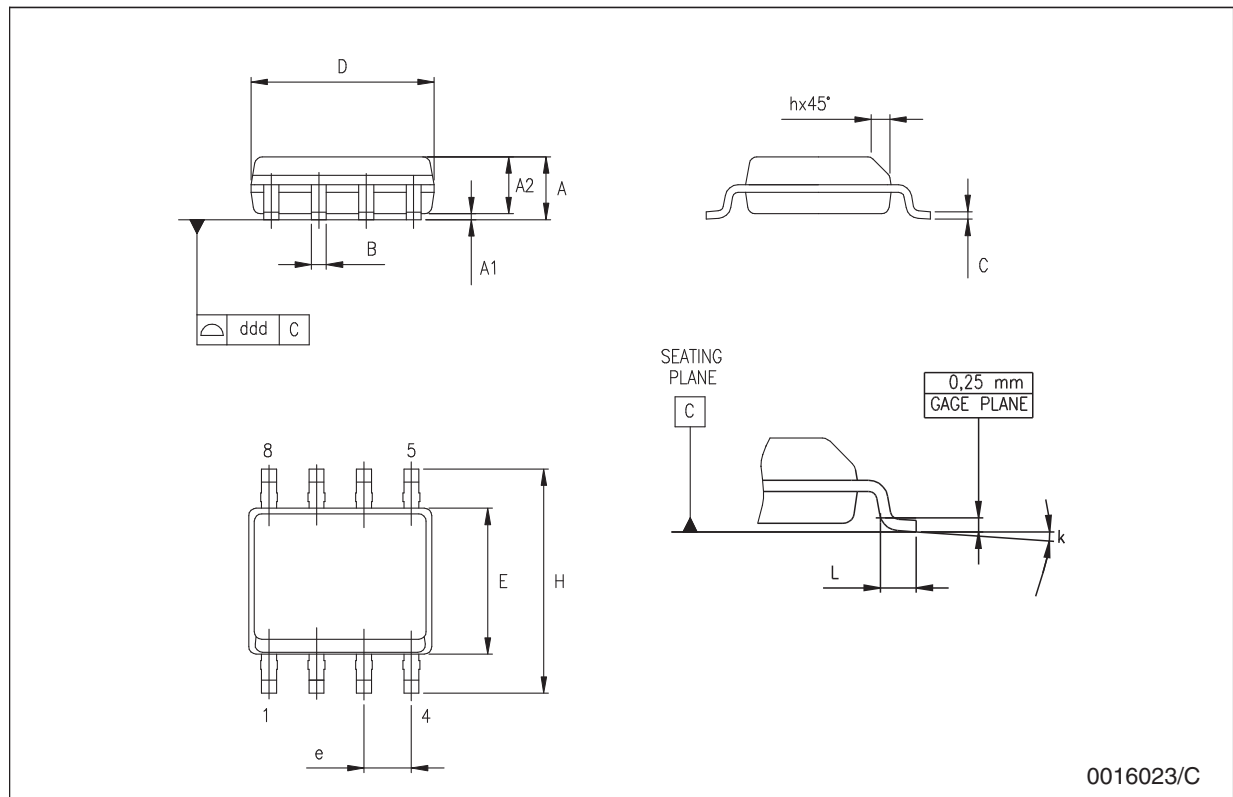


P001F



**SO-8 mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04





**Tape & reel SO-8 mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



## 7 Revision history

**Table 12. Revision history**

Date	Revision	Changes
28-Mar-2006	2	Order codes updated and new template.
24-Aug-2007	3	Added <a href="#">Table 1</a> . in cover page.

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