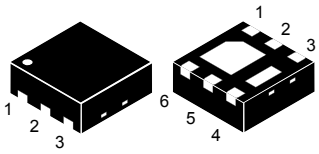
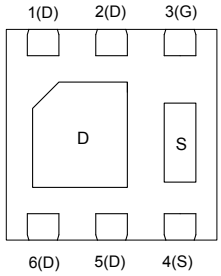
STL4P3LLH6

Datasheet

P-channel 30 V, 48 mΩ typ., 4 A, STripFET H6 Power MOSFET in a PowerFLAT 2x2 package



PowerFLAT 2x2



Bottom view

AM11269v1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL4P3LLH6	30 V	56 mΩ	4 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL4P3LLH6

Product summary	
Order code	STL4P3LLH6
Marking	4K3L
Package	PowerFLAT 2x2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_A = 25 °C	4	A
	Drain current (continuous) at T_A = 100 °C	2.75	
I_{DM} (1)	Drain current (pulsed)	16	A
P_{TOT}	Total power dissipation at T_A = 25 °C	2.4	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature		

1. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA} (1)	Thermal resistance, junction-to-ambient	52	°C/W

1. *When mounted on 1 inch^2 FR-4, 2 Oz copper board.*

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_C = 125 °C(1)			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.0		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		48	56	mΩ
		V_{GS} = 4.5 V, I_D = 2 A		75	90	

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	639	-	pF
C_{oss}	Output capacitance		-	79	-	pF
C_{rss}	Reverse transfer capacitance		-	52	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 4 A, V_{GS} = 4.5 V (see Figure 13. Gate charge test circuit)	-	6	-	nC
Q_{gs}	Gate-source charge		-	1.9	-	nC
Q_{gd}	Gate-drain charge		-	2.1	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Switching times test circuit for resistive load)	-	5.4	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	19.2	-	ns
t_f	Fall time		-	3.4	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0 V	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs, V_{DD} = 16 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	11.2		ns
Q_{rr}	Reverse recovery charge		-	3.5		nC
I_{RRM}	Reverse recovery current		-	0.6		A

1. *Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

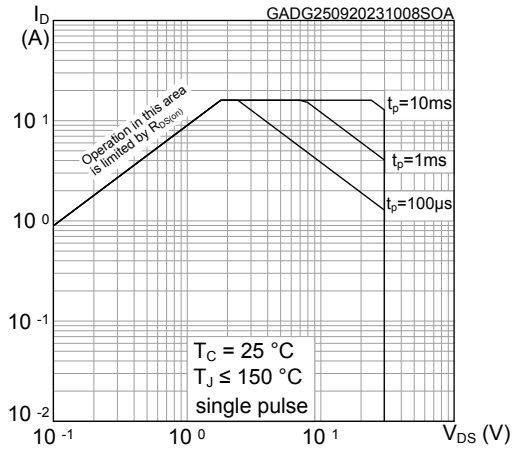


Figure 2. Normalized transient thermal impedance

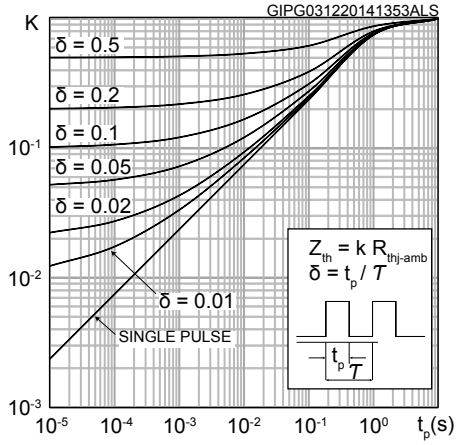


Figure 3. Typical output characteristics

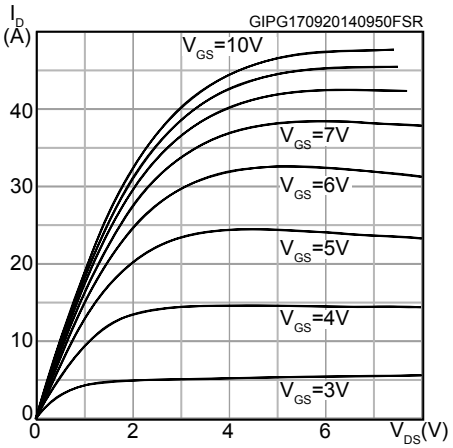


Figure 4. Typical transfer characteristics

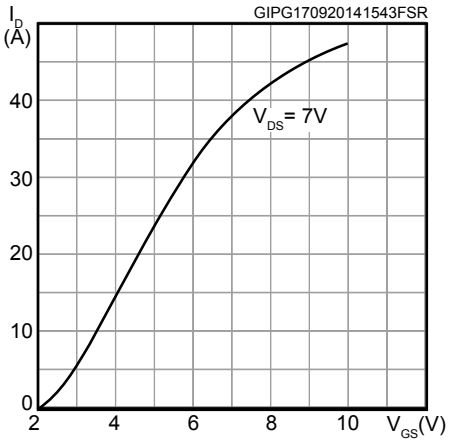


Figure 5. Typical gate charge vs gate-source voltage

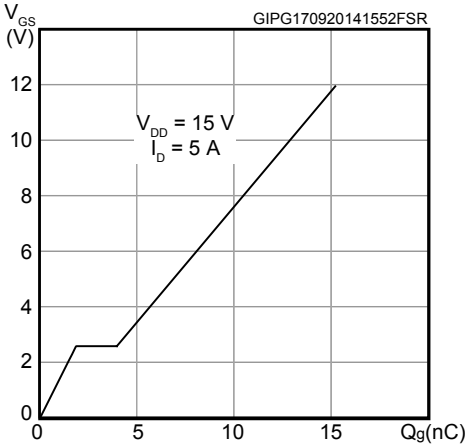


Figure 6. Typical static drain-source on-resistance

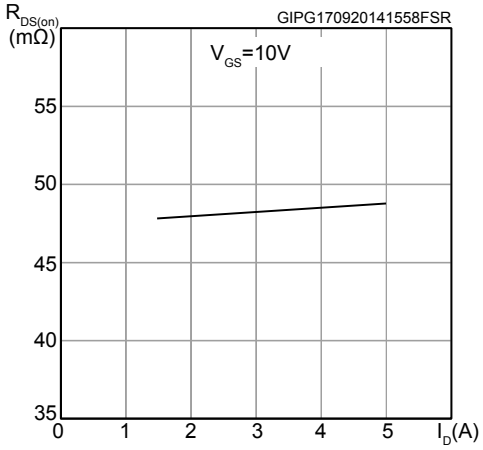


Figure 7. Normalized breakdown voltage vs temperature

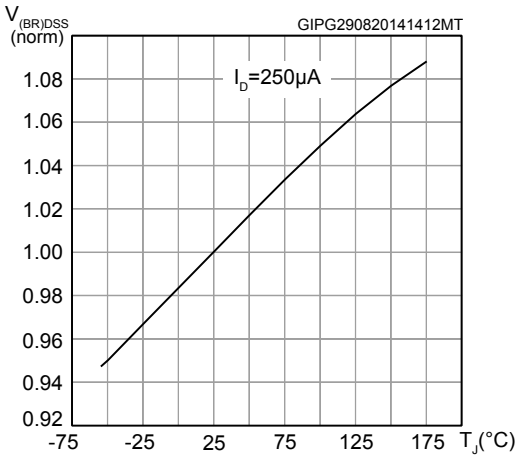


Figure 8. Typical capacitance characteristics

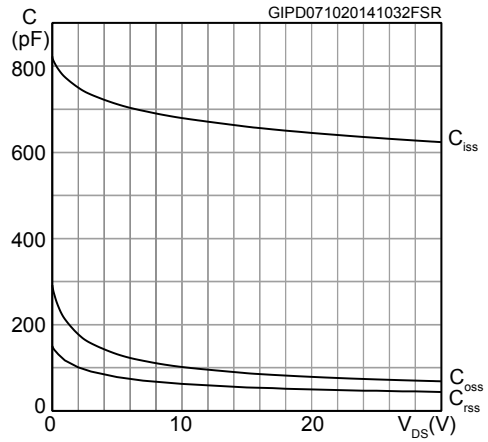


Figure 9. Normalized gate threshold voltage vs temperature

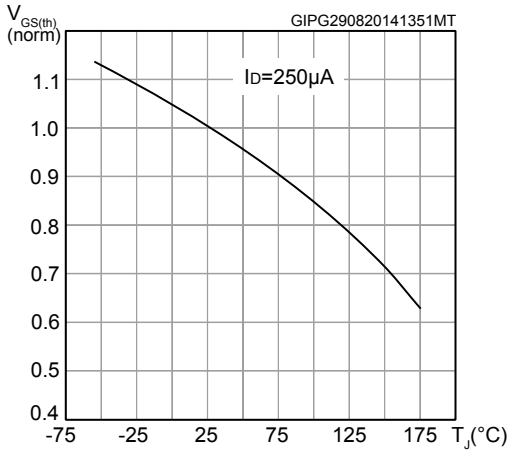


Figure 10. Normalized on-resistance vs temperature

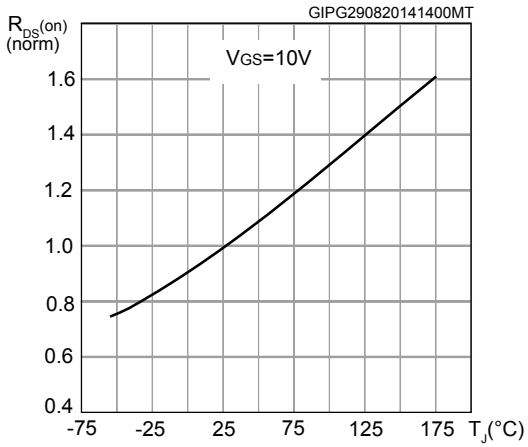
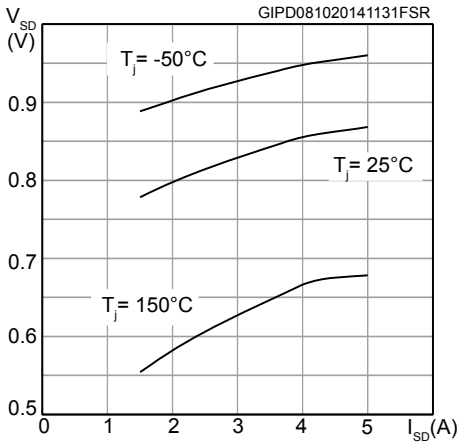


Figure 11. Typical reverse diode forward characteristics



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

3 Test circuits

Figure 12. Switching times test circuit for resistive load

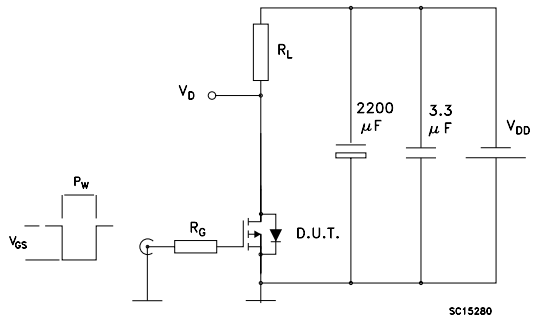


Figure 13. Gate charge test circuit

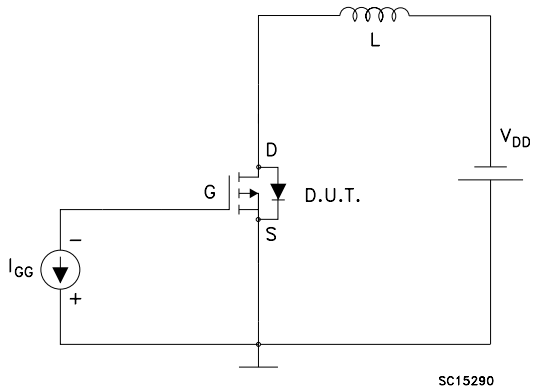
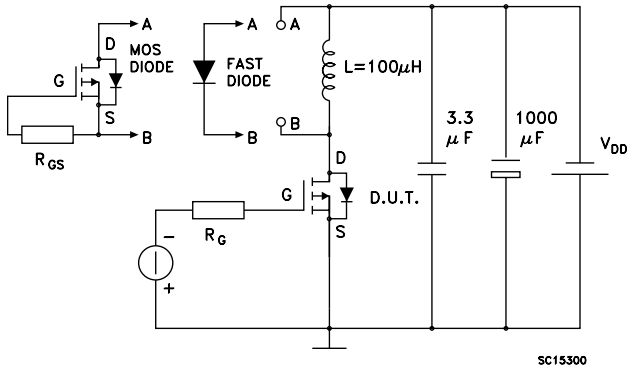


Figure 14. Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 2x2 package information

Figure 15. PowerFLAT 2x2 package outline

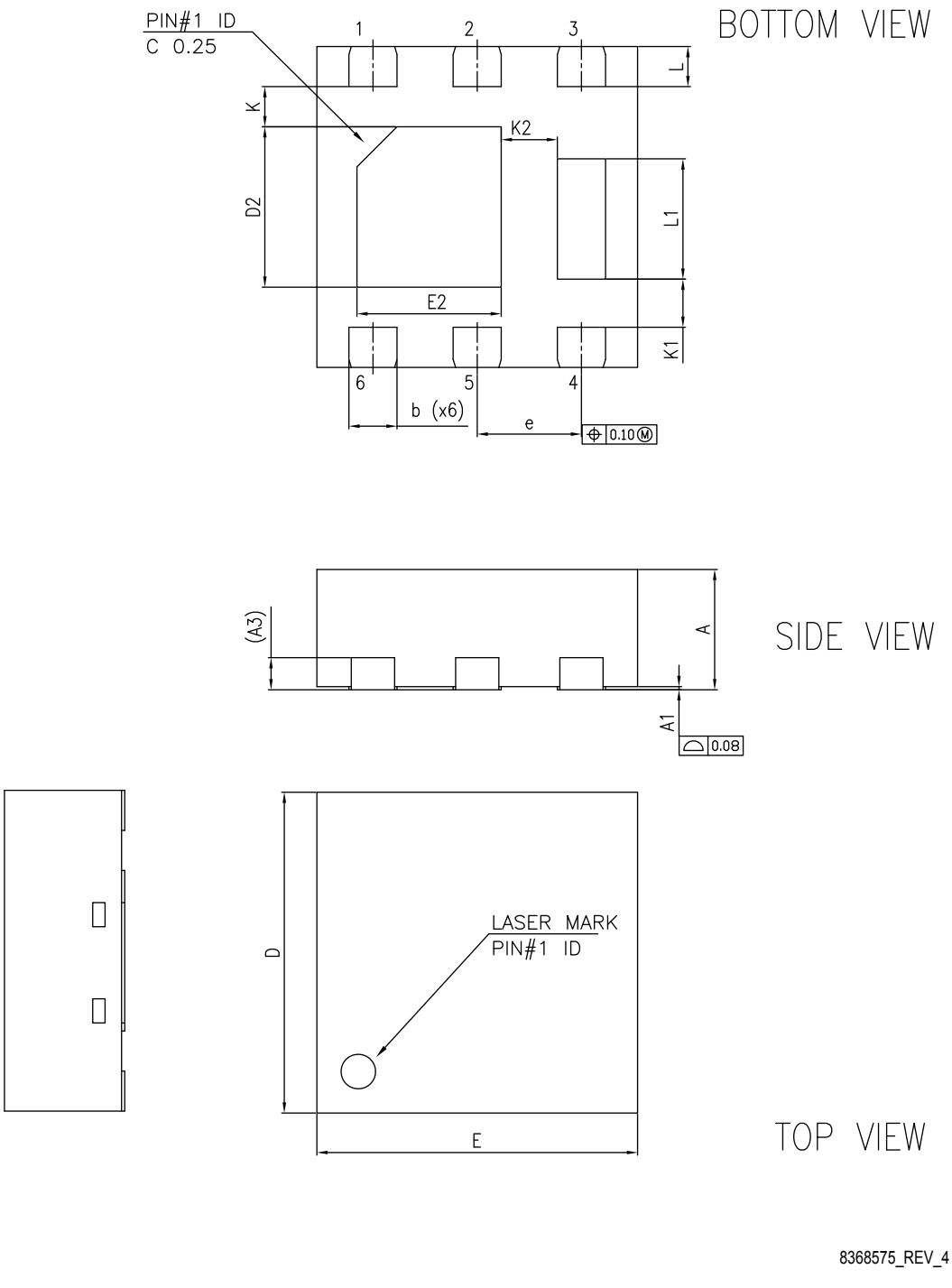


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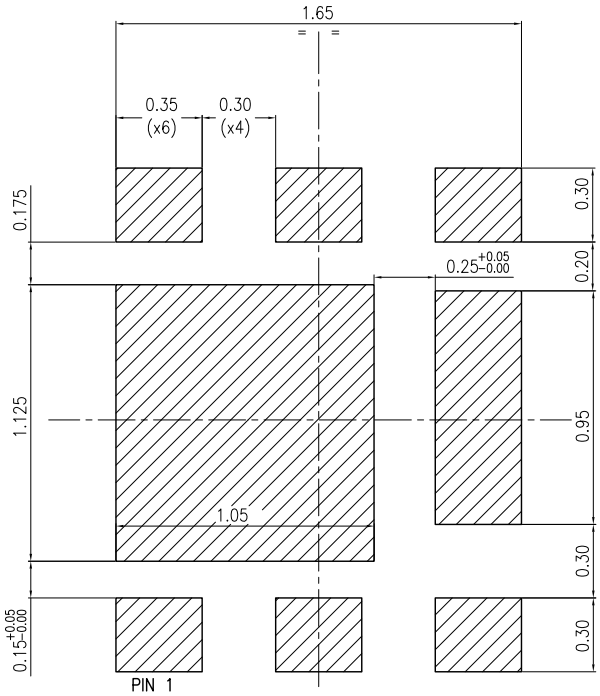
Table 7. **PowerFLAT 2x2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 16. **PowerFLAT 2x2 recommended footprint (dimensions are in mm)**



Footprint

Revision history

Table 8. **Document revision history**

Date	Version	Changes
09-May-2013	1	Initial revision.
09-Dec-2014	2	Text edits throughout document On cover page: – changed title description – updated features and description In Table 4, changed $R_{DS(on)}$ values In Table 5, changed values and test conditions In Table 6, changed values and test conditions In Table 7, changed values and test conditions Added Section 2.1: Electrical characteristics (curves) Updated Section 3: Test circuits Updated Section 4: Package mechanical data
27-Sep-2023	3	Updated Figure 1. Safe operating area. Updated Section 4 Package information. Minor text changes.

Contents

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