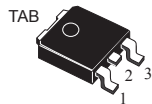
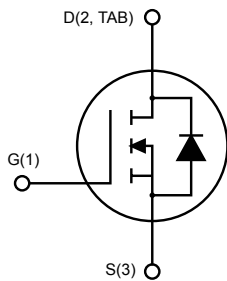



## Automotive-grade N-channel 500 V, 0.7 $\Omega$ typ., 7.5 A, MDmesh™ Power MOSFET in a DPAK package


**DPAK**


AM01475v1\_noZen

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD5NM50AG	500 V	0.8 $\Omega$	7.5 A

- AEC-Q101 qualified 
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. This device offers extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance which is superior to similar products on the market.

#### Product status link

[STD5NM50AG](#)

#### Product summary

<b>Order code</b>	STD5NM50AG
<b>Marking</b>	D5NM50
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Gate-source voltage	500	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	500	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7.5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.7	
$I_{DM}^{(1)}$	Drain current (pulsed)	30	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.25	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 oz Cu board

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{jmax}$ )	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	300	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, T_C = 125\text{ }^\circ\text{C}^{(1)}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.7	0.8	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance		-	415	-	pF
$C_{oss}$	Output capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	88	-	pF
$C_{rss}$	Reverse transfer capacitance		-	12	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	50	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC
$Q_{gs}$	Gate-source charge		-	5	-	nC
$Q_{gd}$	Gate-drain charge		-	6	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 2.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(Voff)}$	Off-voltage rise time	$V_{DD} = 400\text{ V}, I_D = 5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 17. Switching time waveform)	-	14	-	ns
$t_f$	Fall time		-	6	-	ns
$t_c$	Cross-over time		-	13	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		30	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 7.5\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$	-	185		ns
$Q_{rr}$	Reverse recovery charge		-	1.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	11.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	270		ns
$Q_{rr}$	Reverse recovery charge		-	1.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	12	

1. Pulse width is limited by safe operating area
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

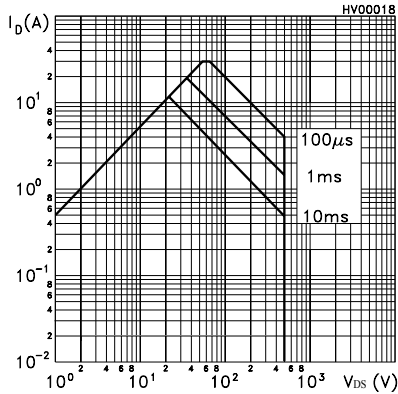


Figure 2. Thermal impedance

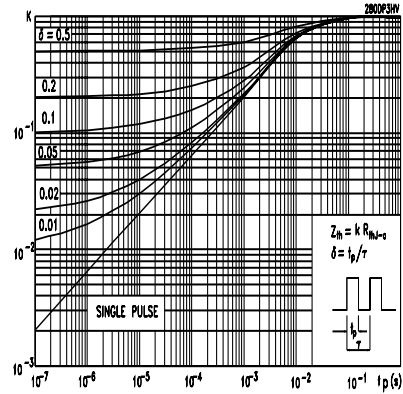


Figure 3. Output characteristics

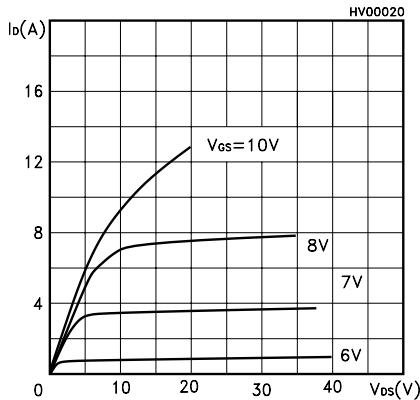


Figure 4. Transfer characteristics

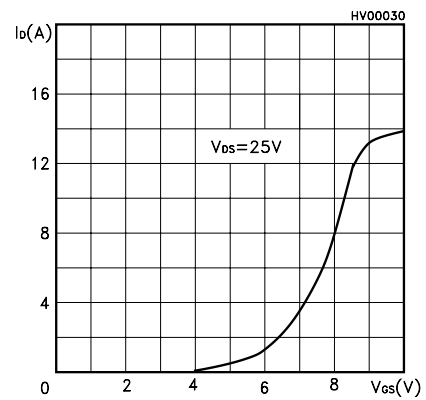


Figure 5. Normalized gate threshold voltage vs temperature

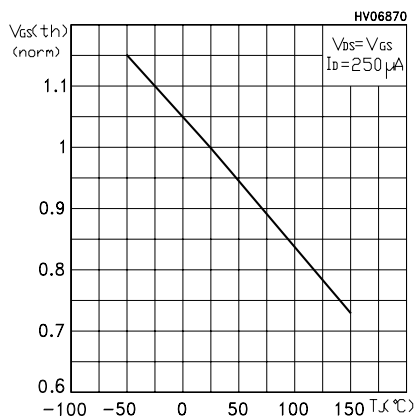
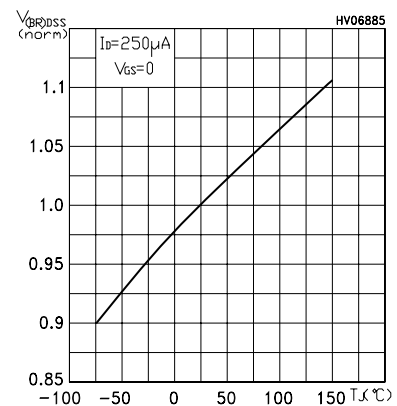
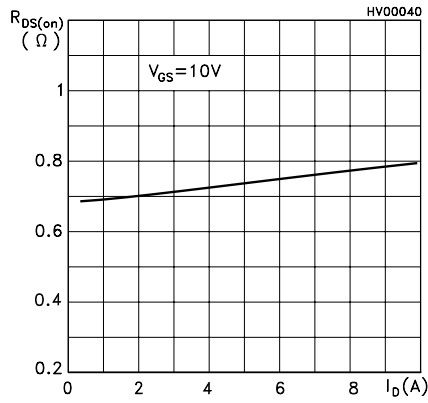


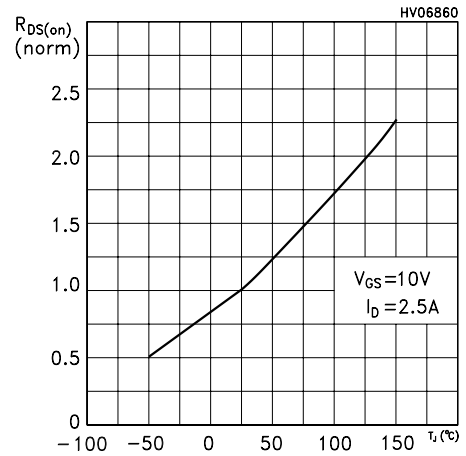
Figure 6. Normalized  $V_{(BR)DSS}$  vs temperature



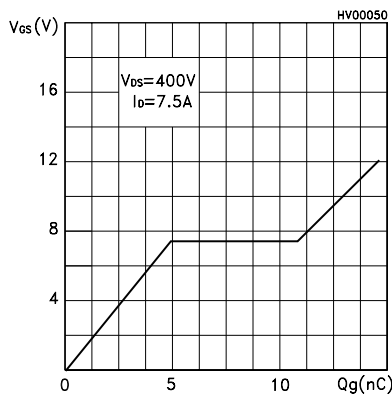
**Figure 7. Static drain-source on-resistance**



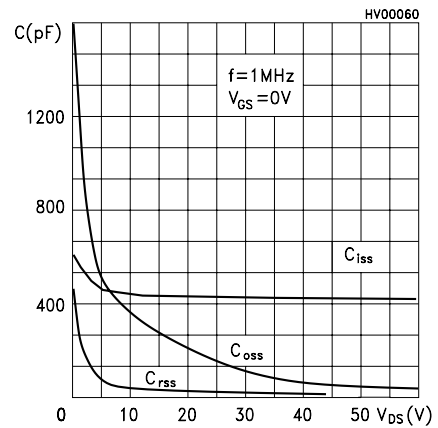
**Figure 8. Normalized on-resistance vs temperature**



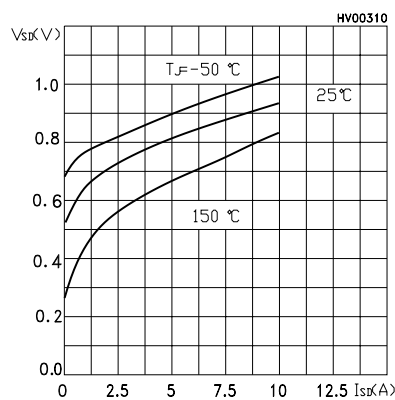
**Figure 9. Gate charge vs gate-source voltage**



**Figure 10. Capacitance variations**



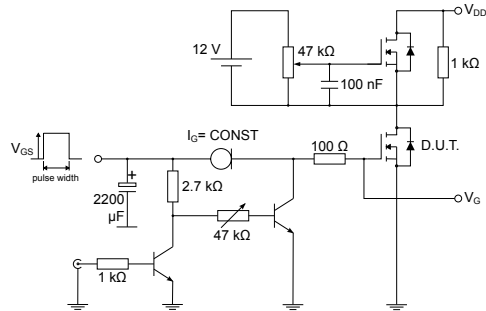
**Figure 11. Source-drain diode forward characteristics**



### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


AM01468v1

**Figure 13. Test circuit for gate charge behavior**


AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**

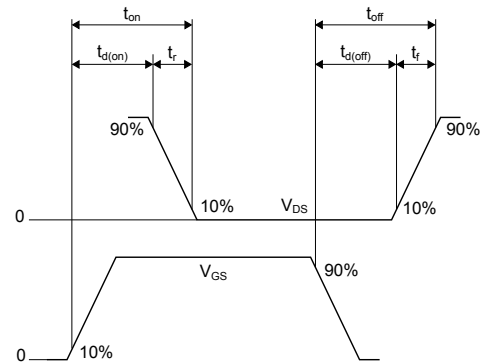

AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

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## 4 Package information

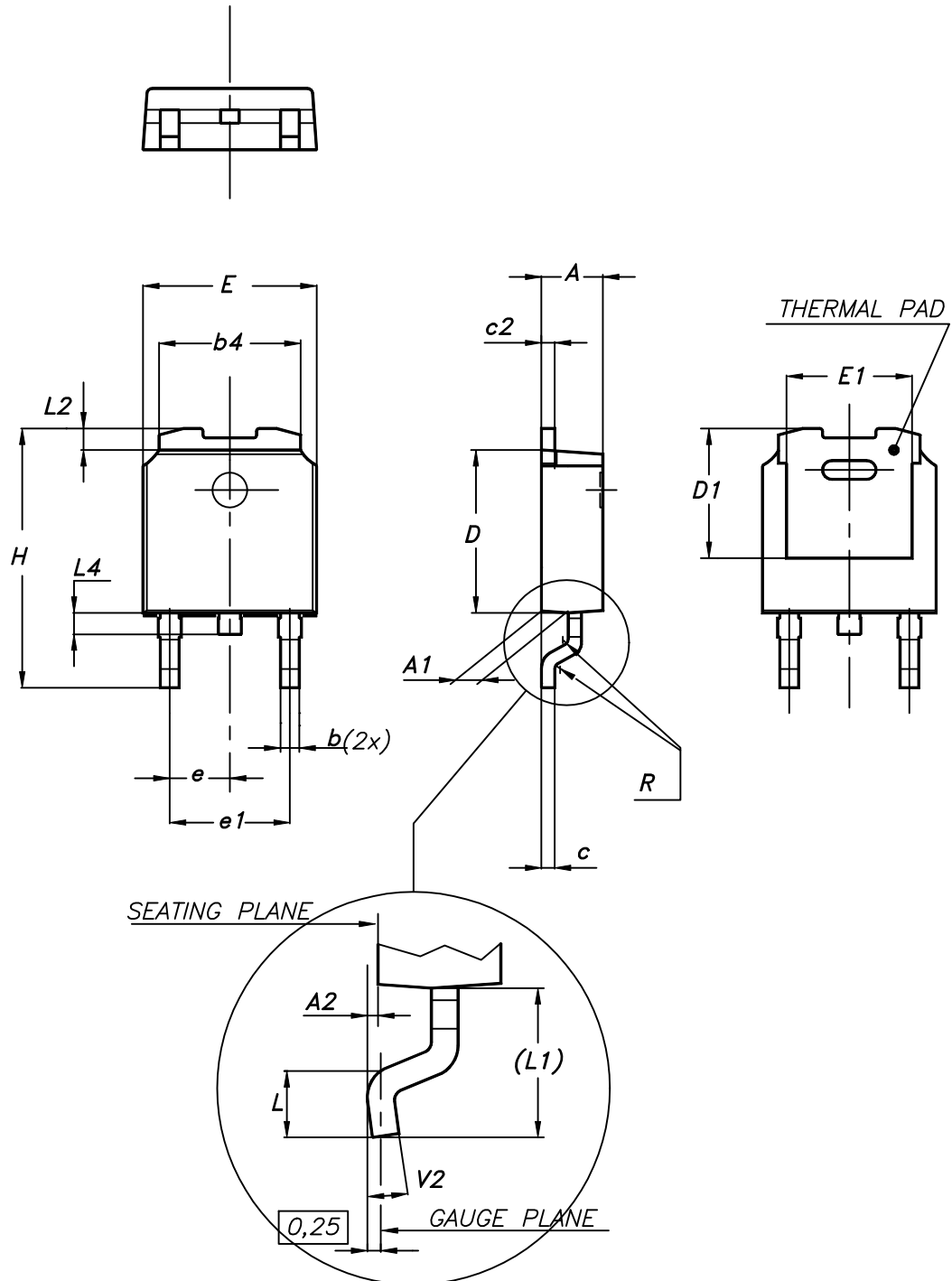
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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



### 4.1 DPAK (TO-252) type A2 package information

Figure 18. DPAK (TO-252) type A2 package outline

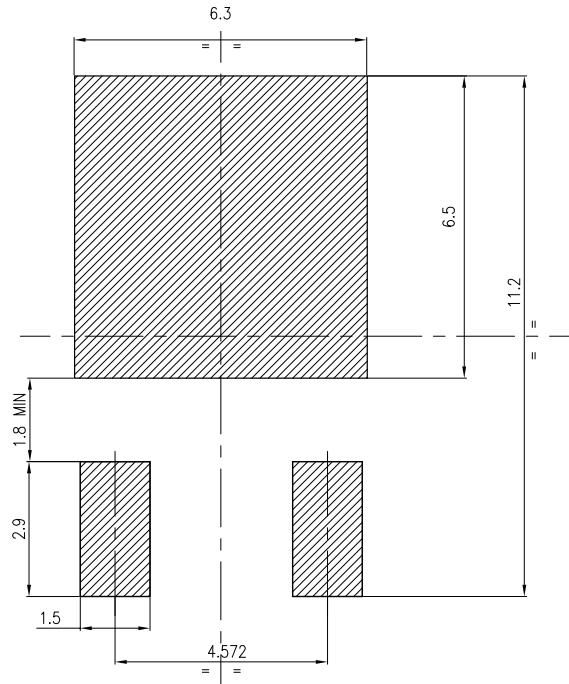


0068772\_type-A2\_rev25

**Table 8. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

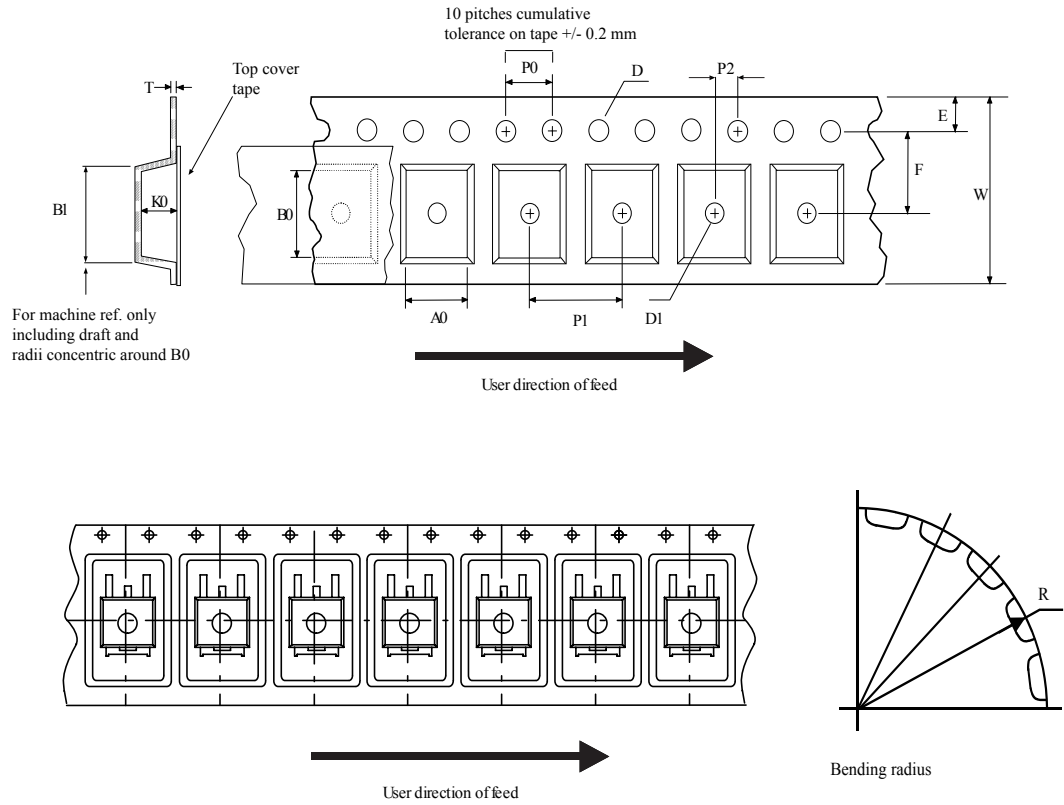
Figure 19. DPAK (TO-252) recommended footprint (dimensions are in mm)



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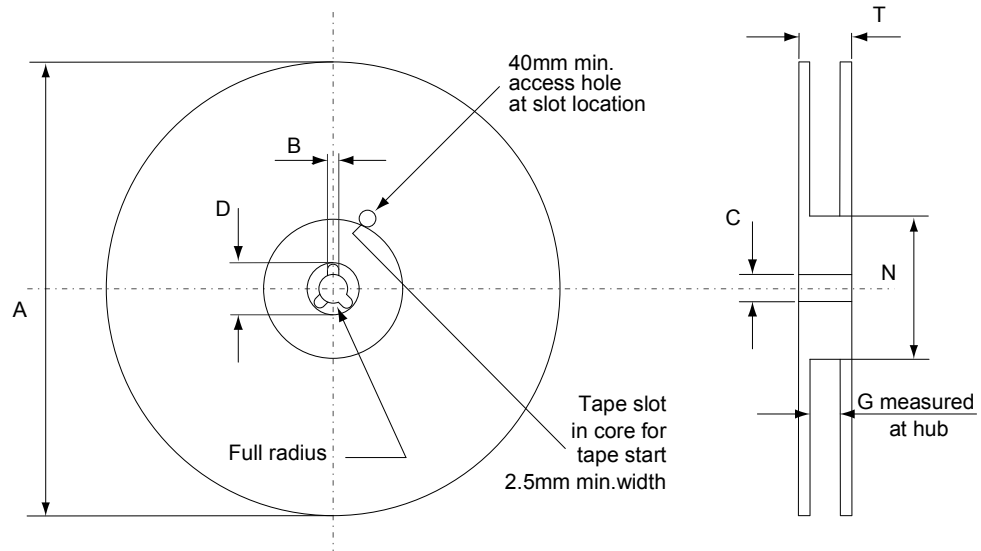
## 4.2 DPAK (TO-252) packing information

Figure 20. DPAK (TO-252) tape outline



AM08852v1

**Figure 21. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
12-Sep-2018	1	Initial release.

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