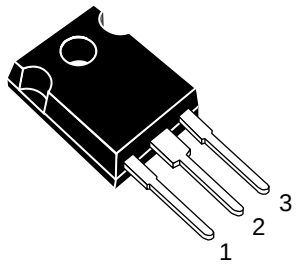
STW22N95K5

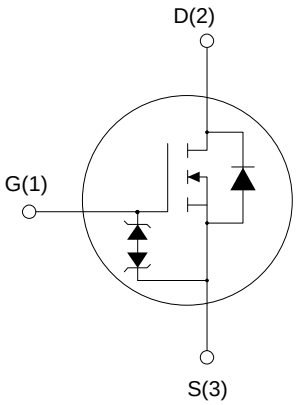
Automotive-grade N-channel 950 V, 0.280 Ω typ., 17.5 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data



TO-247

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW22N95K5	950 V	0.330 Ω	17.5 A	250 W

- AEC-Q101 qualified
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW22N95K5	22N95K5	TO-247	Tube

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	17.5	A
I_D	Drain current (continuous) at T_C = 100 °C	11	A
I_D (1)	Drain current (pulsed)	70	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
ESD	Gate-source human body model (R= 1.5 kΩ, C = 100 pF)	2	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 17.5 A, di/dt ≤ 100 A/µs; V_{DS} peak ≤ $V_{(BR)DSS}$

(3)V_{DS} ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax.}$)	6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	182	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	950			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 950 V			1	µA
		V_{GS} = 0 V, V_{DS} = 950 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		0.280	0.330	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1550	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}$(1)	Equivalent capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 760 V	-	65	-	pF
$C_{o(tr)}$(2)	Equivalent capacitance time related			178	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz , I_D = 0 A	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 17.5 A V_{GS}= 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	48	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	32.5	-	nC

Notes:

(1)$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

(2)$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 475 V, I_D = 9 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 15: "Test circuit for resistive load switching times"* and *Figure 20: "Switching time waveform"*)	-	18	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	65	-	ns
t_f	Fall time		-	18	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		70	A
V_{SD}(2)	Forward on voltage	I_{SD} = 17.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 17.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	513		ns
Q_{rr}	Reverse recovery charge		-	12		µC
I_{RRM}	Reverse recovery current		-	46		A
t_{rr}	Reverse recovery time	I_{SD} = 17.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	670		ns
Q_{rr}	Reverse recovery charge		-	15		µC
I_{RRM}	Reverse recovery current		-	44		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

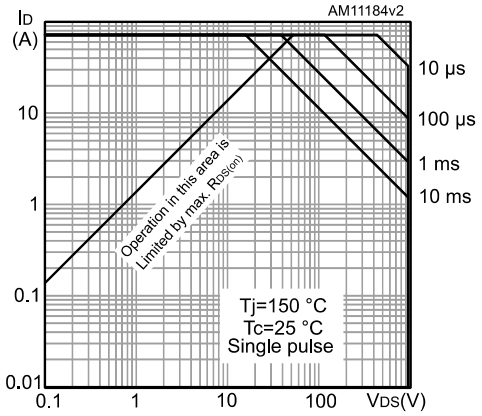


Figure 3: Thermal impedance

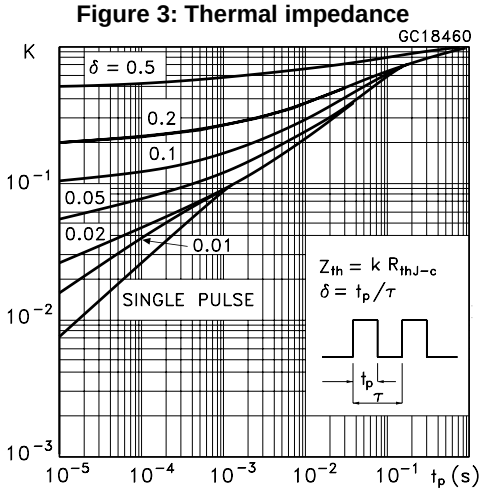


Figure 4: Output characteristics

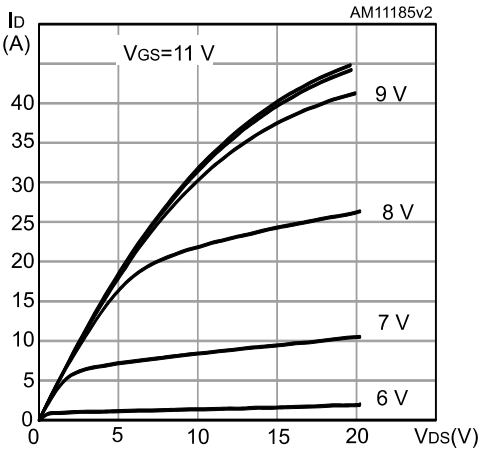


Figure 5: Transfer characteristics

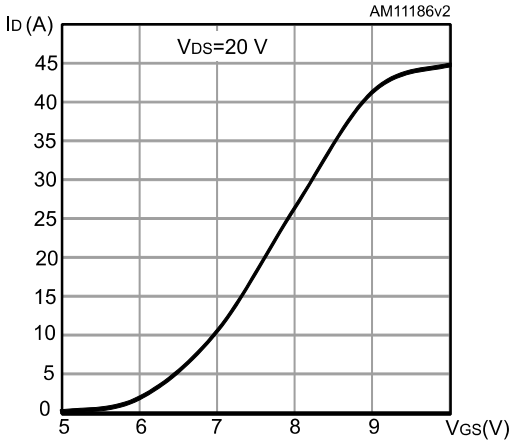


Figure 6: Gate charge vs gate-source voltage

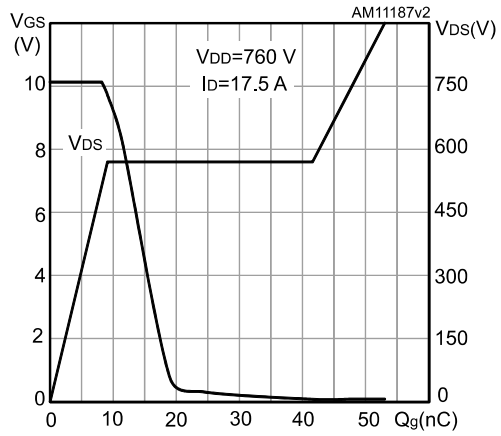


Figure 7: Static drain-source on-resistance

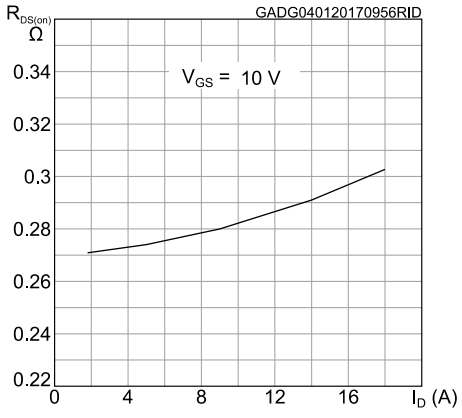


Figure 8: Capacitance variation

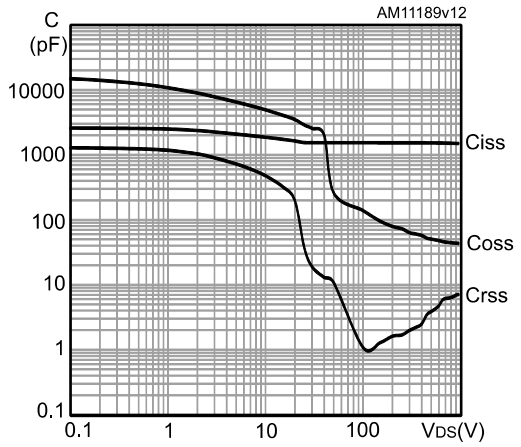


Figure 9: Output capacitance stored energy

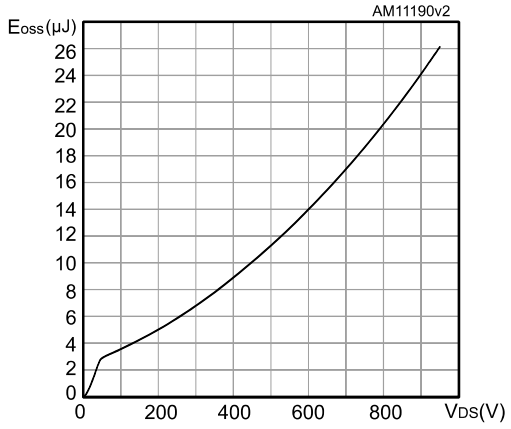


Figure 10: Normalized gate threshold voltage vs temperature

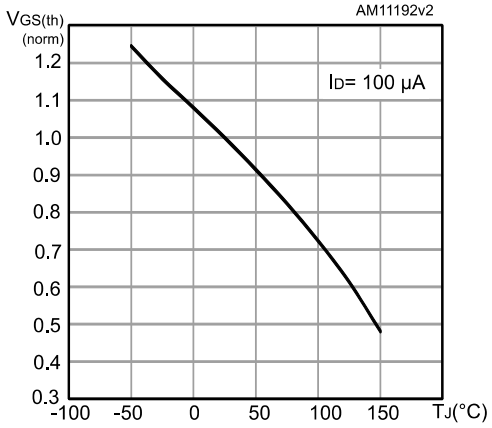


Figure 11: Normalized on-resistance vs temperature

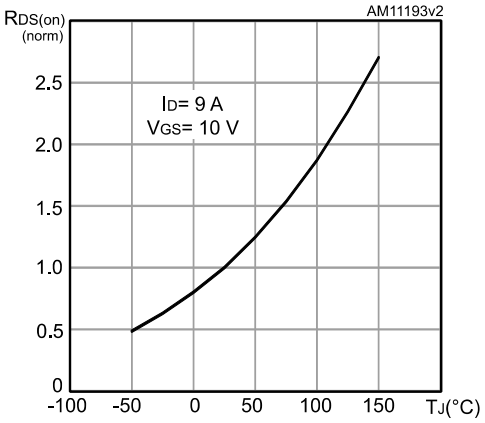


Figure 12: Maximum avalanche energy vs starting T_J

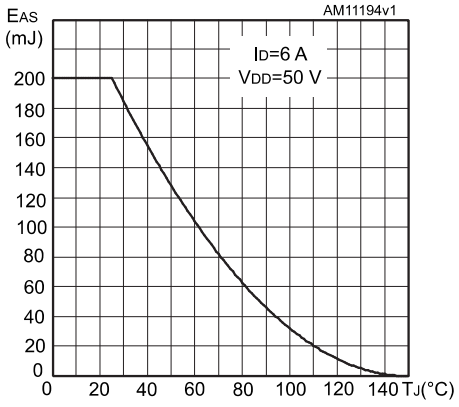


Figure 13: Normalized $V_{(BR)DSS}$ vs temperature

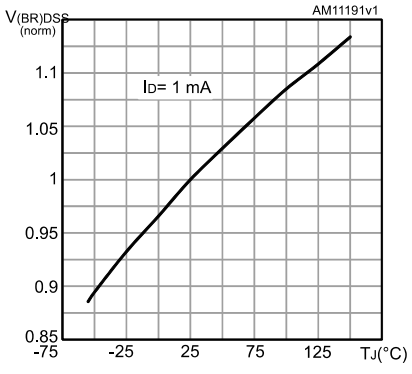
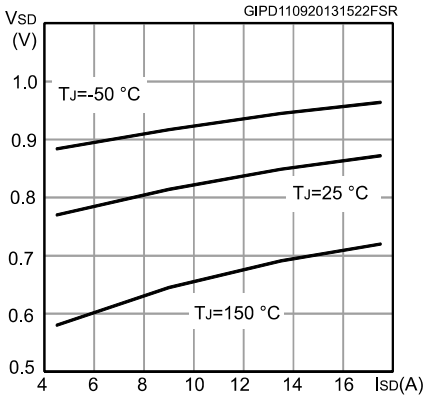


Figure 14: Source-drain diode forward characteristics



3 Test circuits

Figure 15: Test circuit for resistive load switching times

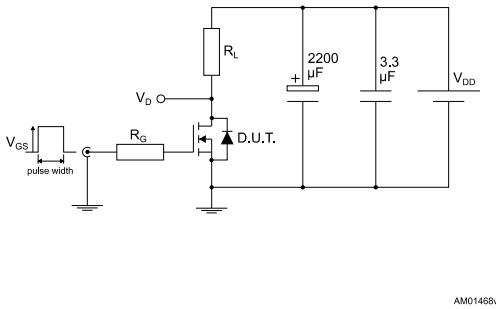


Figure 16: Test circuit for gate charge behavior

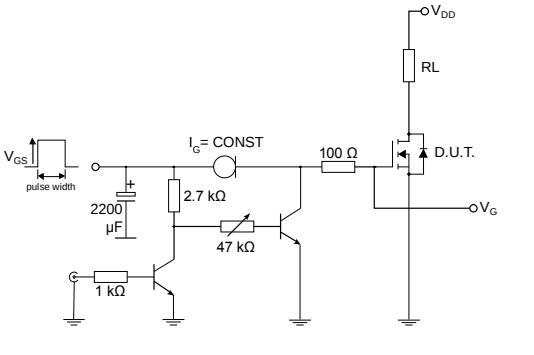


Figure 17: Test circuit for inductive load switching and diode recovery times

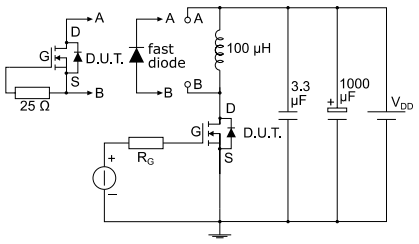


Figure 18: Unclamped inductive load test circuit

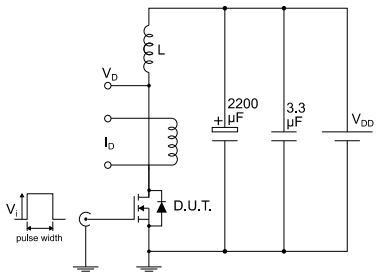


Figure 19: Unclamped inductive waveform

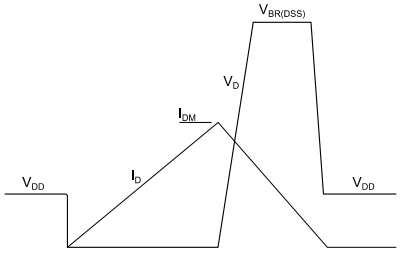
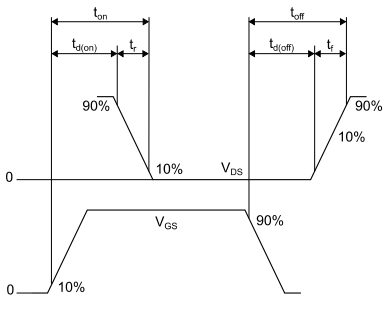


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 21: TO-247 package outline

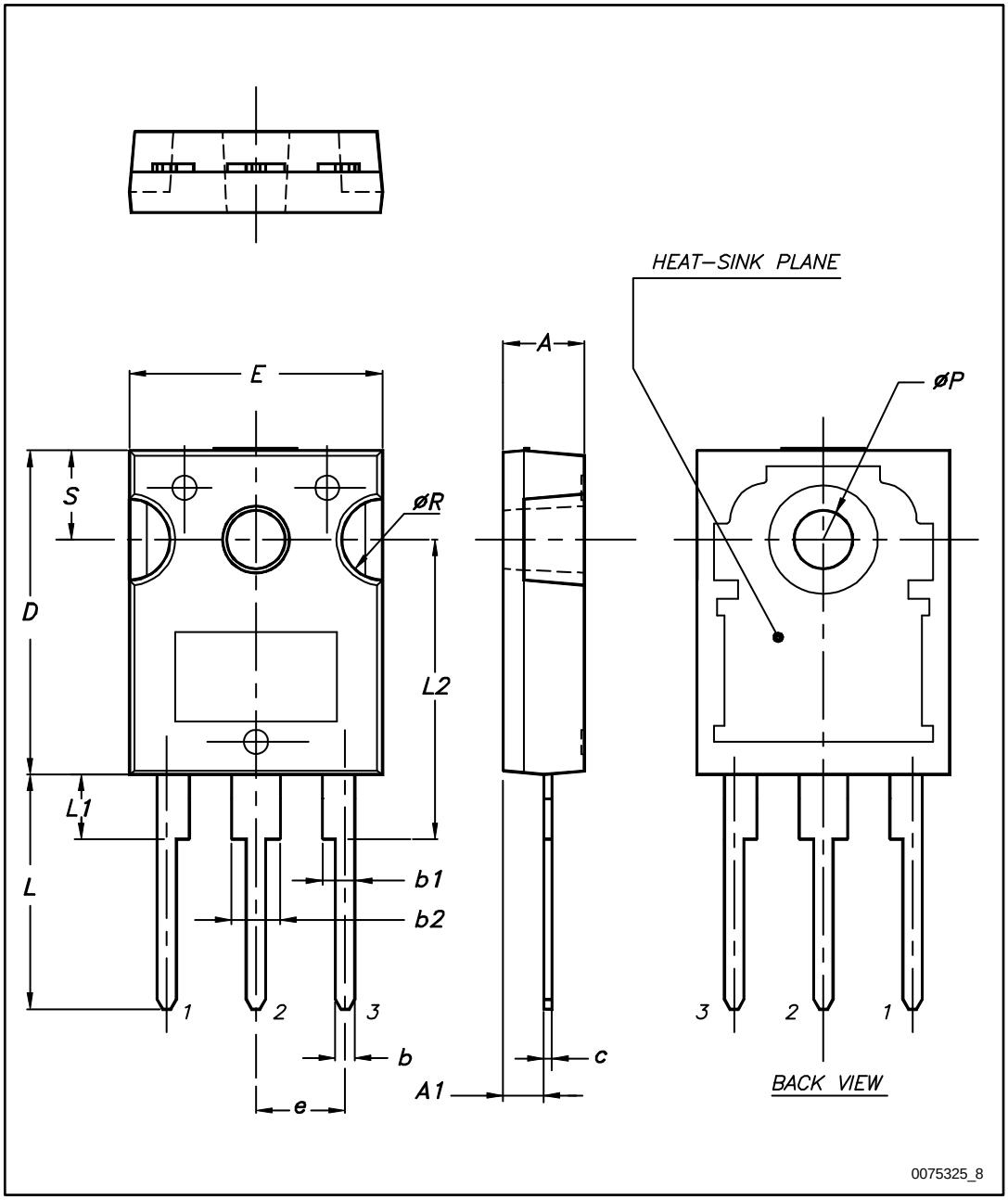


Table 10: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
17-Oct-2013	1	First release.
19-Dec-2013	2	Datasheet promoted from preliminary to production data Modified: title and *Features* Minor text changes
20-Mar-2014	3	– Modified: note 3 in Table 2 – Modified: Q_{gs} and Q_{gd} typical values in *Table 5* – Modified: typical values in *Table 6* and *7* – Updated: *Figure 6* – Minor text changes
11-Jan-2017	4	Updated title, features and description in cover page. Minor text changes in *Section 1: "Electrical ratings"* and *Section 2: "Electrical characteristics"*. Changed *Figure 7: "Static drain-source on-resistance"*.

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