

N-channel 650 V, 0.185  $\Omega$  typ., 16 A MDmesh M2 Power MOSFET in D2PAK, TO-220FP and TO-220 packages

Datasheet - production data

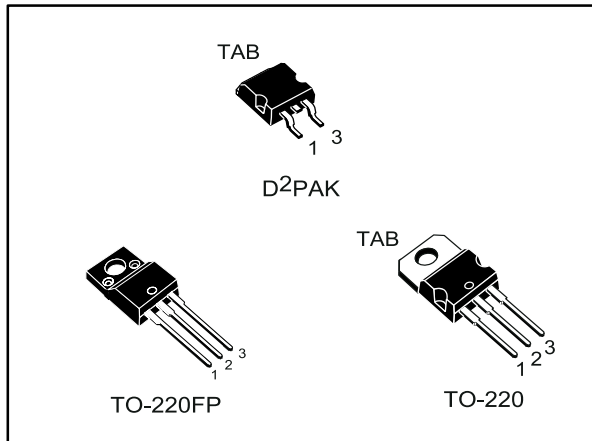
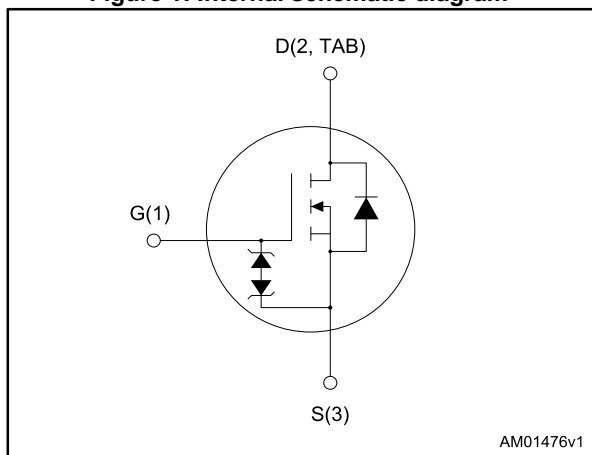


Figure 1: Internal schematic diagram



## Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STB24N65M2	650 V	0.23 $\Omega$	16 A
STF24N65M2			
STP24N65M2			

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STB24N65M2	24N65M2	D <sup>2</sup> PAK	Tape and reel
STF24N65M2		TO-220FP	Tube
STP24N65M2		TO-220	

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK TO-220	TO-220FP	
V <sub>GS</sub>	Gate-source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	16	16 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	10	10 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	64	64 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	150	30	W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)		2500	V
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature			

**Notes:**

<sup>(1)</sup>Limited by maximum junction temperature.

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup>I<sub>SD</sub> ≤ 16 A, di/dt ≤ 400 A/μs; V<sub>D(peak)</sub> < V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 80% V<sub>(BR)DSS</sub>.

<sup>(4)</sup>V<sub>DS</sub> ≤ 520 V

**Table 3: Thermal data**

Symbol	Parameter	Value			Unit
		D <sup>2</sup> PAK	TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.83		4.2	°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max <sup>(1)</sup>	30			°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		62.5		°C/W

**Notes:**

<sup>(1)</sup>When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	2.2	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> =25°C, I <sub>D</sub> = I <sub>AR</sub> ; V <sub>DD</sub> =50V)	650	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$		0.185	0.23	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1060	-	pF
$C_{oss}$	Output capacitance		-	47.5	-	pF
$C_{riss}$	Reverse transfer capacitance		-	1.65	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0$	-	229	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 16\text{ A}$ , $V_{GS} = 10\text{ V}$	-	29	-	nC
$Q_{gs}$	Gate-source charge		-	3.8	-	nC
$Q_{gd}$	Gate-drain charge		-	14	-	nC

**Notes:**

<sup>(1)</sup>  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$ , $I_D = 8\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	10	-	ns
$t_r$	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	68	-	ns
$t_f$	Fall time		-	25.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16 \text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 16 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$	-	350		ns
$Q_{rr}$	Reverse recovery charge		-	4.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	26		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 16 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$	-	496		ns
$Q_{rr}$	Reverse recovery charge		-	6.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	25.5		A

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

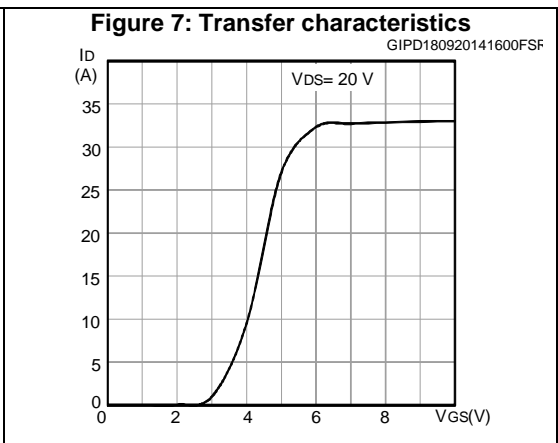
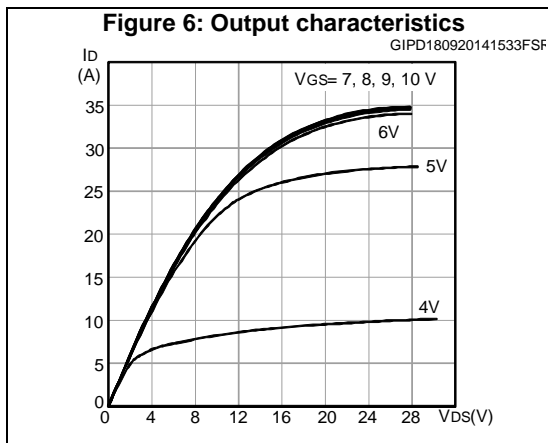
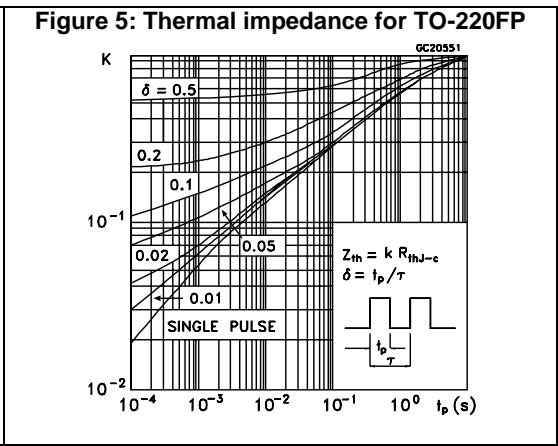
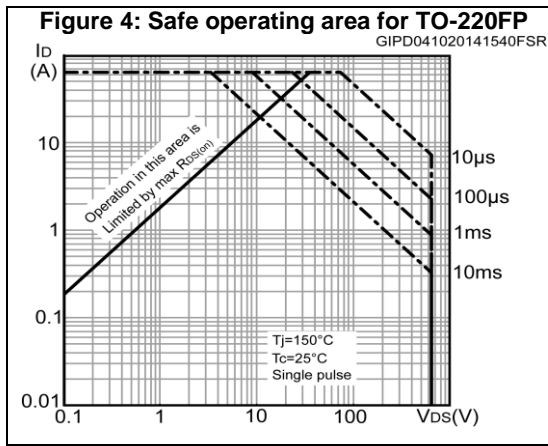
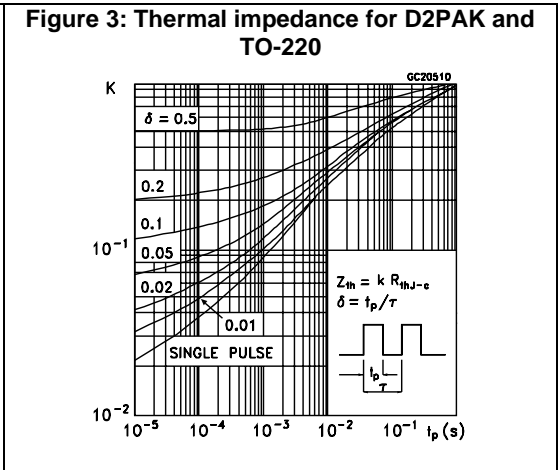
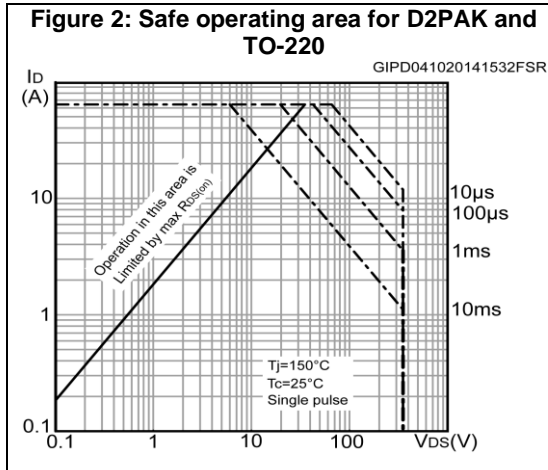


Figure 8: Gate charge vs gate-source voltage

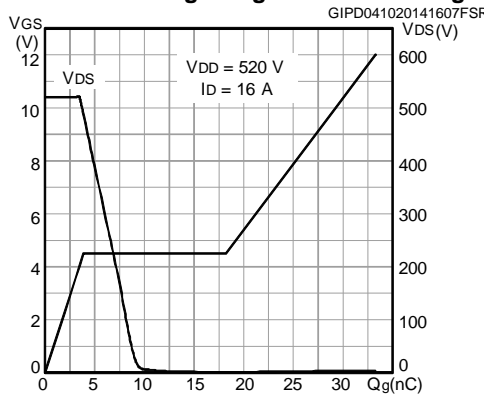


Figure 9: Static drain-source on-resistance

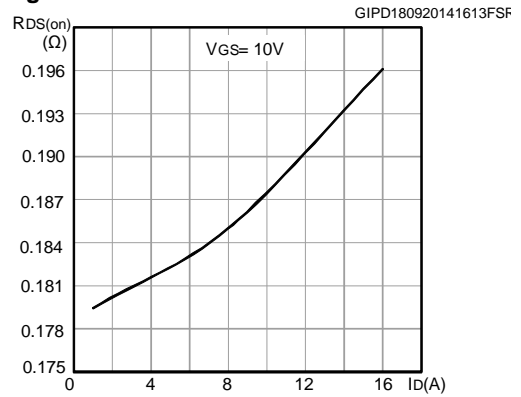


Figure 10: Capacitance variations

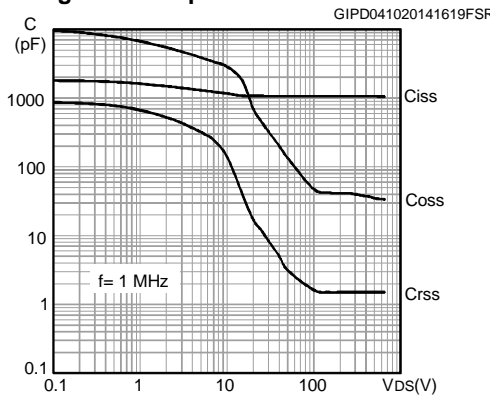


Figure 11: Normalized gate threshold voltage vs temperature

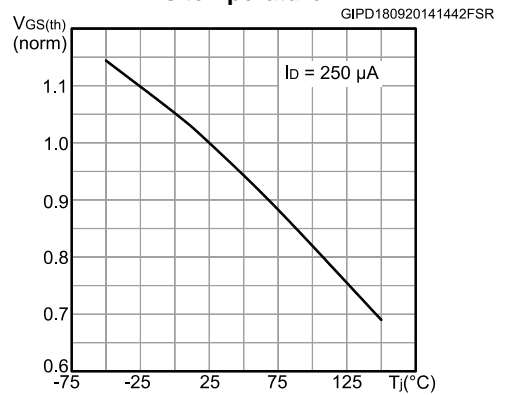


Figure 12: Normalized on-resistance

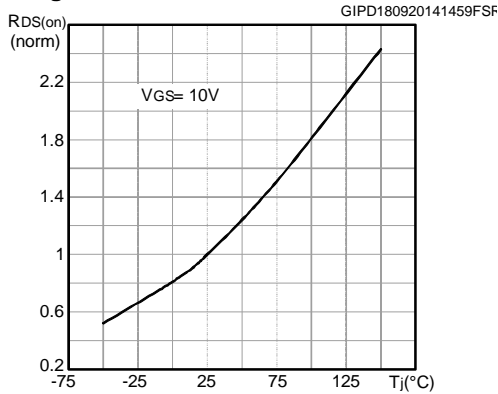


Figure 13: Normalized V(BR)DSS vs temperature

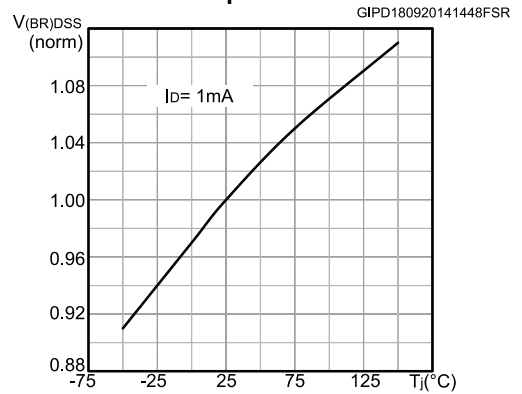


Figure 14: Source-drain diode forward characteristics

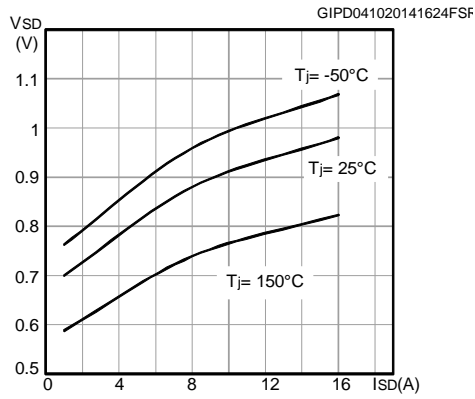
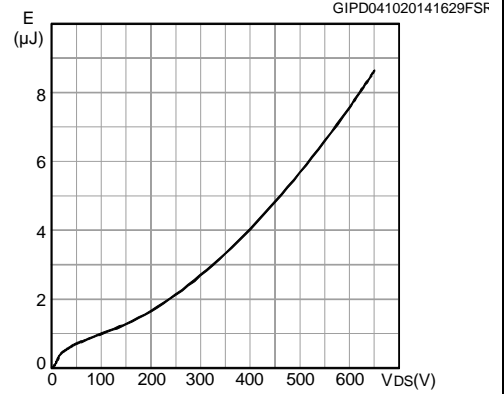
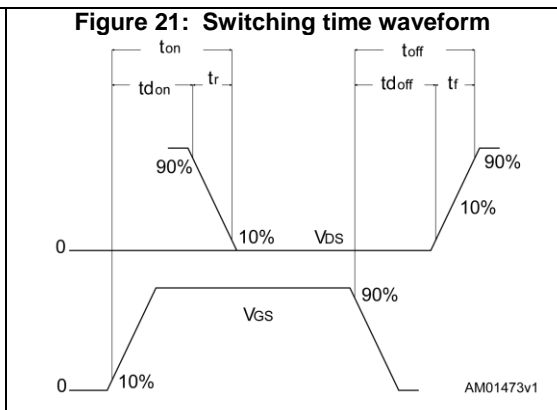
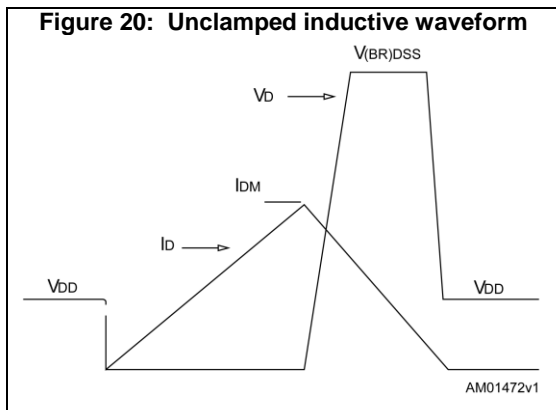
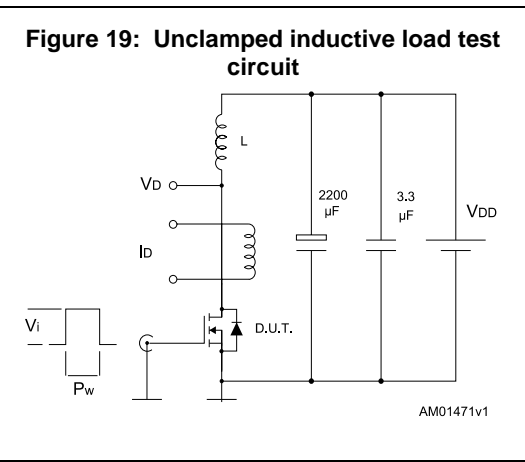
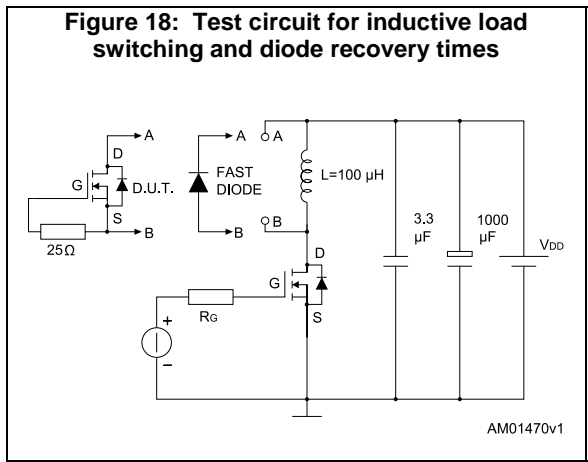
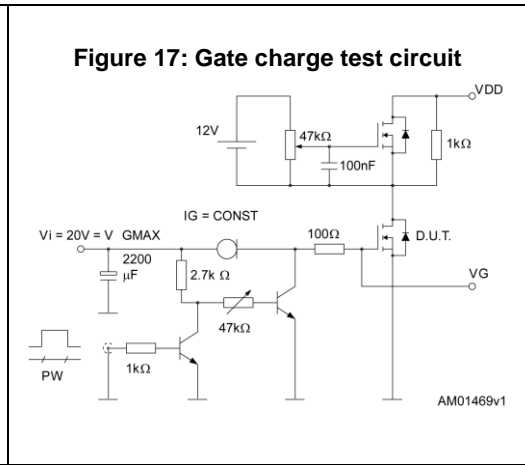
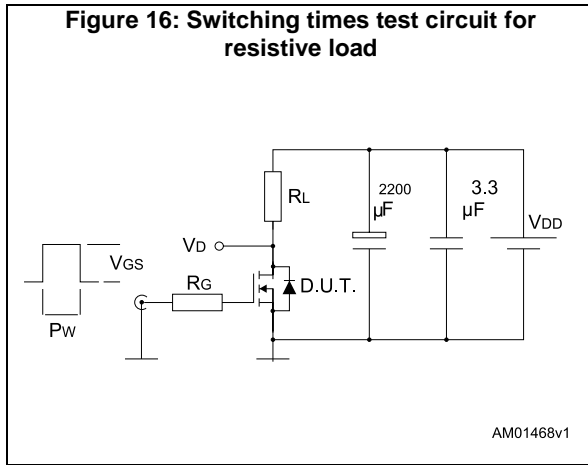


Figure 15: Output capacitance stored energy





### 3 Test circuits



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D2PAK package information

Figure 22: D<sup>2</sup>PAK (TO-263) drawing

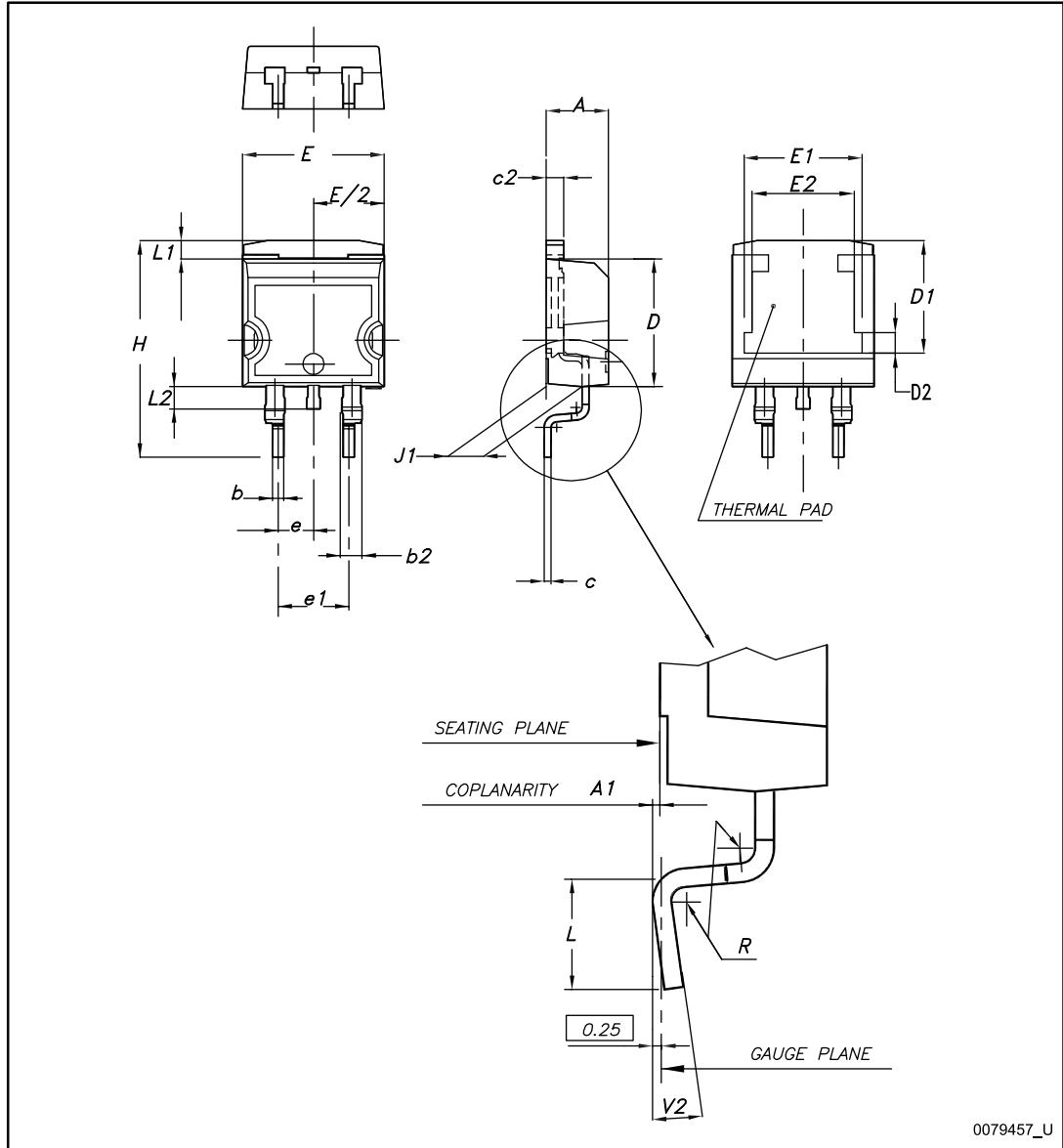
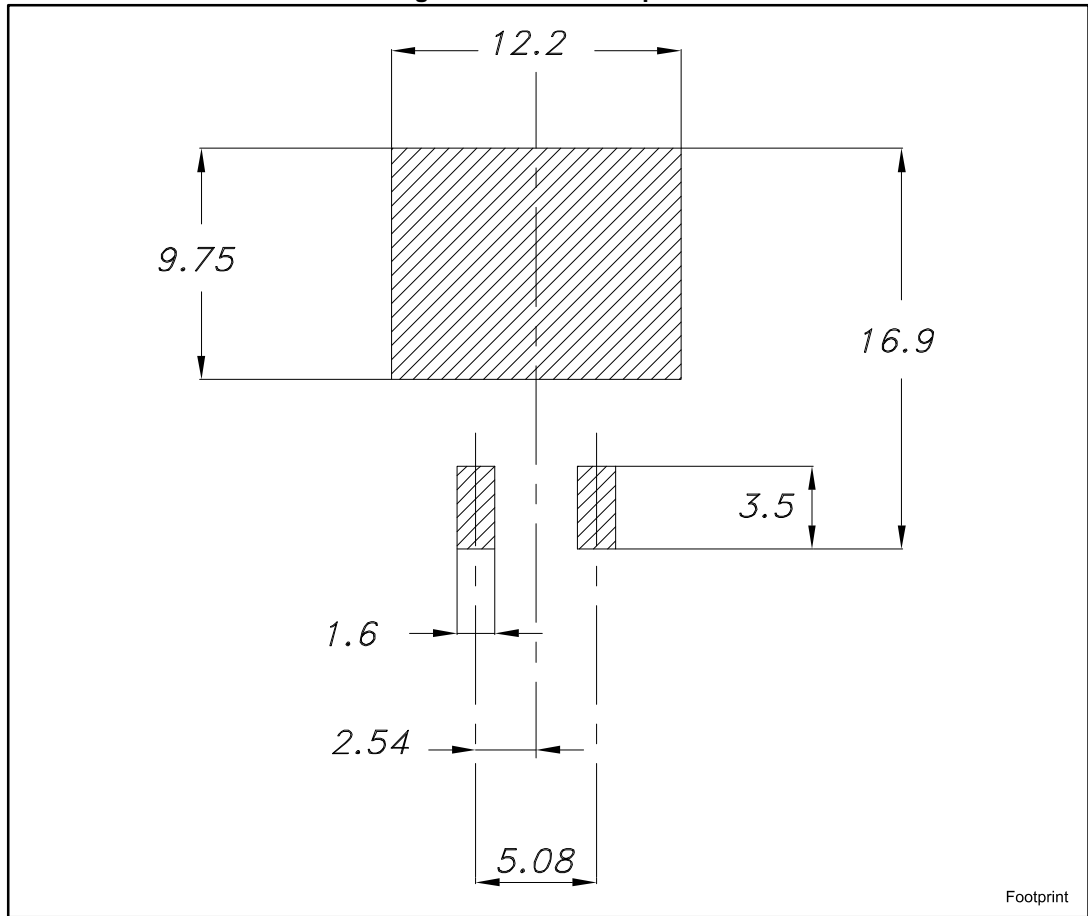


Table 9: D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

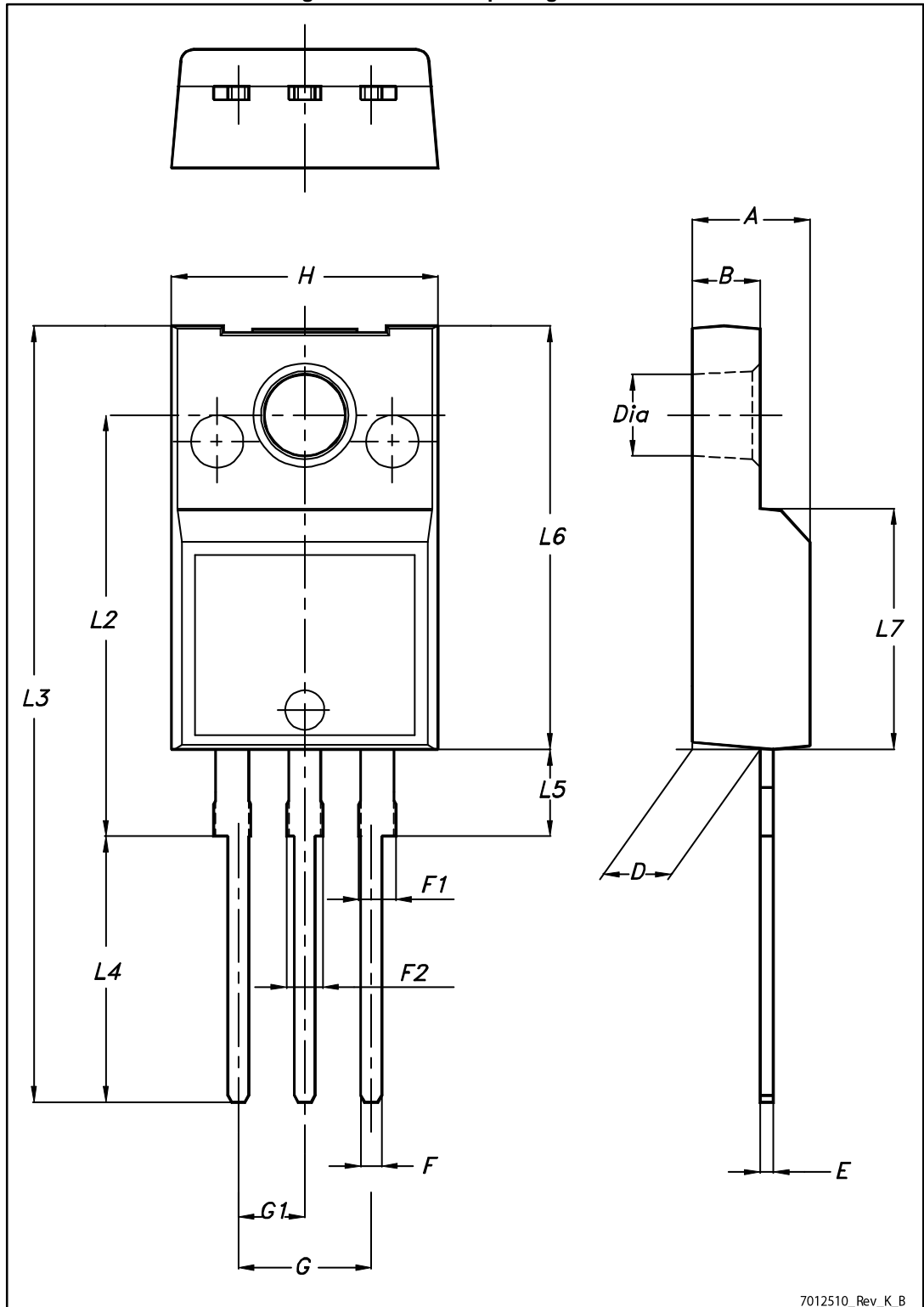
Figure 23: D<sup>2</sup>PAK footprint



All the dimensions are in millimeters.

### 4.2 TO-220FP package information

Figure 24: TO-220FP package outline



7012510\_Rev\_K\_B

Table 10: TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.3 TO-220 type A package information

Figure 25: TO-220 type A package outline

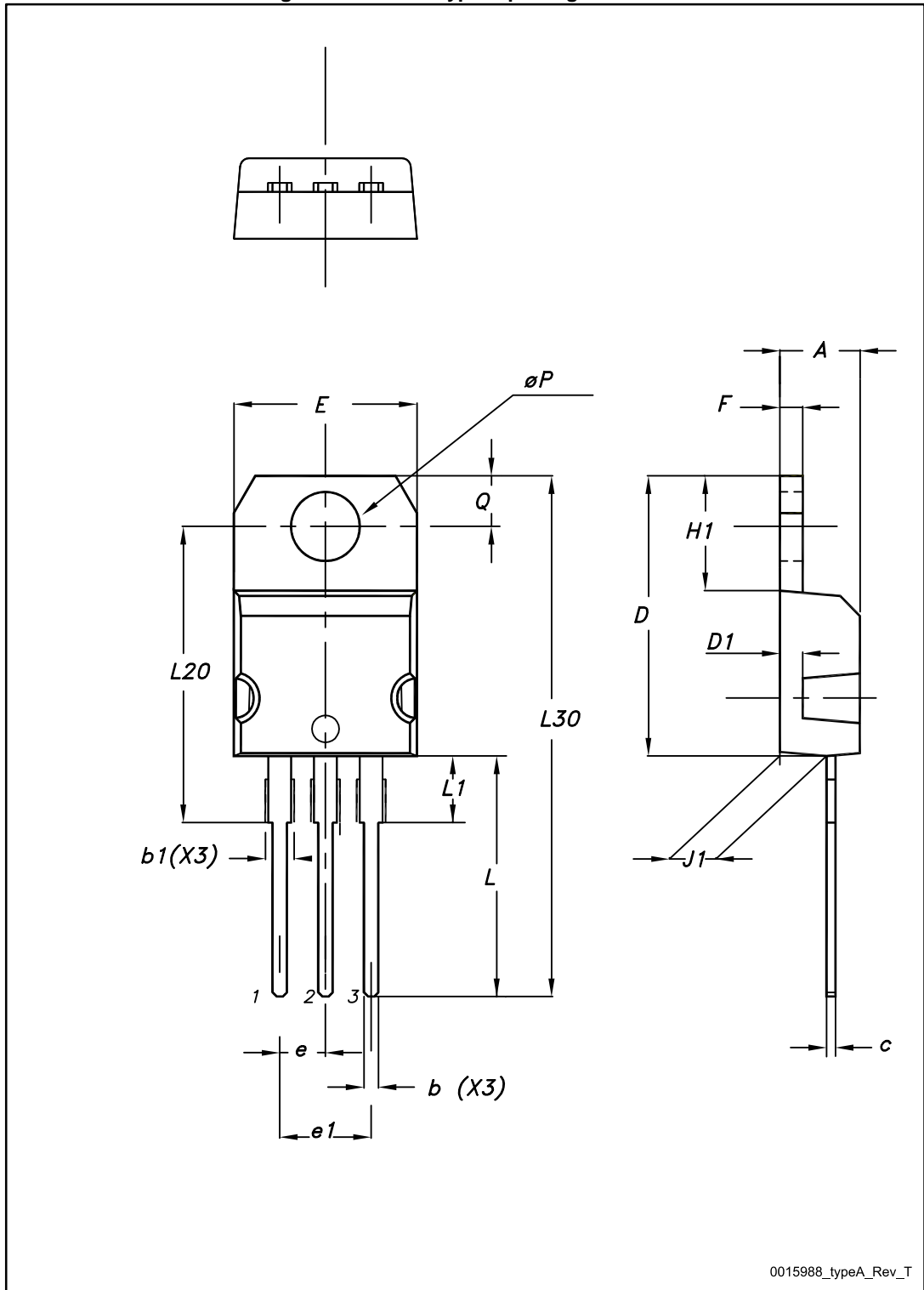


Table 11: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95



# 5 Packaging mechanical data

**Figure 26: Tape**

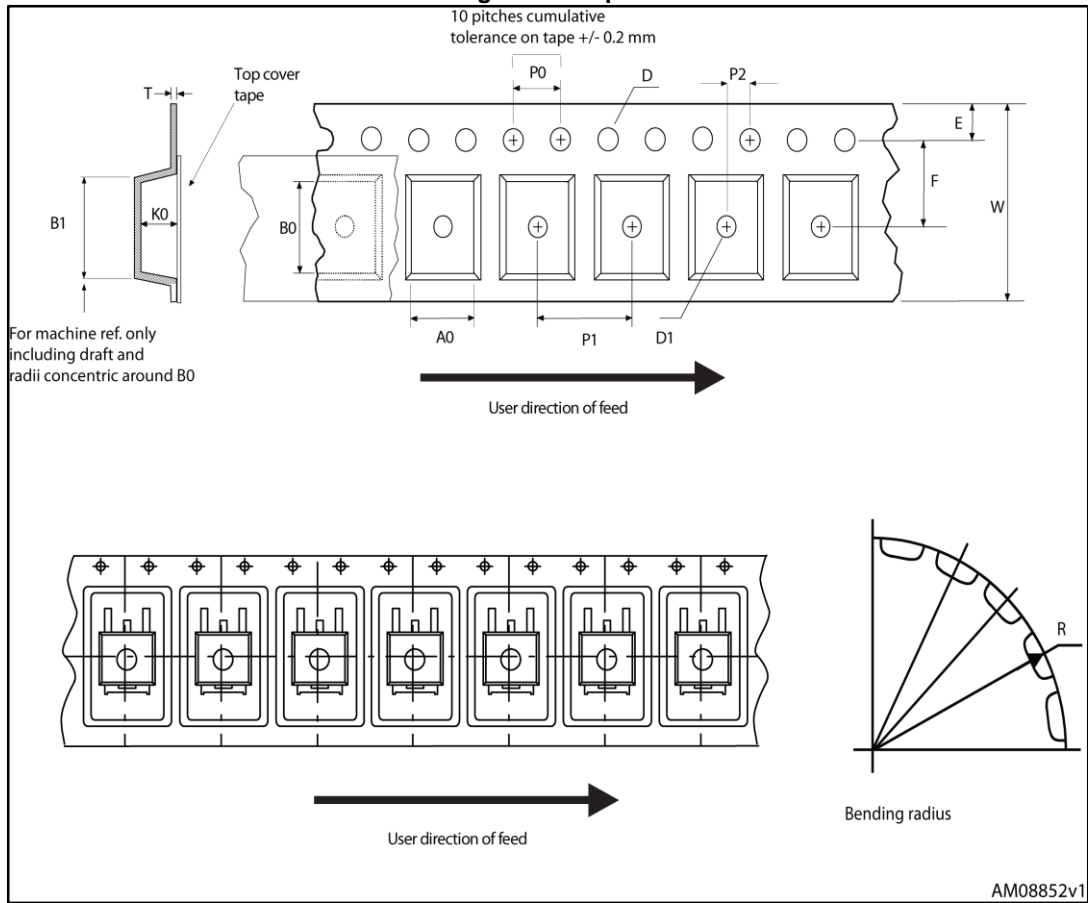


Figure 27: Reel

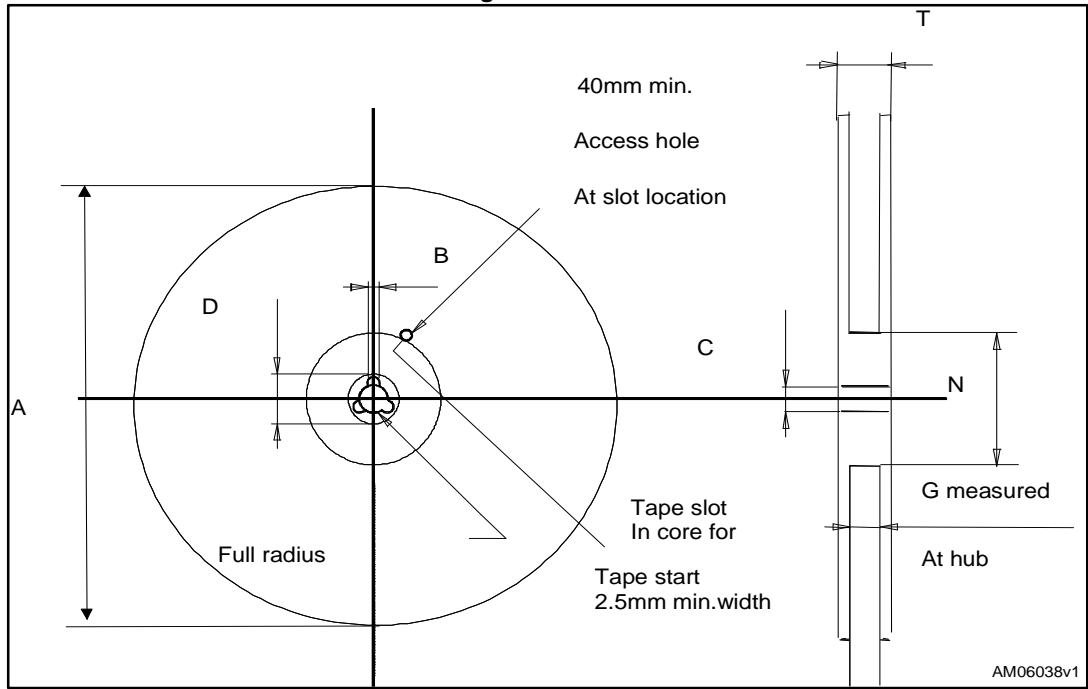


Table 12: D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

Table 13: Document revision history

Date	Revision	Changes
09-Jun-2014	1	First release.
11-Nov-2014	2	Document status promoted from preliminary to production data.

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