![ST logo]

TSH122

Ultra low power video buffer/filter with power-down

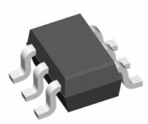
Features

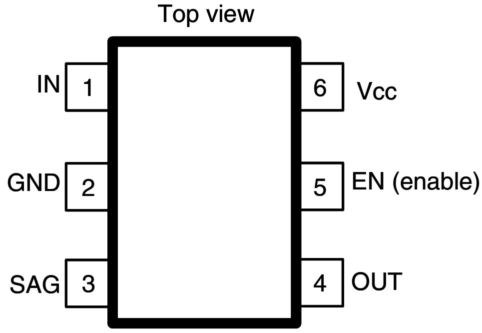
- Very low consumption: 1.7 mA
- Ultra low power-down mode: 4 nA typ., 500 nA max.
- Internal 6th order reconstruction filter
- Internal gain of 6 dB
- Rail-to-rail output buffer for 75 Ω video line
- Excellent video performance
  - Differential gain 0.5%
  - Differential phase 0.10°
  - Group delay of 10 ns
- SAG correction
- Bottom of video signal close to 0 V
- Tested with 2.5 V and 3.3 V single supply
- Data min. and max. are physically tested and guaranteed during production (consumption, gain, filtering, and other parameters are guaranteed)

Applications

- Mobile phones
- Digital still camera
- Digital video camera
- Portable DVD players

SC70





Description

The TSH122 is a video buffer that uses a voltage feedback amplifier, with an internal gain of 6 dB, an output rail-to-rail, an internal input DC-shift and a SAG correction. A power-down function allows switching to a sleep mode with an ultra-low consumption.

The TSH122 features a 6th-order internal reconstruction filter to attenuate the parasitic frequency of 27 MHz from the clock of the video DAC.

The TSH122 operates from 2.25 to 5 V single power supplies and is tested at 2.5 V and 3.3 V.

The TSH122 is a single operator available in a tiny SC70 plastic package for space saving.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage[1]	5.5	V
V_{in}	Maximum input amplitude	0 to Vcc	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	SC70 thermal resistance junction to ambient area	205	°C/W
R_{thjc}	SC70 thermal resistance junction to case	172	°C/W
P_{max}	Maximum power dissipation for Tj=150°C T_{amb} = +25°C T_{amb} = +85°C	 609 317	mW
ESD	CDM: charged device model[2] HBM: human body model[3] MM: machine model[4]	1.5 1.5 300	kV kV V
	Output short-circuit	[5]	

1. All voltage values, except differential voltage, are with respect to network terminal.
2. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
3. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
4. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating
5. An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on amplifiers.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	2.25 to 5 [1]	V
T_{oper}	Operating free air temperature range	-40 to +85	°C

1. Tested in full production at 0 V/2.5 V and 0 V/3.3 V single power supply.

2 Electrical characteristics

Table 3. V_{CC} = +2.5V, +3.3V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{dc}	Output DC level shift	$R_L = 150\Omega$	70	115	168	mV
I_{ib}	Input bias current	V_{CC} = +3.3V	-1.5	-0.87		µA
		V_{CC} = +3.3V, $T_{min} \le T_{amb} \le T_{max}$		-0.93		
G	Internal voltage gain	V_{in}=0V to 1V DC, V_{CC}=+2.5V	5.8	6	6.1	dB
		V_{in}=0V to 1.4V DC, V_{CC}=+3.3V	5.8	6	6.1	
		V_{CC}=3.3V $T_{min} \le T_{amb} \le T_{max}$		5.96		
PSRR	Power supply rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{out}$)	ΔV_{CC}=±100mV at 1kHz Vin=+0.5V DC		55		dB
I_{CC}	Positive supply current DC consumption	V_{in}=0V, no load V_{CC}=+3.3V V_{CC}=+2.5V		2 1.7	2.4 2.1	mA
		V_{CC}=+3.3V $T_{min} \le T_{amb} \le T_{max}$		2.4		mA
Dynamic performance and output characteristics						
BW	Filter bandwidth	Small signal V_{CC}=+3.3V, $R_L = 150\Omega$ -3dB bandwidth -1dB bandwidth	5.4	9.5 7.2		MHz
		-1dB bandwidth V_{CC} = +3.3V, $T_{min} \le T_{amb} \le T_{max}$		6.75		
FR	27 MHz rejection	Small signal V_{CC}=+3.3V, R_L=150Ω	36	47		dB
		V_{CC} = +3.3V, $T_{min} \le T_{amb} \le T_{max}$		46		dB
ΔG	Differential gain	V_{CC}=+3.3V, R_L=150Ω		0.5		%
ΔΦ	Differential phase	V_{CC}=+3.3V, R_L=150Ω		0.1		°
Gd	Group delay	V_{CC}=+3.3V, 10kHz-5MHz		6		ns
V_{OH}	High level output voltage	V_{CC}=+3.3V, R_L=150Ω V_{CC}=+2.5V, R_L=150Ω	3.1 2.3	3.2 2.4		V

Table 3. V_{CC} = +2.5V, +3.3V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	R_L = 150Ω		11	40	mV
I_{out}	Output short circuit current	V_{CC}=+2.5V		75		mA
Noise and distortion						
eN	Total output noise	F = 100kHz, no load		51		nV/√Hz
HD	Harmonic distortion	V_{CC}=+3.3V, R_L = 150Ω V_{in}=1V_{p-p}, F=1MHz H2 H3		 64 61		dBc
Enable/power-down **Low level on pin-5: TSH122 in power-down** **High level on pin-5: TSH122 enabled**						
I_{sd}	Consumption in power-down mode	V_{CC}=+3.3V		4	500	nA
V_{low}	Low-level threshold		0		+0.3	V
V_{high}	High-level threshold		+0.7		V_{CC}	V
T_{on}	Time from power-down to enable			1		µs
T_{off}	Time from enable to power-down			1		µs

Figure 1. Frequency response

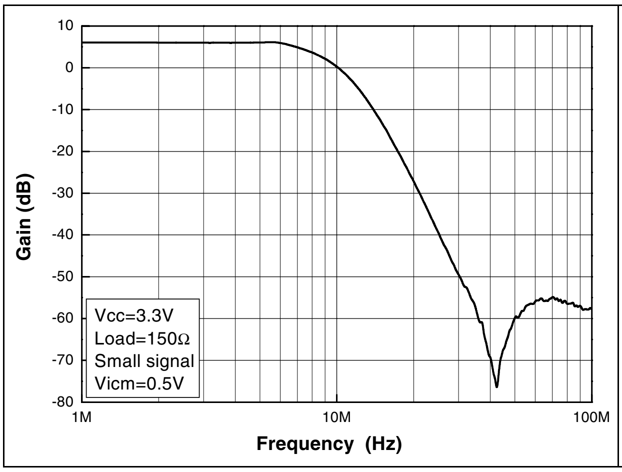


Figure 2. Gain flatness

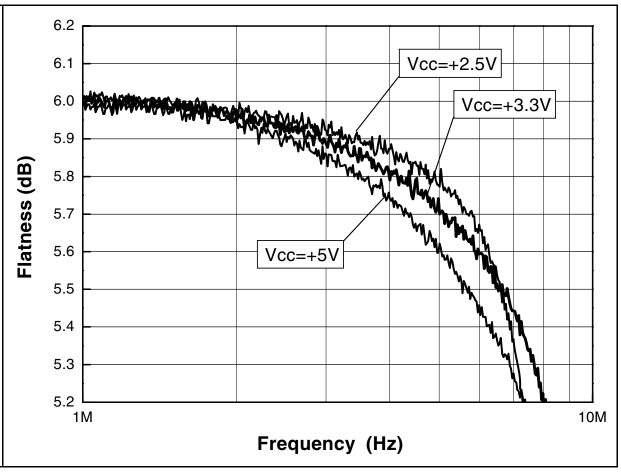


Figure 3. Input noise

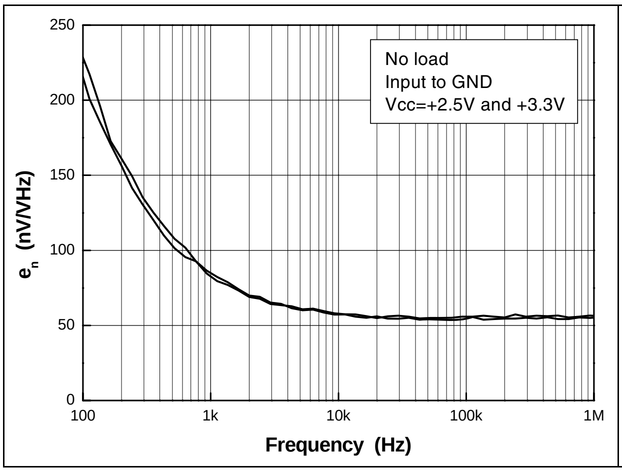


Figure 4. Distortion

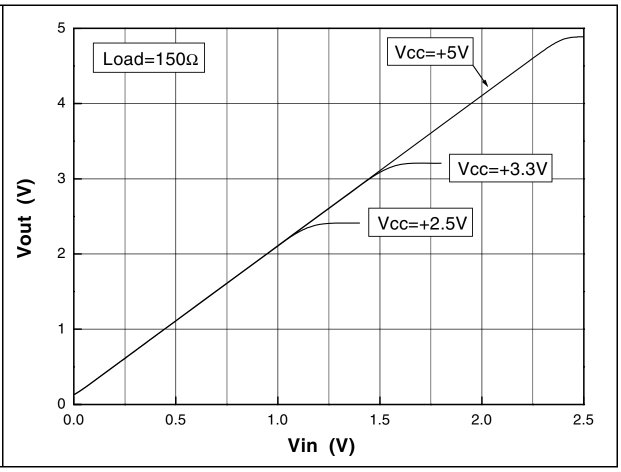


Figure 5. Distortion at Vcc=2.5 V

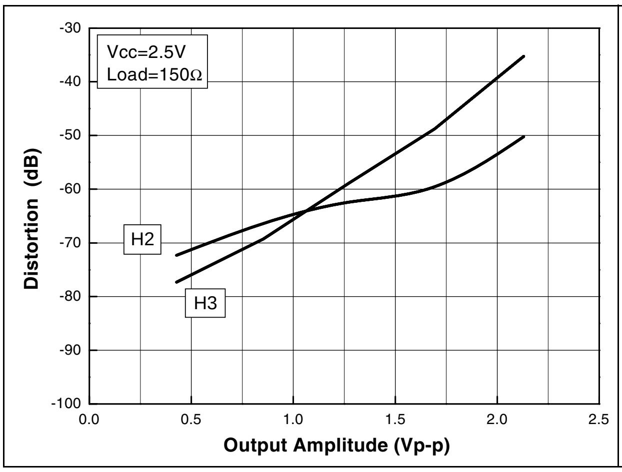


Figure 6. Distortion at Vcc=3.3 V

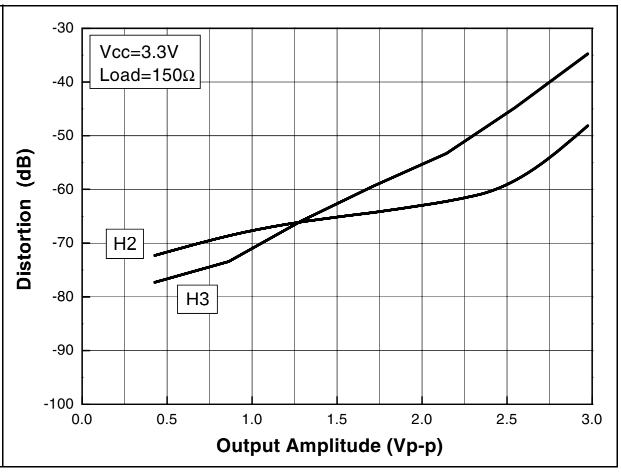


Figure 7. DCshift vs. Vcc

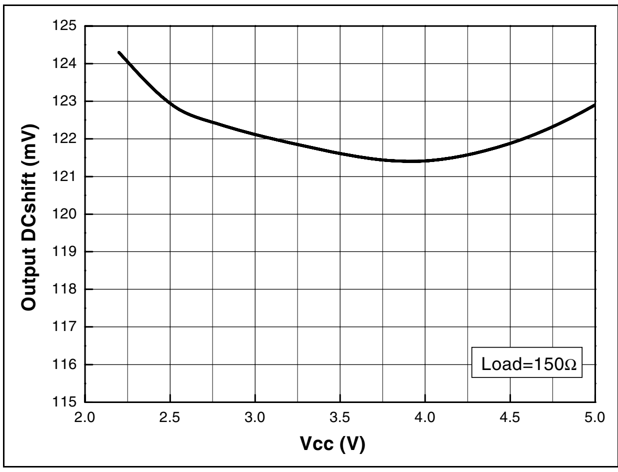


Figure 8. VOL vs. Vcc

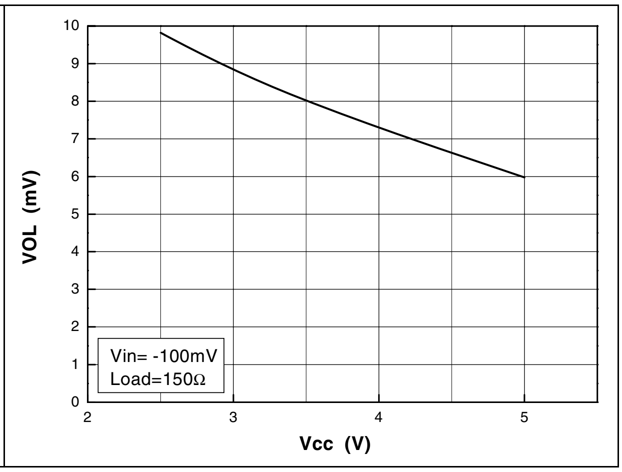


Figure 9. Icc vs. Vcc

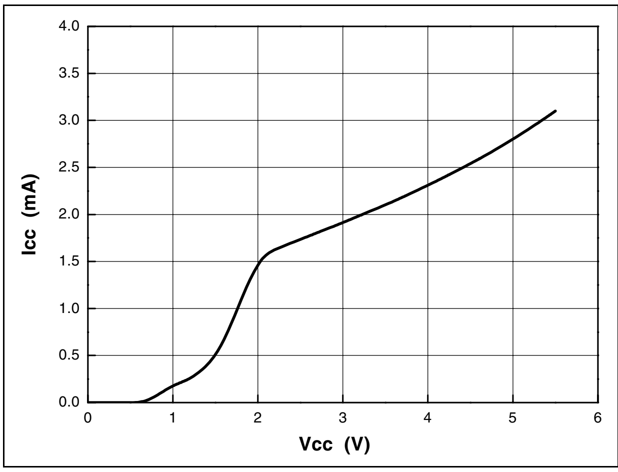


Figure 10. Power down

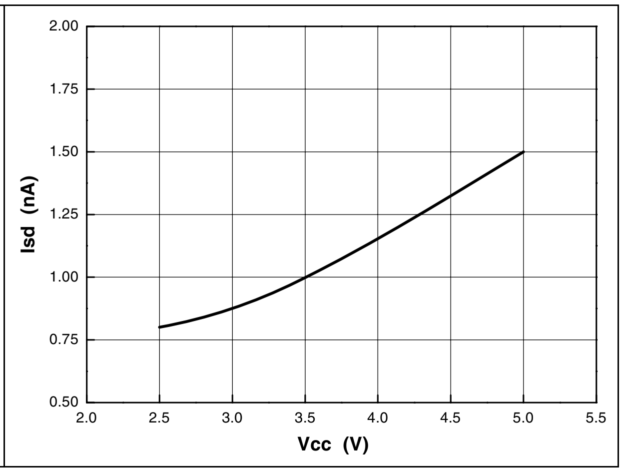


Figure 11. Switch-on output settling

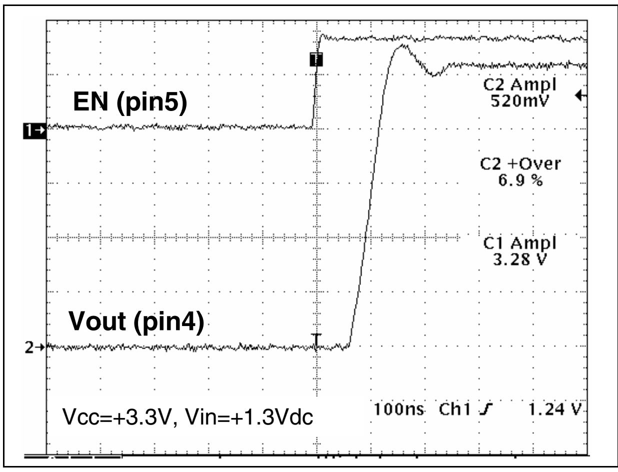


Figure 12. Switch-off output settling

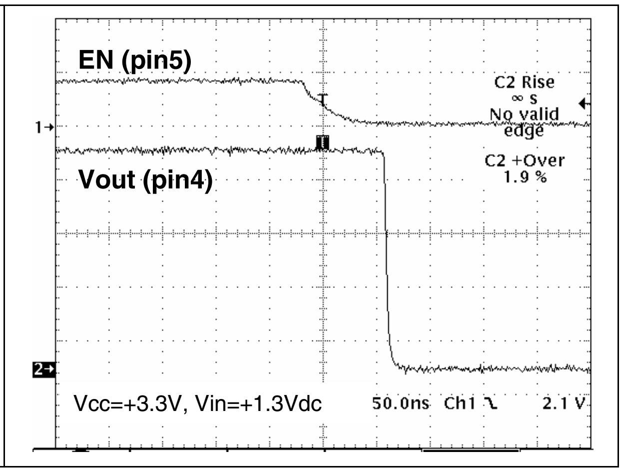


Figure 13. In/Out switch on/off

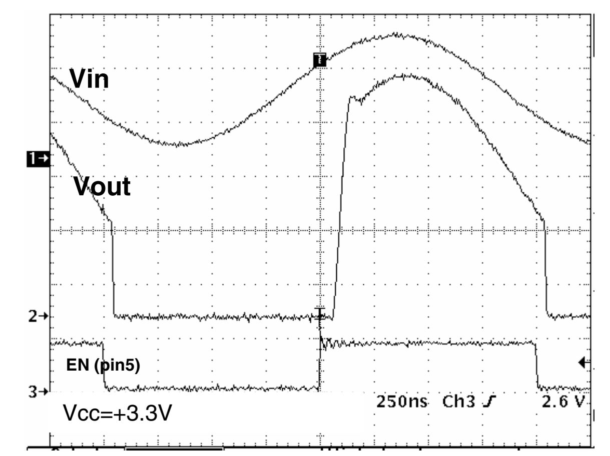


Figure 14. Synchronization tip at 0 V

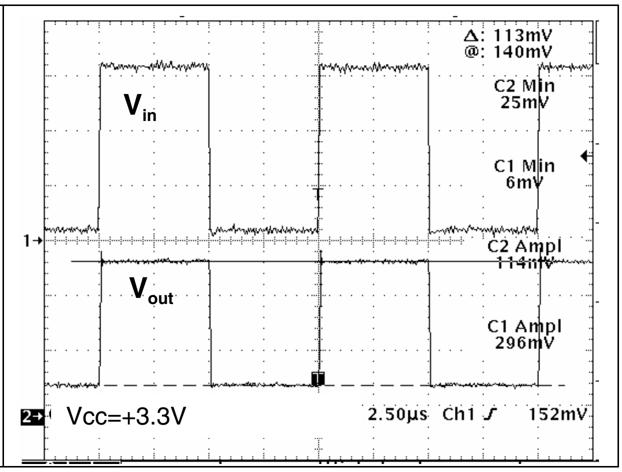


Figure 15. VOL vs. temperature

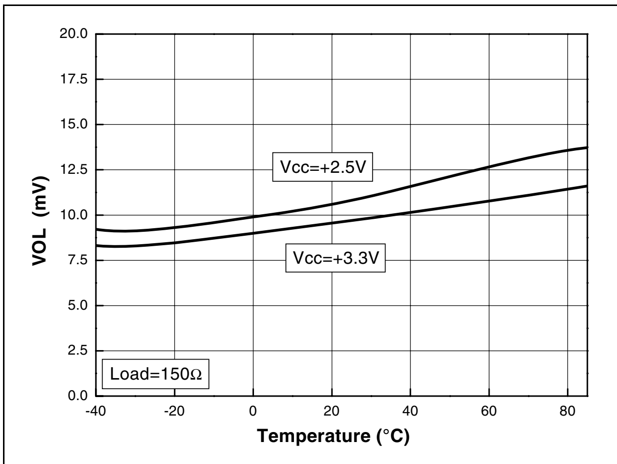


Figure 16. VOH vs. temperature

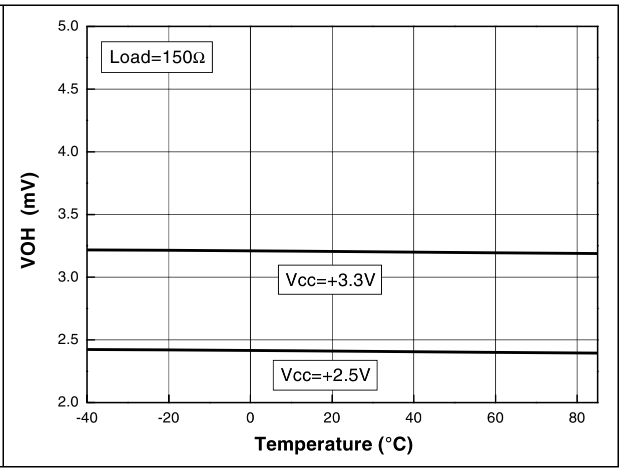


Figure 17. Bandwidth vs. temperature

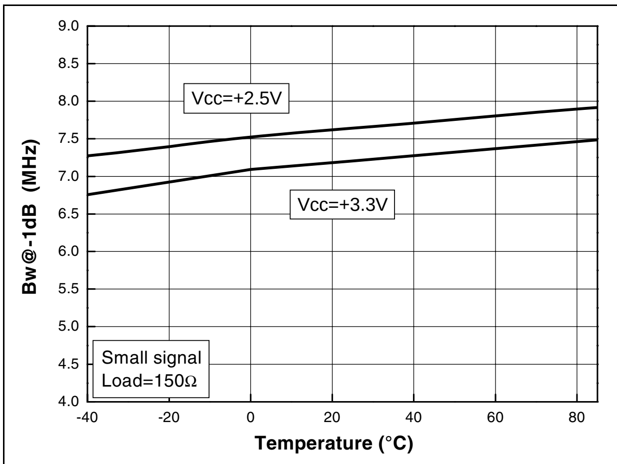


Figure 18. Attenuation vs. temperature

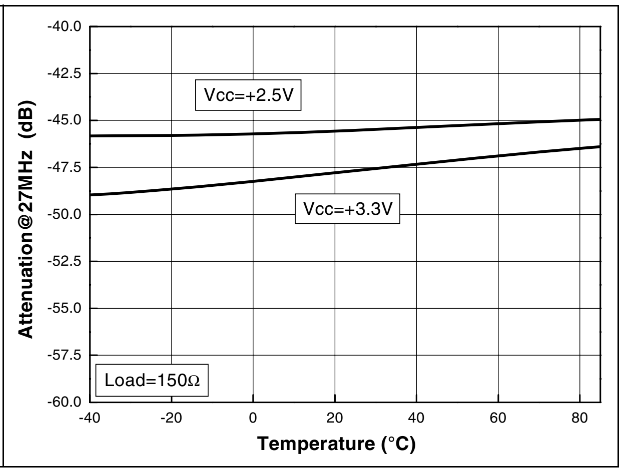


Figure 19. Icc vs. temperature

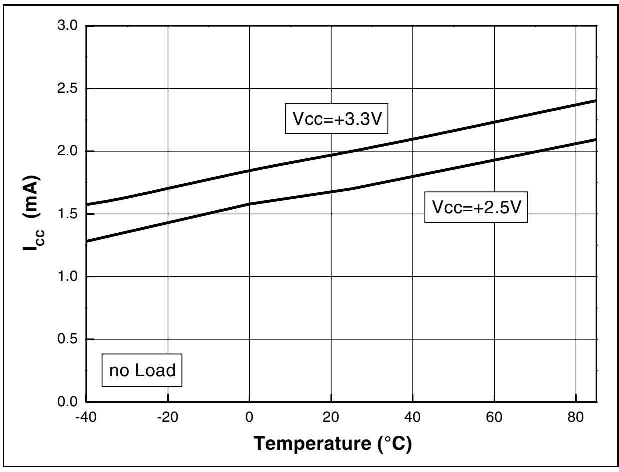


Figure 20. Gain vs. temperature

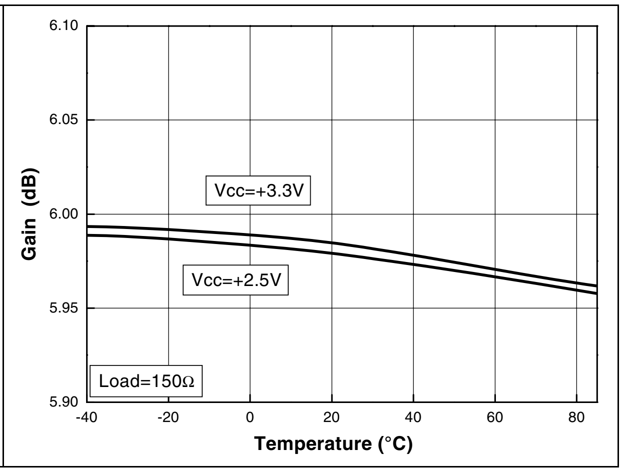


Figure 21. Output DC shift vs. temperature

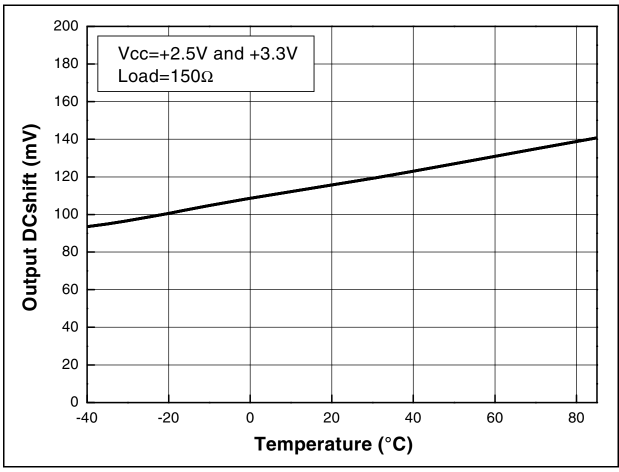
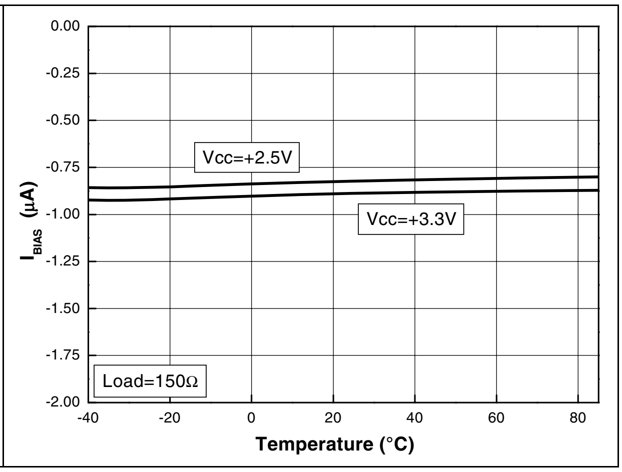


Figure 22. Ibias vs. temperature



3 Application information

3.1 Power supply considerations

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. The bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 10 µF is necessary to minimize the distortion. For better quality bypassing, we recommend adding a 10 nF capacitor, also placed as close as possible to the IC pins.

Figure 23. Circuit for power supply bypassing

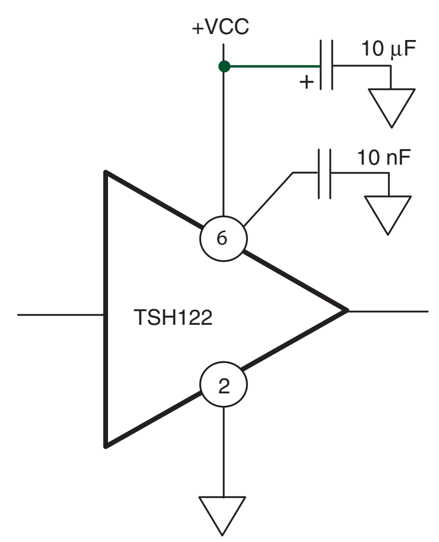
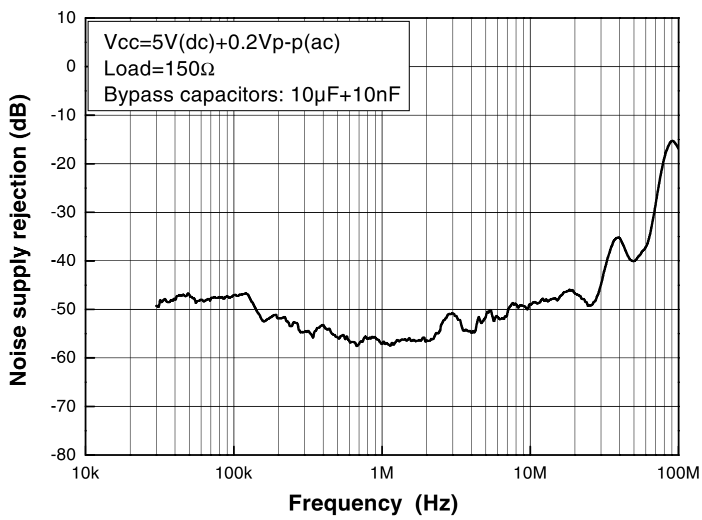


Figure 24. Supply noise rejection



3.2 Implementation considerations

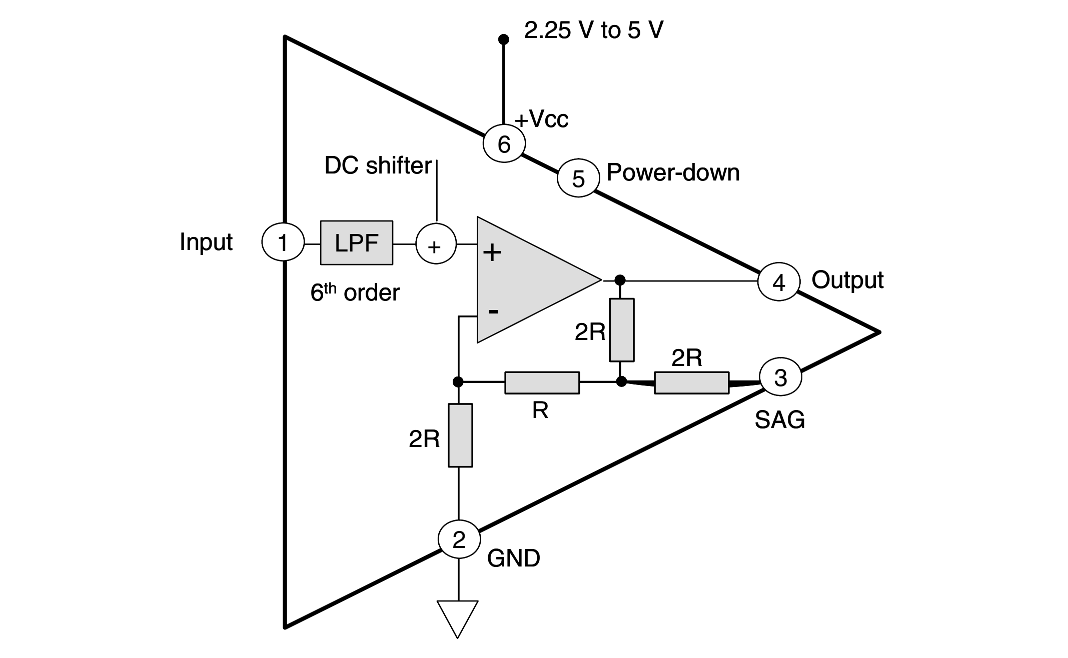
3.2.1 Input

The DC level shifter optimizes the position of the video signal with no clamping on the output rails.

3.2.2 Filter

A reconstruction filter is used to attenuate the DAC's sampling frequency because it generates a parasitic signal in the video spectrum (typically at 27 MHz in the case of standard video). This function is fulfilled while keeping a low group delay and a good gain flatness along the video band.

Figure 25. Internal schematic



3.2.3 Output

In an AC-coupling configuration, the SAG correction allows use of two small low-cost capacitors in place of one large capacitor (see *Figure 26*). The AC-coupling output reduces the power consumption by removing the DC component included in the signal.

Nevertheless, the output can be directly connected to the line without any capacitor. In this case, the OUT and SAG pins are connected together and the equivalent gain of the buffer remains at 6 dB (see *Figure 27*).

Figure 26. Schematic diagram with output capacitor

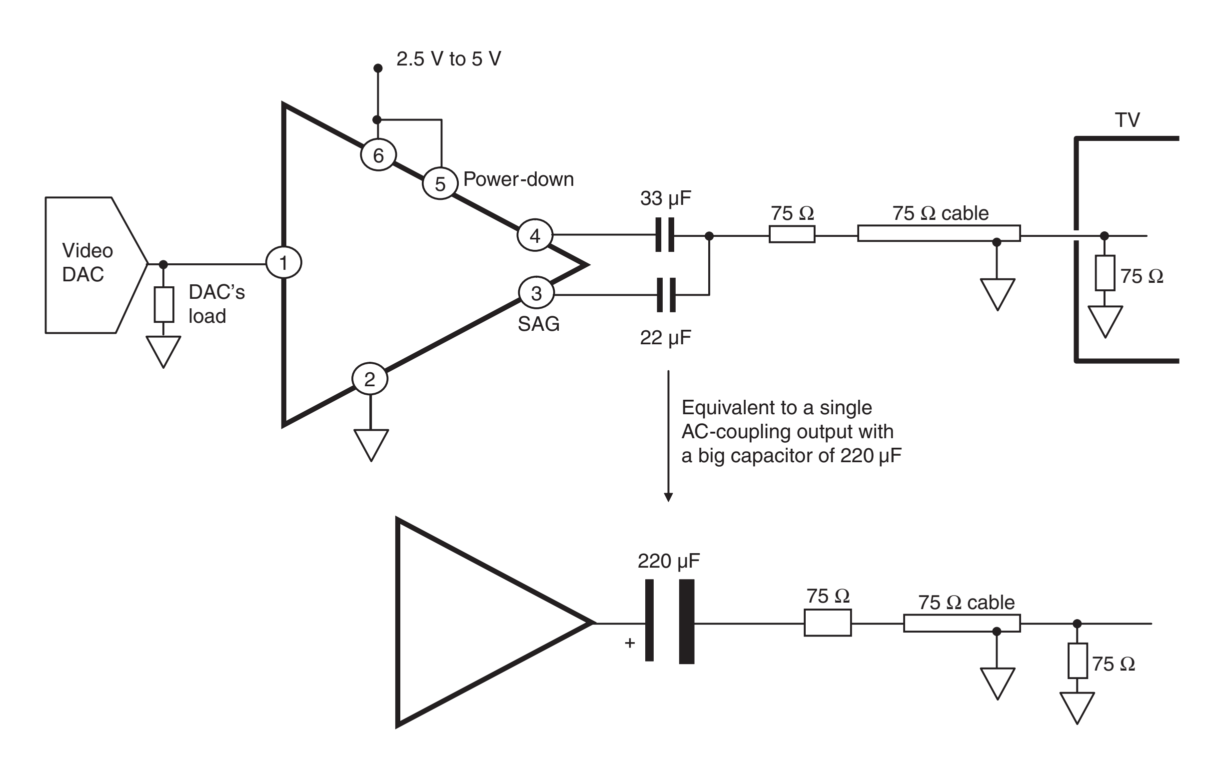
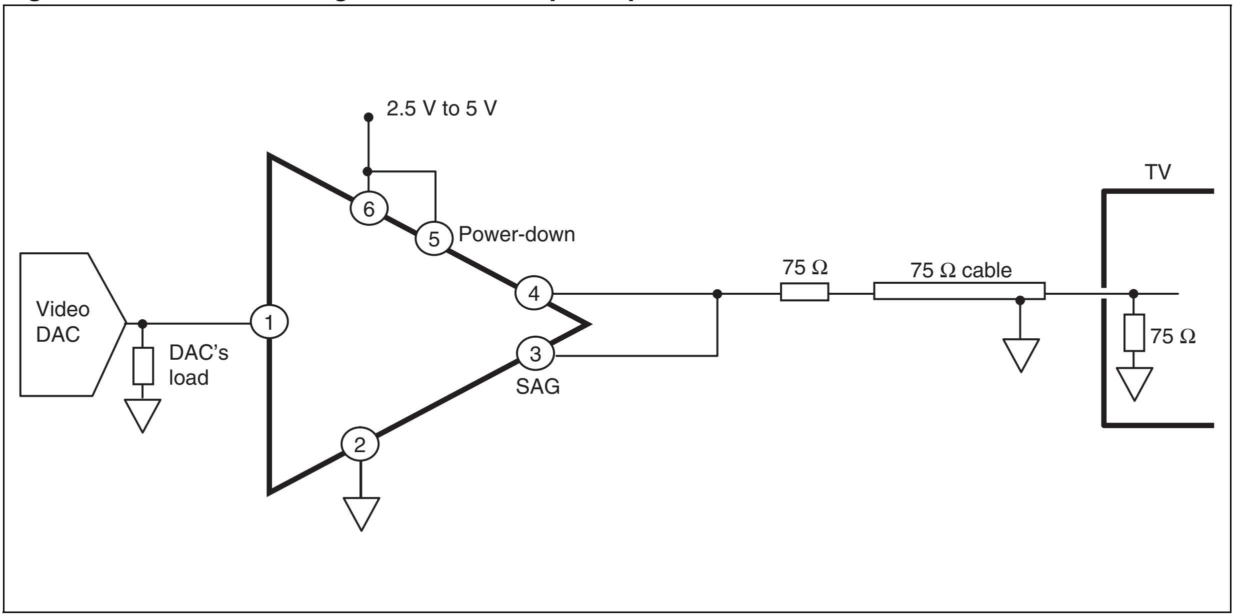
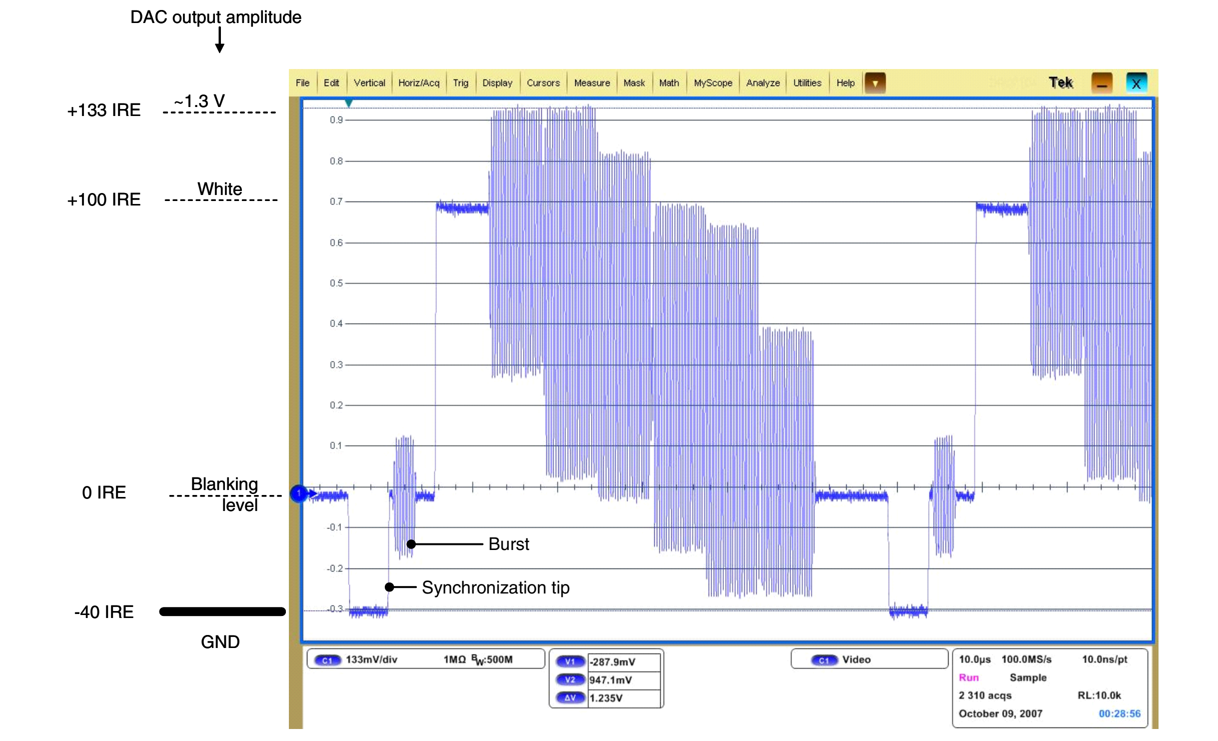


Figure 27. Schematic diagram without output capacitor



3.3 Using the TSH122 to drive a Cvbs signal

Figure 28. Details on Cvbs (NTSC color bar 100%)



With its internal DC shift, the TSH122 can drive a video signal from the DAC output as low as 0 V (bottom of the synchronization tip at 0 V - see *Figure 14*).

4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 29. SC70-6 (or SOT323-6) package footprint (in millimeters)

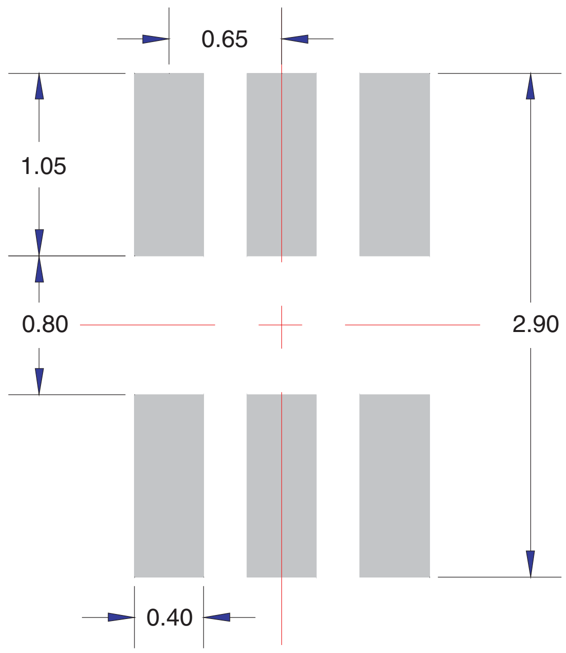
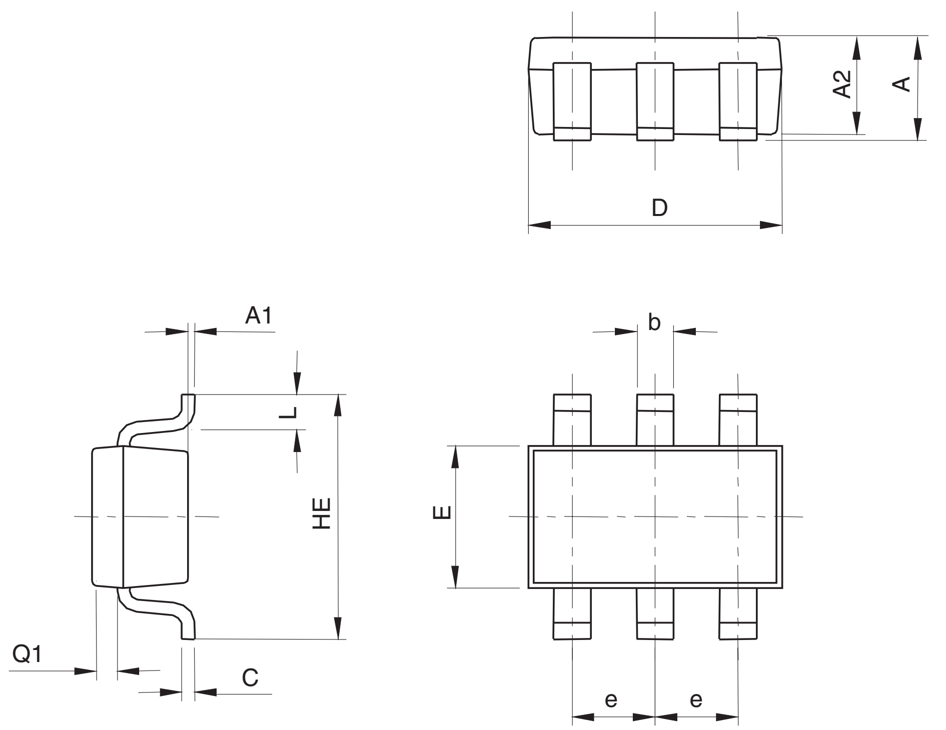


Figure 30. SC70-6 (or SOT323-6) package mechanical data

Ref	Dimensions					
	Millimeters			Mils		
	Min	Typ	Max	Min	Typ	Max
A	0.80		1.10	31.5		43.3
A1	0		0.10	0		3.9
A2	0.80		1.00	31.5		39.3
b	0.15		0.30	5.9		11.8
c	0.10		0.18	3.9		7.0
D	1.80		2.20	70.8		86.6
E	1.15		1.35	45.2		43.1
e		0.65			25.6	
HE	1.8		2.4	70.8		94.5
L	0.10		0.40	3.9		15.7
Q1	0.10		0.40	3.9		15.7



5 Ordering information

Table 4. Order codes

Part number	Temperature range	Package	Packaging	Marking
TSH122ICT	-40°C to +85°C	SC70	Tape & reel	K31

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Aug-2008	1	Initial release.

单击下面可查看定价，库存，交付和生命周期等信息

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