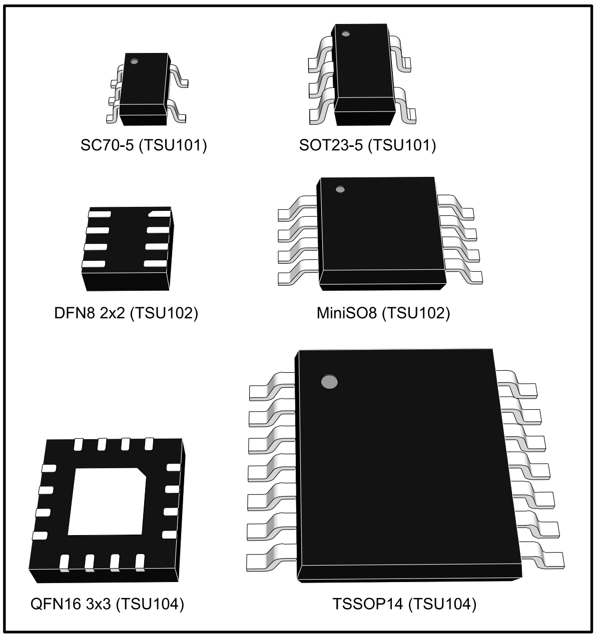
TSU101, TSU102, TSU104

Nanopower, rail-to-rail input and output, 5 V CMOS operational amplifiers

Datasheet - production data



Features

- Submicro ampere current consumption: 580 nA typ per channel at 25 °C at V_{CC} = 1.8 V
- Low supply voltage: 1.5 V - 5.5 V
- Unity gain stable
- Rail-to-rail input and output
- Gain bandwidth product: 8 kHz typ
- Low input bias current: 5 pA max at 25 °C
- High tolerance to ESD: 2 kV HBM
- Industrial temperature range: -40 °C to 85 °C

Benefits

- 42 years of typical equivalent lifetime (for TSU101) if supplied by a 220 mAh coin type Lithium battery
- Tolerance to power supply transient drops
- Accurate signal conditioning of high impedance sensors
- Application performances guaranteed over industrial temperature range
- Fast desaturation

Applications

- Ultra long life battery-powered applications
- Power metering
- UV and photo sensors
- Electrochemical and gas sensors
- Pyroelectric passive infrared (PIR) detection
- Battery current sensing
- Medical instrumentation
- RFID readers

Description

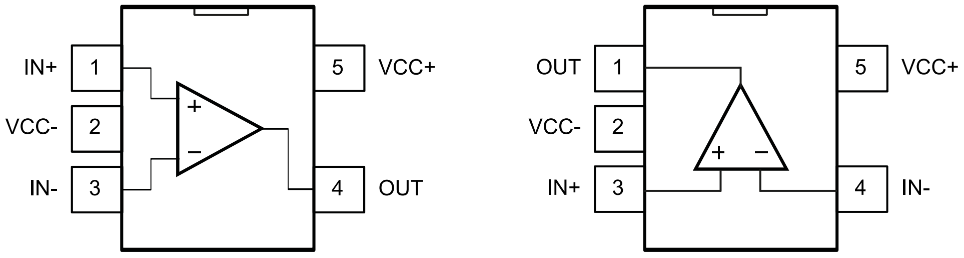
The TSU101, TSU102, and TSU104 operational amplifiers offer an ultra low-power consumption of 580 nA typical and 750 nA maximum per channel when supplied by 1.8 V. Combined with a supply voltage range of 1.5 V to 5.5 V, these features allow the TSU10x series to be efficiently supplied by a coin type Lithium battery or a regulated voltage in low-power applications.

The 8 kHz gain bandwidth of these devices make them ideal for sensor signal conditioning, battery supplied, and portable applications.

Contents

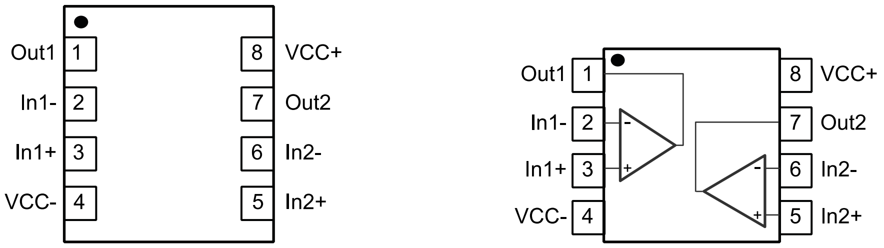
1 Package pin connections

Figure 1: Pin connections for each package (top view)



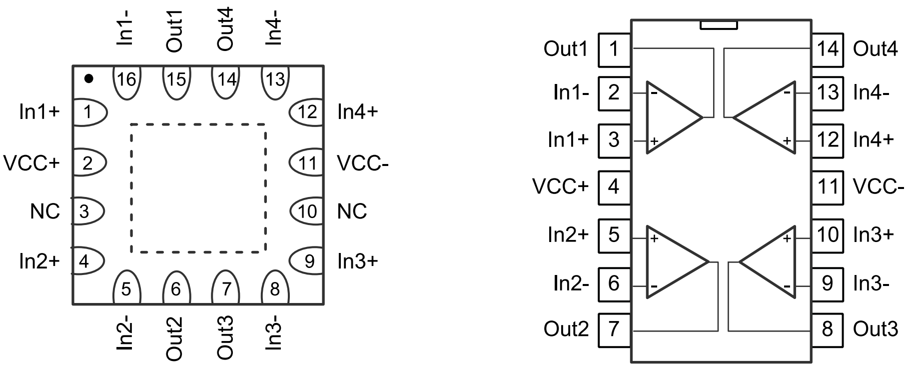
SC70-5/SOT23-5 (TSU101)

SC70-5/SOT23-5 (TSU101R)



DFN8 2x2 (TSU102)

MiniSO8 (TSU102)



QFN16 3x3 (TSU104)

TSSOP14 (TSU104)

2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		±V_{CC}	
V_{in}	Input voltage (3)		$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction to ambient (5)(6)	SC70-5	205	°C/W
		SOT23-5	250	
		DFN8 2x2	117	
		MiniSO8	190	
		QFN16 3x3	45	
		TSSOP14	100	
ESD	HBM: human body model (7)		2000	V
	MM: machine model (8)		200	
	CDM: charged device model (9)	All other packages except SC70-5	1000	
		SC70-5	900	
	Latch-up immunity (10)		200	mA

Notes:

(1) All voltage values, except the differential voltage are with respect to the network ground terminal.

(2) The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.

(3) $((V_{CC+}) - V_{in})$ must not exceed 6 V, $(V_{in} - V_{CC-})$ must not exceed 6 V.

(4) The input current must be limited by a resistor in series with the inputs.

(5) R_{th} are typical values.

(6) Short-circuits can cause excessive heating and destructive dissipation.

(7) Related to ESDA/JEDEC JS-001 Apr. 2010

(8) Related to JEDEC JESD22-A115C Nov.2010

(9) Related to JEDEC JESD22-C101-E Dec. 2009

(10) Related to JEDEC JESD78C Sept. 2010

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
T_{oper}	Operating free air temperature range	-40 to 85	°C

3 Electrical characteristics

Table 3: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 ° C, and RL = 1 MΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-3	0.1	3	mV
		-40 °C < T< 85 °C	-3.4		3.4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 85 °C			5	μV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C (1)		0.18		μV/ √month
I_{io}	Input offset current (2)			1	5	pA
		-40 °C < T< 85 °C			30	
I_{ib}	Input bias current (2)			1	5	
		-40 °C < T< 85 °C			30	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 to 0.6 V, $V_{out} = V_{CC}/2$	65	85		dB
		-40 °C < T< 85 °C	65			
		V_{icm} = 0 to 1.8 V, $V_{out} = V_{CC}/2$	55	74		
		-40 °C < T< 85 °C	55			
A_{vd}	Large signal voltage gain	V_{out} = 0.3 V to ((V_{CC+}) - 0.3 V), R_L = 100 kΩ	95	115		
		-40 °C < T< 85 °C	95			
V_{OH}	High level output voltage, (drop from V_{CC+})	R_L = 100 kΩ			40	mV
		-40 °C < T< 85 °C			40	
V_{OL}	Low level output voltage	R_L = 100 kΩ			40	
		-40 °C < T< 85 °C			40	
I_{out}	Output sink current	$V_{out} = V_{CC}$, V_{ID} = -200 mV	4	5		mA
		-40 °C < T< 85 °C	4			
	Output source current	V_{out} = 0 V, V_{ID} = 200 mV	4	5		
		-40 °C < T< 85 °C	4			
I_{CC}	Supply current, (per channel)	No load, $V_{out} = V_{CC}/2$		580	750	nA
		-40 °C < T< 85 °C			800	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		8		kHz
F_u	Unity gain frequency			8		
ϕ_m	Phase margin			60		Degrees
G_m	Gain margin			10		dB
SR	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF V_{out} = 0.3 V to ((V_{CC+}) - 0.3 V)		3		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		265		nV/√Hz
		f = 1 kHz		265		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		9		μV_{pp}
i_n	Equivalent input noise current	f = 100 Hz		0.64		fA/√Hz
		f = 1 kHz		4.4		
t_{rec}	Overload recovery time	100 mV from rail in comparator, R_L = 100 kΩ, $V_{ID} = \pm V_{CC}$, -40 °C < T< 85 °C		30		µs

Notes:

(1) Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.

(2) Guaranteed by design.

Table 4: Electrical characteristics at VCC+ = 3.3 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 ° C, and RL = 1 MΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-3	0.1	3	mV
		-40 °C < T< 85 °C	-3.4		3.4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 85 °C			5	μV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C (1)		0.36		μV/ √month
I_{io}	Input offset current (2)			1	5	pA
		-40 °C < T< 85 °C			30	
I_{ib}	Input bias current (2)			1	5	
		-40 °C < T< 85 °C			30	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 to 2.1 V, V_{out} = $V_{CC}/2$	70	92		dB
		-40 °C < T< 85 °C	70			
		V_{icm} = 0 to 3.3 V, V_{out} = $V_{CC}/2$	60	77		
		-40 °C < T< 85 °C	60			
A_{vd}	Large signal voltage gain	V_{out} = 0.3 V to ((V_{CC+}) - 0.3 V), R_L= 100 kΩ	105	120		
		-40 °C < T< 85 °C	105			
V_{OH}	High level output voltage (drop from V_{CC+})	R_L = 100 kΩ			40	mV
		-40 °C < T< 85 °C			40	
V_{OL}	Low level output voltage	R_L = 100 kΩ			40	
		-40 °C < T< 85 °C			40	
I_{out}	Output sink current	V_{out} = V_{CC} , V_{ID} = -200 mV	6	9		mA
		-40 °C < T< 85 °C	6			
	Output source current	V_{out} = 0 V, V_{ID} = 200 mV	8	11		
		-40 °C < T< 85 °C	8			
I_{CC}	Supply current, (per channel)	No load, V_{out} = $V_{CC}/2$		600	800	nA
		-40 °C < T< 85 °C			850	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		8		kHz
F_u	Unity gain frequency			8		
ϕ_m	Phase margin			60		Degrees
G_m	Gain margin			11		dB
SR	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to ((V_{CC+}) - 0.3 V)		3		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		260		nV/√Hz
		f = 1 kHz		255		
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.6		μV_{pp}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
i_n	Equivalent input noise current	f = 100 Hz		0.55		fA/√Hz
		f = 1 kHz		3.8		
t_{rec}	Overload recovery time	100 mV from rail in comparator, R_L = 100 kΩ, V_{ID} = $\pm V_{CC}$, -40 °C < T< 85 °C		30		µs

Notes:

(1)Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.

(2)Guaranteed by design.

Table 5: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 ° C, and RL = 1 MΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-3	0.1	3	mV
		-40 °C < T< 85 °C	-3.4		3.4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 85 °C			5	µV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C (1)		1.1		µV/ √month
I_{io}	Input offset current (2)			1	5	pA
		-40 °C < T< 85 °C			30	
I_{ib}	Input bias current (2)			1	5	
		-40 °C < T< 85 °C			30	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 to 3.8 V, V_{out} = $V_{CC}/2$	70	90		dB
		-40 °C < T< 85 °C	70			
		V_{icm} = 0 to 5 V, V_{out} = $V_{CC}/2$	65	82		
		-40 °C < T< 85 °C	65			
SVR	Supply voltage rejection ratio	V_{CC} = 1.5 to 5.5 V, V_{icm} = 0 V	70	90		
		-40 °C < T< 85 °C	70			
A_{vd}	Large signal voltage gain	V_{out} = 0.3 V to ((V_{cc+}) - 0.3 V), R_L= 100 kΩ	110	130		
		-40 °C < T< 85 °C	110			
V_{OH}	High level output voltage, (drop from V_{CC+})	R_L = 100 kΩ			40	mV
		-40 °C < T< 85 °C			40	
V_{OL}	Low level output voltage	R_L = 100 kΩ			40	
		-40 °C < T< 85 °C			40	
I_{out}	Output sink current	V_{out} = V_{CC} , V_{ID} = -200 mV	6	9		mA
		-40 °C < T< 85 °C	6			
	Output source current	V_{out} = 0 V, V_{ID} = 200 mV	8	11		
		-40 °C < T< 85 °C	8			
I_{CC}	Supply current, (per channel)	No load, V_{out} = $V_{CC}/2$		650	850	nA
		-40 °C < T< 85 °C			950	
AC performance						
GBP	Gain bandwidth product	R_L = 1 MΩ, C_L = 60 pF		9		kHz
F_u	Unity gain frequency			8.6		
ϕ_m	Phase margin			60		Degrees
G_m	Gain margin			12		dB
SR	Slew rate (10 % to 90 %)	R_L = 1 MΩ, C_L = 60 pF, V_{out} = 0.3 V to ((V_{CC+}) - 0.3 V)		3		V/ms
e_n	Equivalent input noise voltage	f = 100 Hz		240		nV√Hz
		f = 1 kHz		225		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		8.1		μV_{pp}
i_n	Equivalent input noise current	f = 100 Hz		0.18		fA√Hz
		f = 1 kHz		3.5		
t_{rec}	Overload recovery time	100 mV from rail in comparator, R_L = 100 kΩ, $V_{ID} = \pm V_{CC}$, -40 °C < T< 85 °C		30		µs
EMIRR	Electromagnetic interference rejection ratio (3)	V_{in} = -10 dBm, f = 400 MHz		73		dB
		V_{in} = -10 dBm, f = 900 MHz		88		
		V_{in} = -10 dBm, f = 1.8 GHz		80		
		V_{in} = -10 dBm, f = 2.4 GHz		80		

Notes:

(1) Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.

(2) Guaranteed by design.

(3) Based on evaluations performed only in conductive mode.

Figure 2: Supply current vs. supply voltage

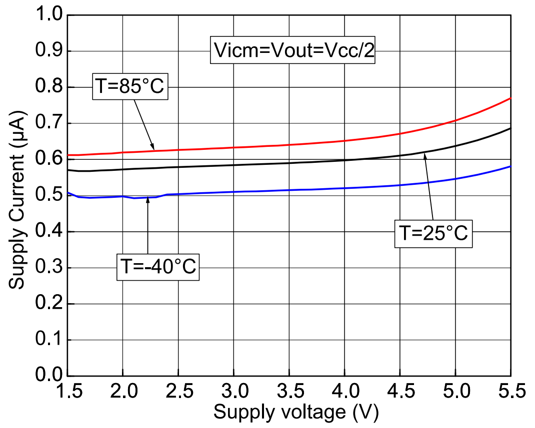


Figure 3: Supply current vs. input common mode voltage

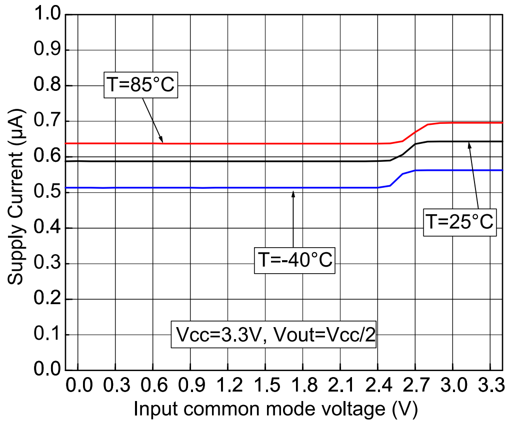


Figure 4: Supply current in saturation mode

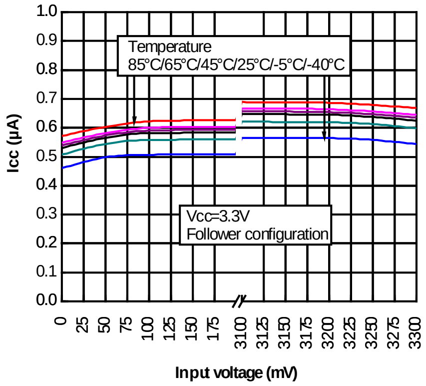


Figure 5: Input offset voltage distribution

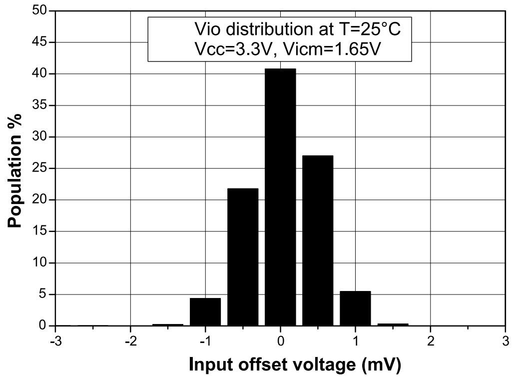


Figure 6: Input offset voltage vs common mode voltage

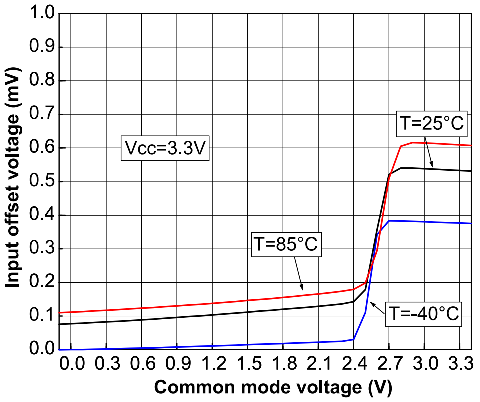


Figure 7: Input offset voltage vs temperature at 3.3 V supply voltage

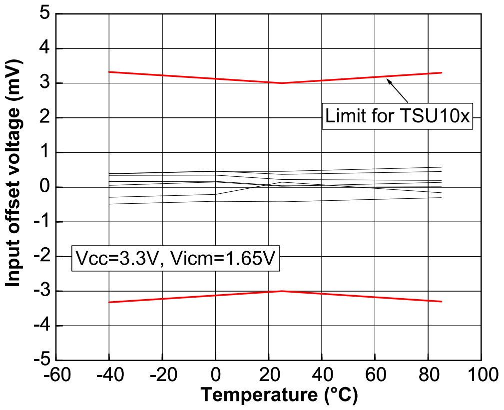


Figure 8: Input offset voltage temperature coefficient distribution

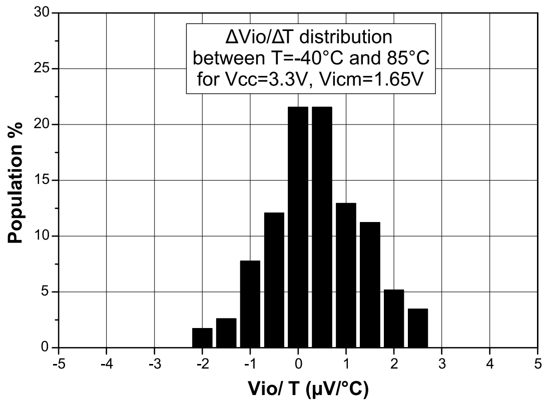


Figure 9: Input bias current vs. temperature at mid VICM

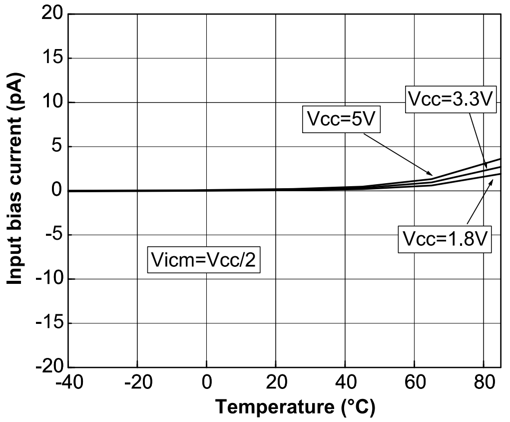


Figure 10: Input bias current vs. temperature at low VICM

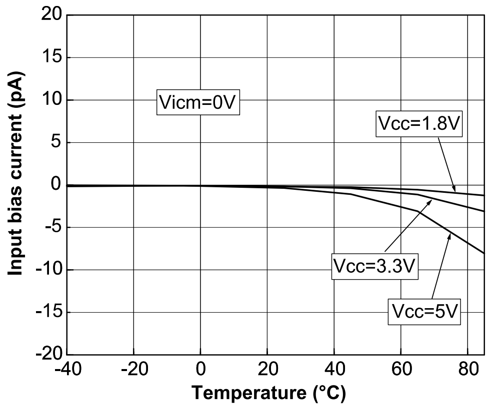


Figure 11: Input bias current vs. temperature at high VICM

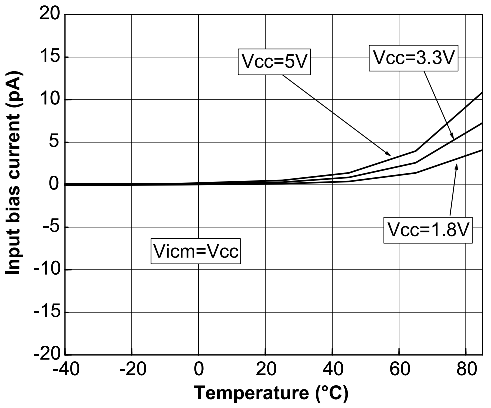


Figure 12: Output characteristics at 1.8 V supply voltage

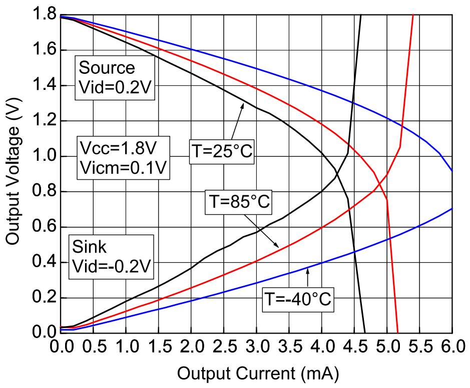


Figure 13: Output characteristics at 3.3 V supply voltage

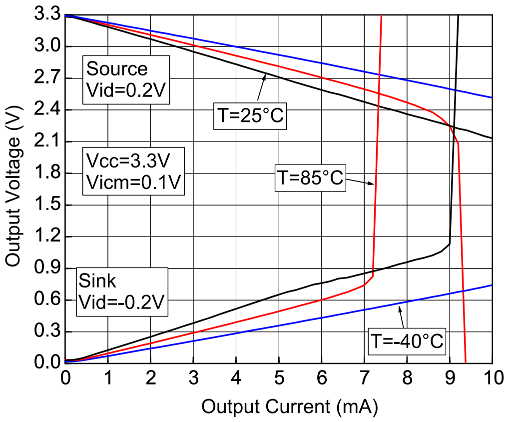


Figure 14: Output characteristics at 5 V supply voltage

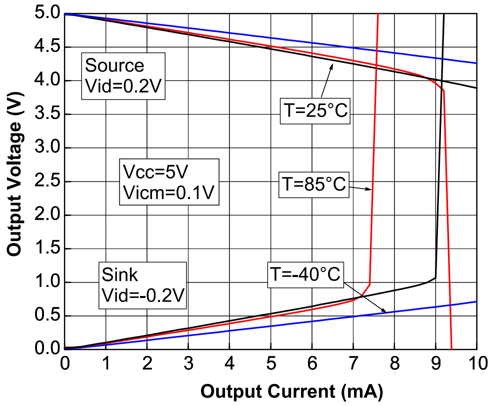


Figure 15: Output voltage vs. input voltage close to the rails

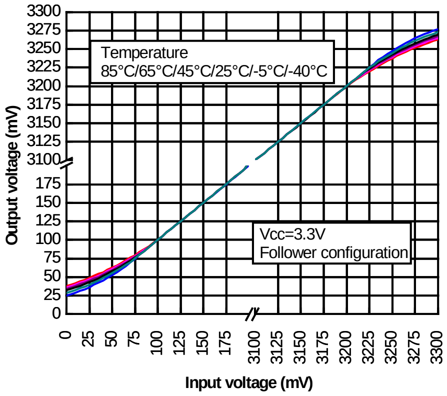


Figure 16: Output saturation with a sine wave on input

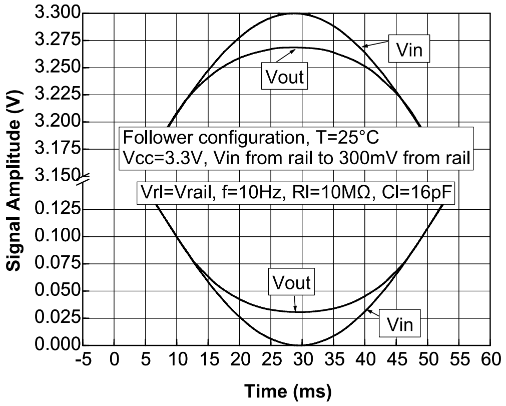


Figure 17: Desaturation time

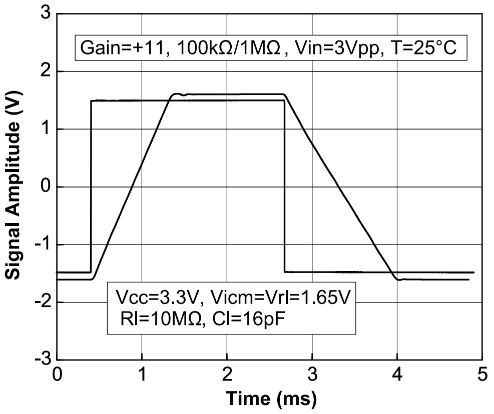


Figure 18: Phase reversal free

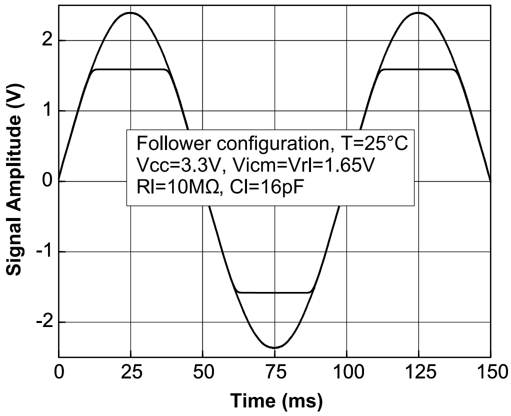


Figure 19: Slew rate vs. supply voltage

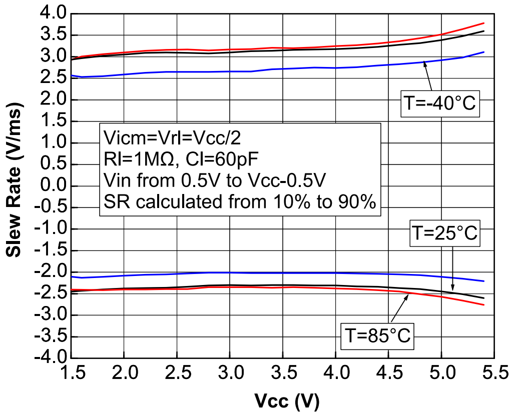


Figure 20: Output swing vs. input signal frequency

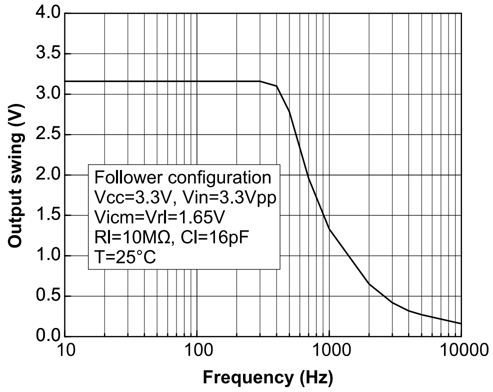


Figure 21: Triangulation of a sine wave

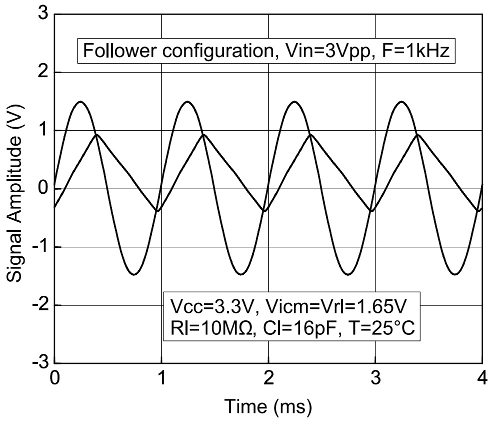


Figure 22: Large signal response at 3.3 V supply voltage

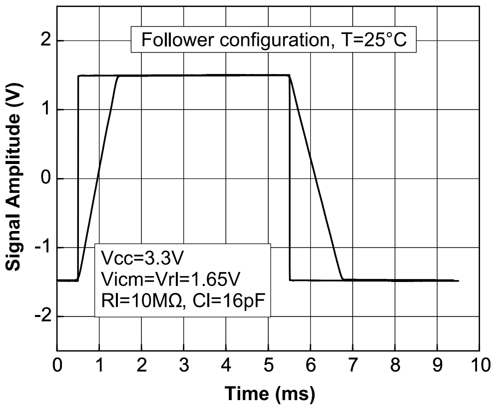


Figure 23: Small signal response at 3.3 V supply voltage

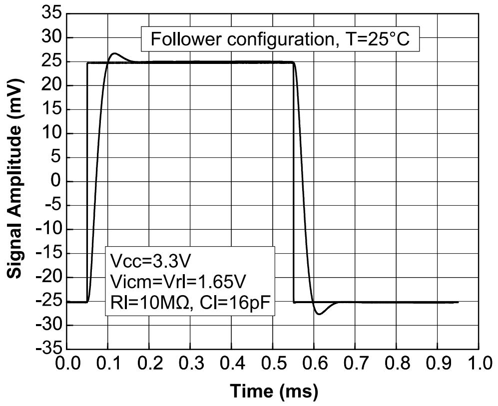


Figure 24: Overshoot vs. capacitive load at 3.3 V supply voltage

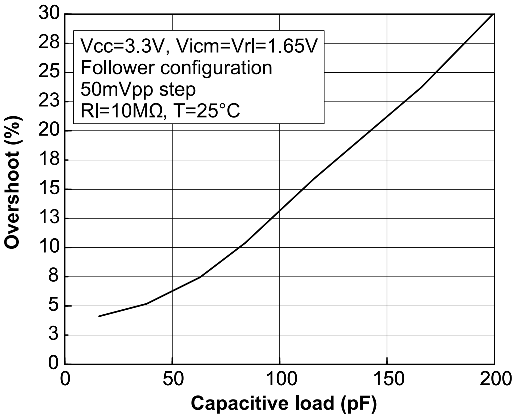


Figure 25: Phase margin vs. capacitive load at 3.3 V supply voltage

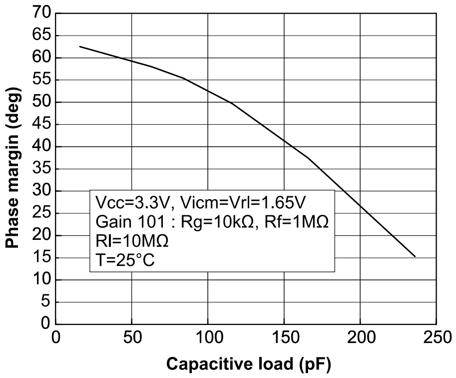


Figure 26: Bode diagram for different feedback values

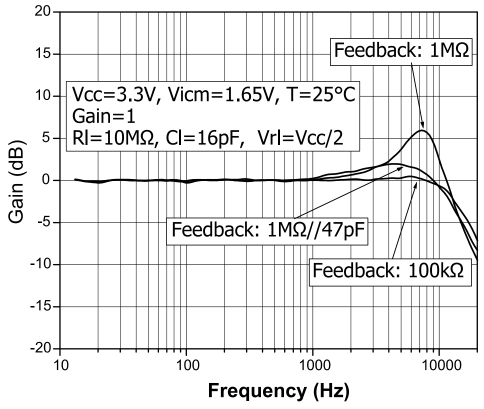


Figure 27: Bode diagram at 1.8 V supply voltage

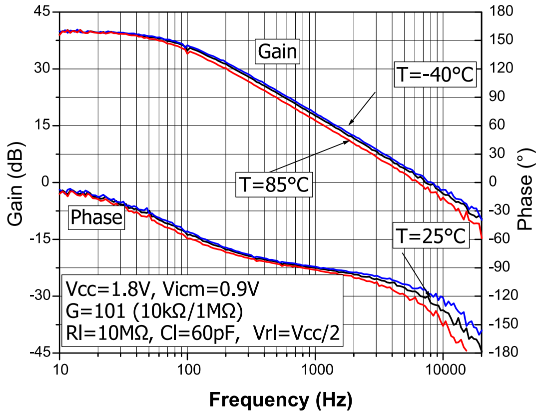


Figure 28: Bode diagram at 3.3 V supply voltage

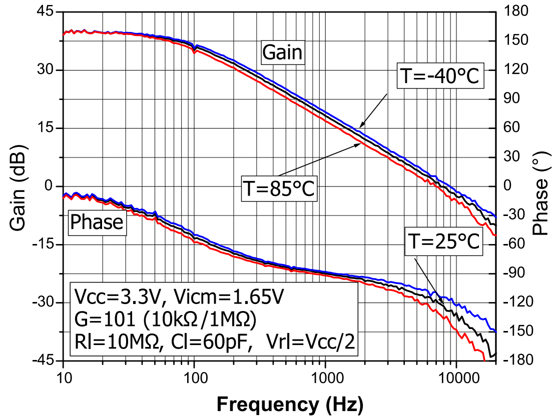


Figure 29: Bode diagram at 5 V supply voltage

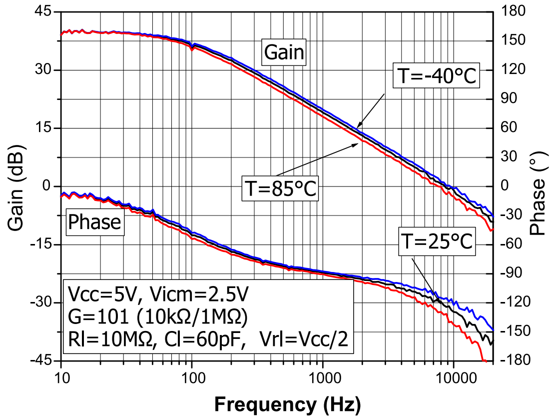


Figure 30: Gain bandwidth product vs. input common mode voltage

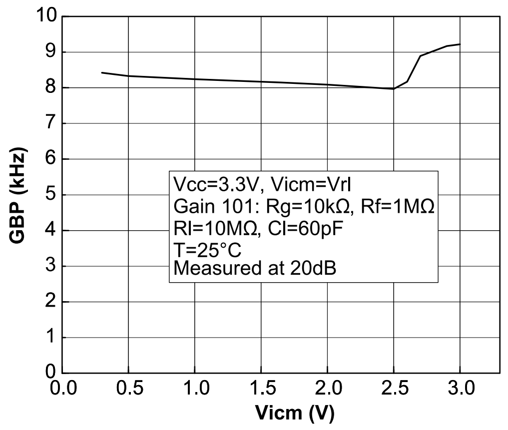


Figure 31: In-series resistor (Riso) vs. capacitive load

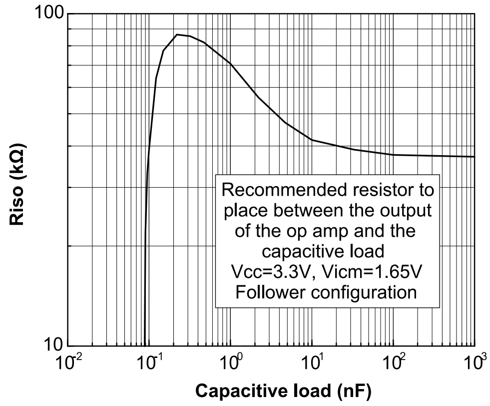


Figure 32: Noise at 1.8 V supply voltage in follower configuration

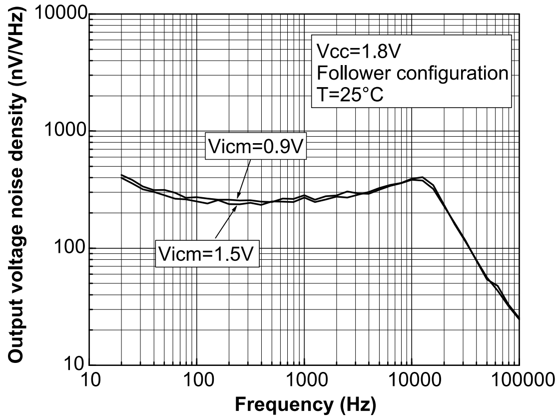


Figure 33: Noise at 3.3 V supply voltage in follower configuration

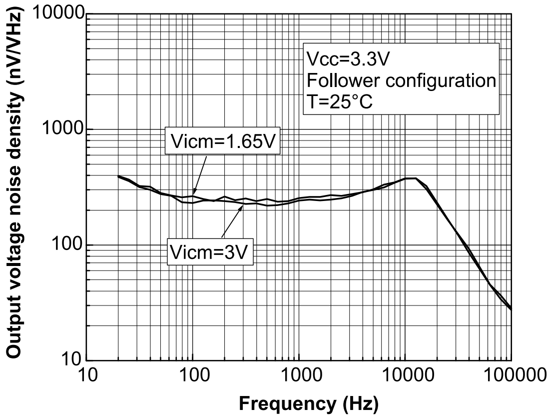


Figure 34: Noise at 5 V supply voltage in follower configuration

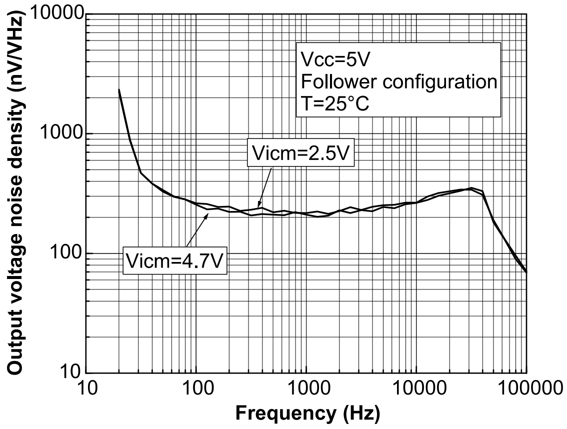


Figure 35: Noise amplitude on 0.1 to 10 Hz frequency range

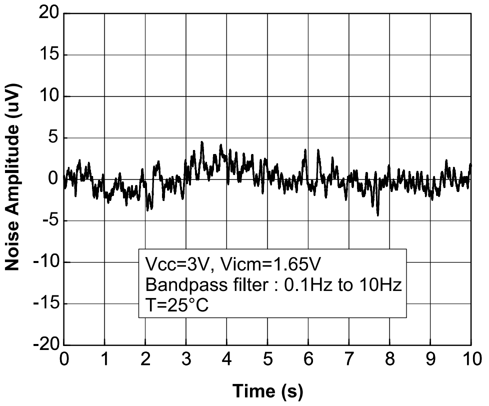


Figure 36: Channel separation on TSU102

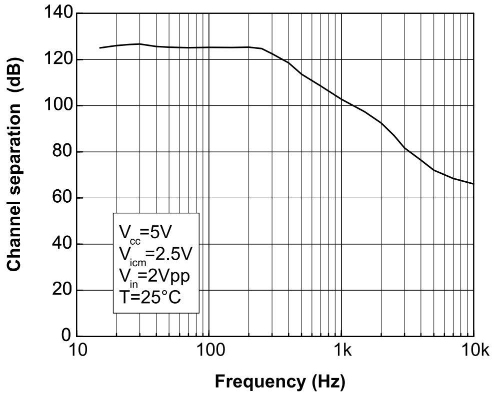
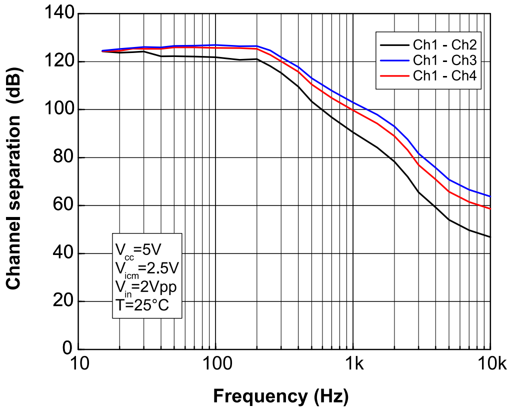


Figure 37: Channel separation on TSU104



4 Application information

4.1 Operating voltages

The TSU101, TSU102, and TSU104 series of amplifiers can operate from 1.5 V to 5.5 V. Their parameters are fully specified at 1.8 V, 3.3 V, and 5 V supply voltages and are very stable in the full V_{CC} range. Additionally, main specifications are guaranteed on the industrial temperature range from -40 to 85 ° C.

4.2 Rail-to-rail input

The TSU101, TSU102, and TSU104 series is built with two complementary PMOS and NMOS input differential pairs. Thus, these devices have a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

The devices have been designed to prevent phase reversal behavior.

4.3 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effects of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

with T = -40 °C and 85 °C.

The datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 2.

4.4 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

b is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eVk^{-1})

T_U is the temperature of the die when V_U is used (°K)

T_S is the temperature of the die under temperature stress (°K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\text{ h} \times 12\text{ months} / (24\text{ h} \times 365.25\text{ days})$$

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC}/2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

4.5 Schematic optimization aiming for nanopower

To benefit from the full performance of the TSU10 series, the impedances must be maximized so that current consumption is not lost where it is not required.

For example, an aluminum electrolytic capacitance can have significantly high leakage. This leakage may be greater than the current consumption of the op-amp. For this reason, ceramic type capacitors are preferred.

For the same reason, big resistor values should be used in the feedback loop. However, there are three main limitations to be considered when choosing a resistor.

1. When the TSU10x series is used with a sensor: the resistance connected between the sensor and the input must remain much higher than the impedance of the sensor itself.
2. Noise generated: a 100 kΩ resistor generates 40 nV/√Hz, a bigger resistor value generates even more noise.
3. Leakage on the PCB: leakage can be generated by moisture. This can be improved by using a specific coating process on the PCB.

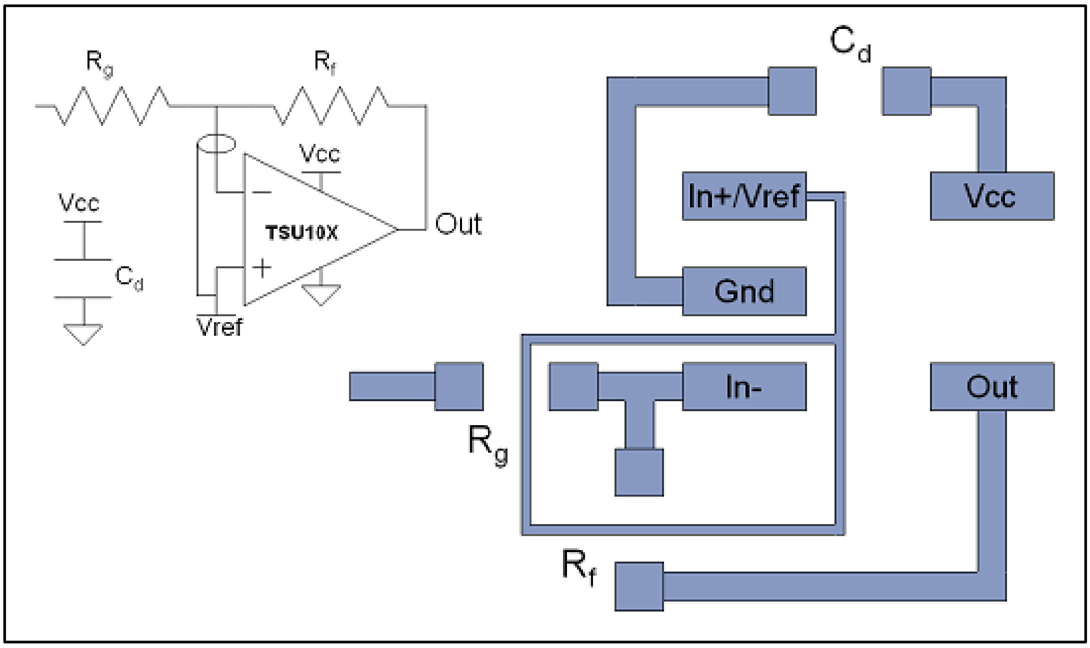
4.6 PCB layout considerations

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

Minimizing the leakage from sensitive high impedance nodes on the inputs of the TSU10x series can be performed with a guarding technique. The technique consists of surrounding high impedance tracks by a low impedance track (the ring). The ring is at the same electrical potential as the high impedance node.

Therefore, even if some parasitic impedance exists between the tracks, no leakage current can flow through them as they are at the same potential (see *Figure 38: "Guarding on the PCB"*).

Figure 38: Guarding on the PCB



4.7 Using the TSU10x series with sensors

The TSU10x series has MOS inputs, thus input bias currents can be guaranteed down to 5 pA maximum at ambient temperature. This is an important parameter when the operational amplifier is used in combination with high impedance sensors.

The TSU101, TSU102, and TSU104 series is perfectly suited for trans-impedance configuration as shown in *Figure 39: "Trans-impedance amplifier schematic"*. This configuration allows a current to be converted into a voltage value with a gain set by the user. It is an ideal choice for portable electrochemical gas sensing or photo/UV sensing applications. The TSU10x series, using trans-impedance configuration, is able to provide a voltage value based on the physical parameter sensed by the sensor.

Electrochemical gas sensors

The output current of electrochemical gas sensors is generally in the range of tens of nA to hundreds of µA. As the input bias current of the TSU101, TSU102, and TSU104 is very low (see *Figure 9*, *Figure 10*, and *Figure 11*) compared to these current values, the TSU10x series is well adapted for use with the electrochemical sensors of two or three electrodes. *Figure 40: "Potentiostat schematic using the TSU101 (or TSU102)"* shows a potentiostat (electronic hardware required to control a three-electrode cell) schematic using the TSU101, TSU102, and TSU104. In such a configuration, the devices minimize leakage in the reference electrode compared to the current being measured on the working electrode.

Figure 39: Trans-impedance amplifier schematic

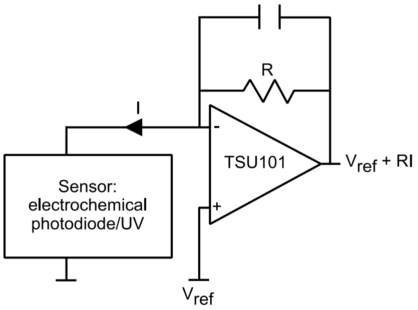
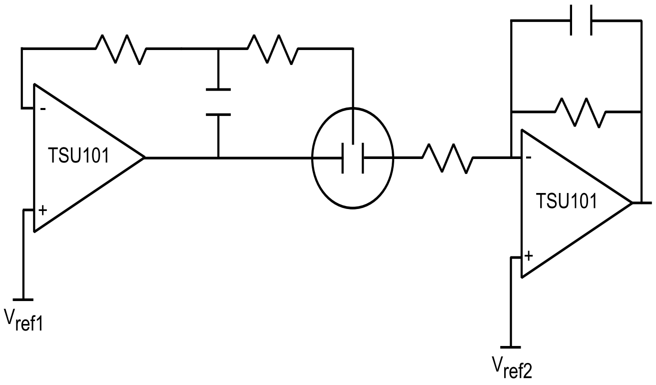


Figure 40: Potentiostat schematic using the TSU101 (or TSU102)



4.8 Fast desaturation

When the TSU101, TSU102, and TSU104 operational amplifiers go into saturation mode, they take a short period of time to recover, typically thirty microseconds. When recovering after saturation, the TSU10x series does not exhibit any voltage peaks that could generate issues (such as false alarms) in the application (see *Figure 17*). This is because the internal gain of the amplifier decreases smoothly when the output signal gets close to the V_{CC+} or V_{CC-} supply rails (see *Figure 15* and *Figure 16*).

Thus, to maintain signal integrity, the user should take care that the output signal stays at 100 mV from the supply rails.

With a trans-impedance schematic, a voltage reference can be used to keep the signal away from the supply rails.

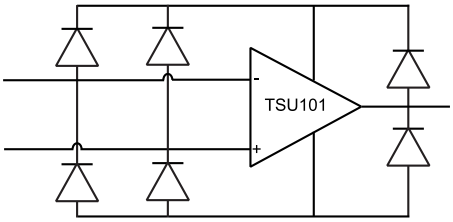
4.9 Using the TSU10x series in comparator mode

The TSU10x series can be used as a comparator. In this case, the output stage of the device always operates in saturation mode. In addition, *Figure 4* shows the current consumption is not bigger and even decreases smoothly close to the rails. The TSU101, TSU102, and TSU104 are obviously operational amplifiers and are therefore optimized to be used in linear mode. We recommend to use the TS88 series of nanopower comparators if the primary function is to perform a signal comparison only.

4.10 ESD structure of TSU10x series

The TSU101, TSU102, and TSU104 are protected against electrostatic discharge (ESD) with dedicated diodes (see *Figure 41: "ESD structure"*). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails (V_{CC+} or V_{CC-}).

Figure 41: ESD structure



Current through the diodes must be limited to a maximum of 10 mA as stated in *Table 1: "Absolute maximum ratings (AMR)"*. A serial resistor or a Schottky diode can be used on the inputs to improve protection but the 10 mA limit of input current must be strictly observed.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

5.1 SC70-5 (or SOT323-5) package information

Figure 42: SC70-5 (or SOT323-5) package outline

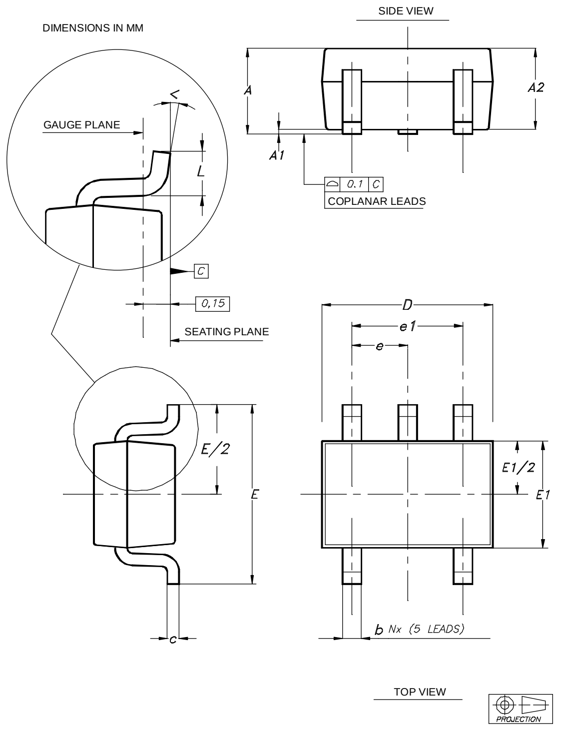


Table 6: SC70-5 (or SOT323-5) mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.315		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.315	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

5.2 SOT23-5 package information

Figure 43: SOT23-5 package outline

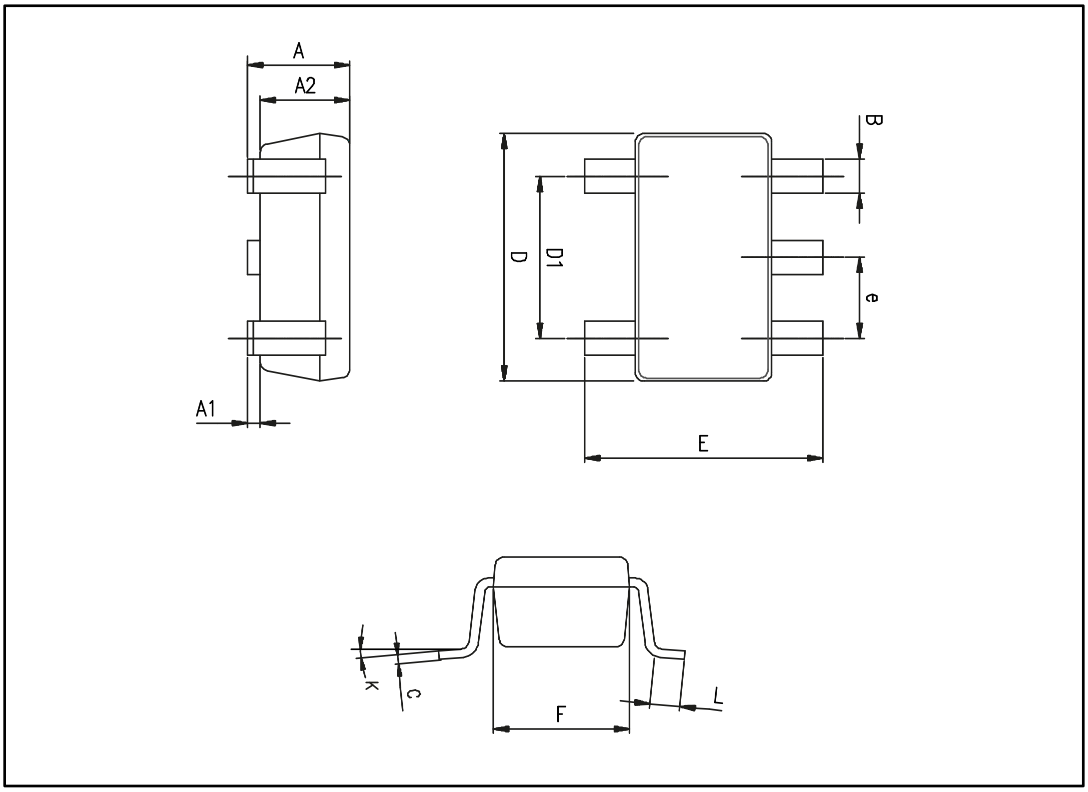


Table 7: SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

5.3 DFN8 2x2 package information

Figure 44: DFN8 2x2 package outline

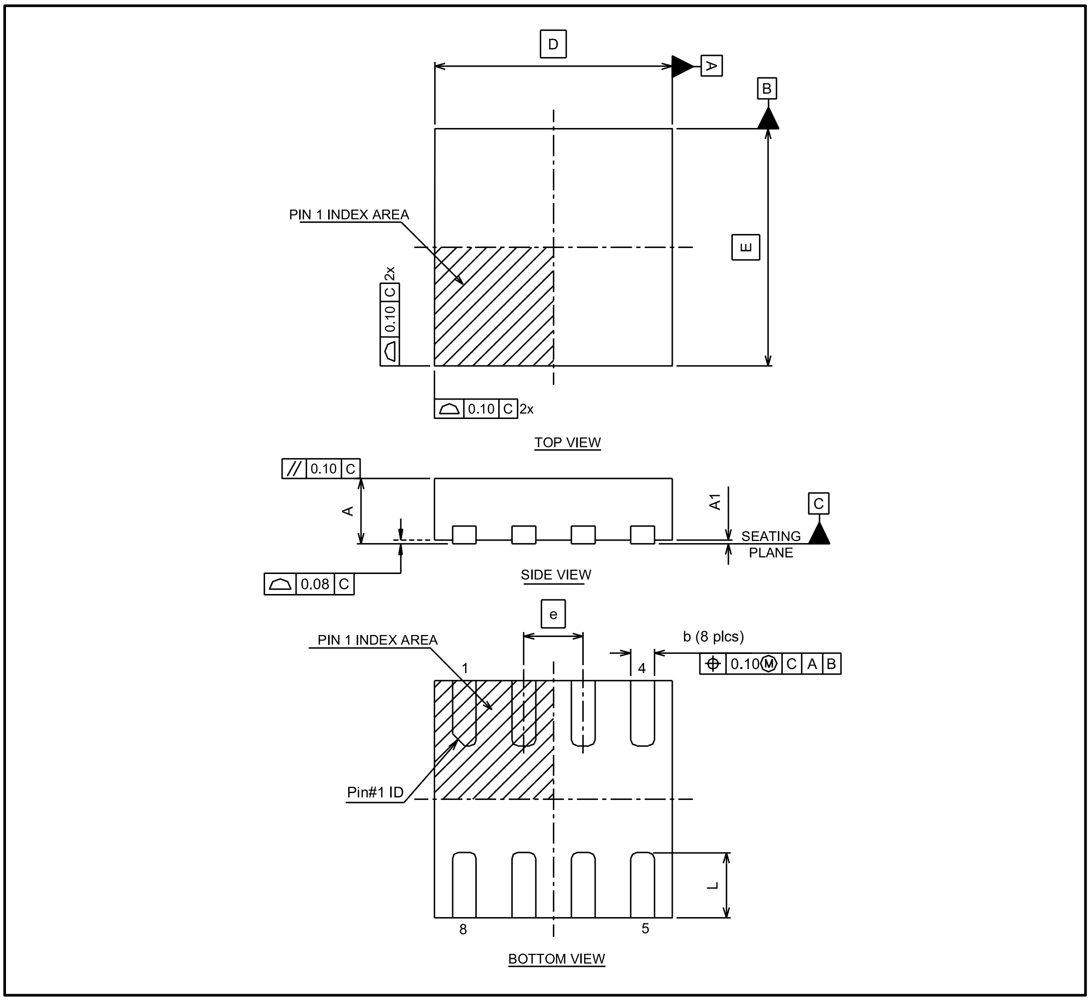


Table 8: DFN8 2x2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8					

5.4 MiniSO8 package information

Figure 45: MiniSO8 package outline

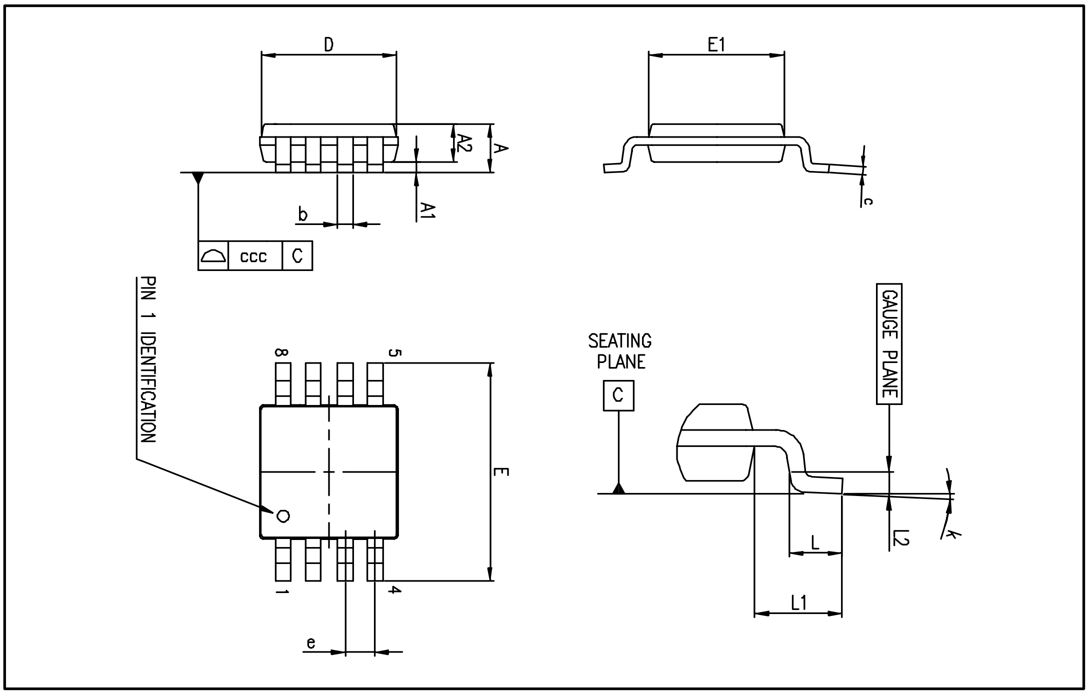
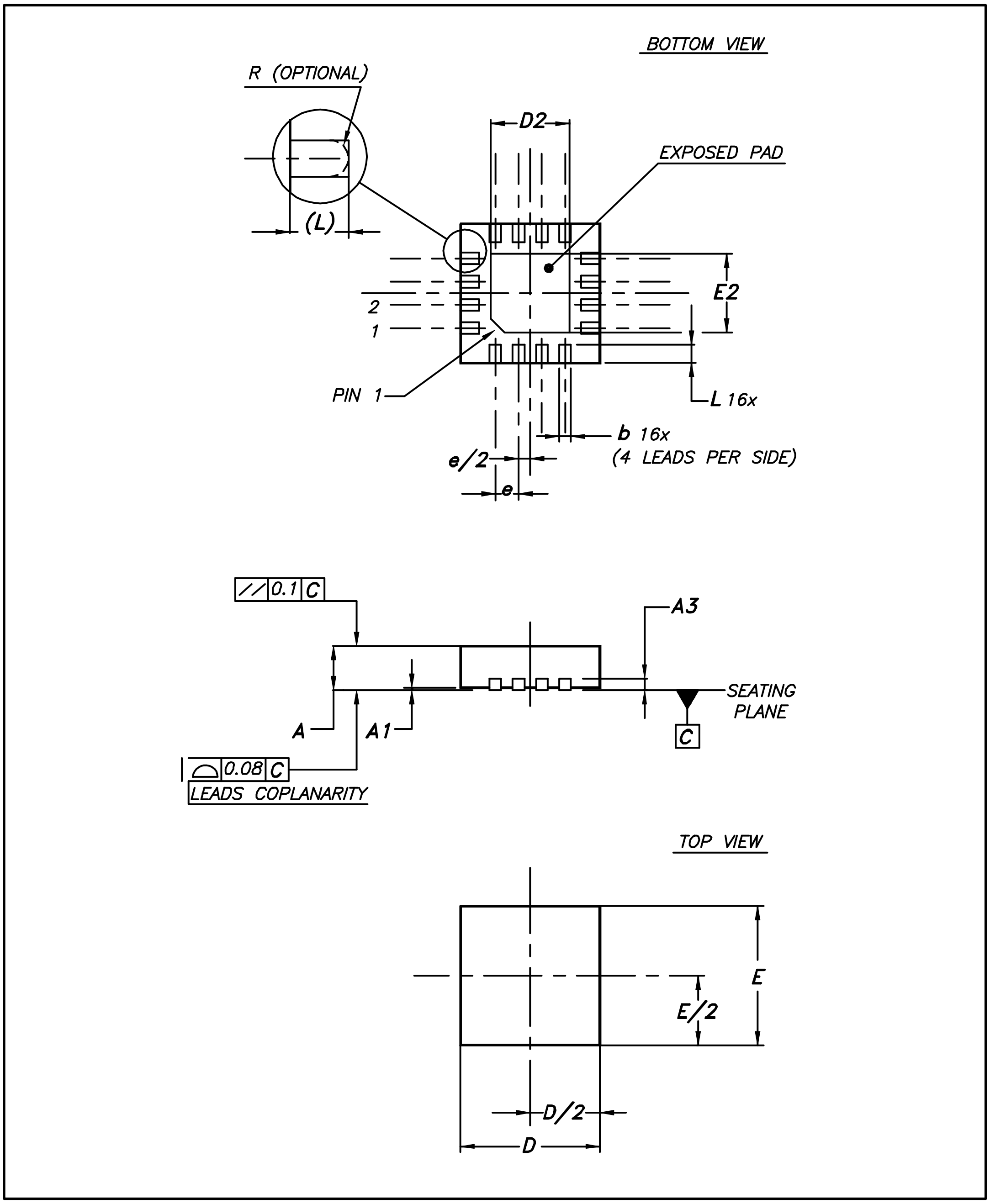


Table 9: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.5 QFN16 3x3 package information

Figure 46: QFN16 3x3 mm package outline

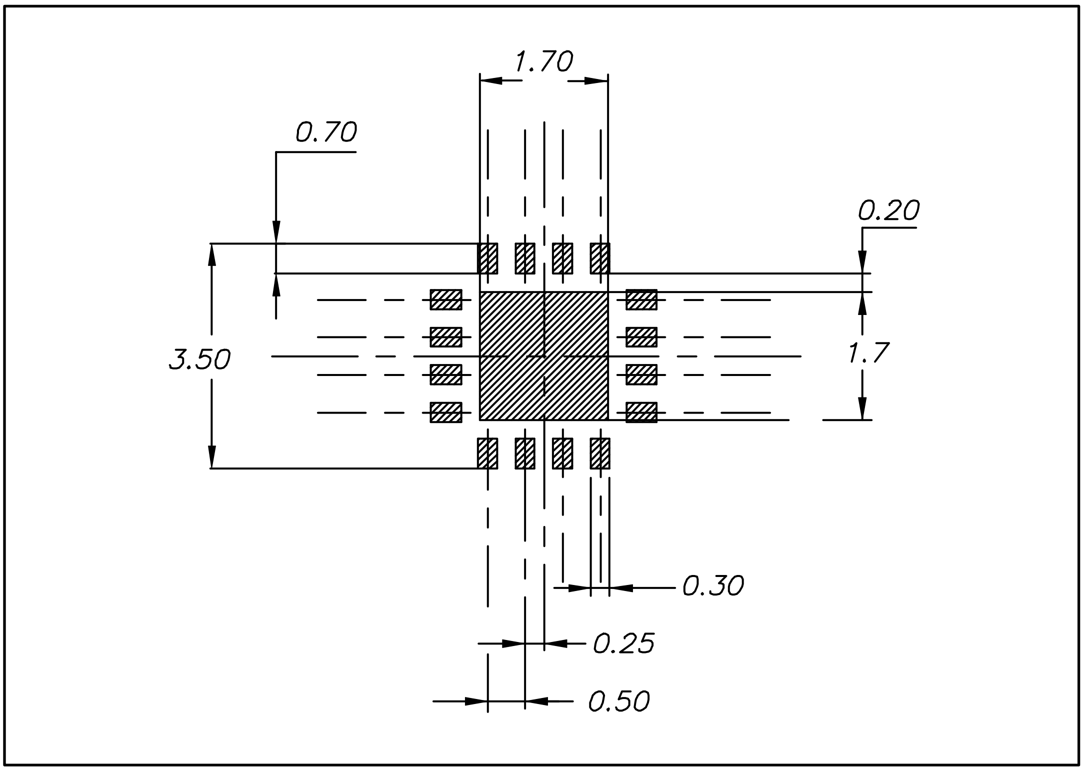


The exposed pad is not internally connected and can be set to ground.

Table 10: QFN16 3x3 mm mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0		0.05	0		0.002
A3		0.20			0.008	
b	0.18		0.30	0.007		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.50		1.80	0.059		0.071
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.80	0.059		0.071
e		0.50			0.020	
L	0.30		0.50	0.012		0.020

Figure 47: QFN16 3x3 mm recommended footprint



5.6 TSSOP14 package information

Figure 48: TSSOP14 package outline

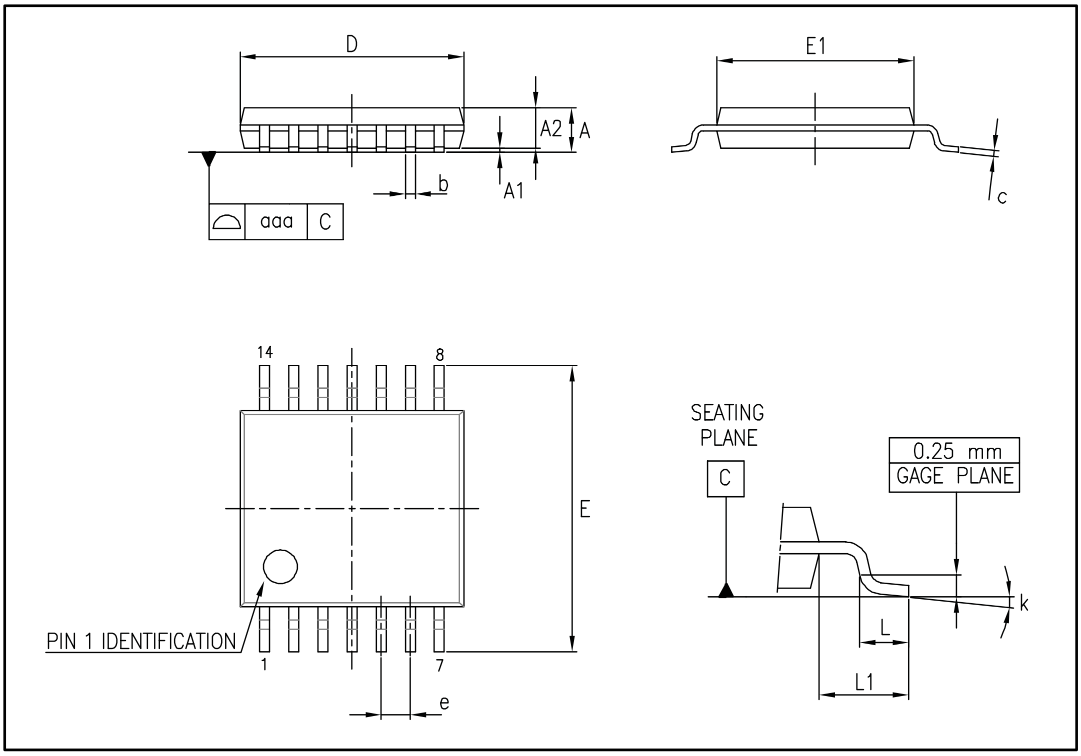


Table 11: TSSOP14 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

6 Ordering information

Table 12: Order codes

Order code	Temperature range	Package	Packing	Marking
TSU101ICT	-40 °C to 85 °C	SC70-5	Tape and reel	K22
TSU101ILT		SOT23-5		K160
TSU101RICT		SC70-5		K24
TSU101RILT		SOT23-5		K169
TSU102IQ2T		DFN8 2x2		K24
TSU102IST		MiniSO8		K160
TSU104IQ4T		QFN16 3x3		K160
TSU104IPT		TSSOP14		TSU104I

7 Revision history

Table 13: Document revision history

Date	Revision	Changes
16-Apr-2013	1	Initial release
02-Jul-2013	2	Added the TSU102 and TSU104 devices and updated the datasheet accordingly. Added the silhouettes, pin connections, and package information for DFN8 2x2, MiniSO8, QFN16 3x3, and TSSOP14. Added *Figure 36* and *Figure 37*
04-Sep-2015	3	Updated title of *Figure 31* Replaced QFN16 3x3 package information (outline, mechanical data, and footprint).

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