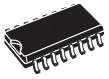
VIPER26

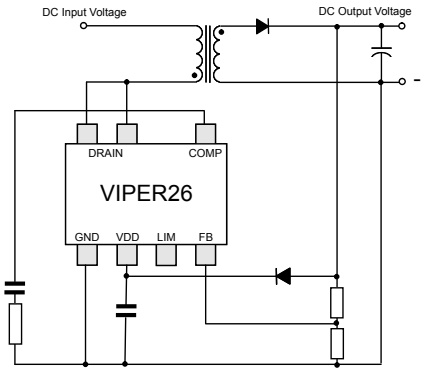
Datasheet

Fixed frequency VIPer plus family



SO16 narrow

DIP-7



Product status link

VIPER26

Product label

SUSTAINABLE TECHNOLOGY

Features

- 800 V avalanche rugged power MOSFET allowing wide range V_{AC} input range to be covered
- Embedded HV startup and sense-FET
- Current mode PWM controller
- Minimized system input power consumption:
  - Less than 30 mW @ 230 V_{AC} in no-load condition
  - Less than 400 mW @ 230 V_{AC} with 250 mW load
- Limiting current with adjustable set point
- Jittered switching frequency to reduce the EMI filter cost:
  - 60 kHz ±4 kHz (L type)
  - 115 kHz ±8 kHz (H type)
- Embedded error amplifier
- Hysteretic thermal shutdown
- Built-in soft-start for improved system reliability
- Protections with automatic restart: overload/short-circuit (OLP), feedback loop disconnection

Application

- Auxiliary power supply for appliances
- Power metering
- LED drivers
- SMPS for set-top boxes, DVD players and recorders

Description

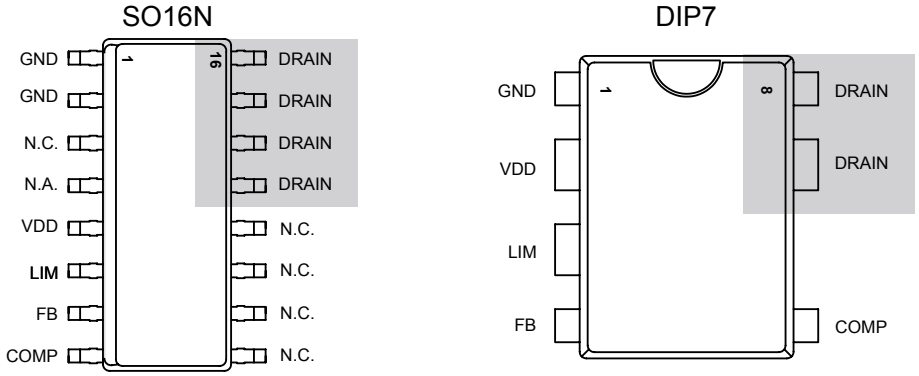
The VIPER26 device is a smart high voltage converter that integrates an 800 V avalanche-rugged power MOSFET with PWM current mode control. The power MOSFET with 800 V breakdown voltage allows an extended input voltage range to be applied, as well as the size of the DRAIN snubber circuit to be reduced.

This IC meets the most stringent energy-saving standards with very low consumption and burst mode operation under light load.

The design of flyback, buck and buck boost converters is supported. The integrated HV startup, sense-FET, error amplifier and oscillator with jitter allow complete application designs with a minimum number of components.

1 Pin settings

Figure 1. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 1. Pin descriptions

Pin number		Name	Function
DIP7	SO16N		
1	1-2	GND	**Ground and MOSFET source.** Connection of the source of the internal MOSFET and controller ground reference.
-	3	N.C.	**Not connected.** This pin can be soldered to GND.
-	4	N. A.	**Not available for user.** This pin is mechanically connected to the controller die pad of the frame. In order to improve noise immunity, it is highly recommended to connect it to GND (pin 1,2).
2	5	VDD	**Controller Supply**. An external storage capacitor has to be connected across this pin and GND. The pin, internally connected to the high voltage current source, provides the VDD capacitor charging current at startup and during fault conditions. A small bypass capacitor (0.1 µF typ.) in parallel, placed as close as possible to the IC, is also recommended for noise filtering purposes.
3	6	LIM	**Drain current limitation.** This pin allows setting the drain current limitation to a lower value than the default I_{Dlim} value. The limit can be reduced by connecting an external resistor between this pin and GND. In case of high electrical noise, a capacitor may be connected between this pin and GND; the capacitor value must be lower than 470 nF in order to not impact the functionality of the pin. The pin can be left open if the default drain current limitation, I_{Dlim}, is used.
4	7	FB	**Direct feedback**. It is the inverting input of the internal transconductance E/A, which is internally referenced to 3.3 V with respect to GND. In a non-isolated converter, the output voltage information is directly fed into the pin through a voltage divider. In primary regulation, the FB voltage divider is connected to the VCC. The E/A is disabled by soldering FB to GND.
5	8	COMP	**Compensation**. It is the output of the internal E/A. A compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the control loop. In case of isolated secondary side regulation, the internal E/A must be disabled and the COMP directly driven by the optocoupler to control the DRAIN peak current setpoint.
-	9-12	N.C.	**Not internally connected.** These pins must be left floating in order to ensure a safe clearance distance.
7,8	13-16	DRAIN	**MOSFET drain.** The internal high voltage current source sinks current from this pin to charge the VCC capacitor at startup. These pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB, the copper area must be placed under these pins in order to decrease the total junction-to-ambient thermal resistance, thus facilitating the power dissipation.

2 Electrical and thermal ratings

Table 2. Absolute maximum ratings

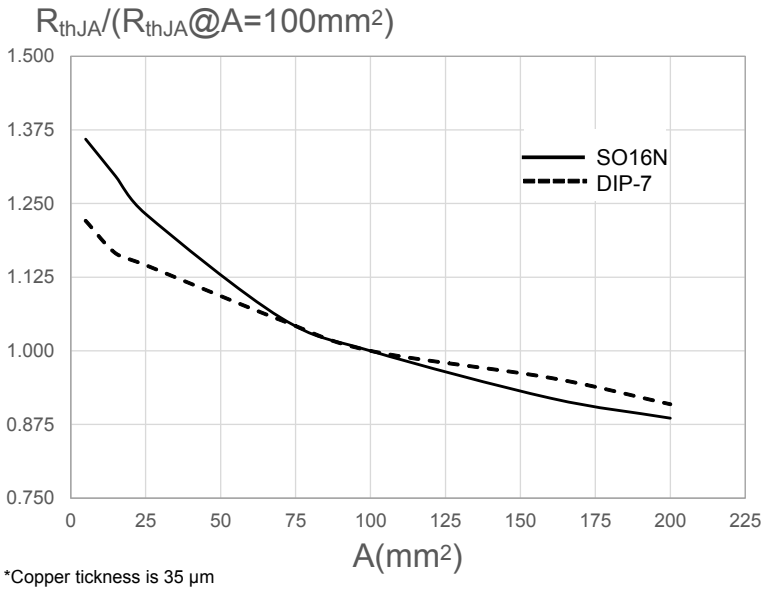
Symbol	Parameter	Min.	Max.	Unit
V_{DRAIN}	Drain-to- source (ground) voltage	-	800	V
I_{DRAIN}	Pulse drain current (limited by T_J = 150 °C)	-	3	A
V_{COMP}	COMP voltage	-0.3	3.5V	V
V_{FB}	FB voltage	-0.3	4.8	V
V_{LIM}	LIM voltage	-0.3	2.4	V
V_{DD}	Supply voltage	-0.3	Self limited	V
I_{DD}	Input current	-0.3	20	mA
P_{TOT}	Power Dissipation @ Tamb < 40 °C (DIP7)	-	1	W
	Power Dissipation @ Tamb < 60 °C (SO16N)	-	1.5	W
T_J	Junction Temperature operating range	-40	150	°C
T_{STG}	Storage Temperature	-55	150	°C

Table 3. Thermal data

Symbol	Parameter	Max. value		Unit
		SO16N	DIP-7	
R_{TH-JC}	Thermal resistance junction to case(1) (Dissipated power = 1 W)	10	10	°C/W
R_{TH-JA}	Thermal resistance junction ambient (1) (Dissipated power = 1 W)	120	120	°C/W
R_{TH-JC}	Thermal resistance junction to case (2) (Dissipated power = 1 W)	5	5	°C/W
R_{TH-JA}	Thermal resistance junction ambient (2) (Dissipated power = 1 W)	85	95	°C/W

1. *When mounted on a standard, single side FR4 board with minimum copper area.*
2. *When mounted on a standard, single side FR4 board with 100 mm2 of Cu (35 µm thick).*

Figure 2. R_{th} versus area



*Copper tickness is 35 µm

Table 4. Avalanche characteristics

Symbol	Parameter	Min.	Max.	Unit
E_{AV}	Repetitive avalanche energy (limited by T_J=150°C)	-	5	mJ
I_{AR}	Repetitive avalanche current (limited by T_J=150°C)	-	1.5	A

2.1 Electrical characteristics

T_J = -40 to 125°C, V_{DD} = 14 V (unless otherwise specified)

Note: Adjust V_{DD} above V_{DD} on startup threshold before setting to 14 V

Table 5. Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{COMP} = V_{GND}, T_J = 25°C	800	-	-	V
I_{OFF}	OFF state drain current	V_{DRAIN} = max. rating, V_{COMP} = V_{GND}, T_J = 25°C	-	-	60	µA
$R_{DS(on)}$	Static drain-source ON-resistance	I_{DRAIN} = 0.2 A, T_J = 25°C	-	-	7	Ω
		I_{DRAIN} = 0.2 A, T_J = 125°C	-	-	14	Ω

Table 6. Supply section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage	I_{DRAIN} = 1 mA; V_{COMP} = GND; T_J = 25°C	-	-	90	V
I_{DDch1}	Charging current during startup	V_{DRAIN} = 100 to 640 V; V_{DD} = 4 V	-0.6	-	-1.8	mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DDch2}	Charging current during autorestart	V_{DRAIN} = 100 to 640 V; V_{DD} = 9 V falling edge	-7	-	-13	mA
V_{DD}	Operating voltage range	-	11.5	-	23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 15 mA;	23.5	-	-	V
V_{DDon}	V_{DD} startup threshold	-	12	13	14	V
V_{DDCSon}	V_{DD} on internal high voltage current generator threshold	-	9.5	10.5	11.5	V
V_{DDoff}	V_{DD} undervoltage shutdown threshold	-	7	8	9	V
Current						
I_{DD0}	Operating supply current, not switching	F_{OSC} = 0 kHz; V_{COMP} = GND	-	-	0.6	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V; V_{SW} = 60 kHz	-	-	2	
		V_{DRAIN} = 120 V; V_{SW} = 115 kHz	-	-	3	
I_{DDoff}	Operating supply current with $V_{DD} < V_{DDoff}$	$V_{DD} < V_{DDoff}$	-	-	0.35	
I_{DDol}	Open loop failure current threshold	$V_{DD} = V_{DDclamp}$; V_{COMP} = 3.3 V	4	-	-	

Table 7. Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Error amplifier						
V_{REF_FB}	FB reference voltage	-	3.2	3.3	3.4	V
$I_{FB\_PULL\ UP}$	Pull-up current	-	-	-1	-	µA
G_M	Trans conductance	V_{COMP} = 1.5 V, V_{FB} > $V_{FB\ REF}$	-	2	-	mA/V
Current setting (LIM) pin						
V_{LIM_LOW}	Low level clamp voltage	I_{LIM} = -100 µA	-	0.5	-	V
Compensation (COMP) pin						
V_{COMPH}	Upper saturation limit	T_J = 25°C	-	3	-	V
V_{COMPL}	Burst mode threshold	T_J = 25°C	1	1.1	1.2	V
V_{COMPL_HYS}	Burst mode hysteresis	T_J = 25°C	-	40	-	mV
H_{COMP}	$\Delta V_{COMP}/\Delta I_{DRAIN}$	-	-	3	-	V/A
$R_{COMP(DYN)}$	Dynamic resistance	V_{FB} = GND	-	15	-	kΩ
I_{COMP}	Source / sink current	V_{FB} > 100 mV	-	150	-	µA
	Max. source current	V_{COMP} = GND; V_{FB} = GND	-	220	-	
Current limitation						
I_{DLIM}	Drain current limitation	I_{LIM} = -10 µA; V_{COMP} = 3.3 V; T_J = 25 °C	0.66	0.7	0.74	A
t_{SS}	Soft-start time	-	-	8.5	-	ms
t_{ON_MIN}	Minuimum turn-on time	-	-	-	480	ns
I_{Dlim_bm}	Burst mode current limitation	$V_{COMP} = V_{COMPL}$	-	145	-	mA
Overload						
t_{OVL}	Overload time	-	-	50	-	ms

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{RESTART}$	Restart time after fault	-	-	1	-	s
Oscillator section						
F_{OSC}	Switching frequency	VIPER26L	54	60	66	kHz
		VIPER26H	103	115	127	
F_D	Modulation depth	F_{OSC} = 60 kHz	-	±4	-	kHz
		F_{OSC} = 115 kHz	-	±8	-	
F_M	Modulation frequency	-	-	230	-	Hz
D_{MAX}	Maximum duty cycle	-	70	-	80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature threshold	-	150	160	-	°C
T_{HYS}	Thermal shutdown hysteresis	-	-	30	-	°C

3 Typical electrical characteristics

Figure 3. I_{DLIM} vs. T_J

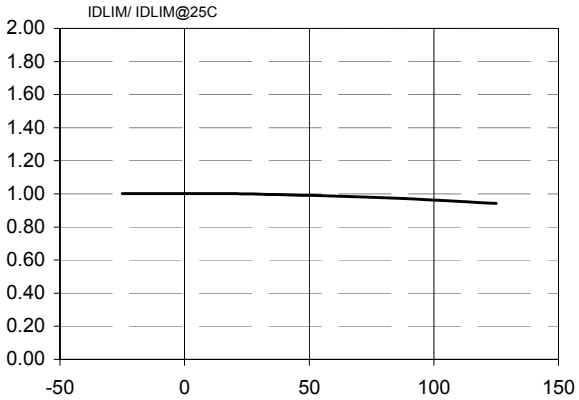


Figure 4. F_{OSC} vs. T_J

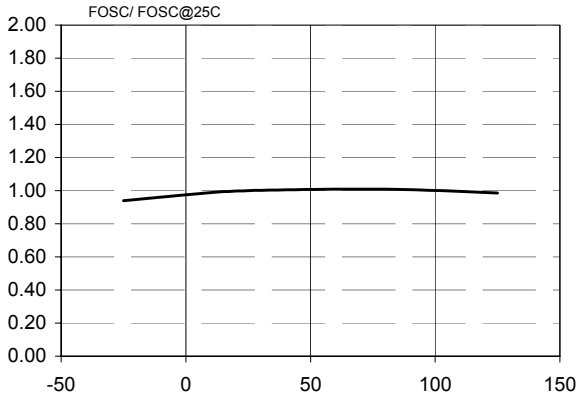


Figure 5. V_{DRAIN_START} vs. T_J

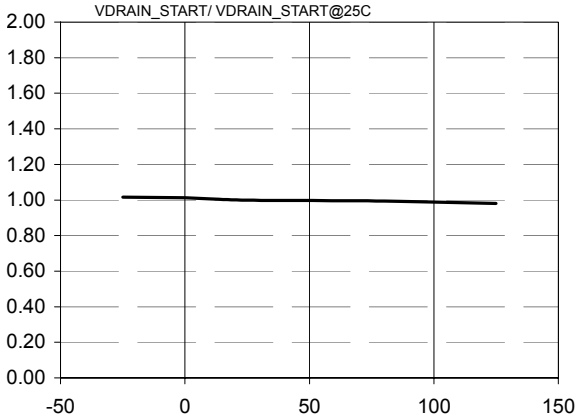


Figure 6. H_{COMP} vs. T_J

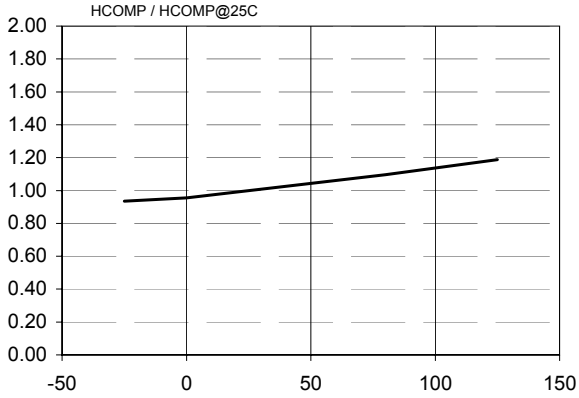


Figure 7. G_M vs. T_J

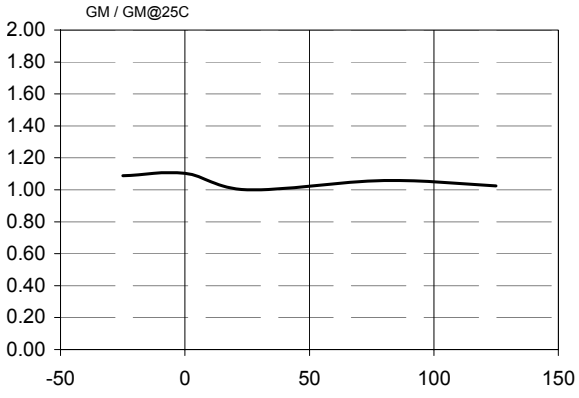


Figure 8. V_{REF_FB} vs. T_J

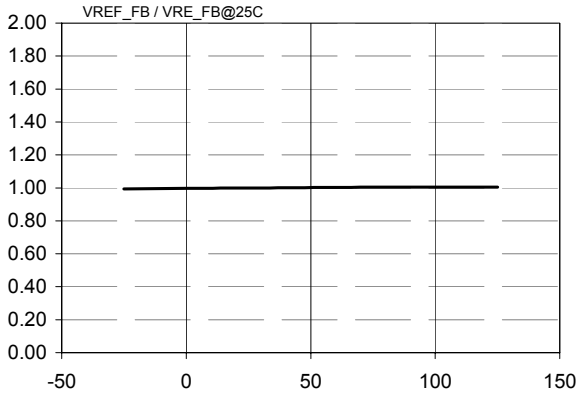


Figure 9. I_{COMP} vs. T_J

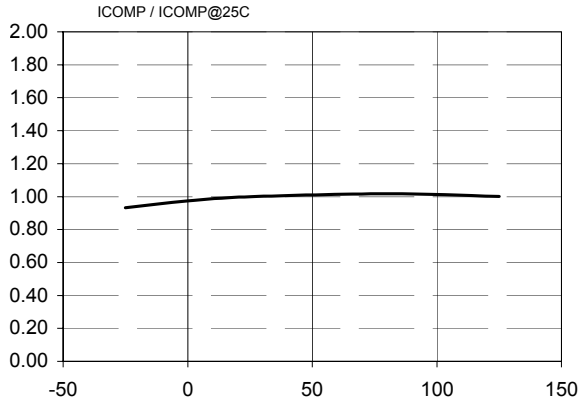


Figure 10. Operating supply current (no switching) vs T_J

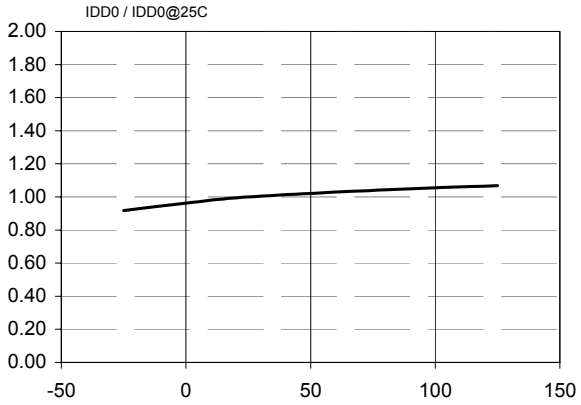


Figure 11. Operating supply current (switching) vs T_J

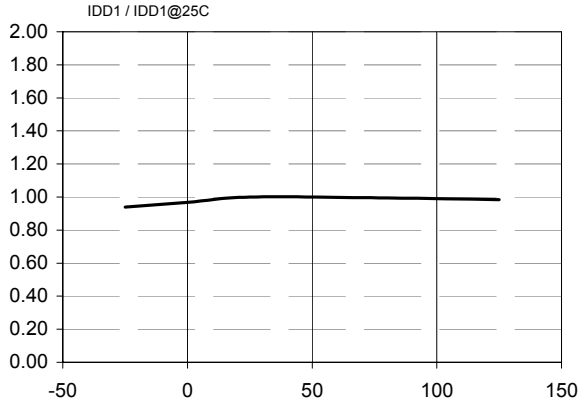


Figure 12. I_{DLIM}vs. R_{LIM}

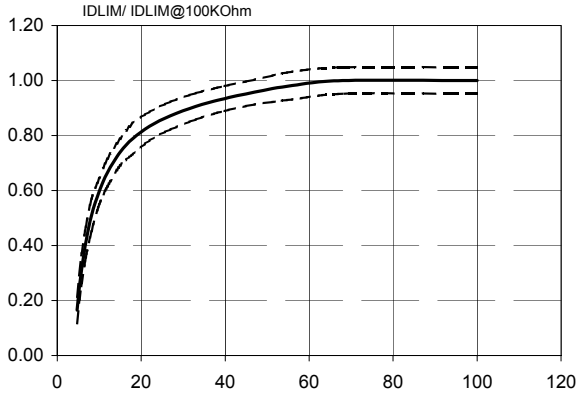


Figure 13. Power MOSFET on-resistance vs T_J

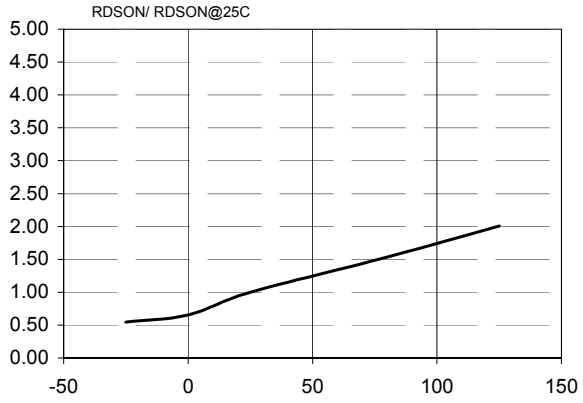


Figure 14. Power MOSFET breakdown voltage vs T_J

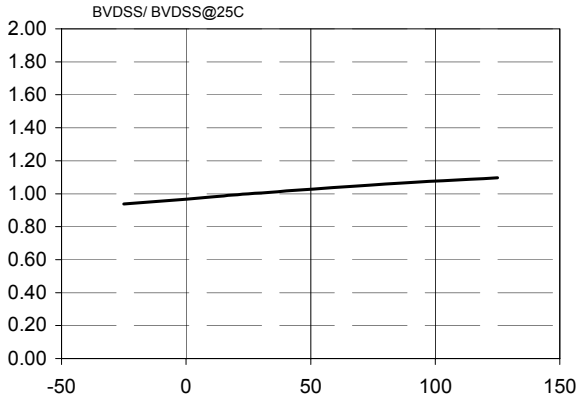


Figure 15. Power MOSFET capacitance variation vs V_{DS}

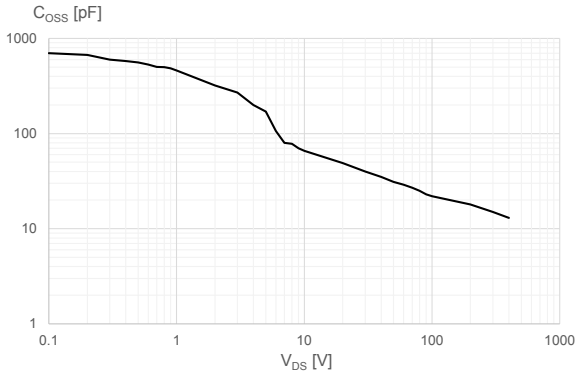


Figure 16. SOA SO16N package

When mounted on a standard single side FR4 board with 100 mm² of Cu (35µm thick)

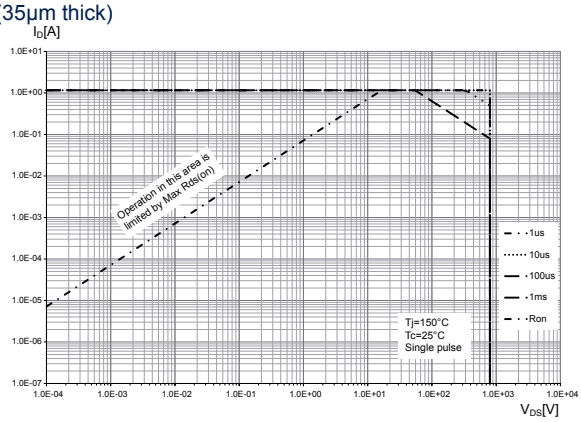


Figure 17. SOA DIP7 package

When mounted on a standard single side FR4 board with 100 mm² of Cu (35µm thick)

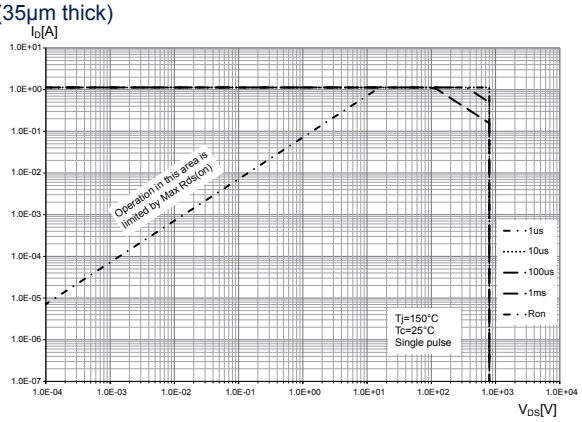
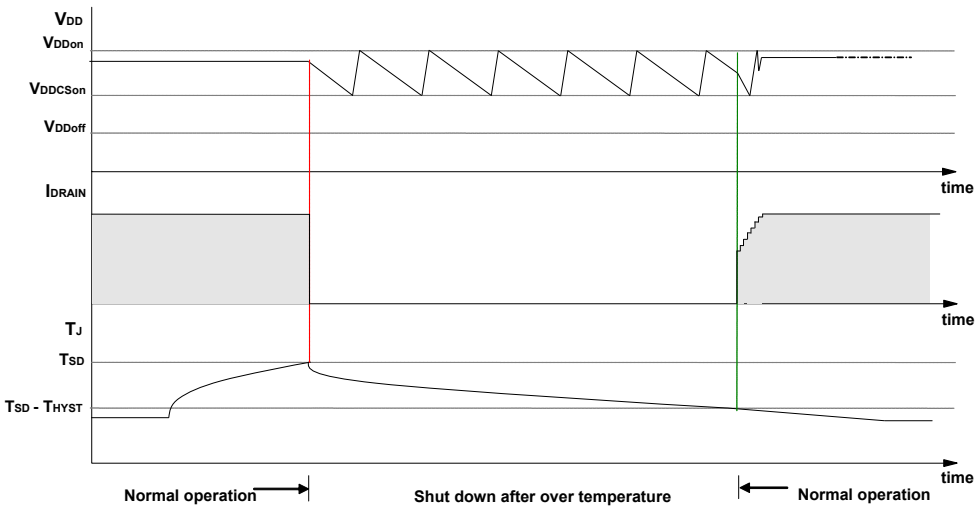


Figure 18. Thermal shutdown



4 Typical circuits

Figure 19. **Buck converter (V_{OUT}>V_{DDCSon})**

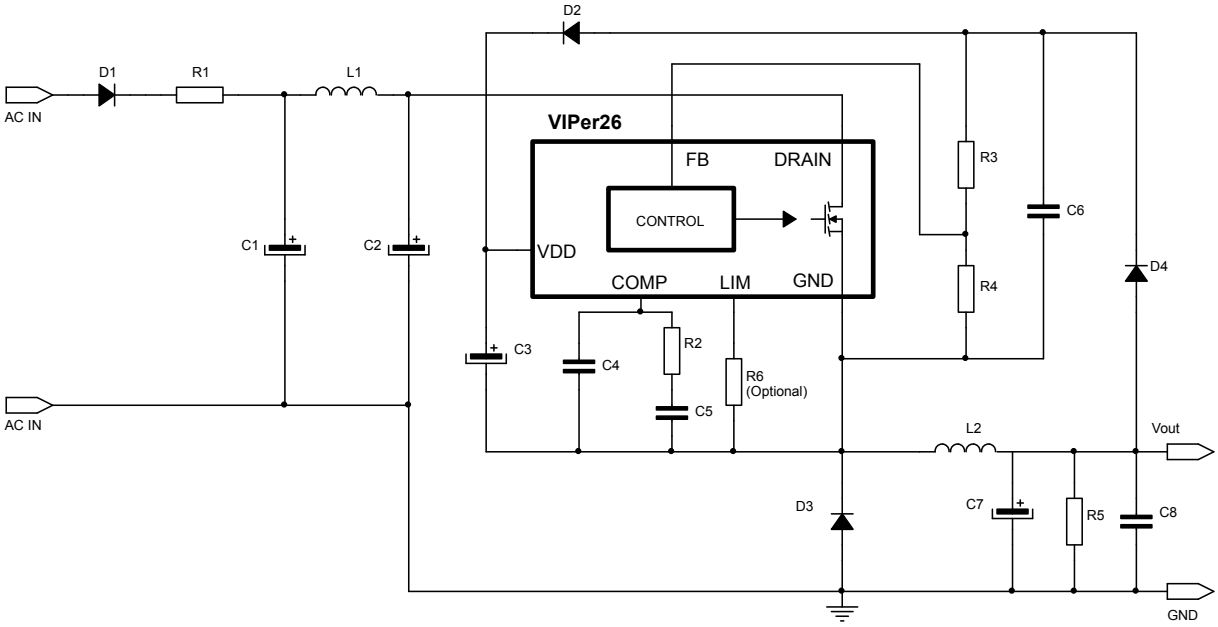


Figure 20. **Flyback converter (isolated)**

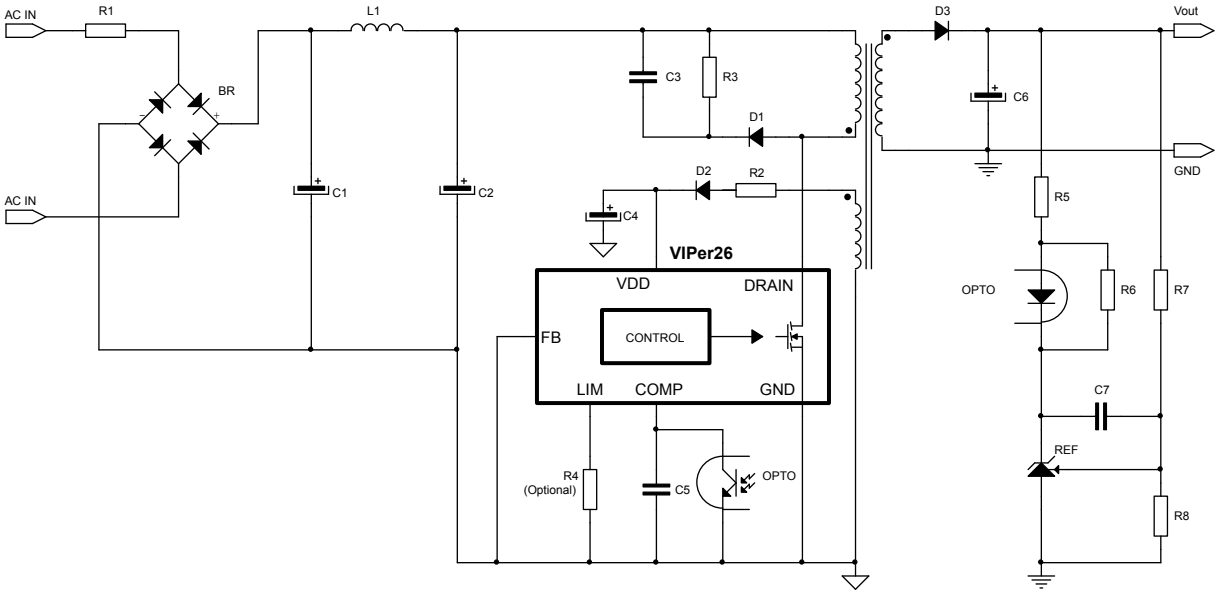


Figure 21. **Flyback converter (primary regulation)**

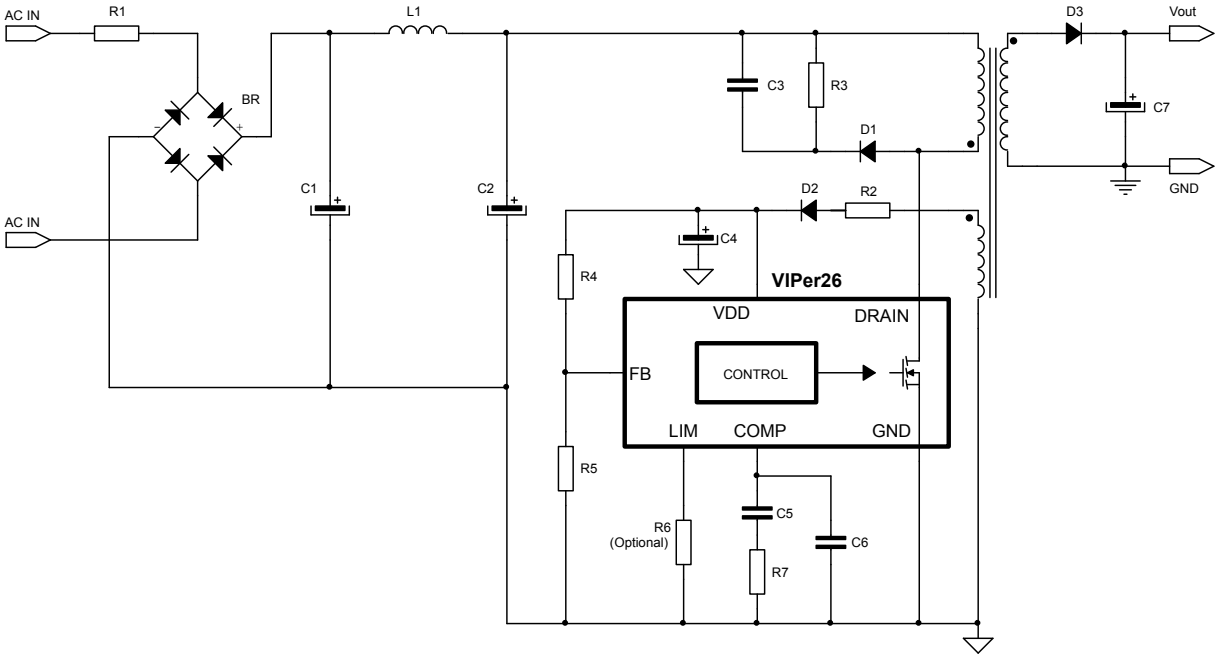


Figure 22. **Flyback converter (non isolated, $V_{OUT} \geq V_{DDCSon}$)**

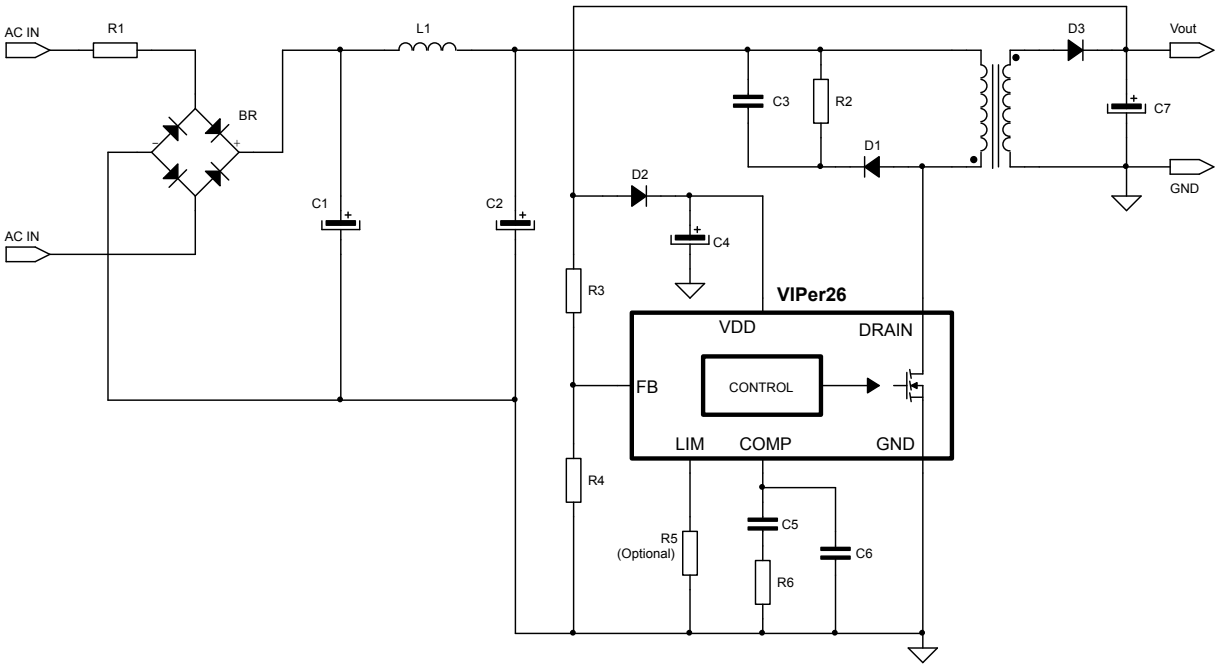
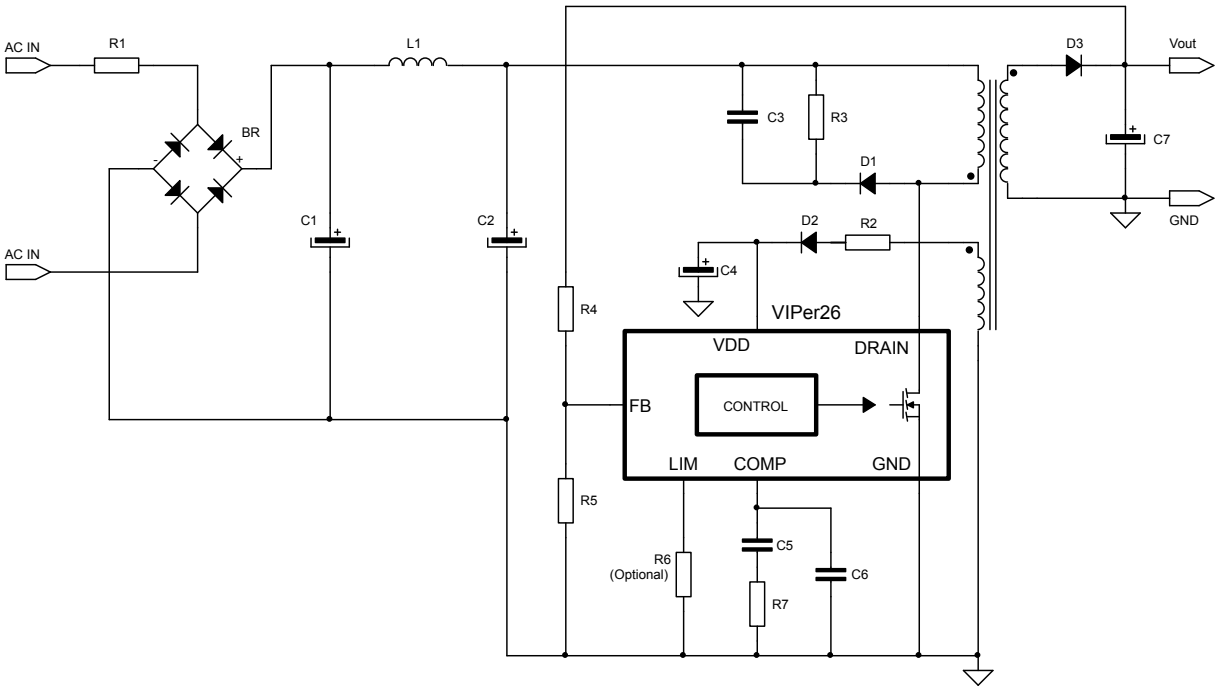
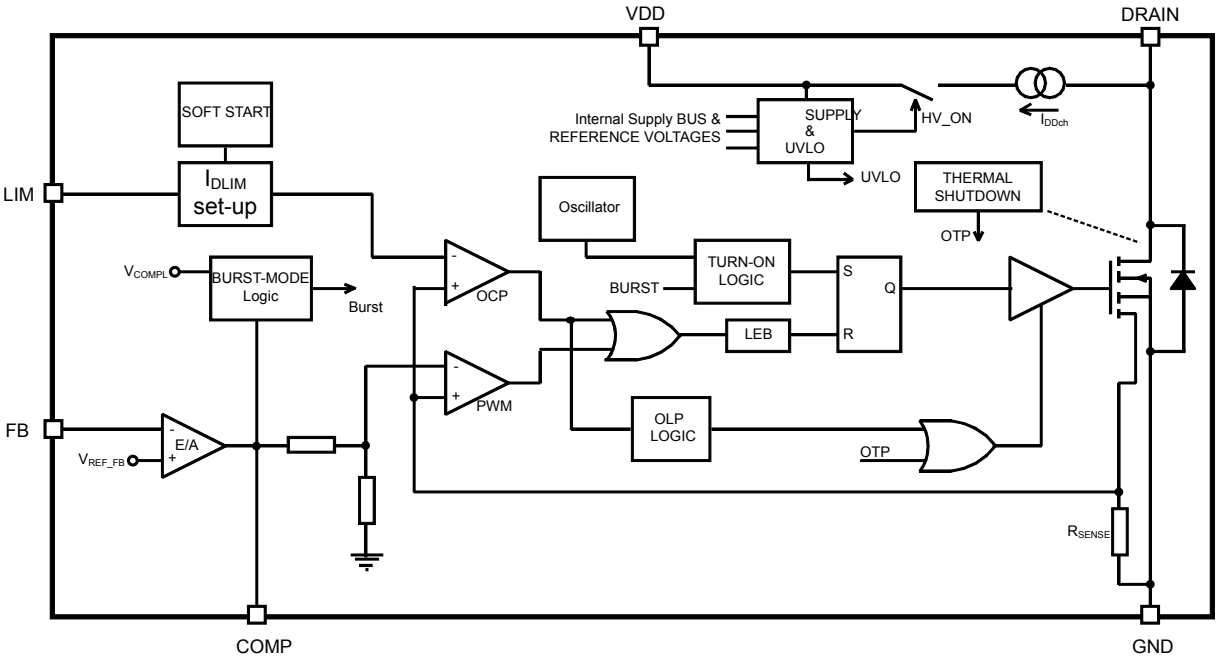


Figure 23. Flyback converter (non isolated, $V_{OUT} < V_{DDCSon}$)



4.1 Block diagram

Figure 24. Block diagram



4.2 Typical power

Table 8. **VIPer26 typical power**

230 V_{AC}		85-265 V_{AC}	
Adapter (1)	Open Frame (2)	Adapter (1)	Open Frame (2)
18 W	20 W	10 W	12 W

1. *Typical continuous power in non-ventilated enclosed adapter measured at 50°C ambient.*
2. *Maximum practical continuous power in an open frame design at 50°C ambient, with adequate heat sinking.*

5 Power section

The power section is implemented with an n-channel power MOSFET with a breakdown voltage of 800 V min. and a typical $R_{DS(on)}$ of 7 Ω. It includes a SenseFET structure to allow virtually lossless current sensing and a thermal sensor.

The gate driver of the power MOSFET is designed to supply a controlled gate current during turn ON and turn OFF in order to minimize common mode EMI. During UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned ON accidentally.

6 High-voltage current generator

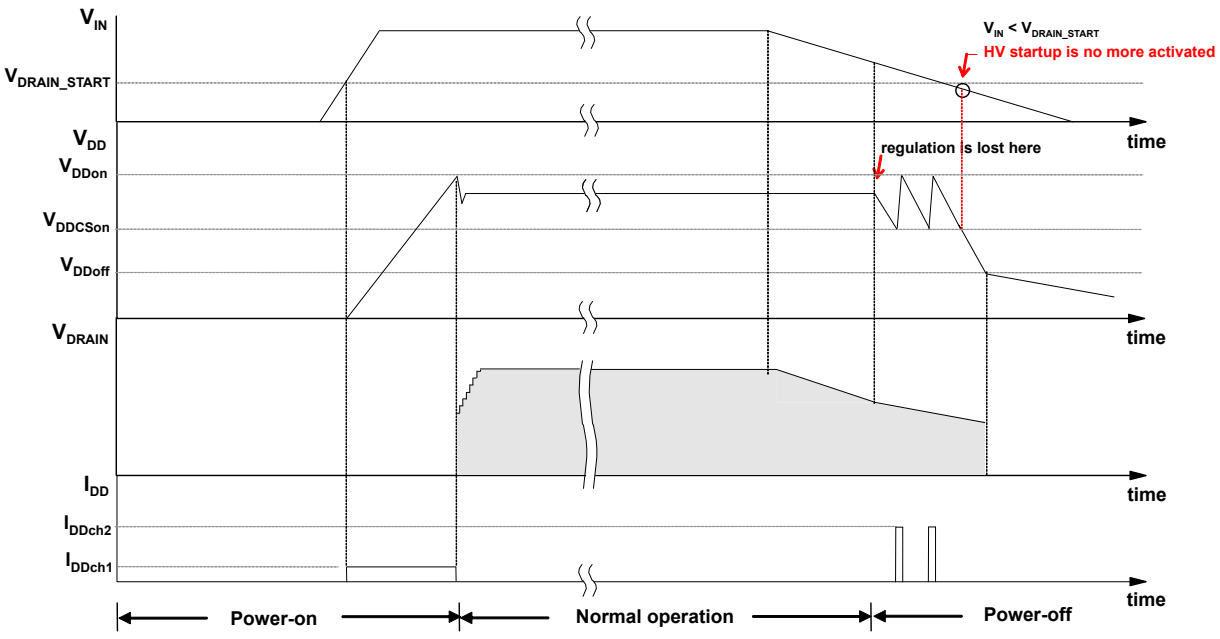
The high voltage current generator is supplied by the DRAIN pin. On initial startup of the converter, it is enabled when the voltage across the input bulk capacitor reaches the V_{DRAIN_START} threshold, sourcing the I_{DDch1} current (see Table 6. Supply section). As the V_{DD} voltage reaches the V_{DDon} start-up threshold, the power section starts switching and the high voltage current generator is turned OFF. The VIPer26 is powered by the external source.

After the start-up, the auxiliary winding or the diode connected to the output voltage must power the V_{DD} capacitor with a voltage higher than the V_{DDCSon} threshold (see Table 6).

During the switching, the internal current source is disabled and the consumptions are minimized. If a fault occurs, switching is stopped and the device is self biased by the internal high voltage current source; it is activated between the levels V_{DDCSon} and V_{DDon} delivering the current I_{DDch2} to the V_{DD} capacitor during the MOSFET OFF time, see Figure 25.

At converter power-down, the V_{DD} voltage drops and the converter activity stops as it falls below the V_{DDoff} threshold (see Table 6).

Figure 25. Power ON and power OFF



7 Oscillator

The switching frequency is internally fixed at 60 kHz (VIPER26LN or LD) or 115 kHz (VIPER26HN or HD).

In both cases, the switching frequency is modulated by approximately ±4 kHz (60 kHz version) or ±8 kHz (115 kHz version) at 230 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of sideband harmonics, having the same net energy but with smaller amplitudes.

8 Soft startup

During the converter start-up phase, the soft-start function progressively increases the cycle-by-cycle drain current limit, up to the default value I_{Dlim}. This way, the drain current is further limited and the output voltage is progressively increased, therefore reducing the stress on the secondary diode. The soft-start time is internally fixed to t_{SS} (see typical value on Table 7. Controller section) and the function is activated for any converter start-up attempt or a fault event.

This function helps prevent transformer saturation during start-up and short-circuit.

9 Adjustable current limit set point

The VIPer26 includes a current mode PWM controller: cycle by cycle the drain current is sensed through the integrated resistor R_{SENSE} and the voltage is applied to the non inverting input of the PWM comparator, see Figure 24. Block diagram. As soon as the sensed voltage is equal to the voltage derived from the COMP pin, the power MOSFET is switched OFF.

In parallel with the PWM operations, the comparator OCP, see Figure 24, checks the level of the drain current and switch OFF the power MOSFET in case the current is higher than the threshold I_{Dlim}, see Table 7. Controller section.

The level of the drain current limit, I_{Dlim}, can be reduced depending on the sunk current from the pin LIM. The resistor R_{LIM}, between LIM and GND pins, fixes the current sunk and therefore the level of the current limit, I_{Dlim}, see Figure 12. I_{DLIM}vs. R_{LIM}.

When the LIM pin is left open or if the R_{LIM} has a high value (i.e., > 80 kΩ), the current limit is fixed to its default value, I_{Dlim}, as reported in Table 7.

10 FB pin and COMP pin

The device can be used both in non-isolated and in isolated topology. In case of non-isolated topology, the feedback signal from the output voltage is applied directly to the FB pin as inverting input of the internal error amplifier with reference voltage, V_{REF_FB}, see Table 7. Controller section.

The output of the error amplifier sources and sinks the current, I_{COMP}, to and from the compensation network connected on the COMP pin. This signal is then compared in the PWM comparator with the signal coming from the SenseFET; the power MOSFET is switched off when the two values are the same on a cycle by cycle basis. See Figure 24. Block diagram and Figure 26. Feedback circuit.

When the power supply output voltage is equal to the error amplifier reference voltage, V_{REF_FB}, a single resistor has to be connected from the output to the FB pin. For higher output voltages, the external resistor divider is needed. If the voltage on FB pin is accidentally left floating, an internal pull-up protects the controller.

The output of the error amplifier is externally accessible through the COMP pin and it is used for the loop compensation: usually an RC network.

As shown in Figure 26, the internal error amplifier has to be disabled in isolated power supplies (FB pin shorted to GND). In this case, an internal resistor is connected between an internal reference voltage and the COMP pin, see Figure 26. The current loop has to be closed on the COMP pin through the opto-transistor in parallel with the compensation network. The V_{COMP} dynamic range is between V_{COMPL} and V_{COMPH}, as shown in Figure 27.

When the voltage VCOMP drops below the voltage threshold V_{COMPL}, the converter enters burst mode, see Section 11 Burst mode.

When the voltage V_{COMP} rises above the V_{COMPH} threshold, the peak drain current will reach its limit, as well as the deliverable output power.

Figure 26. Feedback circuit

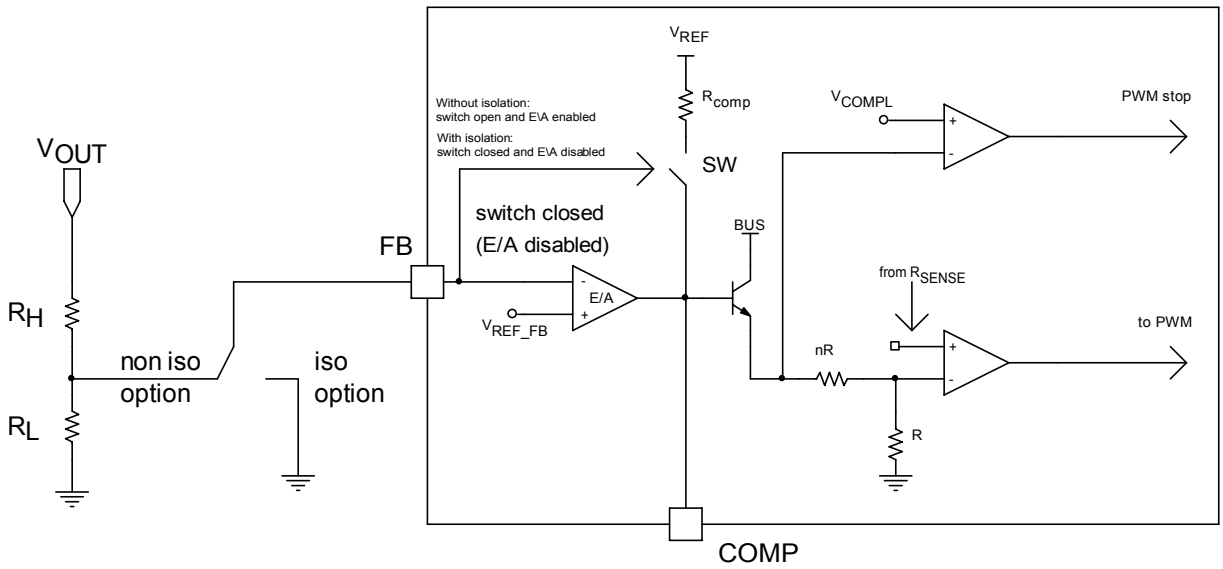
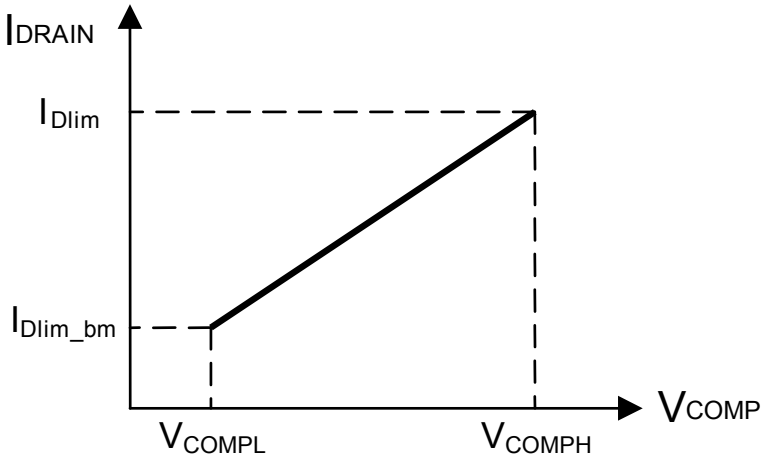


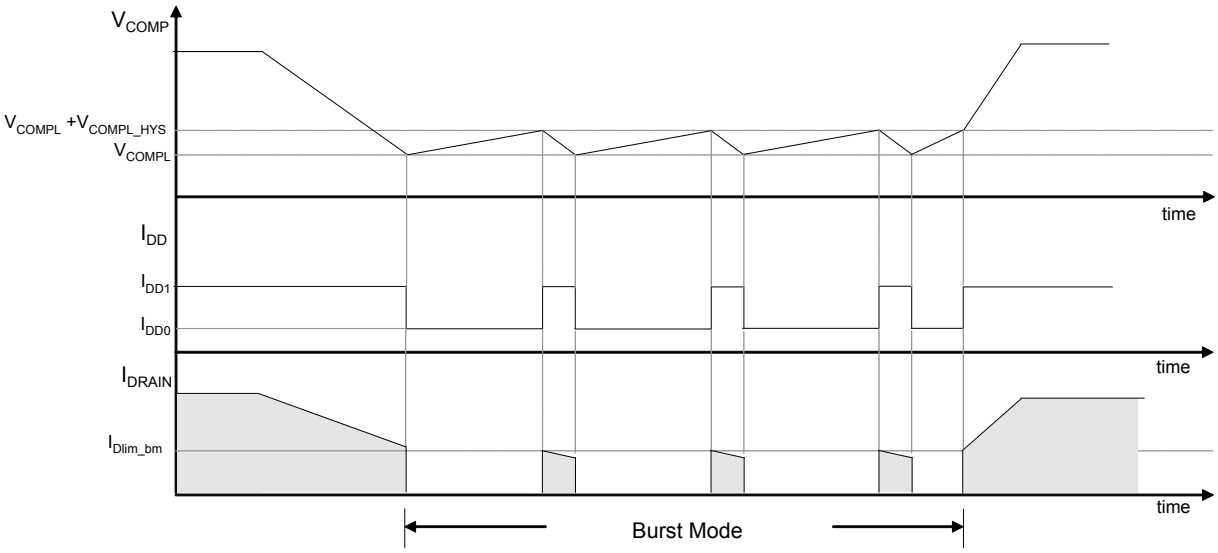
Figure 27. **COMP pin voltage versus I_{DLIM}**



11 Burst mode

When the voltage V_{COMP} drops below the threshold, V_{COMPL}, the power MOSFET is kept in the OFF state and the consumption is reduced to I_{DD0} current, as given in Table 6. Supply section. In reaction to the energy delivery interruption, the V_{COMP} voltage increases and, as soon as it exceeds the threshold V_{COMPL} + V_{COMPL_HYS}, the converter starts switching again with consumption level equal to I_{DD1} current. This ON-OFF operation mode, referred to as “burst mode” (see Figure 28), reduces the average frequency, which can fall down even to a few hundreds hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. During burst mode, the drain current limit is reduced to the value I_{Dlim_bm} (given in Table 7. Controller section) in order to avoid audible noise issues.

Figure 28. Load-dependent operating modes: timing diagrams



12 Automatic restart after overload or short-circuit

The overload protection is implemented automatically through the integrated up-down counter. Every cycle, it is incremented or decremented depending on whether the current logic detects the limit condition or not. The limit condition is the peak drain current, I_{Dlim} given in Table 7. Controller section, or the one set by the user through the R_{LIM} resistor, as shown in Figure 12. I_{DLIM} vs. R_{LIM}.

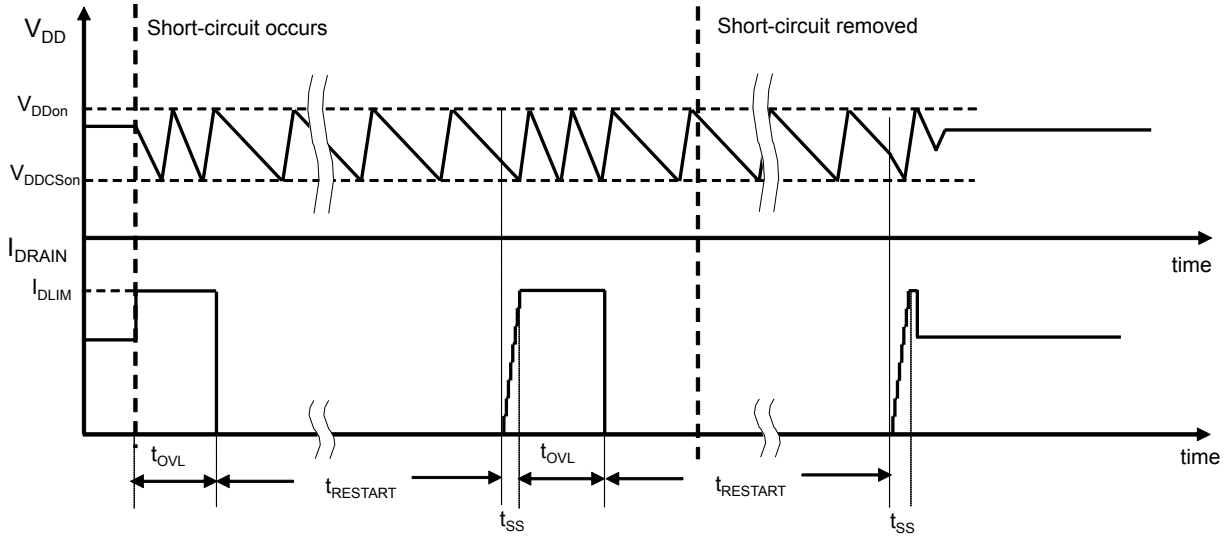
After the reset of the counter, if the peak drain current is continuously equal to the level I_{Dlim}, the counter will be incremented until the fixed time, t_{OVL}, after which the power MOSFET switch ON is disabled. It is activated again, through the soft start, after the $t_{RESTART}$ time, see Figure 29. Timing diagram: OLP sequence and the relevant time values in Table 7.

In case of an overload or short-circuit event, the power MOSFET switching is stopped after a time that depends on the counter and whose maximum can equal t_{OVL}. The protection occurs in the same way until the overload condition is removed, see Figure 29.

This protection ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids IC overheating in case of repeated overload events.

If the overload is removed before the protection tripping, the counter will be decremented cycle by cycle down to zero and the IC will not be stopped.

Figure 29. Timing diagram: OLP sequence



13 Open loop failure protection

If the power supply is built in fly-back topology and the VIPer26 is supplied by an auxiliary winding, as shown in Figure 30. FB pin connection for non-isolated flyback and Figure 31. FB pin connection for isolated fly-back, the converter is protected against feedback loop failure or accidental disconnections of the winding.

Regarding the Figure 30 and Figure 31 schematics for non-isolated flyback and isolated flyback, if R_H is opened or R_L is shorted, the VIPer26 works at its drain current limitation. The output

voltage, V_{OUT}, will increase and so will the auxiliary voltage, V_{AUX}, which is coupled with the output according to the secondary-to-auxiliary turns ratio.

As the auxiliary voltage increases up to the internal V_{DD} active clamp, $V_{DDclamp}$ (value given in Table 7. Controller section) and the clamp current injected on V_{DD} pin exceeds the open loop failure current threshold, I_{DDol} (value given in Table 7), a fault signal is internally generated.

In order to distinguish an actual malfunction from a bad auxiliary winding design, both the above conditions (drain current equal to the drain current limitation and V_{DD} current higher than I_{DDol} through V_{DD} clamp) have to be verified to reveal the fault.

If R_L is opened or R_H is shorted, the output voltage, V_{OUT}, will be clamped to the reference voltage V_{REF_FB} in case of non isolated flyback or to the external T_L voltage reference in case of isolated flyback).

Figure 30. FB pin connection for non-isolated flyback

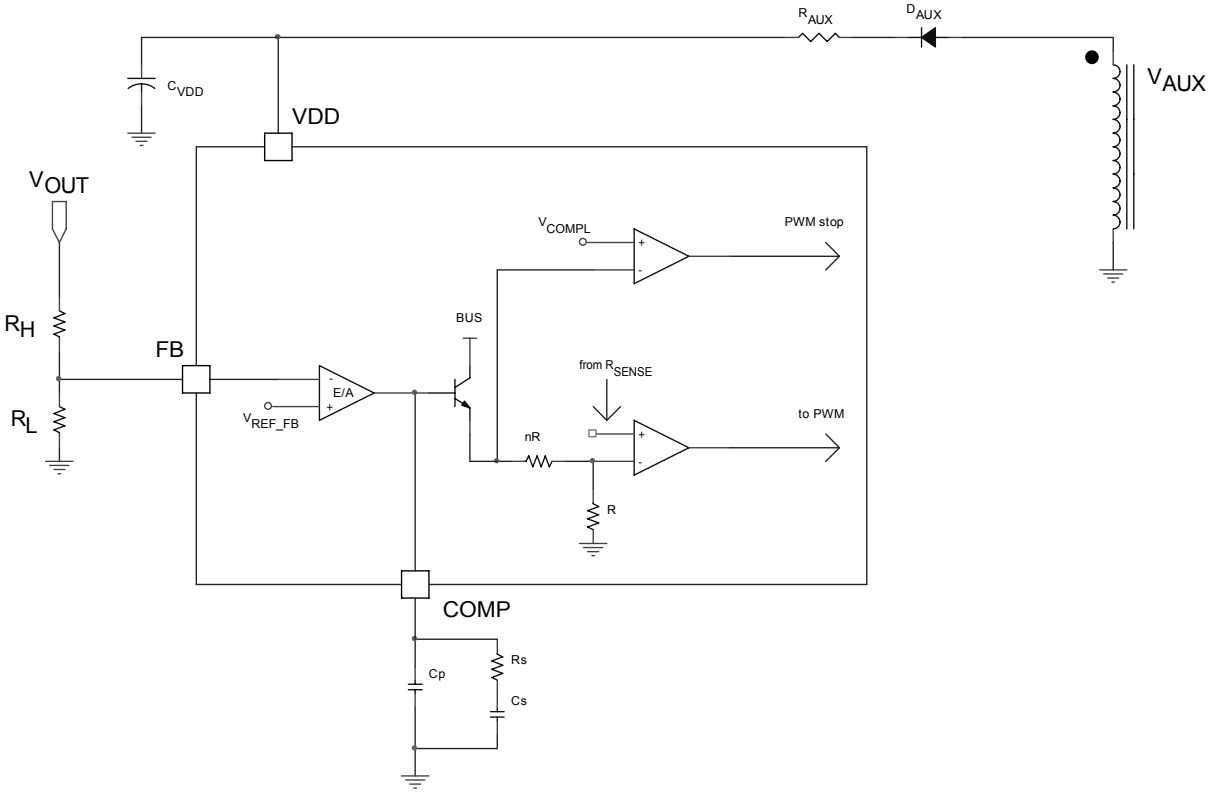
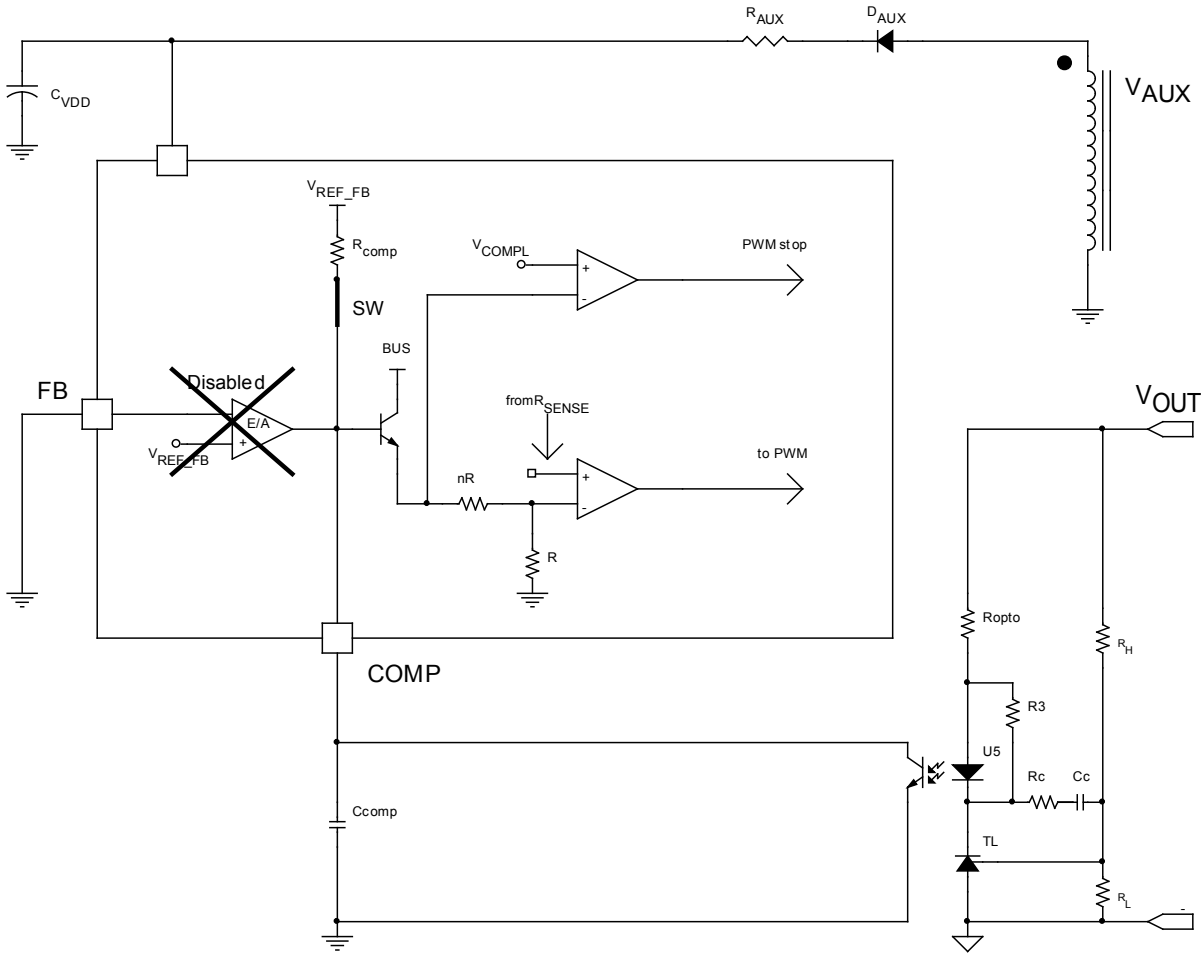


Figure 31. FB pin connection for isolated fly-back



14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

14.1 DIP-7 package information

Figure 32. DIP-7 package outline

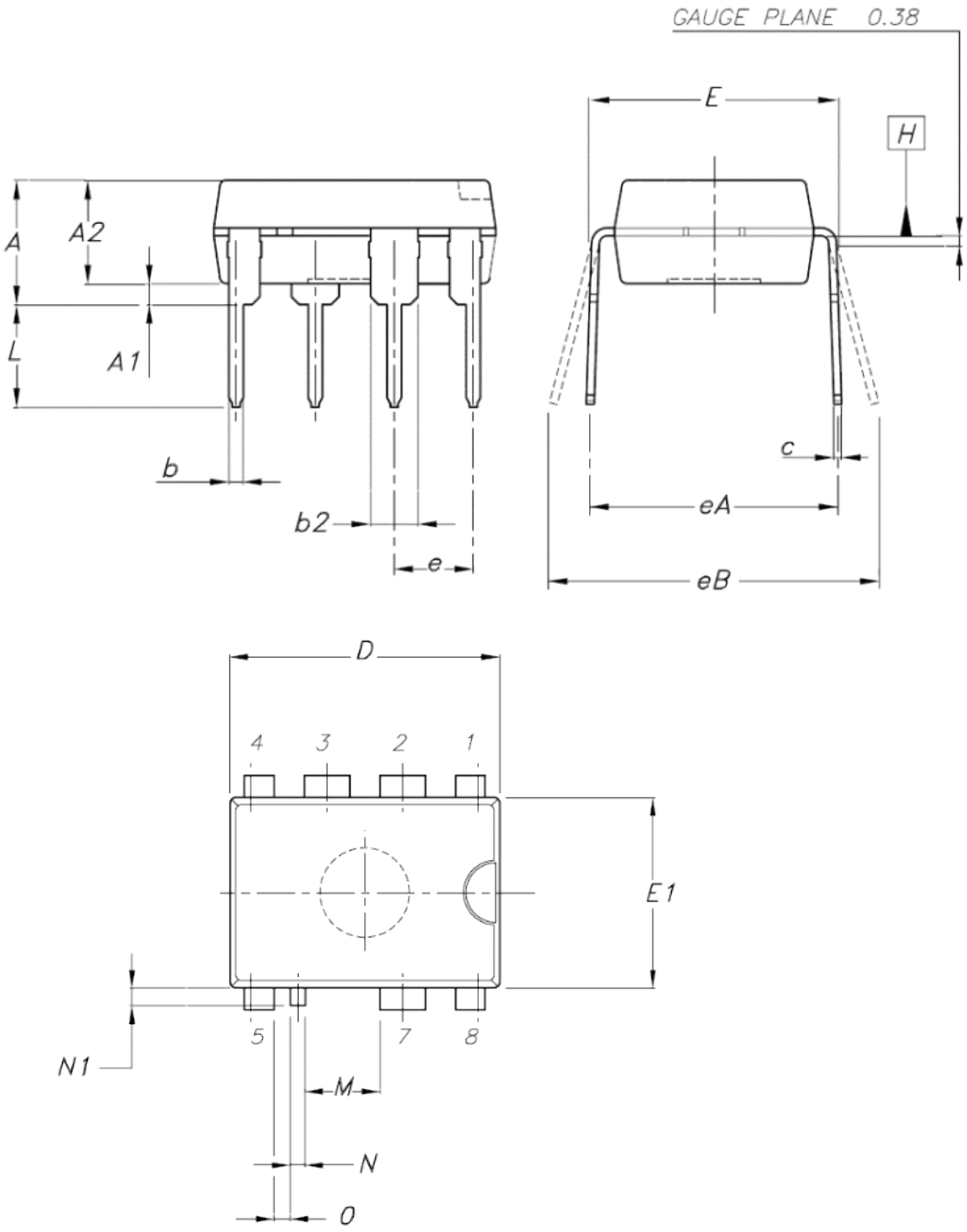


Table 9. **DIP-7 package mechanical data**

Dim.	mm			Notes
	Min.	Typ.	Max.	
A	-	-	5.33	-
A1	0.38	-	-	-
A2	2.92	3.30	4.95	-
b	0.36	0.46	0.56	-
b2	1.14	1.52	1.78	-
c	0.20	0.25	0.36	-
D	9.02	9.27	10.16	-
E	7.62	7.87	8.26	-
E1	6.10	6.35	7.11	-
e	-	2.54	-	-
eA	-	7.62	-	-
eB	-	-	10.92	-
L	2.92	3.30	3.81	-
M	-	2.508		6 - 8
N	0.40	0.50	0.60	-
N1	-	-	0.60	-
O	-	0.548	-	7 - 8

14.2 SO16 narrow package information

Figure 33. **SO16 narrow package outline**

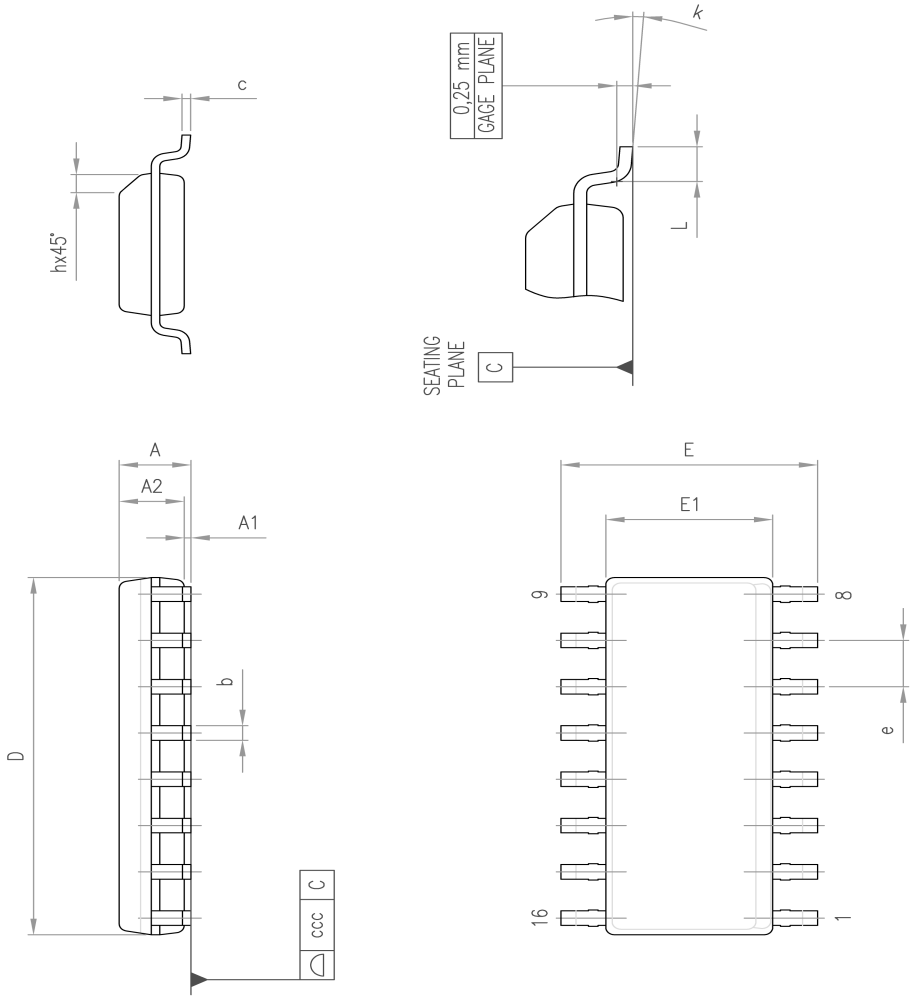


Table 10. **SO16 narrow mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

15 Order code

Table 11. **Order code**

Order code	Package	Packing
VIPER26LN	DIP-7	Tube
VIPER26HN		
VIPER26HD	SO16N	Tube
VIPER26HDTR		Tape and reel
VIPER26LD		Tube
VIPER26LDTR		Tape and reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
26-Aug-2010	1	Initial release.
01-Sep-2010	2	Updated Figure 30 on page 23.
11-Oct-2020	3	Throughout document: - updated document template - general reorganisation of sections - minor text edits On cover page: - updated Features and Description - added Product status link and Product label In Section 1 Pin settings: - updated Table 1. Pin descriptions In Section 2 Electrical and thermal ratings: - updated Table 3. Thermal data - added Figure 2. R_{th} versus area and Table 4. Avalanche characteristics In Table 6. Supply section: - updated V_{DRAIN_START} and I_{DD1} Max. values In Section 3 Typical electrical characteristics: - added Figure 16. SOA SO16N package and Figure 17. SOA DIP7 package In Section 4 Typical circuits: - updated all figures

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