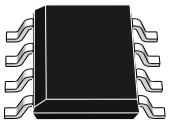
ST3485EB, ST3485EC
ST3485EI, ST3485EIY

Datasheet

3.3 V powered, 15 kV ESD protected, up to 12 Mbps RS-485/ RS-422 transceiver



SO8

Product status link
ST3485EB, ST3485EC, ST3485EI and ST3485EIY

Features

- ESD protection
  - ±15 kV IEC 61000-4-2 air discharge
  - ±8 kV IEC 61000-4-2 contact discharge
- Operate from a single 3.3 V supply - no charge pump required
- Interoperable with 5 V logic
- 1 µA low current shutdown mode max.
- Guaranteed 12 Mbps data rate
- -7 to 12 V common mode input voltage range
- Half duplex versions available
- Industry standard 75176 pinout
- Current limiting and thermal shutdown for driver overload protection
- Guaranteed high receiver output state for floating inputs with no signal present
- Allow up to 64 transceivers on the bus
- Available in SO8 package
- Automotive grade (ST3485EIY)

Description

The ST3485EB, ST3485EC, ST3485EI and ST3485EIY devices are ±15 kV ESD protected, 3.3 V low power transceiver for RS-485 and RS-422 communications. These devices contain one driver and one receiver in half duplex configuration.

These devices transmit and receive at a guaranteed data rate of at least 12 Mbps.

All transmitter outputs and receiver inputs are protected to ±15 kV IEC 61000-4-2 air discharge.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high impedance state.

1 Pin configuration

Figure 1. Pin connections

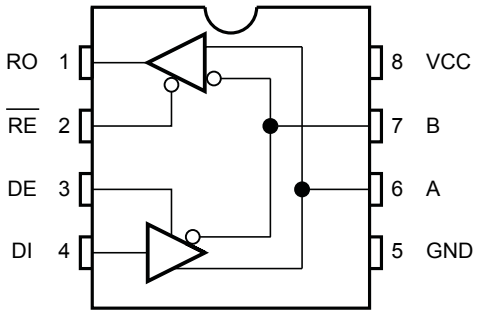


Table 1. Pin description

Pin n°	Symbol	Name and function
1	RO	Receiver output. If A > B by 200 mV, RO will be high; if A < B by 200 mV, RO will be low.
2	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If $\overline{RE}$ is high and DE is low, the device will enter a low power shutdown mode.
3	DE	Driver output enable. The driver outputs are enabled by bringing DE high. They are high impedance when DE is low. If $\overline{RE}$ is high DE is low, the device will enter a low-power shutdown mode. If the driver outputs are enabled, the part functions as line driver, while they are high impedance, it functions as line receivers if $\overline{RE}$ is low.
4	DI	Driver input. A low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low.
5	GND	Ground.
6	A	Non-inverting receiver input and non-inverting driver output.
7	B	Inverting receiver input and inverting driver output.
8	VCC	Supply voltage: V_{CC} = 3 V to 3.6 V.

2 Truth tables

Table 2. Truth table (driver)

Inputs			Outputs		Mode
$\overline{RE}$	DE	DI	B	A	
X	H	H	L	H	Normal
		L	H	L	
L	L	X	Z	Z	
H					Shutdown

Note: X = “don’t care”; Z = high impedance

Table 3. Truth table (receiver)

Inputs			Output	Mode
$\overline{RE}$	DE	A-B	RO	
L	L	≥ 0.2 V	H	Normal
		≤ -0.2 V	L	
		Inputs open	H	
H		X	Z	Shutdown

Note: X = “do not care”; Z = high impedance

3 Maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	7	V
V_I	Control input voltage ($\overline{RE}$, DE)	-0.3 to 7	V
V_{DI}	Driver input voltage (DI)	-0.3 to 7	V
V_{DO}	Driver output voltage (A, B)	±14	V
V_{RI}	Receiver input voltage (A, B)	±14	V
V_{RO}	Receiver output voltage (RO)	-0.3 to (V_{CC} + 0.3)	V
R_{thj-a}	Junction-ambient	125	°C/W
ESD	HBM: human body model for the line inputs (A and B) (1)	12	kV
	HBM: human body model for the logic inputs (DI, DE, $\overline{RE}$) (1)	4	
	HBM: human body model for all other pins (1)	2	
	CDM: charged device model (2)	1.5	

1. *Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.*
2. *Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.*

4 Electrical characteristics

Table 5. Electrical characteristics (V_{CC} = 3 V to 3.6 V, T_A = 0 to 70 °C for ST3485ECDR, T_A = -40 to 85 °C for the ST3485EBDR, T_A = -40 to 125 °C for the ST3485EIDT and ST3485EIYDT, unless otherwise specified. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{SUPPLY}	V_{CC} power supply current	No load, DI = 0 V or V_{CC}	DE = V_{CC}, $\overline{RE}$ = 0 V or V_{CC}	—	1.3	2.2	mA
			DE = 0 V, $\overline{RE}$ = 0 V		1.2	1.9	
I_{SHDN}	Shutdown supply current	DE = 0 V, $\overline{RE}$ = V_{CC}, DI = 0 V or V_{CC}			0.002	1	µA

Table 6. Logic input electrical characteristics (V_{CC} = 3 V to 3.6 V, T_A = 0 to 70 °C for ST3485ECDR, T_A = -40 to 85 °C for the ST3485EBDR, T_A = -40 to 125 °C for the ST3485EIDT and ST3485EIYDT, unless otherwise specified. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{IL}	Input logic threshold low	DE, DI, $\overline{RE}$			1.3	0.8	V
V_{IH}	Input logic threshold high	DE, DI, $\overline{RE}$		2			
I_{IN1}	Logic input current	DE, DI, $\overline{RE}$				±2.0	µA
I_{IN2}	Input current (A, B)	DE = 0 V, V_{CC}= 0 or 3.6 V	V_{IN} = 12 V			1	mA
			V_{IN} = -7 V			-0.8	

Table 7. Transmitter electrical characteristics (V_{CC} = 3 V to 3.6 V, T_A = 0 to 70 °C for ST3485ECDR, T_A = -40 to 85 °C for the ST3485EBDR, T_A = -40 to 125 °C for the ST3485EIDT and ST3485EIYDT, unless otherwise specified. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential drive output	R_L= 100 Ω (RS-422) Figure 2. Driver and V_{OC} test load	2	—		V
		R_L= 54 Ω (RS-485) Figure 2. Driver and V_{OC} test load	1.5			
		R_L= 60 Ω (RS-485)Figure 3. Driver V_{OD} with varying common mode voltage test load	1.5			
ΔV_{OD}	Change in magnitude of driver differential output voltage for complementary output states (1)	R_L= 54 Ω or 100 ΩFigure 2. Driver and V_{OC} test load			0.2	
V_{OC}	Driver common mode output voltage	R_L= 54 Ω or 100 ΩFigure 2. Driver and V_{OC} test load			3	
ΔV_{OC}	Change in magnitude of driver common mode output voltage(1)	R_L= 54 Ω or 100 ΩFigure 2. Driver and V_{OC} test load			0.2	
I_{OSD}	Driver short-circuit output current				±250	mA

1. *ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.*

Table 8. Receiver electrical characteristics (V_{CC} = 3 V to 3.6 V, T_A = 0 to 70 °C for ST3485ECDR, T_A = -40 to 85 °C for ST3485EBDR, T_A = -40 to 125 °C for ST3485EIDT and ST3485EIYDT, unless otherwise specified. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{TH}	Receiver differential threshold voltage	V_{CM} = -7 V to 12 V, DE = 0	-0.2		0.2	V
ΔV_{TH}	Receiver input hysteresis	V_{CM} = 0 V		70		mV
V_{OH}	Receiver output high voltage	I_{OUT} = -4 mA, V_{ID} = 200 mV (Figure 4. Receiver V_{OH} and V_{OL} test circuit)	2			V
V_{OL}	Receiver output low voltage	I_{OUT} = 4 mA, V_{ID} = -200 mV (Figure 4. Receiver V_{OH} and V_{OL} test circuit)			0.4	
I_{OZR}	3-state (high impedance) output current at receiver	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}			±1	µA
R_{RIN}	Receiver input resistance	V_{CM} = -7 V to 12 V	24			kΩ
I_{OSR}	Receiver short-circuit current	V_{RO} = 0 V to V_{CC}	7		60	mA

Table 9. Driver switching characteristics (V_{CC} = 3 V to 3.6 V, T_A = 0 to 70 °C for the ST3485ECDR, T_A = -40 to 85 °C for the ST3485EBDR, T_A = -40 to 125 °C for the ST3485EIDT and ST3485EIYDT, unless otherwise specified. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
D_R	Maximum data rate		12	15		Mbps
t_{DD}	Differential output delay	R_L= 60 Ω, C_L = 15 pF Figure 5. Drive differential output delay transition time test circuit Figure 6. Drive differential output delay transition time waveform		18	30	ns
t_{TD}	Differential output transition time	R_L= 60 Ω, C_L = 15 pF Figure 5. Drive differential output delay transition time test circuit Figure 6. Drive differential output delay transition time waveform		12	20	
t_{PLH} t_{PHL}	Propagation delay	R_L= 27 Ω, C_L = 15 pF Figure 9. Drive propagation time test circuit Figure 10. Drive propagation time waveform		18	30	
t_{PDS}	$\lvert t_{PLH} - t_{PHL} \rvert$ driver propagation delay skew (1)	R_L= 27 Ω, C_L = 15 pF Figure 9. Drive propagation time test circuit Figure 10. Drive propagation time waveform		2	5	
t_{PZL}	Output enable time	R_L= 110 Ω Figure 11. Drive enable and disable times test circuit (pull-up configuration) Figure 12. Drive enable and disable times waveforms (pull-up configuration)		19	35	
t_{PZH}	Output enable time	R_L= 110 Ω Figure 7. Drive enable and disable times test circuit (pull-down configuration) Figure 8. Drive enable and disable times waveforms (pull-down configuration)		30	50	
t_{PHZ}	Output disable time	R_L= 110 Ω Figure 7. Drive enable and disable times test circuit (pull-down configuration) Figure 8. Drive enable and disable times waveforms (pull-down configuration)		19	35	
t_{PLZ}	Output disable time	R_L= 110 Ω Figure 11. Drive enable and disable times test circuit (pull-up configuration) Figure 12. Drive enable and disable times waveforms (pull-up configuration)		30	50	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SKEW}	Differential output delay skew			1	3	ns
t_{PSH}	Driver enable from shutdown to output high	R_L = 110 Ω Figure 7. Drive enable and disable times test circuit (pull-down configuration) Figure 8. Drive enable and disable times waveforms (pull-down configuration)		30	50	
t_{PSL}	Driver enable from shutdown to output low	R_L = 110 Ω Figure 11. Drive enable and disable times test circuit (pull-up configuration) Figure 12. Drive enable and disable times waveforms (pull-up configuration)		19	35	

1. *Measured on $|t_{PLH}(A)-t_{PHL}(A)|$ and $|t_{PLH}(B)-t_{PHL}(B)|$.*

Table 10. Receiver switching characteristics (V_{CC} = 3 V to 3.6 V, T_A = 0 to 70 °C for ST3485ECDR, T_A = -40 to 85 °C for ST3485EBDR, T_A = -40 to 125 °C for ST3485EIDT and ST3485EIYDT, unless otherwise specified. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{RPLH}, t_{RPHL}	Propagation delay	V_{ID} = 0 V to 3 V, C_L = 15 pF (Figure 13. Receiver propagation delay time test circuit and Figure 14. Receiver propagation delay time waveforms)	—	30	50	ns
t_{RPDS}	$\|t_{RPLH} - t_{RPHL}\|$ receiver propagation delay skew	V_{ID} = 0 V to 3 V, C_L = 15 pF (Figure 13. Receiver propagation delay time test circuit and Figure 14. Receiver propagation delay time waveforms)		1	3	
t_{PRZL}	Receiver output enable time to low level	C_L = 15 pF (Figure 15. Receiver enable and disable times test circuit and Figure 17. Receiver enable and disable times waveform (test 2))		10	20	
t_{PRZH}	Receiver output enable time to high level	C_L = 15 pF (Figure 15. Receiver enable and disable times test circuit and Figure 16. Receiver enable and disable times waveform (test 1))		10	20	
t_{PRHZ}	Receiver output disable time from high level	C_L = 15 pF (Figure 15. Receiver enable and disable times test circuit and Figure 18. Receiver enable and disable times waveform (test 3))		10	20	
t_{PRLZ}	Receiver output disable time from low level	C_L = 15 pF (Figure 15. Receiver enable and disable times test circuit and Figure 19. Receiver enable and disable times waveform (test 4))		10	20	
t_{PRSH}	Receiver output enable time from shutdown to high level	C_L = 15 pF (Figure 15. Receiver enable and disable times test circuit and Figure 16. Receiver enable and disable times waveform (test 1))		10	20	
t_{PRSL}	Receiver output enable time from shutdown to low level	C_L = 15 pF (Figure 15. Receiver enable and disable times test circuit and Figure 17. Receiver enable and disable times waveform (test 2))		20	40	µs

Notes:

1. ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.
2. Measured on $|t_{PLH}(A) - t_{PHL}(A)|$ and $|t_{PLH}(B) - t_{PHL}(B)|$.
3. The transceivers are put into shutdown by bring $\overline{RE}$ high and DE low. If the input are in state for less than 80 ns, the part are guaranteed not to enter shutdown. If the inputs are in this state for at least 300 ns, the parts are guaranteed to have entered shutdown.

5 Test circuits and typical characteristics

Figure 2. Driver and V_{OC} test load

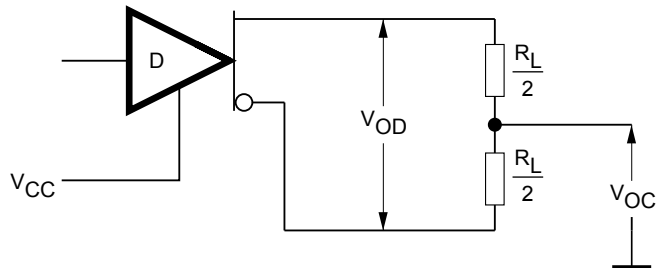


Figure 3. Driver V_{OD} with varying common mode voltage test load

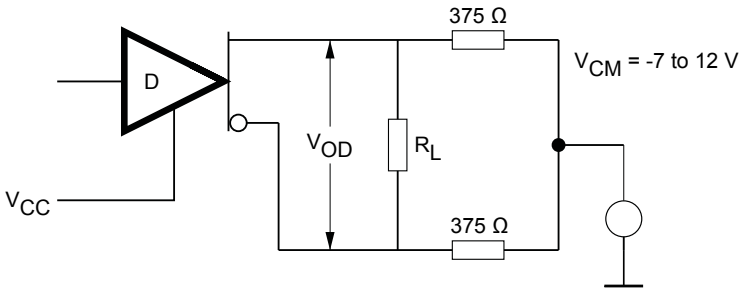


Figure 4. Receiver V_{OH} and V_{OL} test circuit

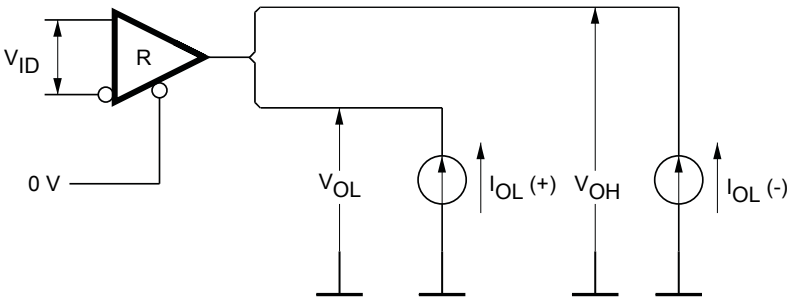
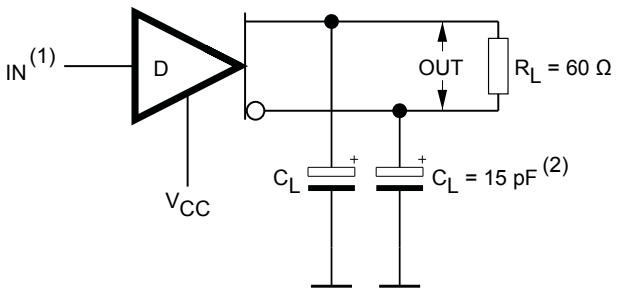


Figure 5. Drive differential output delay transition time test circuit



1. The input pulse is supplied by a generator with the following characteristics: PRR = 250 kHz, 50 % duty cycle, tr ≤ 6.0 ns, Z_O = 50 Ω.
2. C_L includes probe and stray capacitance

Figure 6. Drive differential output delay transition time waveform

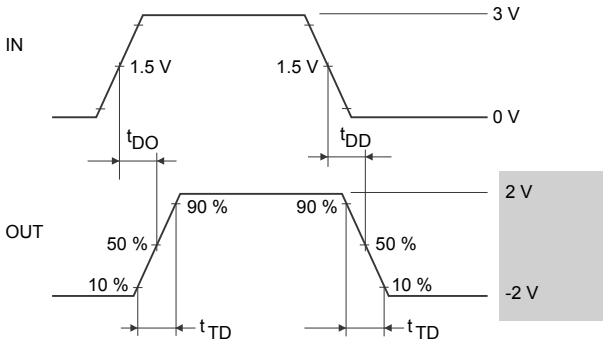
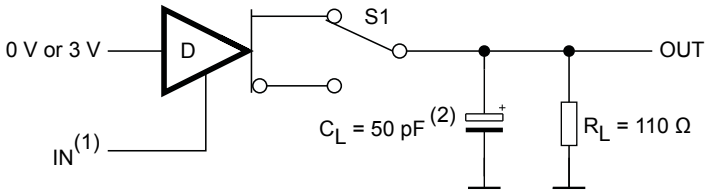
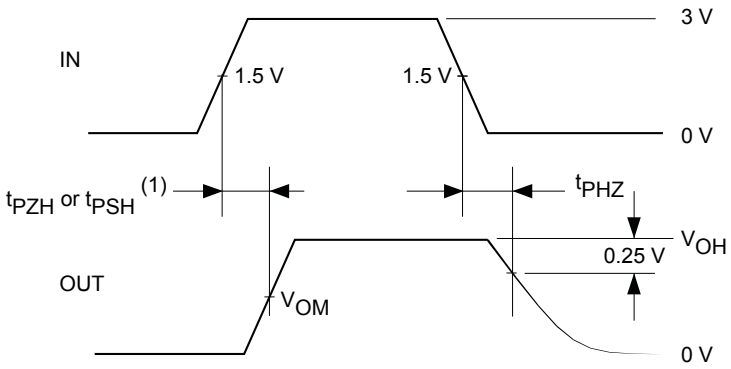


Figure 7. Drive enable and disable times test circuit (pull-down configuration)



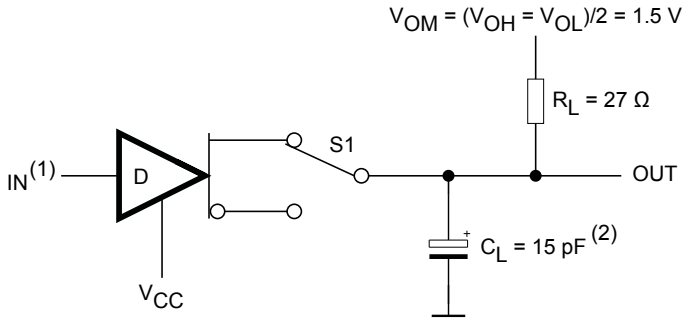
1. The input pulse is supplied by a generator with the following characteristics: PRR = 250 kHz, 50 % duty cycle, tr ≤ 6.0 ns.
2. C_L includes probe and stray capacitance

Figure 8. Drive enable and disable times waveforms (pull-down configuration)



1. t_{PZH} is valid if the driver is initially disabled ($\overline{RE}$ is high), t_{PSH} is valid if the driver is initially in shutdown mode (RE is low).

Figure 9. Drive propagation time test circuit



1. The input pulse is supplied by a generator with the following characteristics: PRR = 250 kHz, 50 % duty cycle, tr ≤ 6.0 ns.
2. C_L includes probe and stray capacitance

Figure 10. Drive propagation time waveform

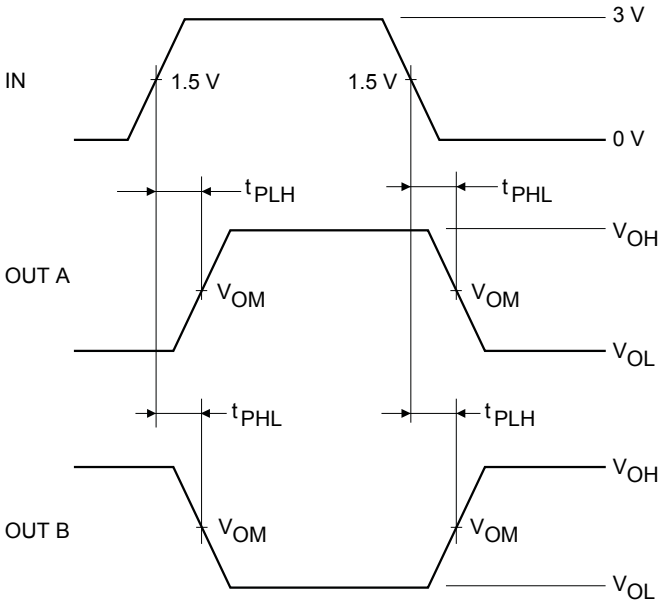
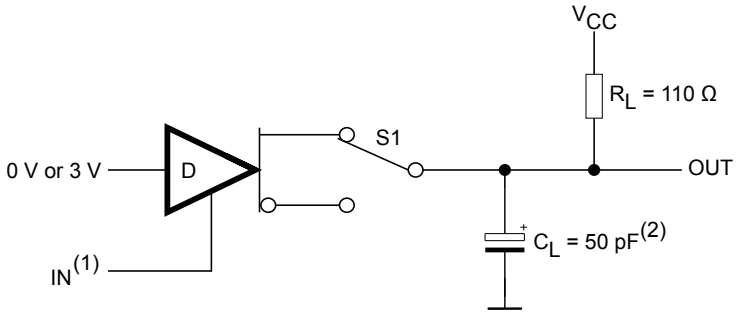
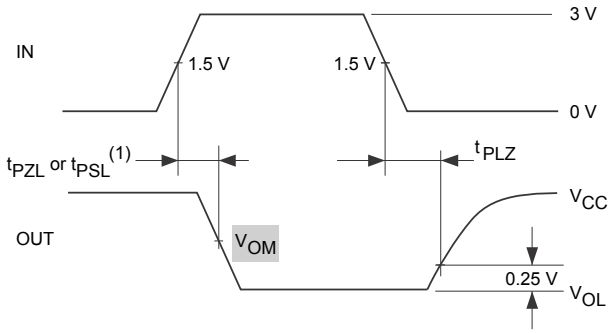


Figure 11. Drive enable and disable times test circuit (pull-up configuration)



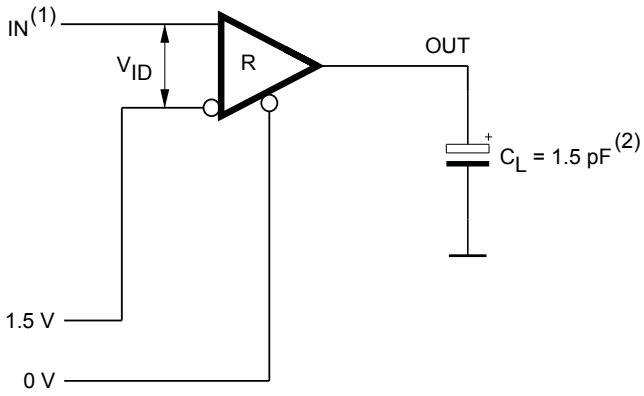
1. The input pulse is supplied by a generator with the following characteristics: PRR = 250 kHz, 50 % duty cycle, tr ≤ 6.0 ns.
2. C_L includes probe and stray capacitance

Figure 12. Drive enable and disable times waveforms (pull-up configuration)



1. t_{PZL} is valid if the driver is initially disabled ($\overline{RE}$ is high), t_{PSL} is valid if the driver is initially in shutdown mode (RE is low).

Figure 13. Receiver propagation delay time test circuit



1. The input pulse is supplied by a generator with the following characteristics: PRR = 250 kHz, 50 % duty cycle, tr ≤ 6.0 ns.
2. C_L includes probe and stray capacitance

Figure 14. Receiver propagation delay time waveforms

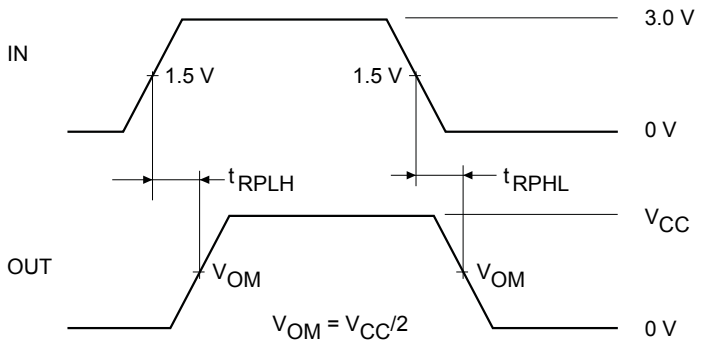
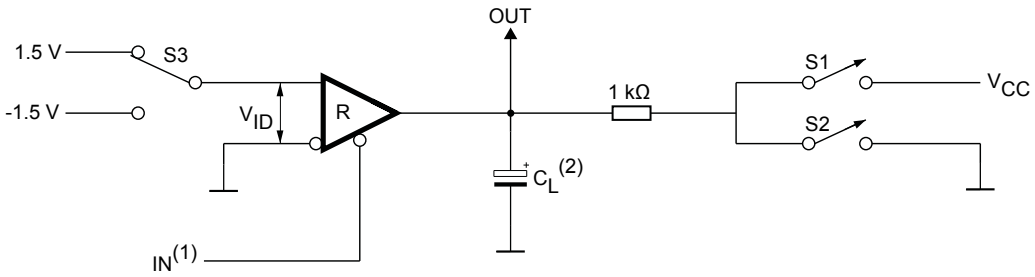


Figure 15. Receiver enable and disable times test circuit



1. The input pulse is supplied by a generator with the following characteristics: PRR = 250 kHz, 50 % duty cycle, tr ≤ 6.0 ns.
2. C_L includes probe and stray capacitance

Figure 16. Receiver enable and disable times waveform (test 1)

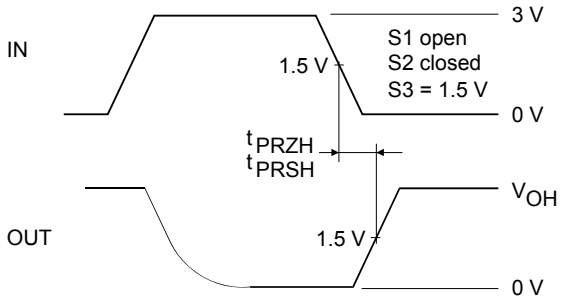


Figure 17. **Receiver enable and disable times waveform (test 2)**

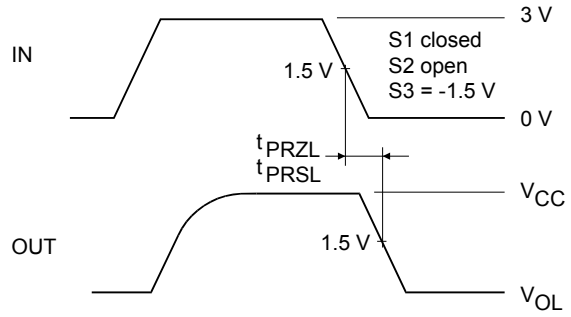


Figure 18. **Receiver enable and disable times waveform (test 3)**

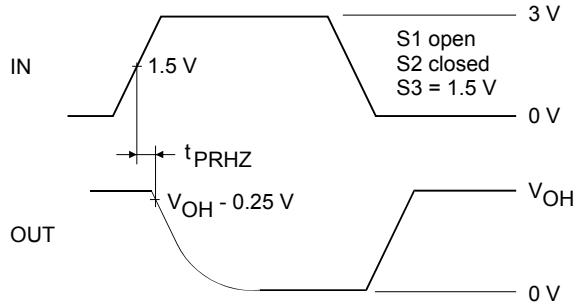


Figure 19. **Receiver enable and disable times waveform (test 4)**

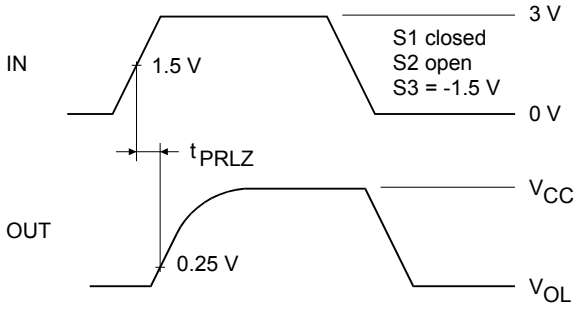


Figure 20. Receiver output current vs. output low voltage

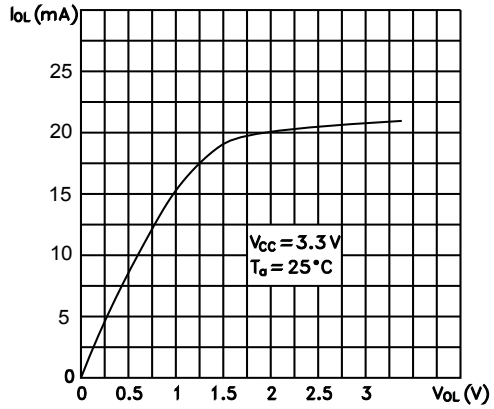


Figure 21. Receiver output current vs. output high voltage

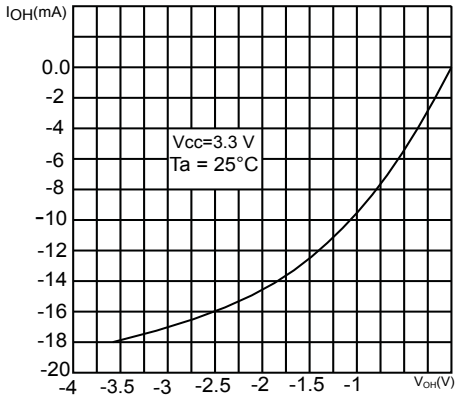


Figure 22. Low level driver output capability

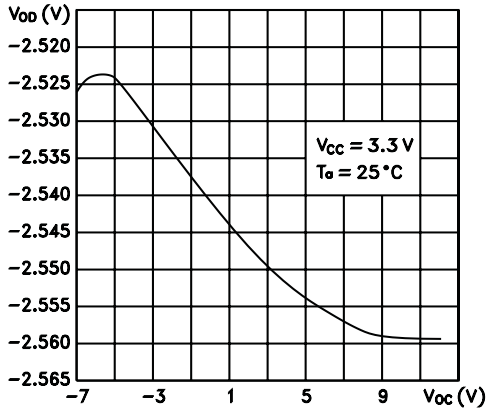


Figure 23. High level driver output capability

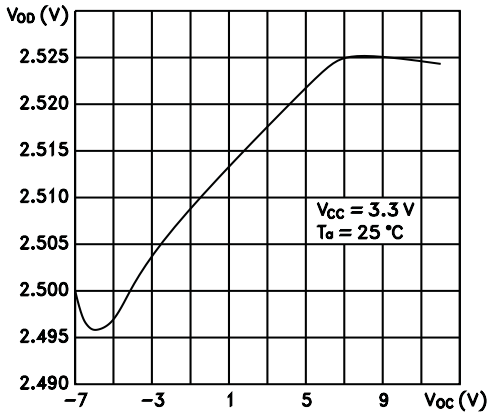


Figure 24. Receiver input characteristics

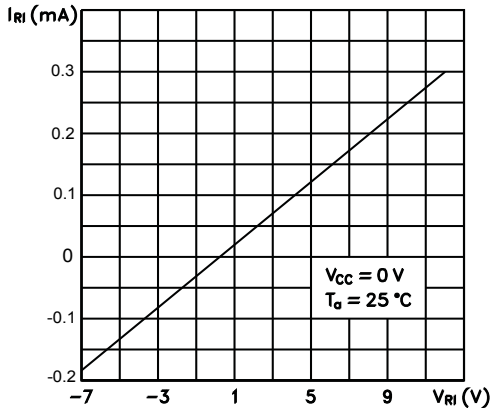


Figure 25. Driver short-circuit current (test 1)

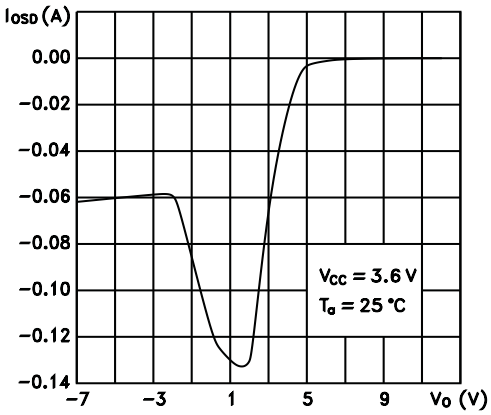
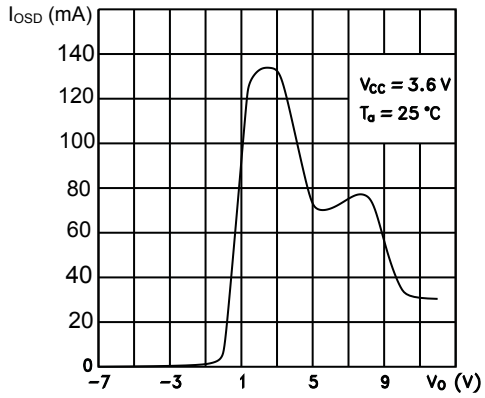


Figure 26. **Driver short-circuit current (test 2)**



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO8 package information

Figure 27. **SO8 package outline**

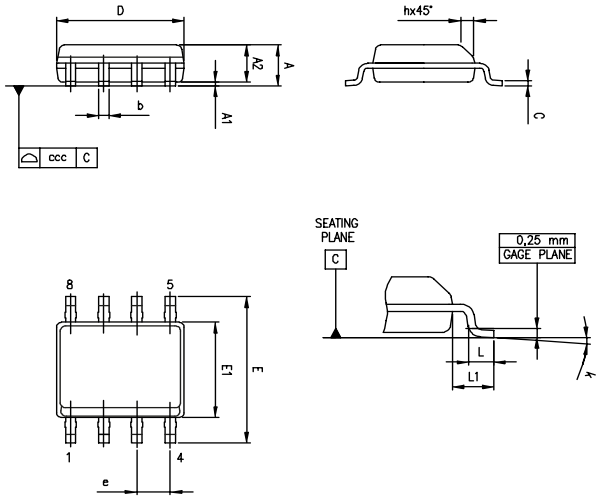
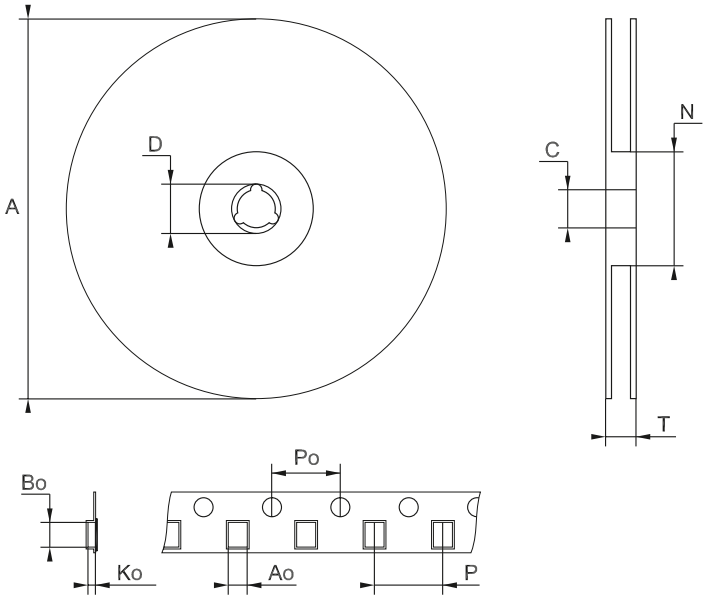


Table 11. **SO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.2 SO8 packing information

Figure 28. **SO8 tape and reel outline**



1. Drawing not to scale

Table 12. **SO8 tape and reel mechanical data**

Symbol	Dimensions					
	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		—	330		—	12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

7 Ordering information

Table 13. Order codes

Order code	Temperature range	Package	Packing	Marking
ST3485ECDR	0 to 70 °C	SO8	2500 parts per reel	3485EC
ST3485EBDR	-40 to 85 °C			3485EB
ST3485EIDT	-40 to 125 °C			3485EI
ST3485EIYDT(1)	-40 to 125 °C (automotive grade)			3485EIY

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.*

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
20-Jun-2005	2	Mistake on table 12 $t_{ZL(SHDN)}$ ms ==> µs.
30-Aug-2005	3	Remove (TRUE) on title, description has been updated in cover page. The V_{TH} and DV_{TH} values are changed in table 10.
07-Apr-2006	4	Order codes updated.
12-Nov-2007	5	Added Table 1.
18-Dec-2013	6	Updated Features (added SO-8 package, replaced human body model by ±15 kV IEC 61000-4-2 air discharge and IEC 1000-4-2 by IEC 61000-4-2). Updated Description (renamed device to ST3485EB/EC, replaced human body model by ±15 kV IEC 61000-4-2 air discharge). Removed ST3485ECN device from Table 1. Updated title of Table 6, cross-references, replaced human body model (HBM) by ±15 kV IEC 61000-4-2 air discharge and IEC 1000-4-2 by IEC 61000-4-2. Added notes below Table 9. Updated Table 10 to Table 12 (updated data, cross-references). Updated Figure 5 to Figure 16 (updated data, added notes below figures and highlighted some parts of Figure 6 and Figure 12). Removed DIP-8 package from Section 6: "Package information" and whole document. Reformatted Section 6: "Package information" (added Figure 27, Figure 28, Table 13 and Table 14, reversed order of figures and table). Minor corrections throughout document.
12-Jun-2015	7	Added part number ST3485EIY Added order code ST3485EIYDT and pointed out in Features it is automotive grade. Table 7 and Table 9 through to Table 12: replaced T_A = -40 to 85 °C with T_A = 0 to 70 °C (ST3485ECDR), T_A = -40 to 85 °C (ST3485EBDR), and T_A = -40 to 125 °C (ST3485EIYDT). Updated titles of figures 7, 8, 11, 12, 16, 17, 18, 19, 25, and 26
15-Mar-2016	8	Table 5: added ESD information Removed "Table 6: ESD performance: transmitter outputs, receiver inputs (A, B)". Added Section 7: "Ordering information"
02-Aug-2016	9	Added new part number ST3485EI Table 1: "Device summary": added information for new part number ST3485EI. Removed " ***Note*** " icons throughout datasheet Section 4: "Electrical characteristics": updated TA information Section 5: "Test circuits and typical characteristics": removed overline bar concerning "RE is low" in note 1 of figures 8 and 12. Table 14: "Order codes": added ST3485EIDT and updated footnote 1 (ST3485EIYDT now qualified).
25-Aug-2016	10	Table 14: "Order codes": updated order codes ST3485EBDR and ST3485ECDR.
26-Oct-2017	11	Updated Figure 20: "Receiver output current vs. output low voltage", Figure 21: "Receiver output current vs. output high voltage", Figure 24: "Receiver input characteristics" and Figure 26: "Driver short-circuit current (test 2)".
05-Mar-2021	12	Updated Table 4. Absolute maximum ratings.

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单击下面可查看定价，库存，交付和生命周期等信息

>>STMicro(意法半导体)