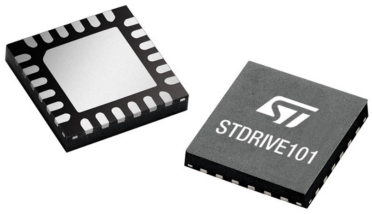
STDRIVE101

Datasheet

Triple half-bridge gate driver



VFQFPN 4 x 4 x 1.0 mm
24 leads pitch 0.5 mm

Features

- Operating voltage from 5.5 to 75 V
- 600 mA sink/source current capability
- 3.3 V and 5 V control logic
- Two input strategies:
  - ENx/INx with adjustable deadtime generation
  - INHx/INLx with interlocking
- Matched propagation delay for all channels
- Very short propagation delay: 40 ns
- Integrated bootstrap diodes
- 12 V LDO linear regulator (50 mA max.)
- Embedded V_{DS} monitor for each external MOSFET
- Overcurrent comparator
- UVLO and thermal shutdown protection
- Standby mode for low current consumption operation

Application

- Home automation and appliances
- e-bikes
- Power tools
- Fans and pumps
- Industrial automation
- Textile machines
- Gaming and consoles

Product status link

STDRIVE101

Product label

SUSTAINABLE TECHNOLOGY

Description

The STDRIVE101 is a low voltage gate driver suitable for driving three-phase brushless motors.

It is a single-chip with three half-bridge gate drivers for N-channel power MOSFETs. Each driver has a current capability of 600 mA (sink/source). It integrates a low drop linear regulator generating the supply voltage for both low-side and high-side gate drivers through a bootstrap circuitry.

The device provides Under Voltage Lock Out (UVLO) on both the low-side and high-side sections, preventing the power switches from operating in low efficiency or dangerous conditions.

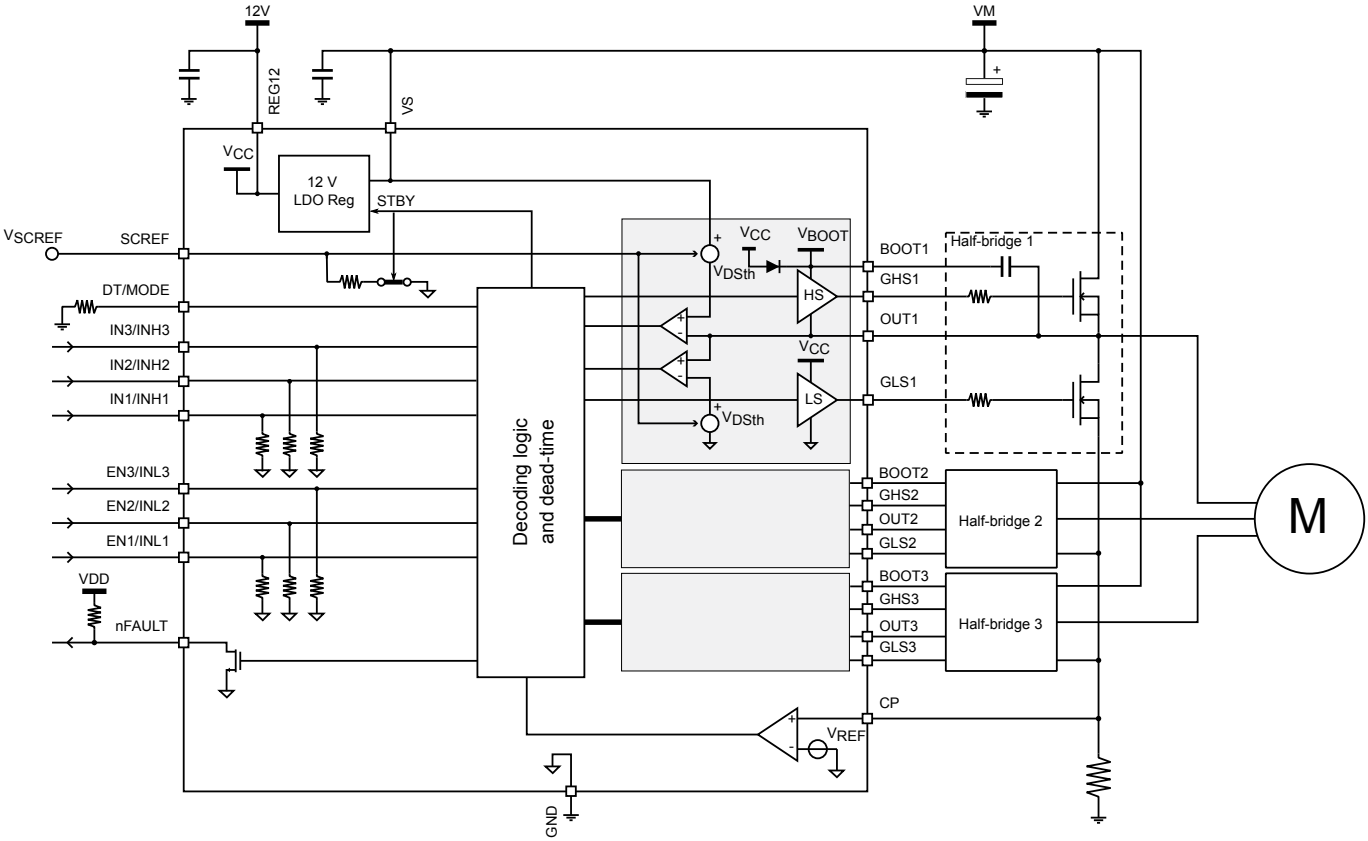
The control logic integrated into the STDRIVE101 allows two input strategies (high-side and low-side or enable and PWM driving signals). The driving method is selected according to DT/MODE pin. In both cases, prevention from cross conduction is ensured by interlocking or internally generated deadtime.

The STDRIVE101 also features a V_{DS} monitoring protection for each external MOSFET, thermal shutdown and can be put in the standby mode to reduce the power consumption.

The device is available in a VFQFPN 4x4 24 leads package option.

1 Block diagram

Figure 1. **STDRIVE101 block diagram**



2 Electrical data

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test Condition	Value	Unit
V_S	Supply voltage		-0.3 to 78	V
dV_S/dt	Supply voltage slew rate		± 10	V/µs
V_{REG12}	Gate driving supply voltage	REG12 shorted to VS	-0.3 to 20	V
V_{OUTx}	OUTx pin voltage		-2 to V_S + 2	V
V_{BOOTx}	Bootstrap pin voltage		-0.3 to 98	V
V_{BOx}	High-side driver supply voltage	V_{BOOTx} - V_{OUTx}	-0.3 to 20	V
V_{GHSx}	High-side gates voltage		V_{OUT}-0.3 to V_{BOOT}+0.3	V
V_{GLSx}	Low-side gates voltage		-0.3 to V_{REG12}+0.3	V
dV_{OUT}/dt	Output slew rate		± 10	V/ns
V_{IN}	Logic input voltage		-0.3 to 5.5	V
V_{CP}	Overcurrent comparator inputs voltage		-2 to 5.5	V
$V_{DT/MODE}$	Deadtime input voltage		-0.3 to 3.6	V
V_{SCREF}	V_{DS} monitoring protection reference voltage		-0.3 to 3.6	V
V_{FAULT}	nFAULT output voltage		-0.3 to 5.5	V
I_{FAULT}	nFAULT output sink current		Up to 8	mA
T_{stg}	Storage temperature		-55 to 150	°C
T_J	Junction temperature		-40 to 150	°C

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		5.5 (1)		75	V
V_{REG12}	12 V linear regulator output and gate driving supply voltage	$V_S \geq 15$ V		12		V
		VS shorted to REG12 (2)	5.5 (1)		15	V
V_{BOOTx}	Bootstrap pin voltage				89	V
I_{REG12}	12 V linear regulator total current consumption (3)	Internal (gate drivers) and external consumption			50	mA
C_{REG12}	12 V linear regulator output capacitance		4.7			µF
R_{DT}	Deadtime resistor	ENx/INx mode	50		250	kΩ
		INHx/INLx mode	Short to ground			
V_{IN}	Logic input voltage		0		5 (4)	V
V_{CP}	Overcurrent comparator input voltage		-1		1	V
V_{SCREF}	V_{DS} monitoring protection reference voltage (5)	Protection enabled	0.2		2.5	V
		Protection disabled	2.9		3.3	V
V_{FAULT}	nFAULT output voltage		0		5	V
T_{amb}	Operative ambient temperature		-40		125 (6)	°C

1. *Actual operative range can be limited by UVLO protections*
2. *Refer to Figure 12*
3. *Actual linear regulator current consumption can be limited by power dissipation*
4. *All digital inputs are 3.3 V TTL/CMOS thresholds compliant and 5 V tolerant. They can be biased within the respective AMR whatever the supply condition of the device (supplied, floating or shorted to ground) without causing damage to the device.*
5. *SCREF pin structure does not allow a bias without VS supply voltage*
6. *Actual operative range is limited by thermal shutdown*

Important:
It is mandatory to use a VS voltage equal or greater than power stage voltage (VM in Figure 1). If not, the device is damaged.

2.3 Thermal data

Table 3. **Thermal data**

Symbol	Parameter	Conditions	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	Natural convection, according to JESD51-2a (1)	94.5	°C/W
$R_{thJCtop}$	Junction-to-case thermal resistance (top side)	Cold plate on top, according to JESD51-12 (1)	28.4	°C/W
$R_{thJCbot}$	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12(1)	1.47	°C/W
R_{thJB}	Junction-to-board thermal resistance	According to JESD51-8(1)	14.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	According to JESD51-2a(1)	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	According to JESD51-2a(1)	14.2	°C/W

1. *Simulated on a 21.2x21.2 mm board, 2s2p 1 Oz copper and four 300 µm vias below exposed pad.*

2.4 Electrical sensitivity characteristics

Table 4. **ESD protection ratings**

Symbol	Parameter	Test Condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2017	H2	2	kV
CDM	Charge Device Model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2B	750	V

3 Electrical characteristics

Testing conditions: V_S = 60 V unless otherwise specified.

Typical values are tested at T_J = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply and standby mode						
$V_{REG12(On)}$	V_{REG12} UVLO turn-on threshold	V_{REG12} rising			5.5	V
$V_{REG12(Hyst)}$	V_{REG12} UVLO hysteresis	V_{REG12} falling	100			mV
$V_{BO(On)}$	V_{BOOT} - V_{OUT} UVLO turn-on threshold	V_{BOOT} rising			5	V
$V_{BO(Hyst)}$	V_{BOOT} - V_{OUT} UVLO hysteresis	V_{BOOT} falling	100			
I_{BOOT}	V_{BOOT} - V_{OUT} quiescent current	T_J = 25 °C	85	155	225	µA
I_{qu}	Overall quiescent consumption from VS	V_S = 60 V All gate driver outputs low SCREF = 3.3 V		1700	2800	µA
I_{STBY}	Overall standby consumption from VS	V_S = 60 V, Device in standby mode T_J = 25 °C		10	16	µA
t_{STBY}	Standby time	See Figure 15 and Figure 16	300		1200	µs
t_{WAKE}	Wake-up time	V_S = V_{REG12} = 12 V Figure 15 and Figure 16			50	µs
12 V Linear regulator						
V_{REG12}	12 V linear regulator output and gate driving supply voltage	V_S = 60 V I_{REG12} = 50 mA All gate driver outputs low	11.4	12.2	12.75	V
$I_{REG12lim}$	12 V linear regulator current limit	REG12 shorted to ground	55			mA
Gate drivers						
I_{SI}	Maximum sink current capabilities	V_S = V_{REG12} = 12 V V_{BOOTx}-V_{OUTx} = 12 V T_J = 25 °C	400	600		mA
		V_S = V_{REG12} = 12 V V_{BOOTx}-V_{OUTx} = 12 V Full temperature range	300			mA
		V_S = V_{REG12} = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V T_J = 25 °C	350			mA

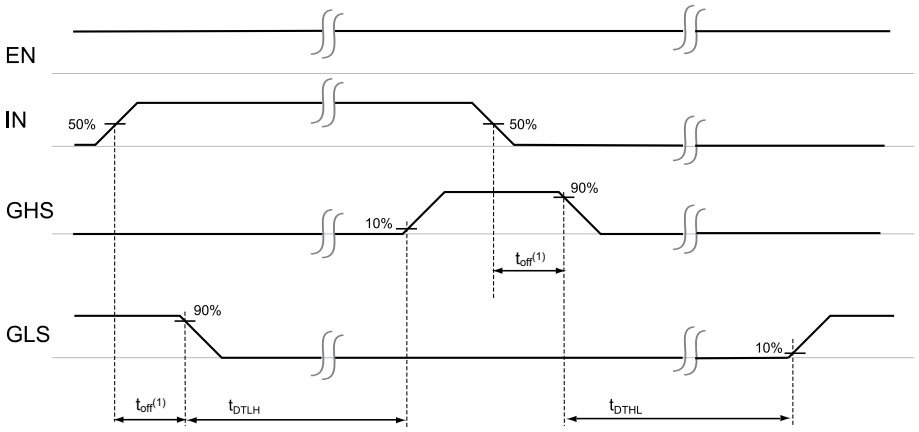
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{SI}	Maximum sink current capabilities	$V_S = V_{REG12}$ = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V Full temperature range	250			mA
I_{SO}	Maximum source current capabilities	$V_S = V_{REG12}$ = 12 V V_{BOOTx}-V_{OUTx} = 12 V T_J = 25 °C	350	600		mA
		$V_S = V_{REG12}$ = 12 V V_{BOOTx}-V_{OUTx} = 12 V Full temperature range	300			mA
		$V_S = V_{REG12}$ = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V T_J = 25 °C	300			mA
		$V_S = V_{REG12}$ = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V Full temperature range	250			mA
R_{PMOS}	PMOS on resistance	$V_S = V_{REG12}$ = 12 V V_{BOOTx}-V_{OUTx} = 12 V I_{source} = 100 mA T_J = 25 °C		3.8	4.8	Ω
		$V_S = V_{REG12}$ = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V I_{source} = 100 mA Full temperature range			6.1	Ω
R_{NMOS}	NMOS on resistance	$V_S = V_{REG12}$ = 12 V V_{BOOTx}-V_{OUTx} = 12 V I_{sink} = 100 mA T_J = 25 °C		1.8	2.3	Ω
		$V_S = V_{REG12}$ = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V I_{sink} = 100 mA Full temperature range			3	Ω
$I_{OUT,bias}$	OUTx bias current	OUTx = VS = 60 V T_J = 25 °C	85	155	225	µA
		OUTx = 0 V T_J = 25 °C	85	155	225	µA
t_{on}, t_{off}	Input to output propagation delay	(1)		40	70	ns
		$V_S = V_{REG12}$ = 5.5 V V_{BOOTx}-V_{OUTx} = 5.5 V Full temperature range			120	ns
MT	Delay matching, HS and LS turn-on/off	(2)			20	ns

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MT_{CH}	Delay matching between channels	(3)			20	ns
R_{DS_diode}	Bootstrap diode ON resistance			100	240	Ω
t_{DT}	Deadtime	R_{DT} = 50 kΩ	480	570	650	ns
		R_{DT} = 250 kΩ; T_J = 25 °C	2100	2600	3200	
MDT	Matching deadtime	R_{DT} = 50 kΩ (4)			70	ns
MDT_{CH}	Matching deadtime between channels	R_{DT} = 50 kΩ (5)			70	ns
Logic inputs						
V_{IL}	Low logic input voltage				0.8	V
V_{IH}	High logic input voltage		2			V
I_{IH}	Logic “1” input bias current	IN = 3.3 V T_J = 25 °C	12	16.5	25	µA
I_{IL}	Logic “0” input bias current	IN = 0 V T_J = 25 °C			100	nA
R_{PDin}	Input lines pull-down resistor	T_J = 25 °C	132	200	275	kΩ
$V_{FAULT,L}$	nFAULT low logic output voltage	I_{SINK} = 4 mA			0.6	V
Overcurrent Comparator						
V_{REF}	Comparator reference voltage	Full temperature range	470	505	525	mV
I_{CP}	Comparator input leakage current	V_{CP} = 1 V			2	µA
		V_{CP} = -0.5 V	-2.5			µA
$t_{DELAY,OC}$	Overcurrent delay time	See Figure 5			200	ns
t_{DFOC}	Deglitch filter time	See Figure 5	1.3	1.8	2.8	µs
$t_{DISABLE}$	Overcurrent disable time	See Figure 5	455	600	865	µs
V_{DS} monitoring protection						
V_{DSth}	V_{DS} monitoring protection threshold	V_{SCREF} = 0.2 V	0.1	0.2	0.3	V
		V_{SCREF} = 1 V	0.8	1	1.2	
		V_{SCREF} = 2.5 V	2.2	2.5	2.8	
$V_{SCREF,dis}$	V_{DS} monitoring protection disable voltage		2.9			V
$V_{SCREF,en}$	V_{DS} monitoring protection enable voltage				2.54	V
R_{SCREF}	V_{DS} monitoring reference pull-down resistor			450		kΩ
t_{DFSC}	V_{DS} monitoring protection deglitch time	See Figure 6	2.75	4.4	6.45	µs
$t_{DELAY,SC}$	V_{DS} monitoring protection delay time	See Figure 6			200	ns

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Thermal protection(6)						
T_{SD}	Thermal shutdown temperature		150	165		°C
T_{SDhys}	Thermal shutdown hystreresis			30		°C

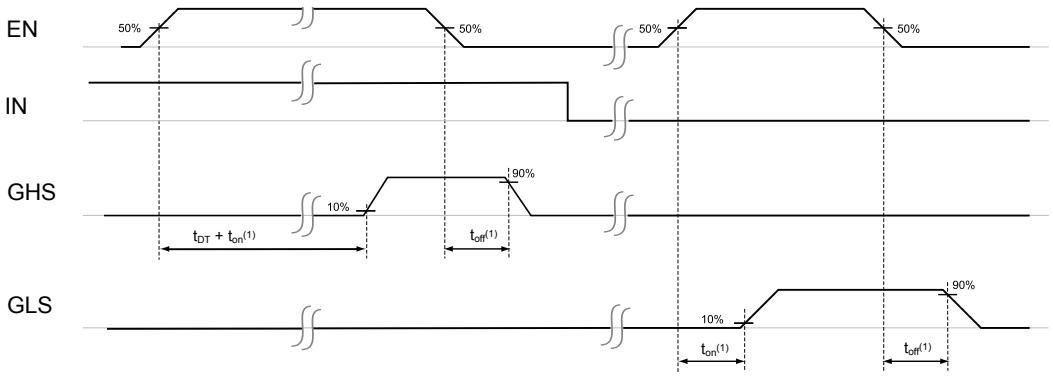
1. *These timings are measured using INHx/INLx mode (refer to Figure 4). An extra time is added when the device works with ENx/INx mode (refer to Figure 2 and Figure 3)*
2. *MT = max. ($|t_{on(GLS)} - t_{off(GLS)}|$, $|t_{on(GHS)} - t_{off(GHS)}|$, $|t_{off(GLS)} - t_{on(GHS)}|$, $|t_{off(GHS)} - t_{on(GLS)}|$).*
3. *MT_{CH} is the difference between the t_{on} and t_{off} of a channel and the same timings of any other channel.*
4. *MDT = $| t_{DTHL} - t_{DTLH} |$ see Figure 2.*
5. *MDT_{CH} is the difference between the t_{DTHL} and t_{DTLH} of a channel and the same timings of any other channel.*
6. *Based on characterization data on a limited number of samples, not tested during production*

Figure 2. INx timings and deadtime (ENx/INx mode)



Note:
(1) this propagation delay is typically 16 ns longer than the one measured in INH/INL driving mode (testing condition).

Figure 3. ENx timings (ENx/INx mode)



Note:
(1) this propagation delay is typically 16 ns longer than the one measured in INH/INL driving mode (testing condition).

Figure 4. **INHx and INLx timings (INHx/INLx mode)**

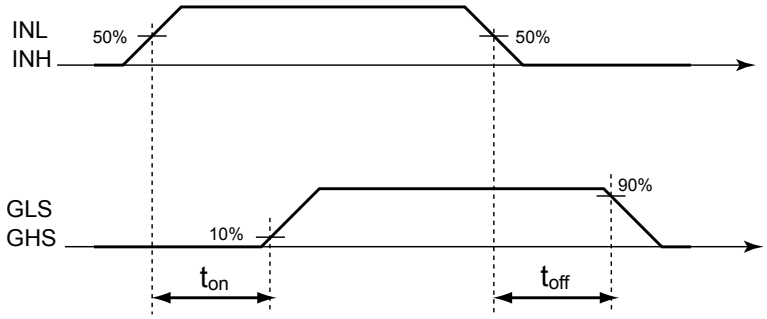


Figure 5. **Overcurrent comparator timings**

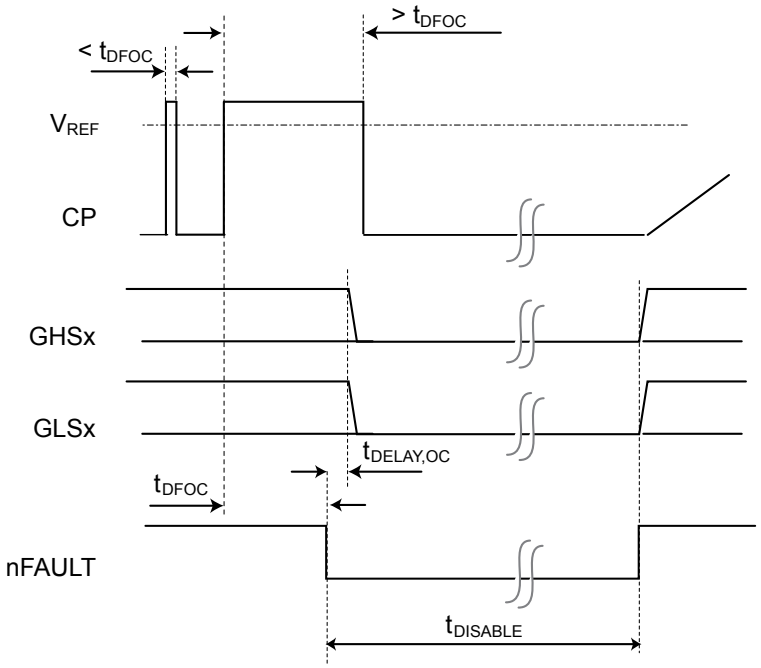
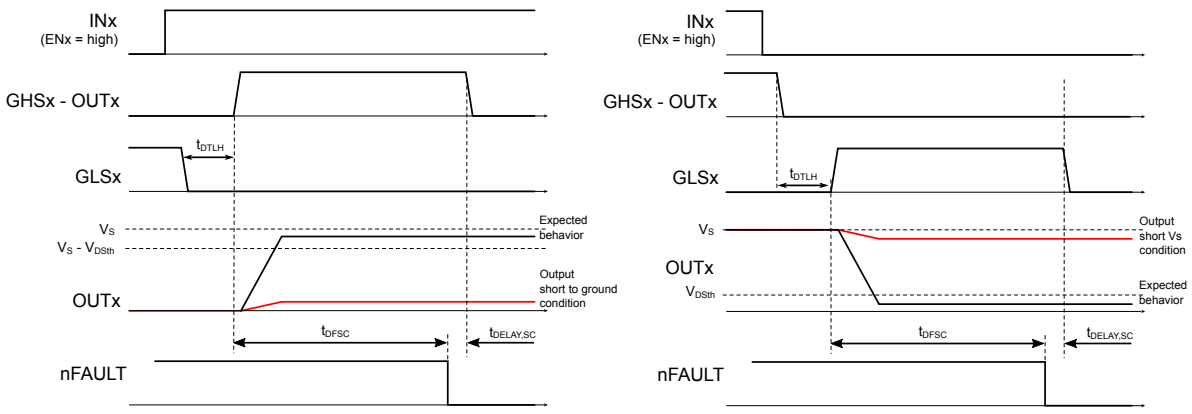
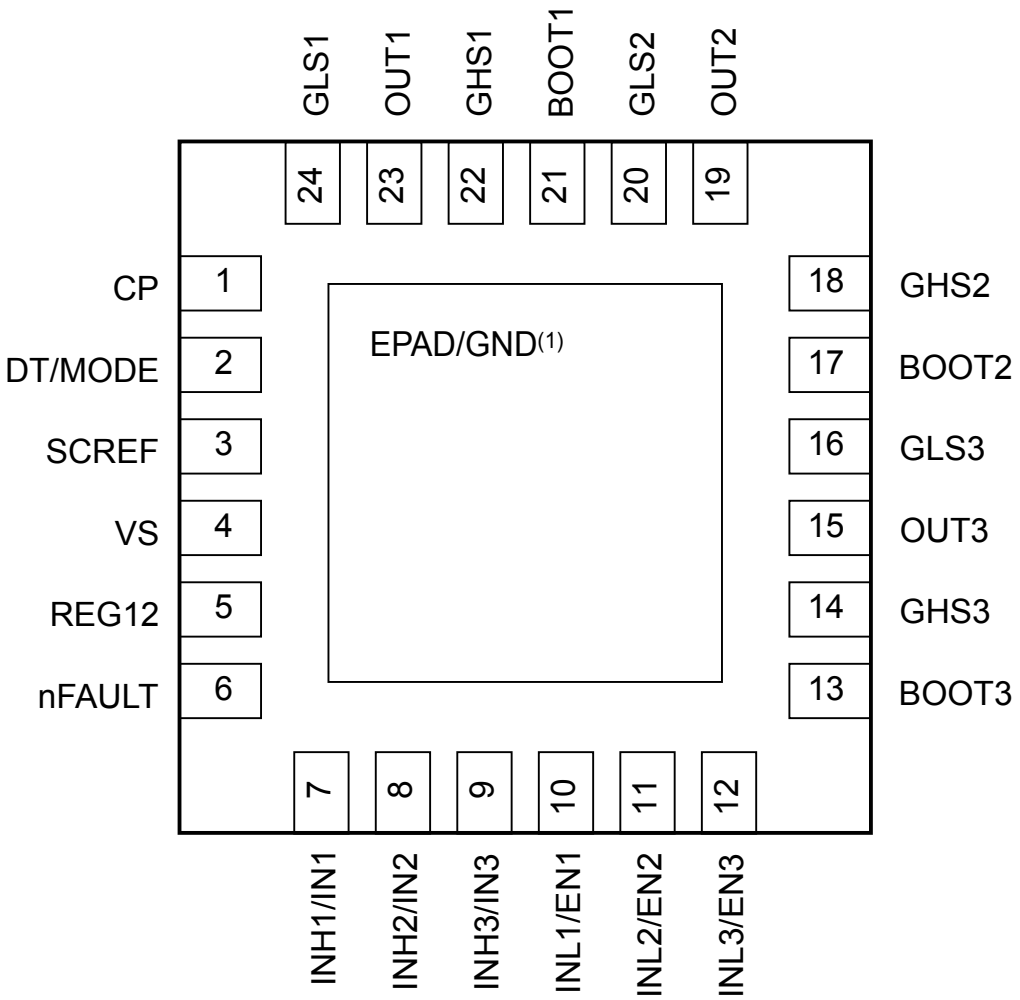


Figure 6. **V_{DS} monitoring protection timing**



4 Pin description

Figure 7. **STDRIVE101 pin connection in QFN 4x4 24L with exposed PAD (Top view)**



(1) The Exposed PAD is the ground connection of the device

Table 6. **STDRIVE101 pin description**

QFN 24L	Name	Type	Function
1	CP	Analog in	Overcurrent comparator input.
2	DT/MODE	Analog in	Adjust deadtime duration through a pull-down resistor (EHx/INx mode). When shorted to ground, deadtime is disabled and the INHx/INLx driving mode is selected.
3	SCREF	Analog in	Set the threshold voltage of the V_{DS} monitoring protection (internal pull-down resistor).
4	VS	Power	Supply voltage.
5	REG12	Power	12 V linear regulator output and gate drivers supply voltage.
6	nFAULT	Open-drain output	Fault output Forced low when one of the following failure conditions occurs: • Overcurrent • V_{DS} monitoring protection triggered • Thermal shutdown • UVLO on REG12 pin
7	INH1/IN1	Digital in	Output 1 high-side driving input (INHx/INLx mode) Output 1 driving input (EHx/INx mode)
8	INH2/IN2	Digital in	Output 2 high-side driving input (INHx/INLx mode) Output 2 driving input (EHx/INx mode)
9	INH3/IN3	Digital in	Output 3 high-side driving input (INHx/INLx mode) Output 3 driving input
10	INL1/EN1	Digital in	Output 1 low-side driving input (INHx/INLx mode) Output 1 enable input (EHx/INx mode)
11	INL2/EN2	Digital in	Output 2 low-side driving input (INHx/INLx mode) Output 2 enable input (EHx/INx mode)
12	INL3/EN3	Digital in	Output 3 low-side driving input (INHx/INLx mode) Output 3 enable input (EHx/INx mode)
13	BOOT3	Power	Half-bridge 3 bootstrap voltage
14	GHS3	Analog out	Half-bridge 3 high-side gate driver output
15	OUT3	Power	Half-bridge 3 high-side (floating) common voltage
16	GLS3	Analog out	Half-bridge 3 low-side gate driver output
17	BOOT2	Power	Half-bridge 2 bootstrap voltage
18	GHS2	Analog out	Half-bridge 2 high-side gate driver output
19	OUT2	Power	Half-bridge 2 high-side (floating) common voltage
20	GLS2	Analog out	Half-bridge 2 low-side gate driver output
21	BOOT1	Power	Half-bridge 1 bootstrap voltage
22	GHS1	Analog out	Half-bridge 1 high-side gate driver output
23	OUT1	Power	Half-bridge 1 high-side (floating) common voltage
24	GLS1	Analog out	Half-bridge 1 low-side gate driver output
	EPAD/GND	Power	Ground

5 Device description

The STDRIVE101 is a low voltage gate driver for three-phase power stages with integrated linear regulator.

The device supply voltage is applied to VS pin. The VS is also used both as input voltage of 12 V LDO linear regulator and to supply some internal circuitries, including the V_{DS} monitoring protection reference voltage for the high-side driver.

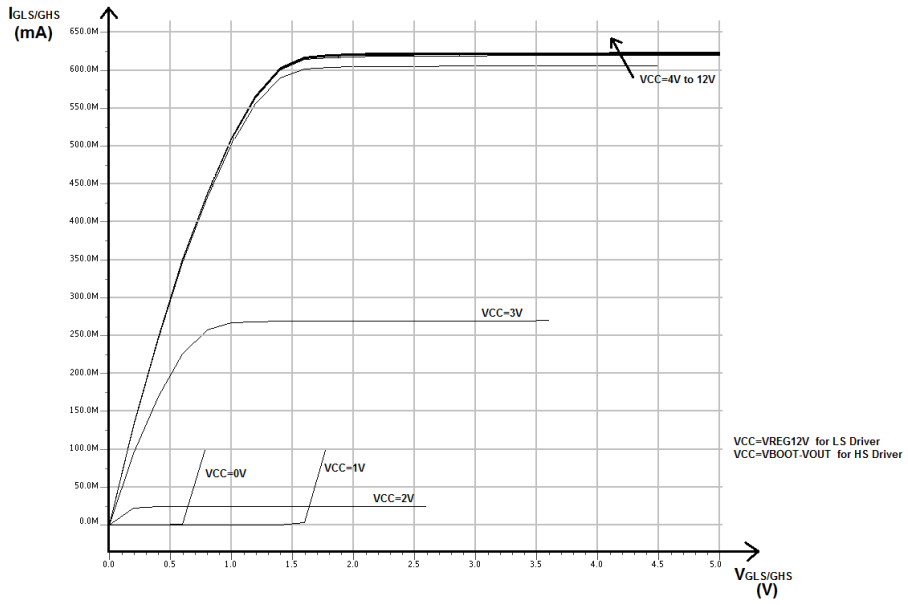
The power stage voltage (VM in Figure 1) must be equal or lower than VS voltage. If the VM voltage exceeds the VS voltage, the device is damaged due to the violation of OUT pins absolute maximum rating as reported in Table 1.

If a VM voltage lower than VS is used, the V_{DS} monitoring protection cannot be used (refer to dedicated Section 5.6).

5.1 Gate drivers' characteristics

The STDRIVE101 integrates a triple half-bridge gate driver able to drive N-channel power MOSFETs. The high-side section is supplied by a bootstrapped voltage technique with integrated bootstrap diode.

Figure 8. Gate drivers' outputs characteristics in UVLO conditions

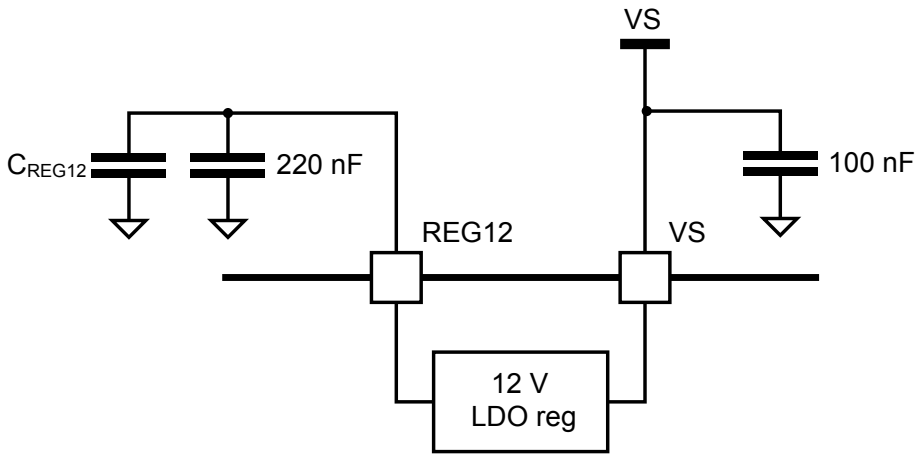


The device is designed to operate using VS as the supply voltage of the external power stage (i.e. motor supply voltage). For this reason, the AMR rating of the OUTx pins is strictly related to the VS value and, more generally, it is not possible to bias the OUT pins when the VS supply is not present (i.e. floating or shorted to ground).

5.2 12 V LDO linear regulator

The device integrates a LDO linear regulator generating 12 V output starting from the VS supply. The regulator is disabled during standby mode.

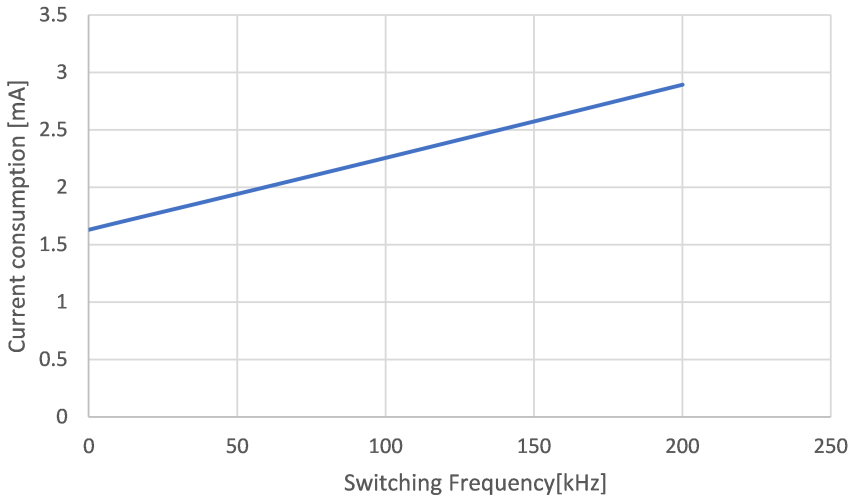
Figure 9. **12 V LDO linear regulator typical configuration**



The regulator supplies the gate drivers and can be used to supply small external loads. The average current consumption I_{REG12} is given by the internal consumption of the gate drivers, the current provided to the gates of the external MOSFETs and the external load consumption, if any. I_{REG12} cannot exceed $I_{REG12lim}$.

The internal consumption of the gate drivers is proportional to the switching frequency and its typical value is reported in Figure 10; this is the overall consumption of the six gate drivers and it is measured without any load connected on the drivers' outputs.

Figure 10. **Typical current consumption (gate driver's outputs unloaded)**



On top of this, the current supplied to the external MOSFETs' gates must be considered. The overall gate current $I_{G,tot}$ for the six MOSFETs of the power stage can be calculated as:

Equation 1

$$I_{G,tot} = 6 \cdot Q_g \cdot f_{SW} \quad (1)$$

where Q_g is the gate charge value of the external MOSFETs, taken at gate voltage equal to V_{REG12} and f_{SW} is the switching frequency of the MOSFETs (i.e. the frequency of the PWM signals applied to the drivers).

Another aspect to consider for the maximum current of the linear regulator is the power dissipation. An excessive power dissipation leads to the thermal shutdown of the device (Section 5.8). The total power dissipation of the regulator P_{REG12} can be calculated as:

Equation 2

(2)

$$P_{REG12} = (V_S - V_{REG12}) \cdot I_{REG12}$$

where V_S is the voltage supply of the STDRIVE101, V_{REG12} is the regulator output voltage and I_{REG12} is the average current consumption described previously.

Note: ***The size of the external power MOSFETs and the switching frequency increase the gate driver's consumption, thus reducing the current availability for external loads.***

In addition to the average value I_{REG12} dynamic contributions must be considered: these are the currents needed to charge the bootstrap capacitors, e.g. after the high-side MOSFET is kept on for a considerable amount of time or after leaving the stand-by condition. In these cases, the amount of current is higher than $I_{REG12lim}$, so it is mainly provided by the bypass capacitor C_{REG12} connected to REG12 pin. In this situation, a voltage drop ΔV_{REG12} occurs on REG12, while the LDO maximum current $I_{REG12lim}$ mainly recharges C_{REG12}. During this recharge time ($t_{charge,REG12}$ expressed in Equation 3), the availability of current for external loads is reduced.

Equation 3

(3)

$$t_{charge,REG12} > C_{REG}\frac{\Delta V_{REG12}}{I_{REG12lim}}$$

5.2.1 Bootstrap section

The bootstrap circuitry allows to generate a voltage higher than the supply VS and it is used to supply the high-side drivers. When one high-side MOSFET is turned on, its source voltage (OUTx pin) increases up to VS. Therefore, the gate must be driven at a voltage higher than VS. The bootstrap capacitor is referred to the OUTx pin:

- When the OUTx pin is forced to GND (i.e. the respective low-side MOSFET is on), the bootstrap capacitor is charged through the bootstrap diode.
- When the OUTx is forced to VS (i.e. the respective high-side MOSFET is on), the bootstrap capacitor supplies the respective high-side driver and discharges.

The voltage drop on the bootstrap capacitors corresponds to the supply of the high-side drivers. Each bootstrap capacitor must be charged after the corresponding high-side is turned on, otherwise its voltage falls below the $V_{BO(On)}$ - $V_{BO(Hyst)}$ threshold, causing the turning off of the respective driver (Section 5.5). A limitation in a bootstrap architecture is that the high-side MOSFET cannot be kept on for an indefinite amount of time. In fact, when the high-side is on, the respective bootstrap capacitor starts discharging. If not recharged, the bootstrap capacitor voltage falls below the $V_{BO(On)}$ - $V_{BO(Hyst)}$ (i.e. the UVLO on BOOTx pin). For this reason, working at 100% duty cycle is possible, but only for a limited number of PWM periods. The bigger the bootstrap capacitor, the longer the time the high-side MOSFET can be kept on.

To avoid excessive drop on the REG12 pin, a proper bypass capacitor is required. Even using an external supply connected to the REG12 pin, it is important to have a bypass capacitor with low ESR providing fast current transients when required by the bootstrap capacitors.

The bypass capacitor on REG12 pin must provide the charge for the three bootstrap capacitors: the bigger the bootstrap capacitors are, the bigger should be the REG12 capacitor (refer to Equation 4 in Section 5.2.1.2).

5.2.1.1 Power-up and wake-up

During the power-up or after leaving the standby condition, there may be no charge in bootstrap capacitors. In these cases, the drivers cannot start immediately with normal operation, but the bootstrap capacitor should be charged turning on the low-side MOSFET. At the beginning of this procedure, a large amount of current could be required. If the internal 12 V LDO regulator is used, its current is limited at $I_{REG12lim}$ (Section 5.2).

5.2.1.2 Charging time and external bootstrap diodes

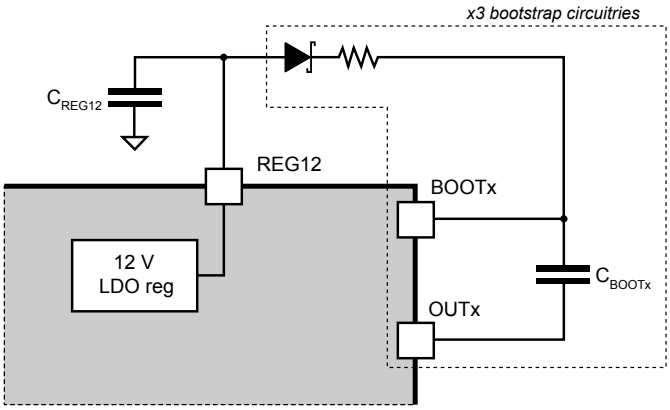
The charging time required to charge the bootstrap capacitors depends on their value but also on the resistance of the bootstrap diode (R_{DS_diode}), which limits the current flow. In order to reduce the minimum time for bootstrap recharge (i.e. the minimum time the low-side MOSFET must be on), external bootstrap diodes can be used as shown in Figure 11.

Each diode is in parallel with the corresponding internal bootstrap diode. An external series resistor, smaller than R_{DS_diode}, can be still used together with each diode to reduce the maximum charging current and helps to limit the voltage drop on the REG12 pin. The maximum drop on the C_{REG12} capacitor occurs when the three bootstrap capacitors must be recharged and no series resistor is used with the external diodes. This drop can be approximated as:

Equation 4

$$\Delta V_{CREG12} \approx V_{REG12} \cdot \frac{3 \cdot C_{BOOT}}{C_{REG12} + 3 \cdot C_{BOOT}} \quad (4)$$

Figure 11. External bootstrap diode configuration

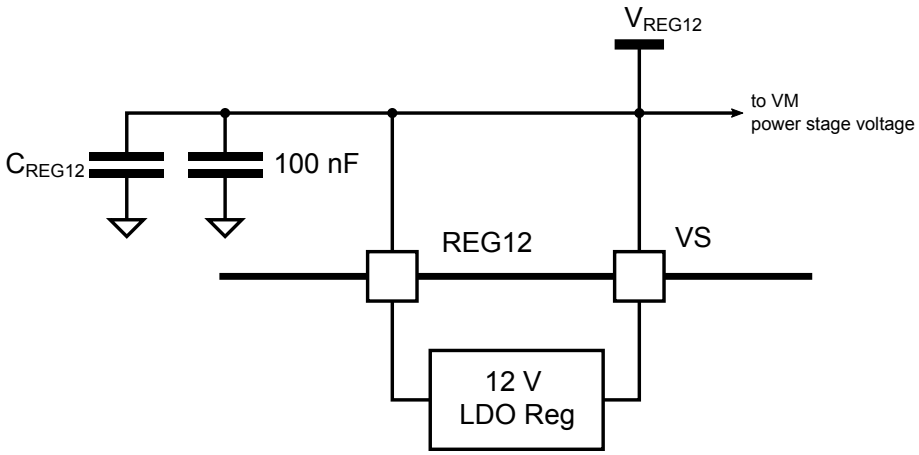


5.2.2 Externally provided gate driver's supply voltage

It is possible to provide externally the supply voltage for the gate driving circuitry directly, bypassing the integrated regulator and shorting VS and REG12 pins together.

Important: ***Using this configuration the consumption is partially reduced in standby mode.***

Figure 12. 12 V LDO supply voltage externally provided



5.3 Control logic

The device integrates a control logic providing two input strategies. The driving method is selected according to DT/MODE pin status:

- DT/MODE connected to the ground through an R_{DT} resistor: digital inputs provide enable and input lines for each half-bridge and an internal deadtime is generated according to R_{DT} value (ENx/INx mode).
- DT/MODE shorted to ground: digital inputs provide high and low-side driving lines for each half-bridge, no deadtime is internally generated (INHx/INLx mode). In any case, the high and low-side outputs of same half-bridge cannot be simultaneously driven high because of the integrated interlocking function.

Note: ***The DT/MODE pin status must not be changed during device operation.***

All the input lines have an internal pull-down to guarantee the low logic level even if no driving input is present.

Table 7. INxL and INxH inputs truth table

INxH	INxL	GHSx	GHLx	'x' Half-bridge condition
L	L	L	L	Disabled
L	H	L	H	Low-side on
H	L	H	L	High-side on
H	H	L	L	Disabled (interlocking)

Table 8. ENx and INx inputs truth table

ENx	INx	GHSx	GLSx	'x' Half-bridge condition
L	X	L	L	Disabled
H	L	L	H	Low-side on
H	H	H	L	High-side on

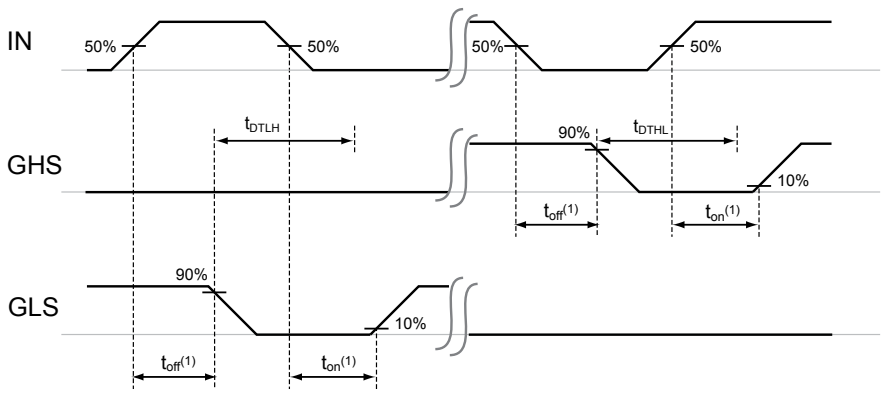
Note: *X: don't care*

5.3.1 Deadtime

When the DT/MODE pin is connected to the ground through an R_{DT} resistor (ENx/INx mode selected), the device internally generates a deadtime between the MOSFET turn-off and the turn-on of the opposite one.

Input pulses shorter than the deadtime cause an immediate turn on of the gate driver, back to the former status as shown in Figure 13.

Figure 13. Deadtime management for short pulses



Note:
(1) this propagation delay is typically 16 ns longer than the one measured in INH/INL driving mode (testing condition).

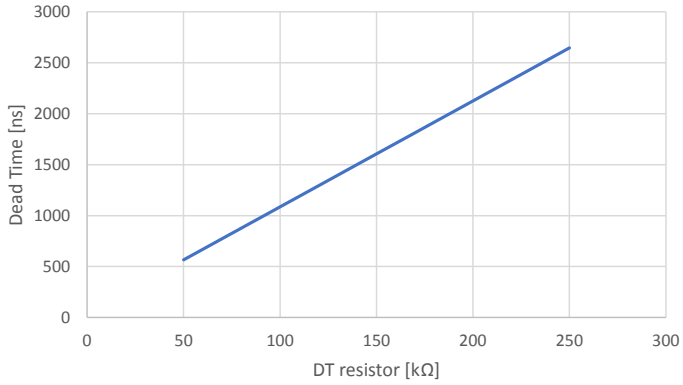
The deadtime depends on the R_{DT} value according to the following equation:

Equation 5

$$R_{DT}[k\Omega] = 96.15 \cdot DT\ [\mu s] - 4.45 \quad (5)$$

The equation is valid only with R_{DT} value ranging from 50 kΩ to 250 kΩ.

Figure 14. Typical deadtime vs. DT resistor value



Note: ***If DT/MODE pin is left floating, the resulting deadtime is about 1 µs (typical at T_J = 25°C). However, it should not be considered an operative condition. If the DT/MODE pin is shorted to ground, the device operates in INHx/INLx mode.***

5.4 Standby mode

The STDRIVE101 provides a standby mode to reduce power consumption, in particular:

- All the outputs driver forced low (external power switches turned off)
- The overcurrent comparator is disabled
- TheV_{DS} monitoring protection is disabled
- The UVLO protection is disabled
- The 12 V LDO linear regulator is switched off

Important: ***If the 12 V regulator is bypassed, the consumption in standby mode is not reduced.***

The device enters standby mode keeping low all the driving input pins (INx/INHx and ENx/INLx) for at least t_{STBY} time. At power-up, if all the driving inputs are low, the device is immediately set in standby condition. The device leaves standby mode after a t_{WAKE} time after at least one of the logic inputs is set high (refer to Figure 15 and Figure 16). Considering the standby condition disables the 12 V regulator, the device returns operative only after the REG12 voltage returns above the UVLO turn-on threshold. When the device exits from standby condition, the bootstrap capacitors charge via low-side turn-on is required, as described in Section 5.2.1.1

Figure 15. **Standby and wake-up time (ENx/INx mode, with $V_S = V_{REG12} = 12$ V)**

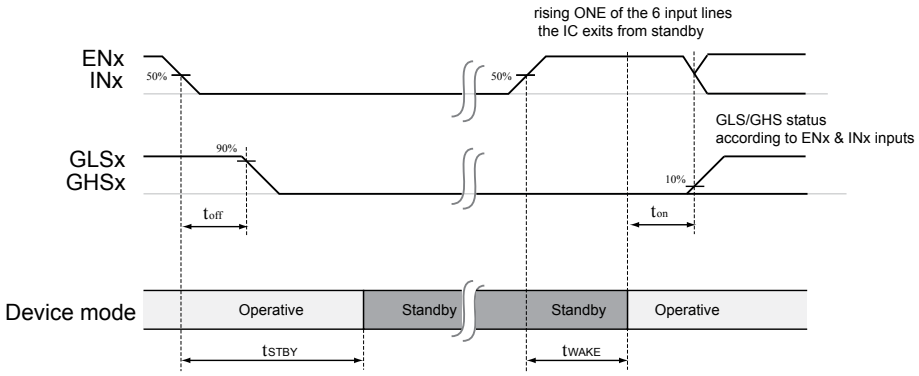
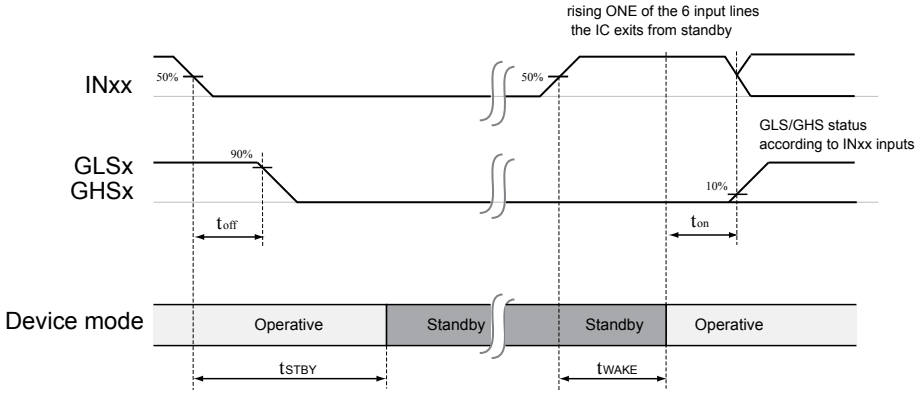


Figure 16. **Standby and wake-up time (INHx/INLx mode, with $V_S = V_{REG12} = 12$ V)**



5.5 Undervoltage protection

The device provides UVLO protections on each power supply.

During power-up (see Figure 17), the device leaves the UVLO condition when the respective supply voltage rises above the turn-on threshold. When the supply voltage is below the on-threshold voltage of a hysteresis, the UVLO condition is set.

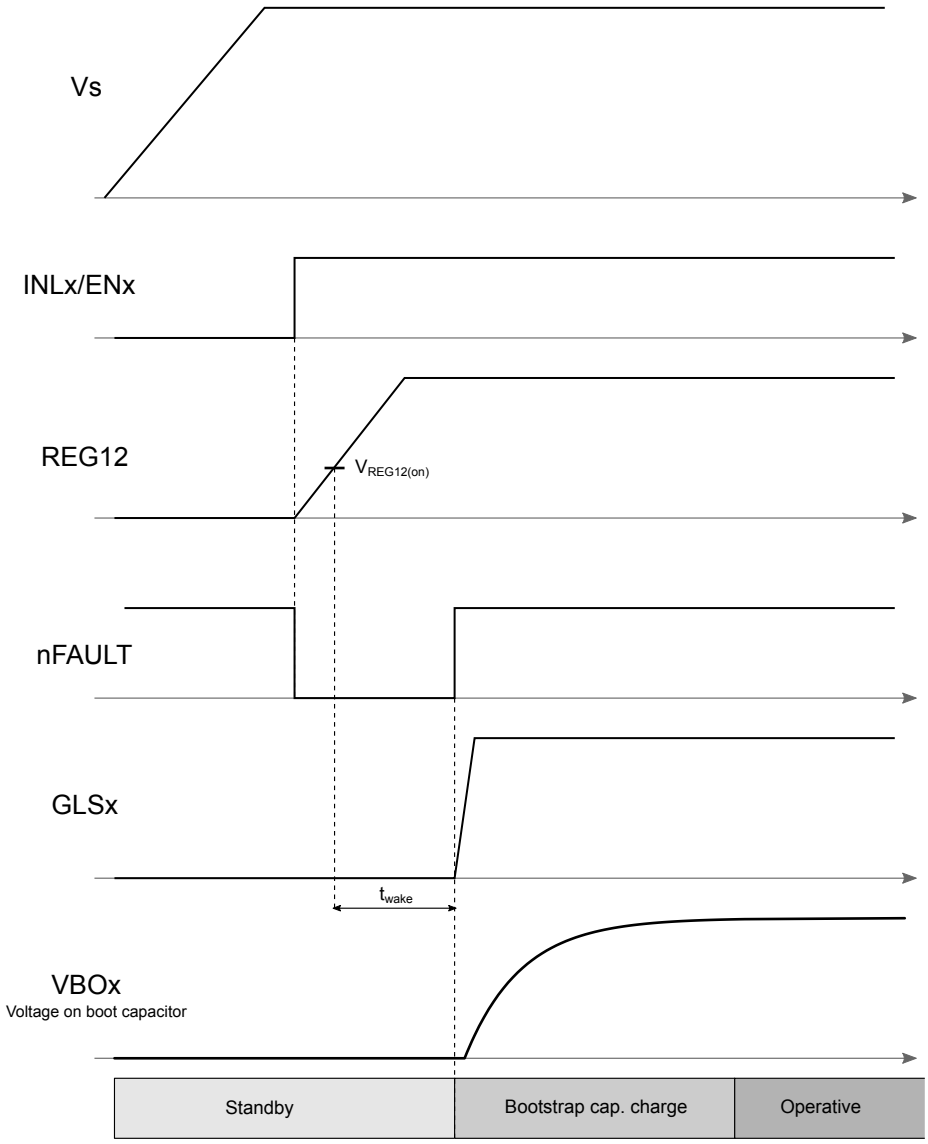
Table 9 summarizes which blocks are switched off in UVLO condition.

Table 9. **UVLO and OT protection management**

Block	VREG12 UVLO	VBOOTx UVLO
HSU, HSV, HSW output	LOW(1)	LOW(1) (2)
LSU, LSV, LSW output	LOW(1)	
nFAULT open-drain output	LOW	OPEN

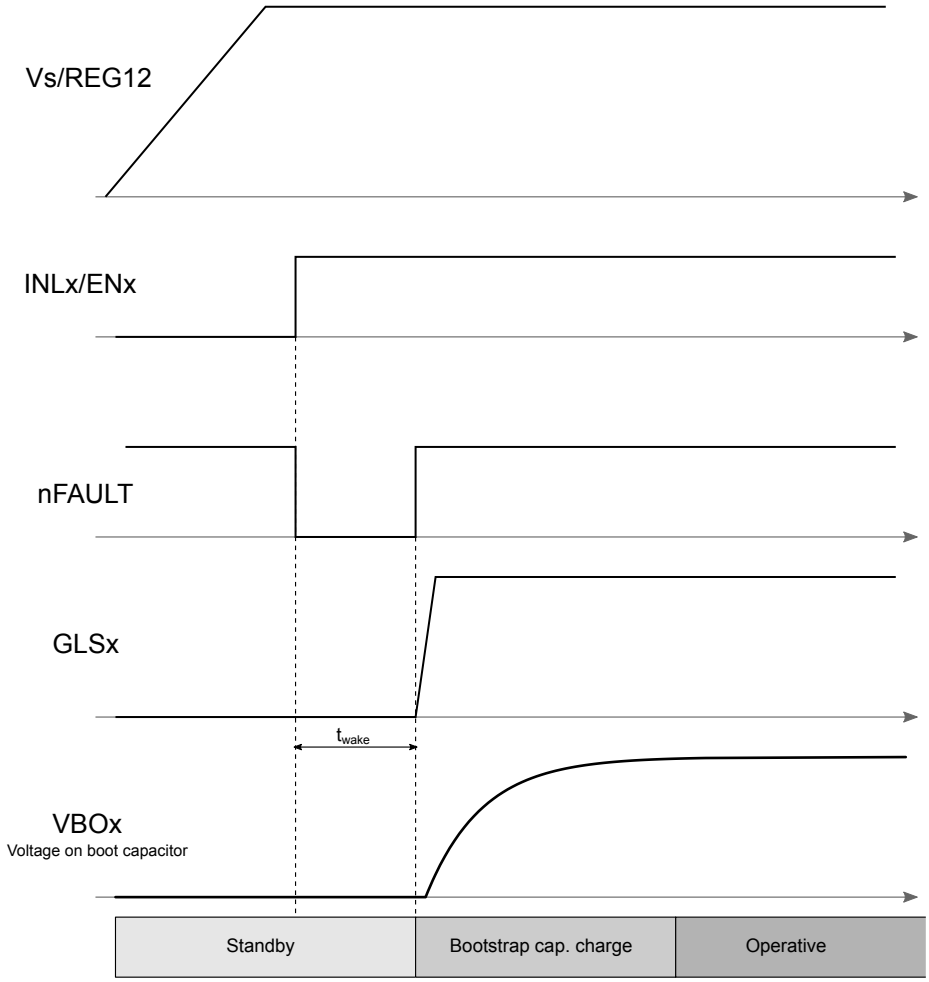
1. *The N-channel of the gate driver is turned ON with all the available supply voltage, refer to Figure 8 .*
2. *Each high-side gate driver provides independent UVLO protection (e.g. UVLO on BOOTU causes the HSU to turn off only).*

Figure 17. **Power-up sequence, internal 12 V regulator used**



When the REG12 pin is supplied externally, the internal regulator is disabled. When leaving the standby condition raising one of the digital inputs, the nFAULT pin goes low, even if there is no UVLO condition on the REG12 pin, as shown in Figure 18

Figure 18. Power-up sequence, external supply on REG12 pin



5.6 V_{DS} monitoring protection

The device monitors the V_{DS} of the power stage's MOSFETs in order to detect anomalous conditions. The V_{DS} of each MOSFET is compared to a reference threshold (V_{DSth}).

The reference threshold is generated according to the voltage applied to the SCREF pin:

Equation 6

$$V_{DSth} = V_{SCREF} \quad (6)$$

The SCREF voltage must be in the range between 0.2 V to $V_{SCREF,en}$.

If the voltage is above $V_{SCREF,dis}$, the protection is disabled.

When enabled, the protection triggers one of the following conditions occur:

- GLSx output is high and $V_{OUTx} > V_{DSth}$ for more than t_{DFSC}
- GHSx output is high and $(V_S - V_{OUTx}) > V_{DSth}$ for more than t_{DFSC}

Important:
The V_{DS} monitoring is implemented assuming that the supply of the power stage (VM) is at the same voltage of the STDRIVE101 supply (VS). Supplying the power stage with a voltage VM lower than VS the V_{DS} monitoring protection could not work properly. In particular, if the voltage difference 'VS - VM' is greater than V_{DSth}, the protection will be triggered each time the high-side is turned on, regardless of the current flowing in the MOSFET.
For this reason it is recommended, when using the V_{DS} monitoring protection to supply the STDRIVE101 (VS) and the power stage (VM) at the same voltage. In case it is required to use a VM voltage lower than VS, the V_{DS} monitoring protection must be disabled setting the SCREF pin above the $V_{SCREF,dis}$ voltage.

As soon as the protection is triggered, all the gate drivers outputs are forced low, the nFAULT output is forced low and the protection is latched. In this condition all the gate driver outputs are kept low whatever the driving inputs (refer to Figure 6).

The protection is released only when the device enters standby mode.

Note: ***SCREF pins structure does not allow a bias without VS supply voltage.***

5.7 Overcurrent comparator

The STDRIVE101 embeds a comparator suitable for overcurrent detection of the power stage through a shunt resistor.

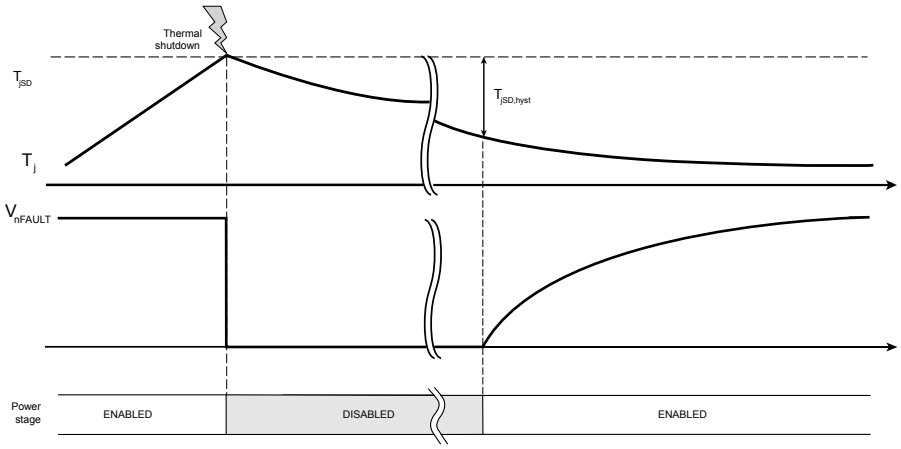
When the input voltage at CP pin is higher than internal reference voltage (V_{REF}), the device enters into a protection state: all the gate driver outputs are forced low and the nFAULT open drain output is forced low. The device automatically leaves the protection state after a $t_{DISABLE}$ time (refer to Figure 5 for details).

5.8 Thermal protection

The device embeds an overtemperature shutdown protection through thermal sensor placed next to the linear regulator block.

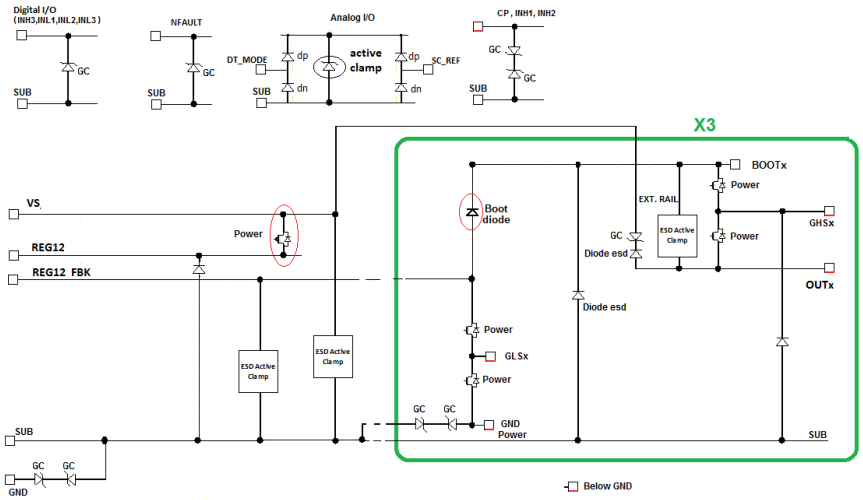
When the overtemperature protection occurs, the linear regulator is switched off and the nFAULT output is forced low. The thermal shutdown condition expires when the temperature goes below the "T_{SD}- T_{SDhys}" temperature (auto-restart).

Figure 19. **Thermal shutdown management**



6 ESD protection strategy

Figure 20. **ESD protection strategy**



7 Application example

Figure 21 shows an application example using the STDRIVE101 to drive a three-phase motor with triple shunt configuration.

Table 10. Typical application values (V_{DD} = 3.3 V)

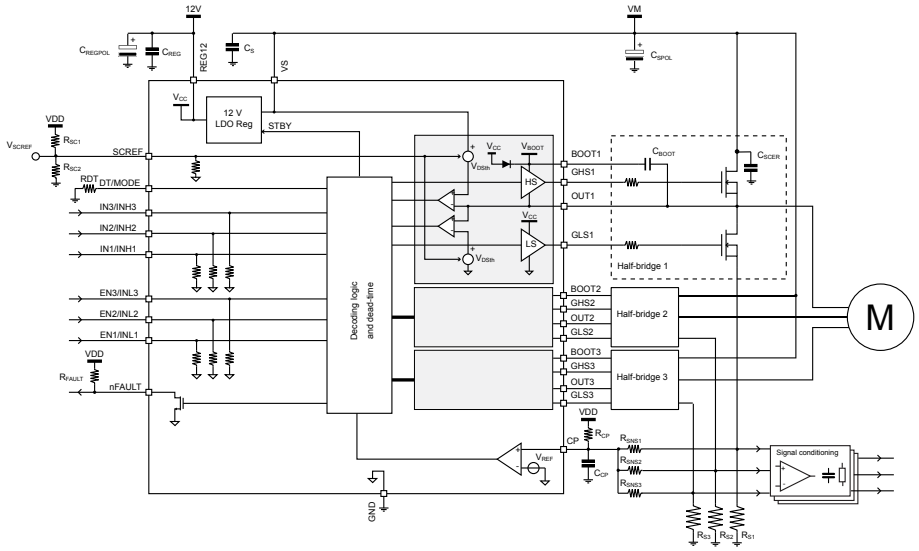
Name	Value
C_S	100 nF / 100 V
C_{SCER}	100 nF / 100 V (1)
C_{SPOL}	120 µF / 100 V
C_{REG}	100 nF / 25 V
C_{REGPOL}	4.7 µF / 25 V
C_{BOOT}	1 µF / 25 V
R_{DT}	50 kΩ (t_{DT} ≅570 ns)
R_{SC1}	18 kΩ
R_{SC2}	10 kΩ
R_{FAULT}	39 kΩ
R_{S1}, R_{S2}, R_{S3}	Values according to application requirements
R_{SNS1}, R_{SNS2}, R_{SNS3}	Values according to application requirements
C_{CP}	2.2 nF / 16 V
R_{CP}	Values according to application requirements

1. *to be kept close to the relative HS MOSFET (see Figure 21)*

The others features implemented are:

- V_{DS} monitoring protection with SCREF = 1.2 V (V_{DD} = 3.3 V)
- Overcurrent protection with internal comparator (CP pin)

Figure 21. Typical application schematic



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 22. VFQFPN 4x4x1.0 24 PITCH 0.5 package outline

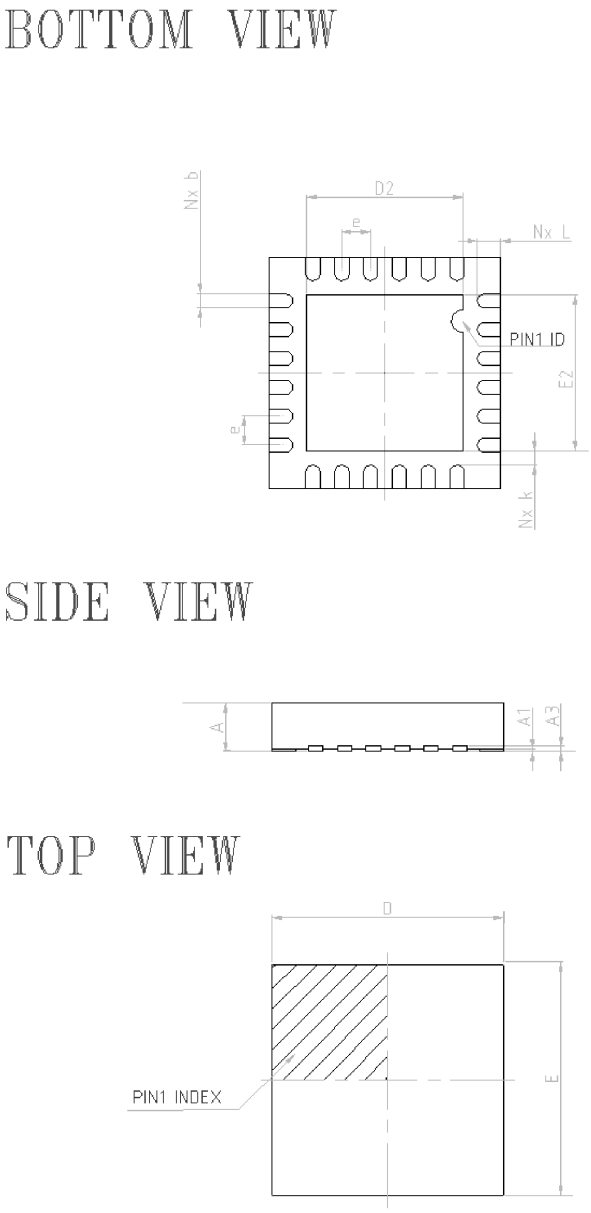
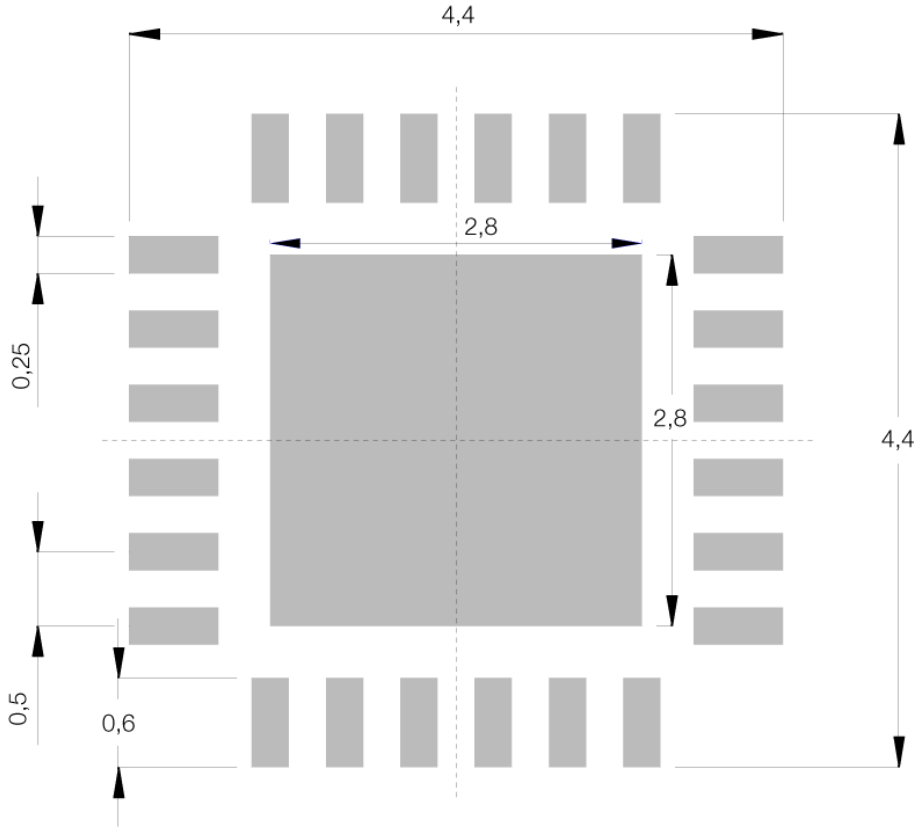


Table 11. **VFQFPN 4x4x1.0 24 PITCH 0.5 package mechanical data**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.60	2.70	2.80
E	3.85	4.00	4.15
E2	2.60	2.70	2.80
e		0.50	
L	0.30	0.40	0.50
k		0.25	

Figure 23. **VFQFPN 4x4x1.0 24 PITCH 0.5 suggested footprint**



9 Ordering information

Table 12. **Device summary**

Order code	Package	Packaging
STDRIVE101	VFQFPN 4x4x1.0 24 PITCH 0.5	Tube
STDRIVE101TR	VFQFPN 4x4x1.0 24 PITCH 0.5	Tape & Reel

Revision history

Table 13. **Document revision history**

Date	Version	Changes
26-Oct-2020	1	Initial release.
24-Jun-2022	2	Added Note 2 in Table 2, updated SCREF description in Table 6 Updated Table 10 and Table 11. Updated Figure 10 title, Figure 12, Figure 21, Figure 22.

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