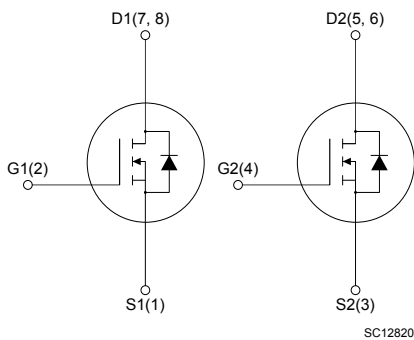
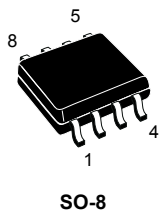



## Automotive-grade dual N-channel 60 V, 35 mΩ typ., 5 A STripFET II Power MOSFET in an SO-8 package



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STS5DNF60L	60 V	45 mΩ	5 A

- AEC-Q101 qualified 
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

### Applications

- Switching applications

### Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



#### Product status link

[STS5DNF60L](#)

#### Product summary

<b>Order code</b>	STS5DNF60L
<b>Marking</b>	5DF60L
<b>Package</b>	SO-8
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 15$	V
$I_D$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	5	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(2)}$	Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2	W
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $P_{TOT} = 1.6\text{ W}$  for single operation.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	62.5	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 Oz Cu,  $t \leq 10\text{ s}$ , dual operation.

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified.

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	60			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}^{(1)}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 15\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$		35	45	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$		45	55	

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1030	-	pF
$C_{oss}$	Output capacitance		-	140	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	40	-	pF
$Q_g$	Total gate charge	$V_{DD} = 48\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see Figure 12. Test circuit for gate charge behavior)	-	15	-	nC
$Q_{gs}$	Gate-source charge		-	4	-	nC
$Q_{gd}$	Gate-drain charge		-	4	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 2.2\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 4.5\text{ V}$	-	15	-	ns
$t_r$	Rise time		-	28	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	45	-	ns
$t_f$	Fall time		-	10	-	ns

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 20 \text{ V}$ (see Figure 16. Switching time waveform)	-	85		ns
$Q_{rr}$	Reverse recovery charge		-	85		nC
$I_{RRM}$	Reverse recovery current		-	2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

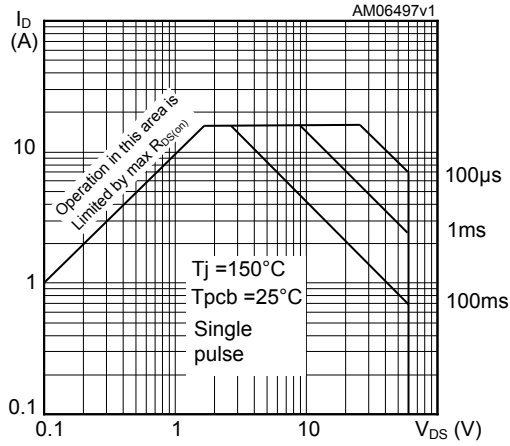


Figure 2. Thermal impedance

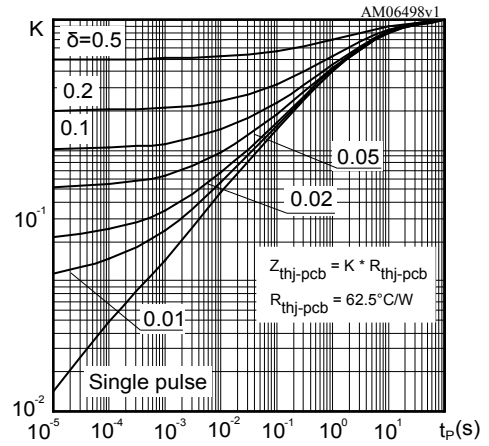


Figure 3. Output characteristics

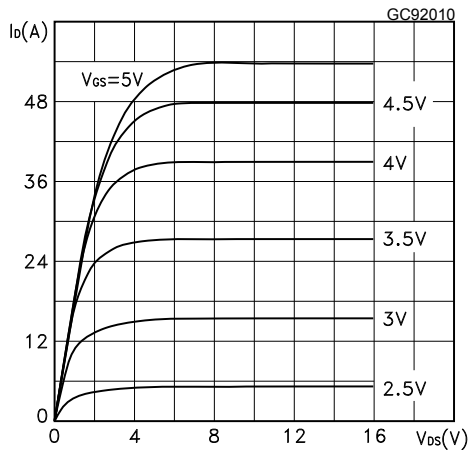


Figure 4. Transfer characteristics

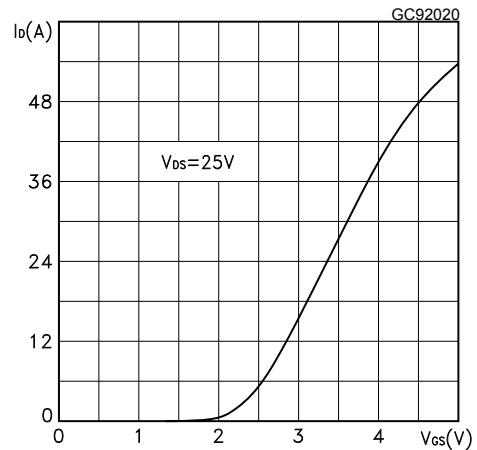


Figure 5. Source-drain diode forward characteristics

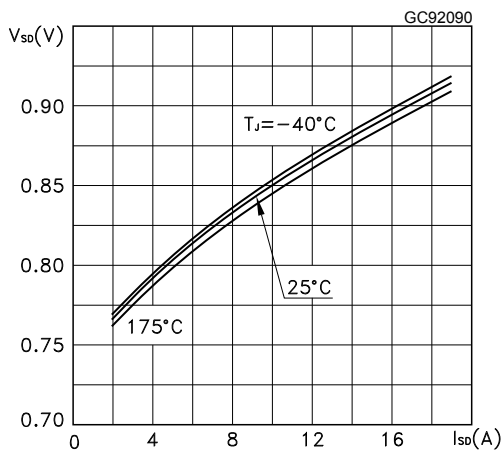
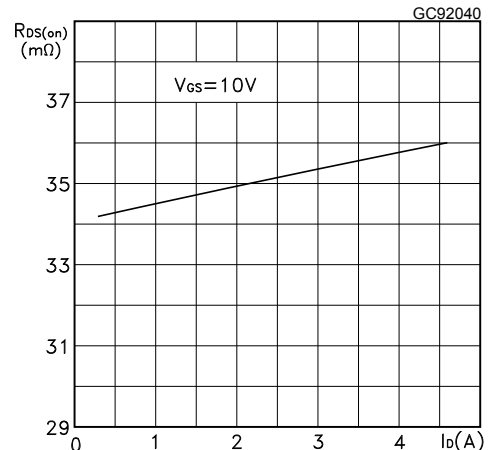
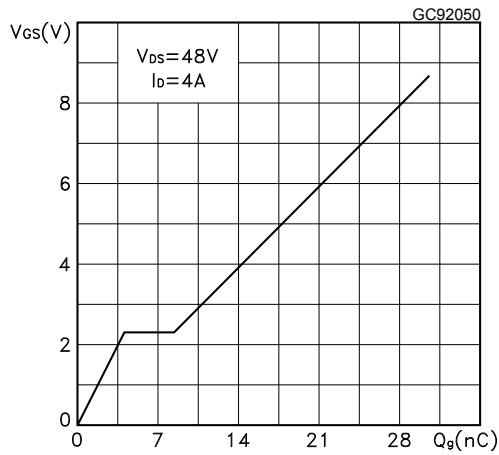


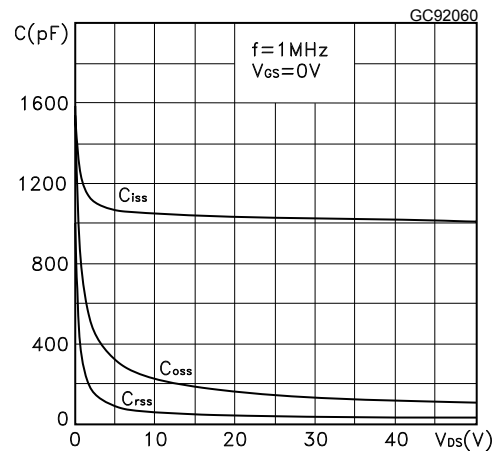
Figure 6. Static drain-source on-resistance



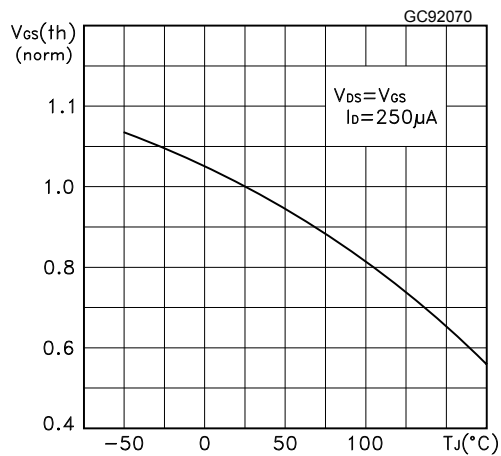
**Figure 7. Gate charge vs gate-source voltage**



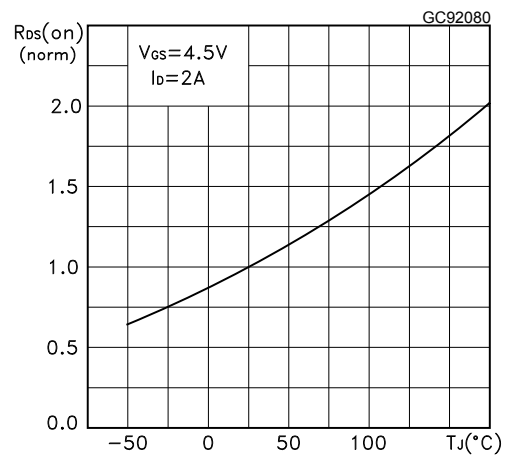
**Figure 8. Capacitance variations**



**Figure 9. Normalized gate threshold voltage vs temperature**

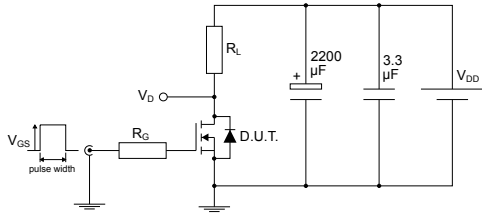


**Figure 10. Normalized on-resistance vs temperature**



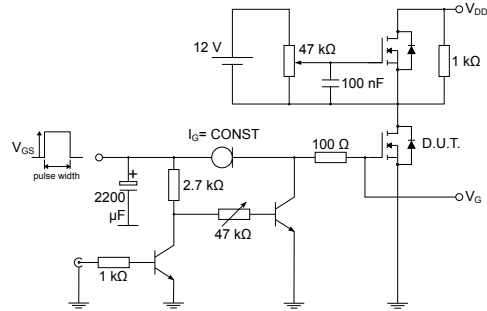
### 3 Test circuits

Figure 11. Test circuit for resistive load switching times



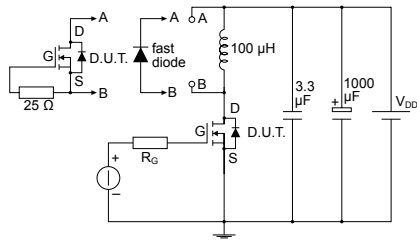
AM01468v1

Figure 12. Test circuit for gate charge behavior



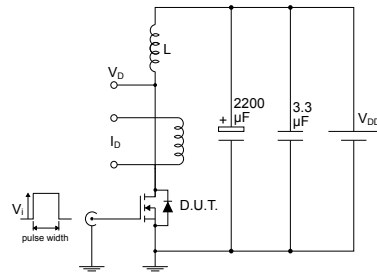
AM01469v1

Figure 13. Test circuit for inductive load switching and diode recovery times



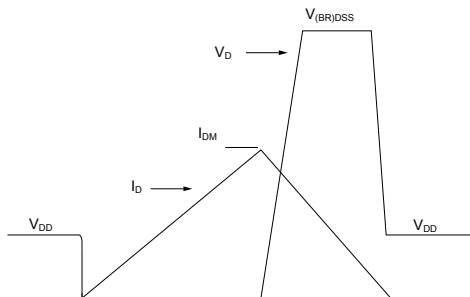
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Figure 14. Unclamped inductive load test circuit



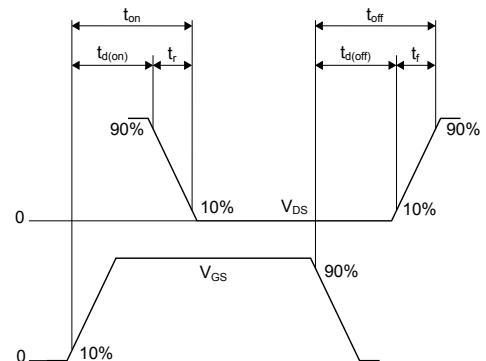
AM01471v1

Figure 15. Unclamped inductive waveform



AM01472v1

Figure 16. Switching time waveform



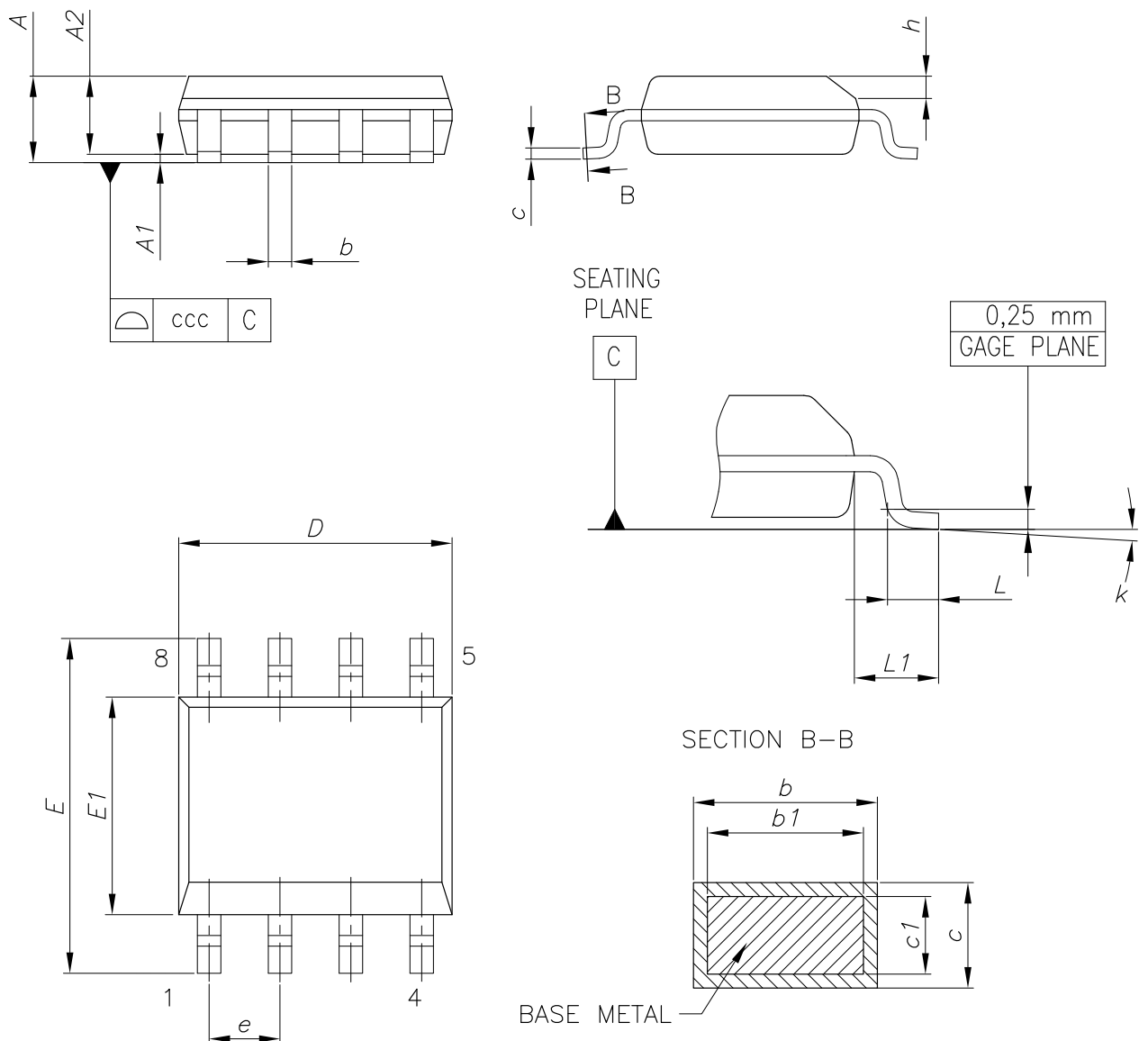
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 SO-8 package information

Figure 17. SO-8 package outline



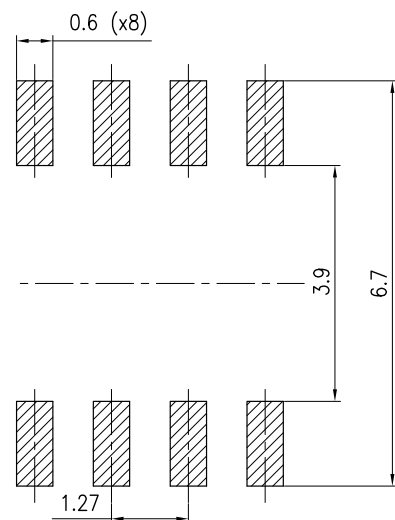
0016023\_So-807\_fig2\_Rev10



**Table 7. SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

**Figure 18. SO-8 recommended footprint (dimensions are in mm)**



0016023\_So-807\_footprint\_Rev10

## 4.2 SO-8 packing information

Figure 19. SO-8 tape and reel dimensions

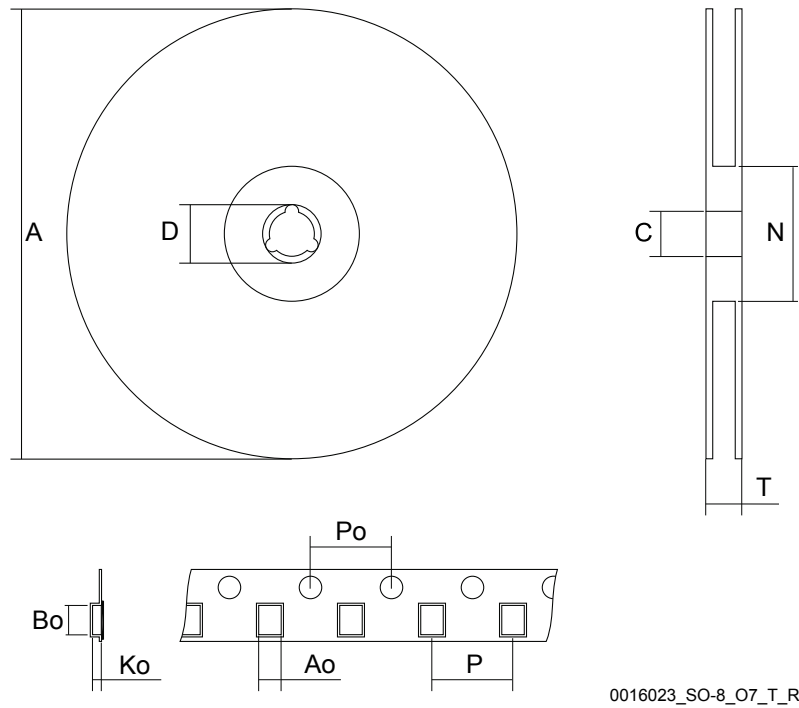
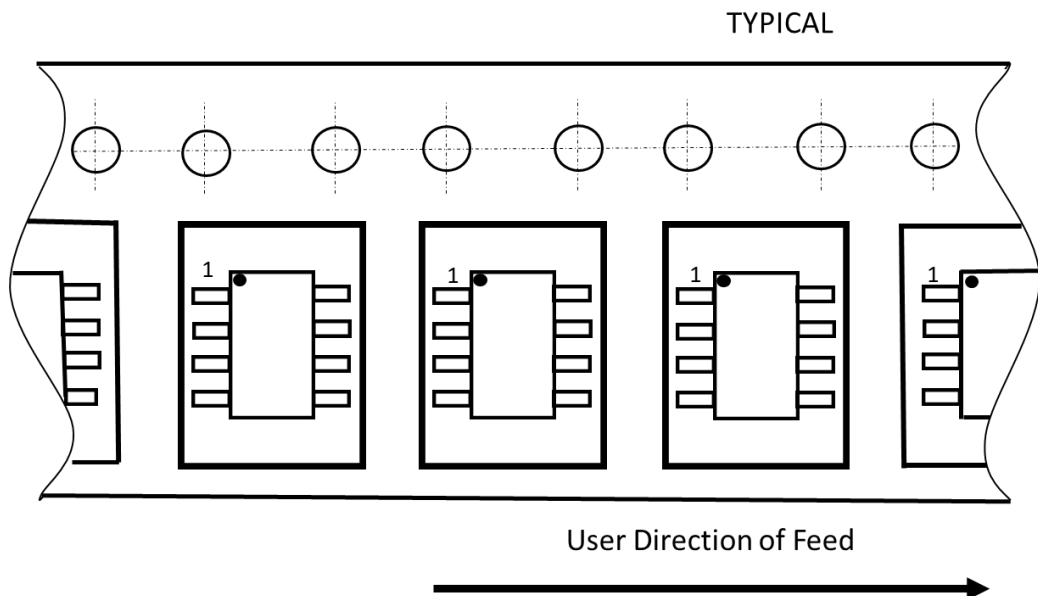


Figure 20. Tape orientation



**Table 8. SO-8 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5	-	6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
03-Mar-2008	1	First release.
18-Mar-2010	2	<i>Figure 2: Safe operating area</i> and <i>Figure 3: Thermal impedance</i> have been changed.
17-Oct-2016	3	Updated title, features and description in cover page. Added AEC-Q101 qualified in the Features section. Updated <i>Package information</i> and <i>Packing information</i> . Minor text changes.
04-Mar-2021	4	Updated <a href="#">Internal schematic for SO-8 dual N-channel</a> and <a href="#">Features</a> in cover page. Updated <a href="#">Table 4. Dynamic</a> . Updated <a href="#">Section 4.2 SO-8 packing information</a> . Minor text changes.

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