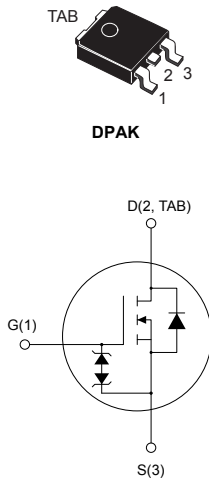


# N-channel 900 V, 4.7 $\Omega$ typ., 2.1 A SuperMESH Power MOSFET in a DPAK package



AM01476v1\_tab



## Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD2NK90ZT4	900 V	6.5 $\Omega$	2.1 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

## Applications

- Switching applications

## Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of  $dv/dt$  capability for the most demanding applications.

### Product status link

[STD2NK90ZT4](#)

### Product summary

Order code	STD2NK90ZT4
Marking	D2NK90Z
Package	DPAK
Packing	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	900	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.1	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	8.4	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
ESD	Gate-source, human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 2.1\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\%V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.78	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^\circ\text{C}/\text{W}$

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width is limited by $T_J$ max.)	2.1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	150	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	900			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.05\text{ A}$		4.7	6.5	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	485		pF
$C_{oss}$	Output capacitance		-	50		pF
$C_{riss}$	Reverse transfer capacitance		-	10		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ V to } 720\text{ V}$	-	24		pF
$Q_g$	Total gate charge	$V_{DD} = 720\text{ V}$ , $I_D = 2\text{ A}$ , $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	19.5	27	nC
$Q_{gs}$	Gate-source charge		-	3.4		nC
$Q_{gd}$	Gate-drain charge		-	10.8		nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$ , $I_D = 1\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	21	-	ns
$t_r$	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	43	-	ns
$t_f$	Fall time		-	40	-	ns

**Table 7. Source-drain diode**

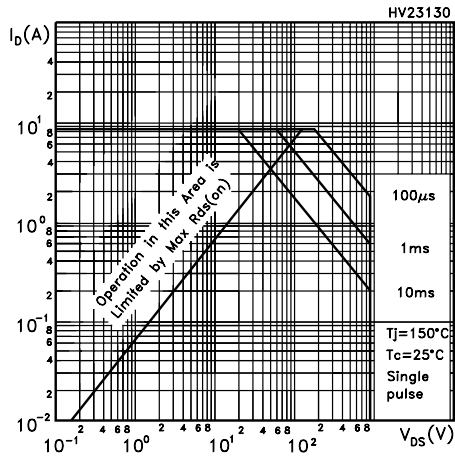
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		2.1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8.4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.1 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	415		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50 \text{ V}$	-	1.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.2		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	515		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.5		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

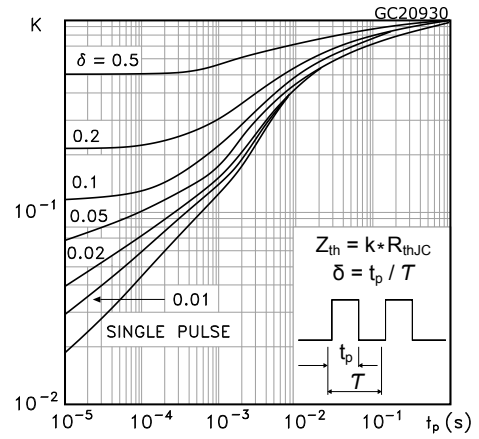
2. Pulse width is limited by safe operating area.

## 2.1 Electrical characteristics (curves)

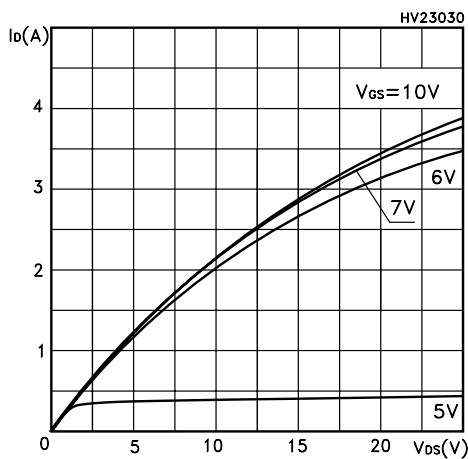
**Figure 1. Safe operating area**



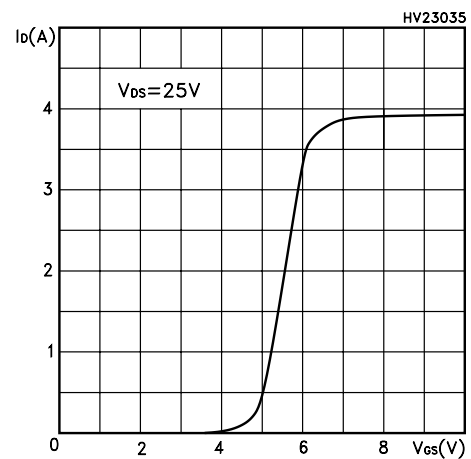
**Figure 2. Thermal impedance**



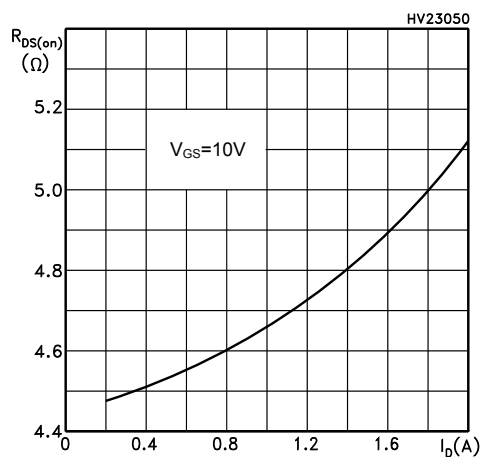
**Figure 3. Output characteristics**



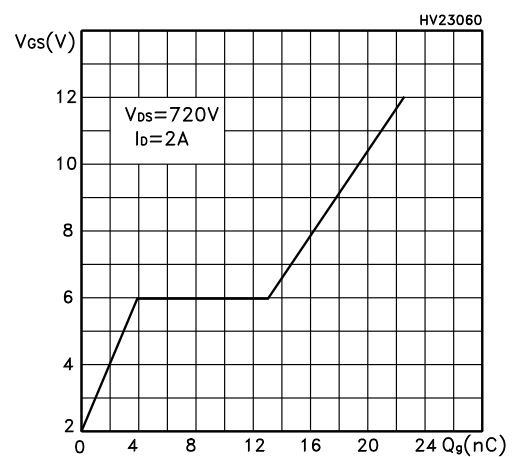
**Figure 4. Transfer characteristics**



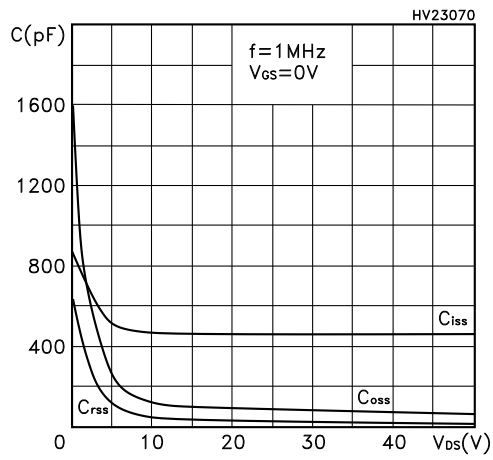
**Figure 5. Static drain-source on resistance**



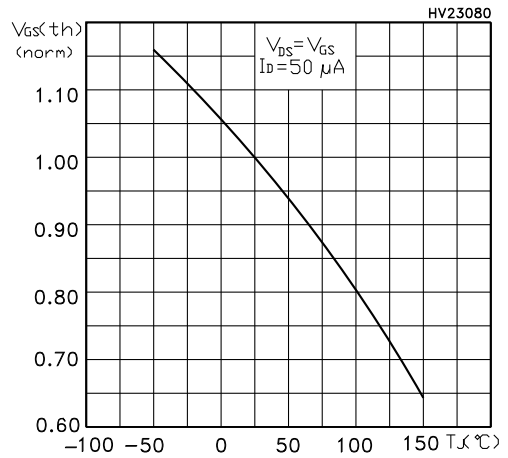
**Figure 6. Gate charge vs gate-source voltage**



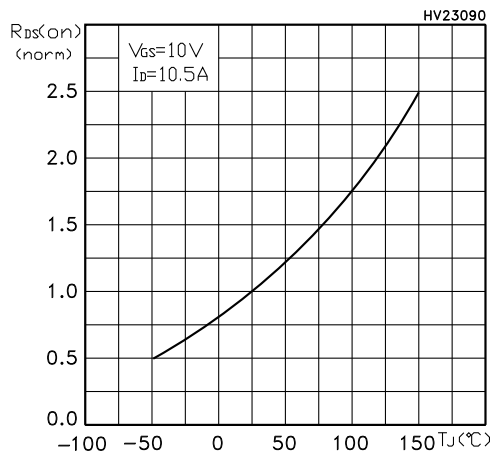
**Figure 7. Capacitance variations**



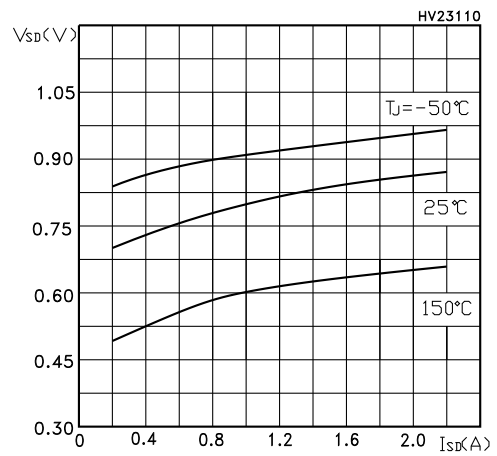
**Figure 8. Normalized gate threshold voltage vs temperature**



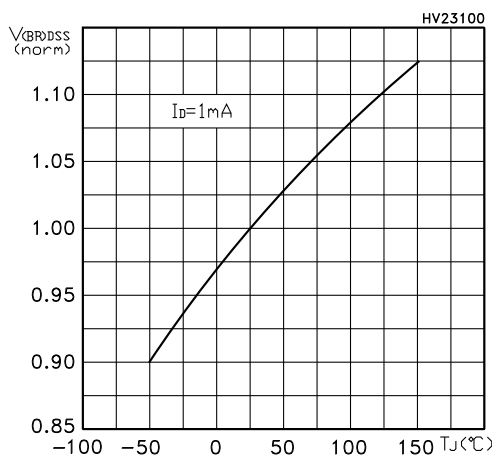
**Figure 9. Normalized on resistance vs temperature**



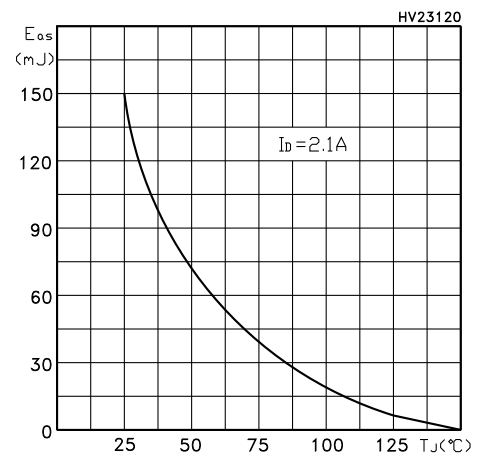
**Figure 10. Source-drain diode forward characteristics**



**Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature**



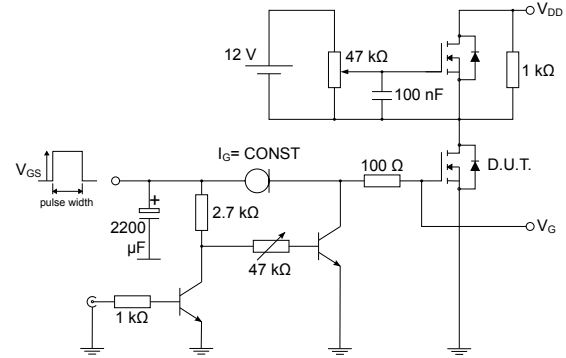
**Figure 12. Maximum avalanche energy vs temperature**



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

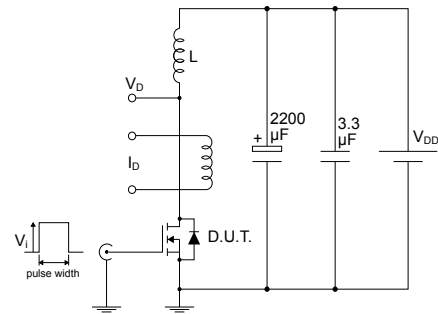

AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**

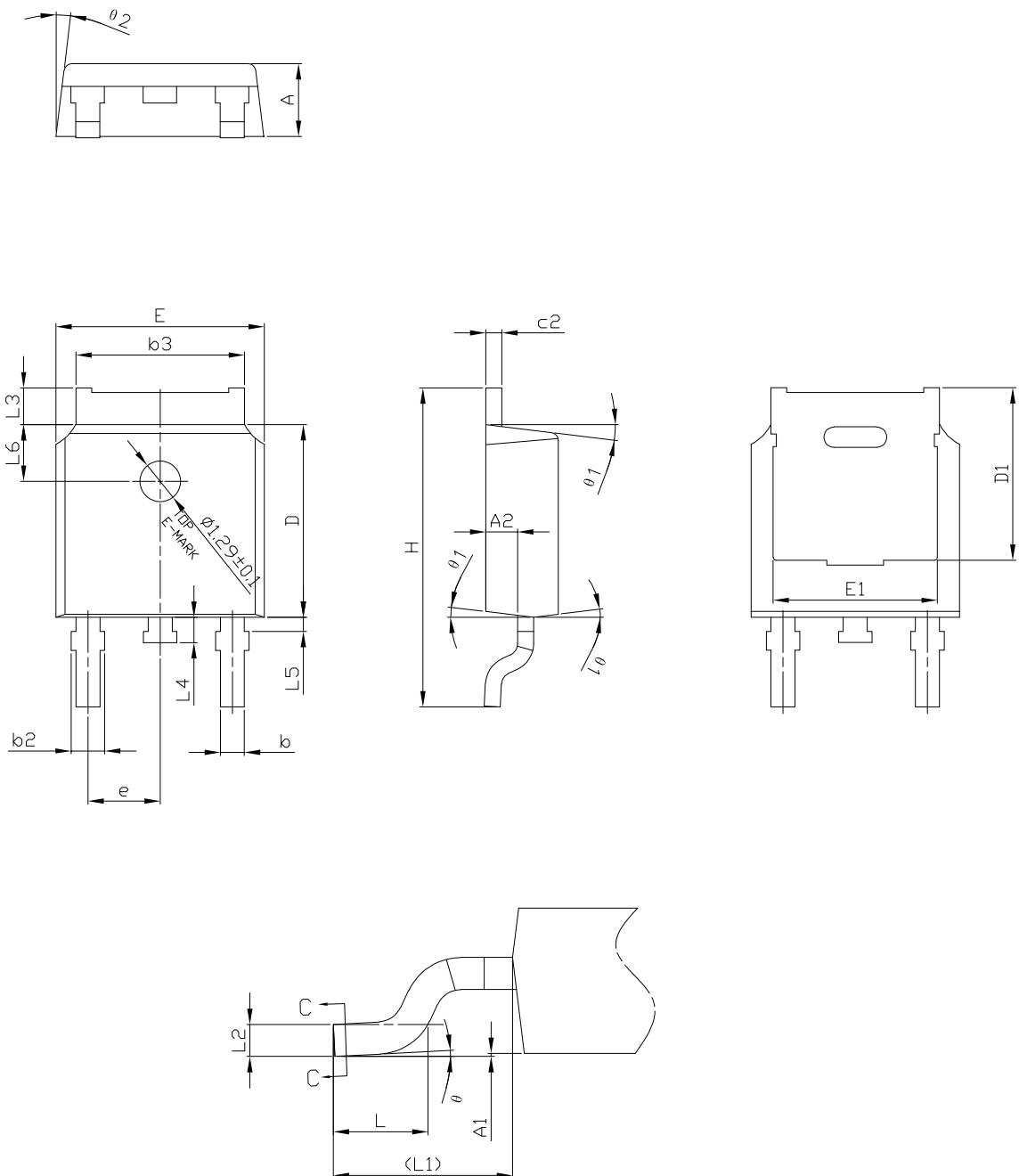

AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type C3 package information

Figure 19. DPAK (TO-252) type C3 package outline



0068772\_type-C3\_rev34

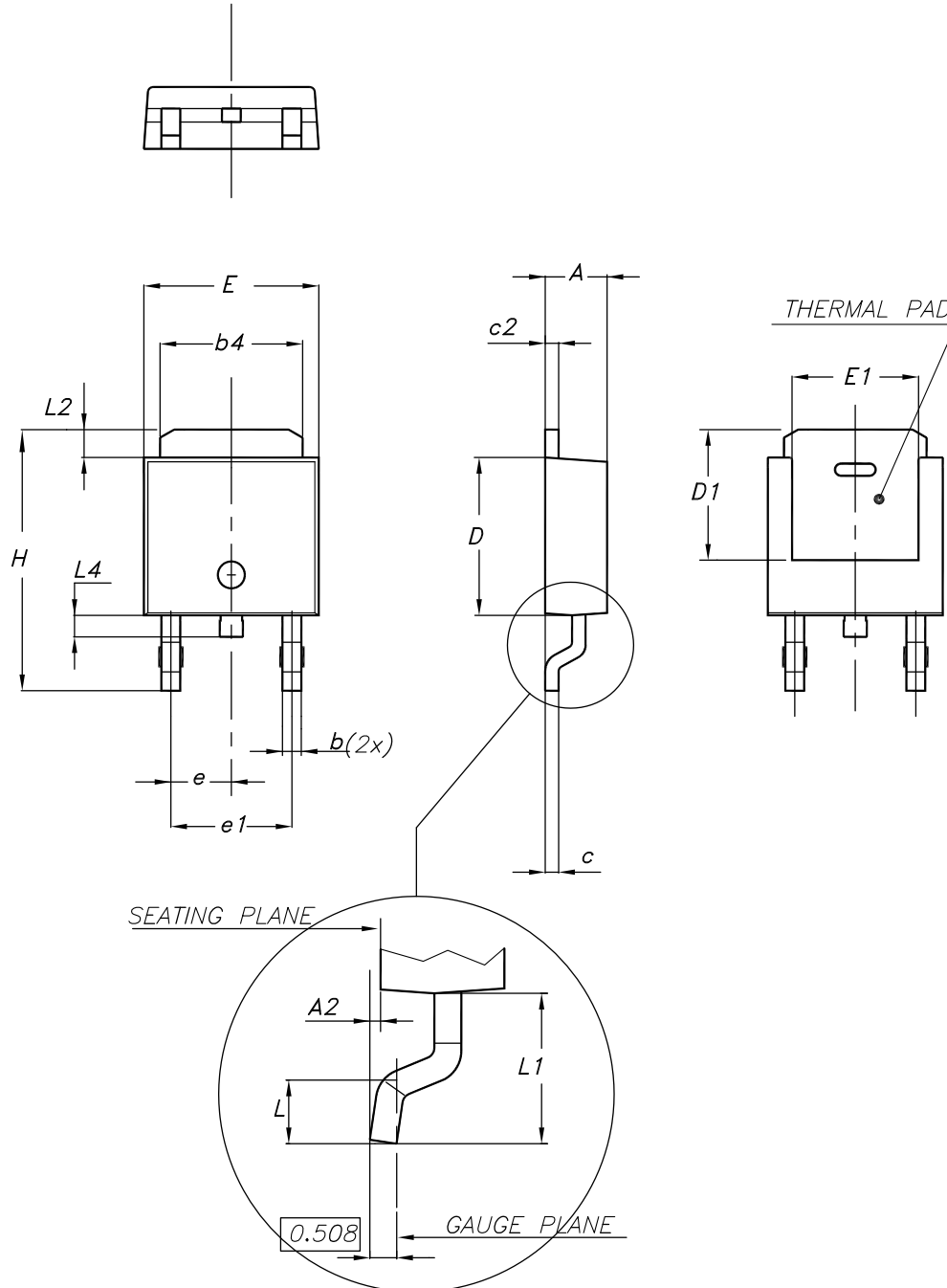


**Table 8. DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

## 4.2 DPAK (TO-252) type E package information

Figure 20. DPAK (TO-252) type E package outline

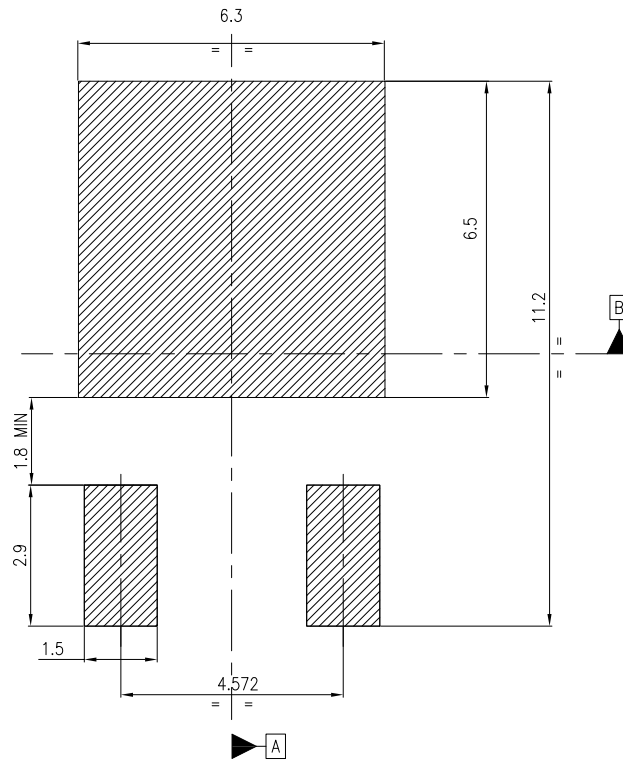


0068772\_typeE\_rev.34

**Table 9. DPAK (TO-252) type E mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

**Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)**



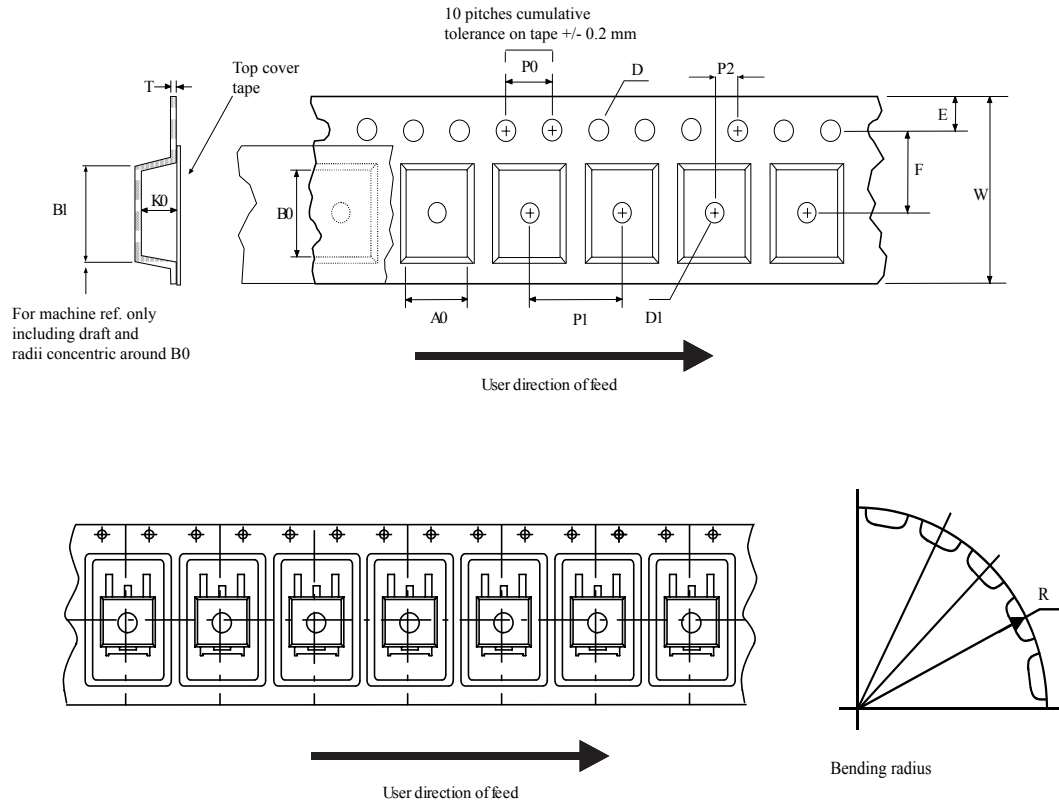
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within  $\oplus 0.05$  A B

FP\_0068772\_34

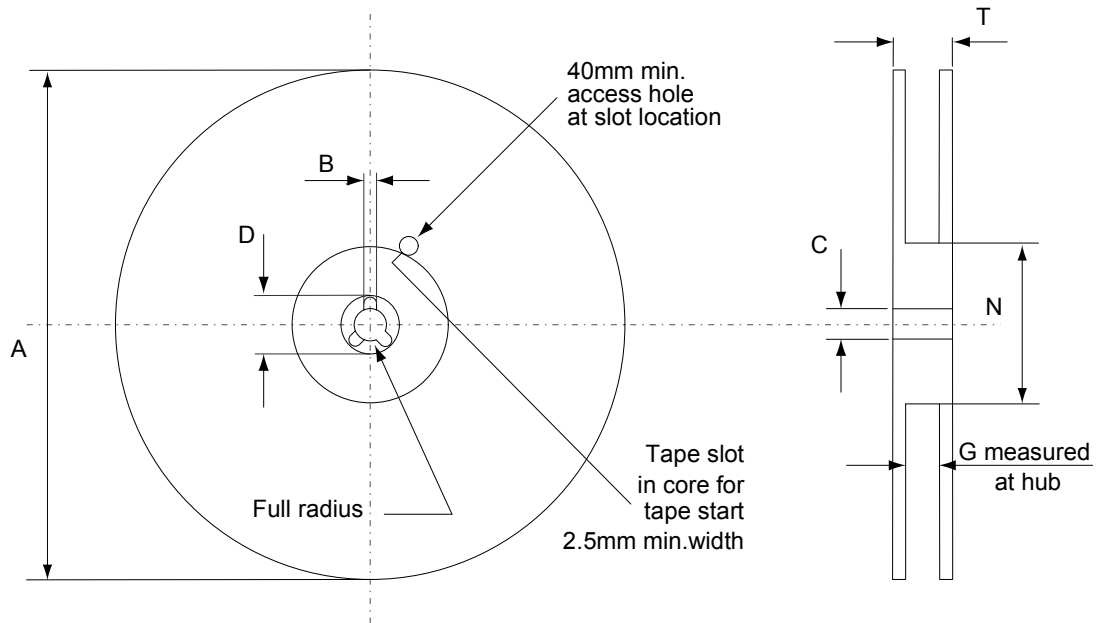
### 4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



AM08852v1

**Figure 23. DPAK (TO-252) reel outline**



AM06038v1

**Table 10. DPAK (TO-252) tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
06-Oct-2004	1	First version
08-Sep-2005	2	Complete version
05-Mar-2006	3	Inserted Ecopack indication
27-Jul-2006	4	New template, no content change
28-Jun-2018	5	Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, <i>Section 1 Electrical ratings</i> , <i>Section 2 Electrical characteristics</i> and <i>Section 4 Package information</i> . Minor text changes.
02-Oct-2023	6	The part numbers STD2NK90Z-1 and STP2NK90Z have been moved to a separate datasheet and the document has been updated accordingly. Updated title on cover page. Removed " <i>Table 8. Gate-source Zener diode</i> ". Removed " <i>Section 4.2 DPAK (TO-252) type A2 package information</i> ", replaced " <i>Section 4.3 DPAK (TO-252) type A2 package information</i> " with <a href="#">Section 4.1 DPAK (TO-252) type C3 package information</a> and updated <a href="#">Section 4.2 DPAK (TO-252) type E package information</a> . Minor text changes.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	DPAK (TO-252) type C3 package information .....	<b>8</b>
<b>4.2</b>	DPAK (TO-252) type E package information .....	<b>10</b>
<b>4.3</b>	DPAK (TO-252) packing information .....	<b>13</b>
	<b>Revision history</b> .....	<b>15</b>



**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved

单击下面可查看定价，库存，交付和生命周期等信息

[>>STMicro\(意法半导体\)](#)