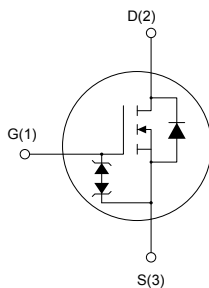


Automotive-grade N-channel 600 V, 37 mΩ typ., 66 A, MDmesh™ DM2 Power MOSFET in a TO-247 long leads package




TO-247 long leads



AM01476v1_No_tab

Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D | P_{TOT} |
|----------------|----------|-------------------|-------|-----------|
| STWA72N60DM2AG | 600 V | 42 mΩ | 66 A | 446 W |

- AEC-Q101 qualified 
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STWA72N60DM2AG](#)

Product summary

| | |
|-------------------|-------------------|
| Order code | STWA72N60DM2AG |
| Marking | 72N60DM2 |
| Package | TO-247 long leads |
| Packing | Tube |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| I_D | Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$ | 66 | A |
| | Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$ | 42 | |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 220 | A |
| P_{TOT} | Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$ | 446 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 50 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature range | | |

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 66\text{ A}$, $di/dt=800\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$. $V_{DD} = 80\% V_{(BR)DSS}$.
3. $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 0.28 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 50 | |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 8 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 1500 | mJ |

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------------------------------|---|------|------|---------|------------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage | $V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$ | | | 10 | μA |
| | | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{C}} = 125\text{ }^{\circ}\text{C}^{(1)}$ | | | 100 | |
| I_{GSS} | Gate-body leakage current | $V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$ | | | ± 5 | μA |
| $V_{\text{GS}(\text{th})}$ | Gate threshold voltage | $V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{\text{DS}(\text{on})}$ | Static drain-source on-resistance | $V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 33\text{ A}$ | | 37 | 42 | $\text{m}\Omega$ |

1. Defined by design, not subject to production test.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|--|------|------|------|-------------|
| C_{iss} | Input capacitance | $V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$ | - | 5508 | - | pF |
| C_{oss} | Output capacitance | | - | 241 | - | |
| C_{riss} | Reverse transfer capacitance | | - | 2.8 | - | |
| $C_{\text{oss eq.}}^{(1)}$ | Equivalent output capacitance | $V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$ | - | 470 | - | pF |
| R_{G} | Intrinsic gate resistance | $f = 1\text{ MHz}$ open drain | - | 2 | - | Ω |
| Q_{g} | Total gate charge | $V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 66\text{ A}$, $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior) | - | 121 | - | nC |
| Q_{gs} | Gate-source charge | | - | 26 | - | |
| Q_{gd} | Gate-drain charge | | - | 61 | - | |

1. $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|---------------------|--|------|------|------|-------------|
| $t_{\text{d}(\text{on})}$ | Turn-on delay time | $V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 33\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 32 | - | ns |
| t_{r} | Rise time | | - | 67 | - | |
| $t_{\text{d}(\text{off})}$ | Turn-off delay time | | - | 112 | - | |
| t_{f} | Fall time | | - | 10.4 | - | |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|---|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 66 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 220 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 66\text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 66\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 480\text{ V}$ | - | 150 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 0.75 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 10.5 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 66\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 480\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ | - | 250 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.5 | | μC |
| I_{RRM} | Reverse recovery current | | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 20.7 | |

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

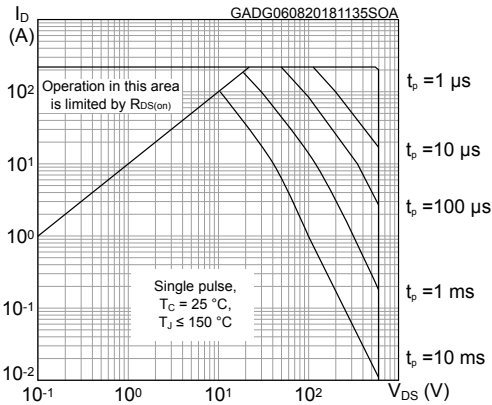


Figure 2. Thermal impedance

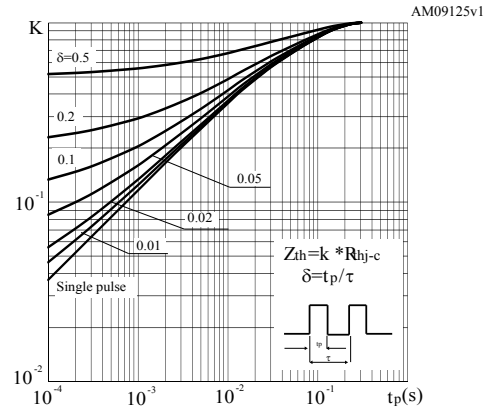


Figure 3. Output characteristics

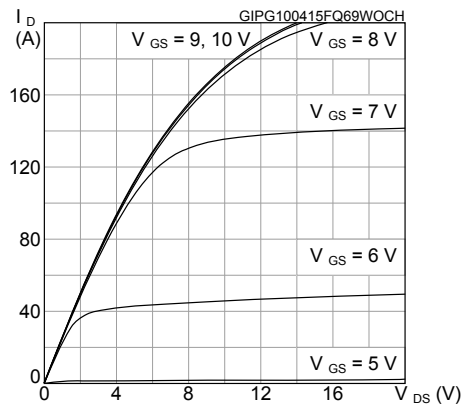


Figure 4. Transfer characteristics

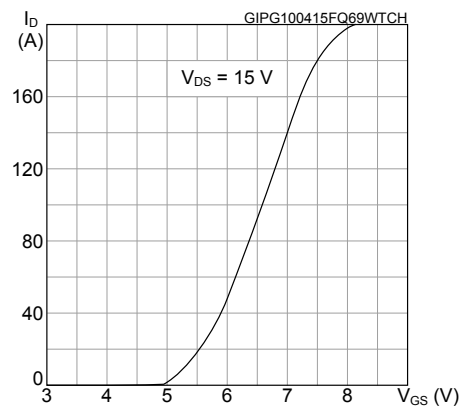


Figure 5. Gate charge vs gate-source voltage

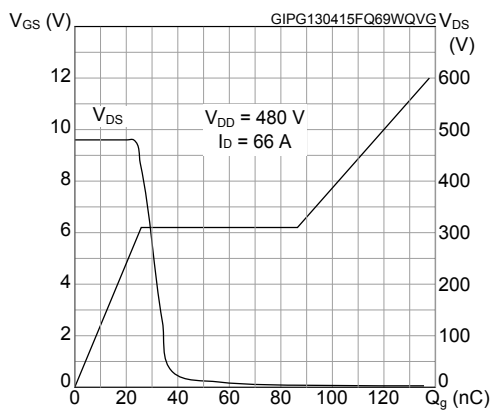


Figure 6. Static drain-source on-resistance

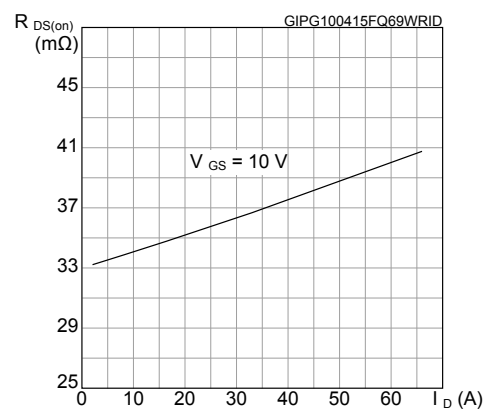


Figure 7. Capacitance variations

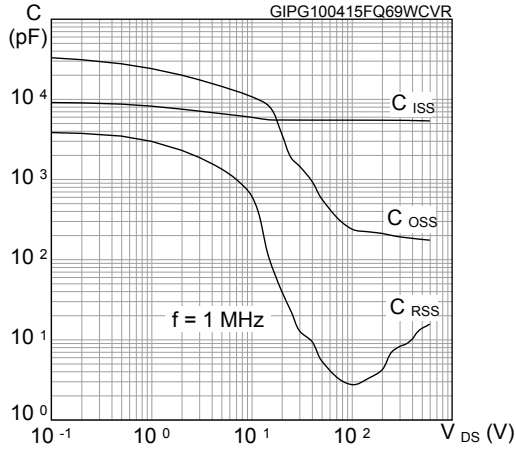


Figure 8. Normalized gate threshold voltage vs temperature

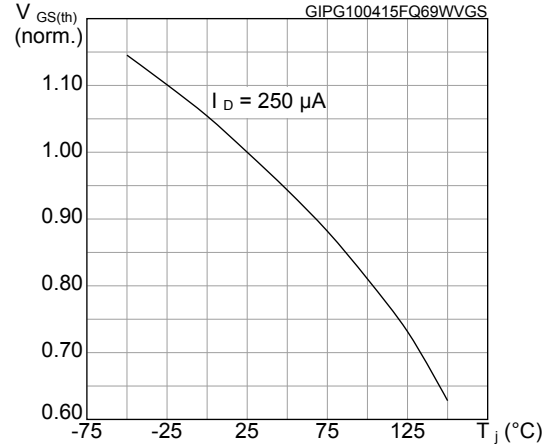


Figure 9. Normalized on-resistance vs temperature

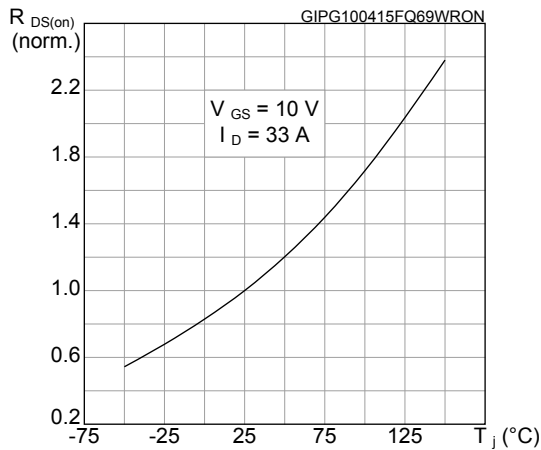


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

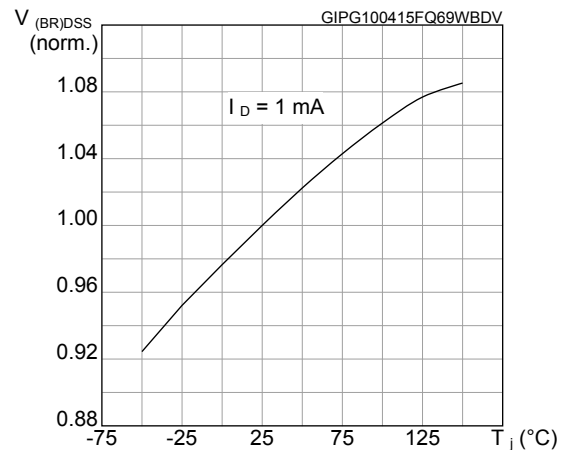


Figure 11. Output capacitance stored energy

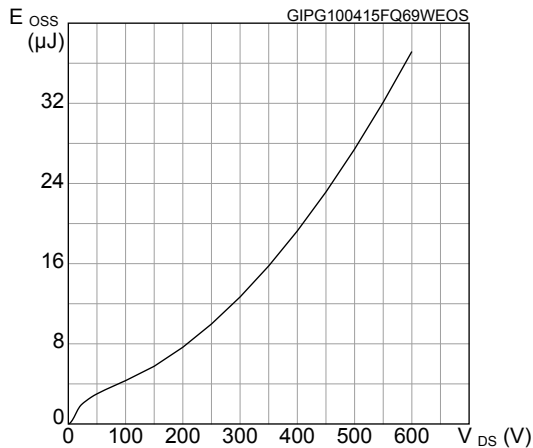
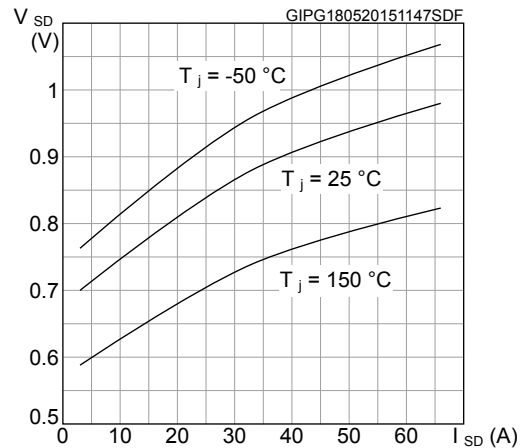
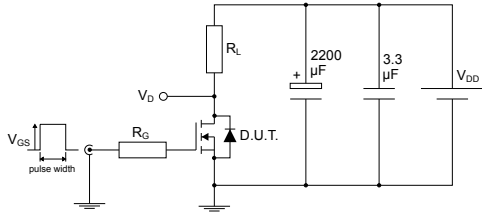


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times


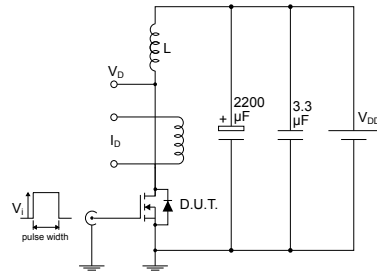
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Figure 14. Test circuit for gate charge behavior


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Figure 15. Test circuit for inductive load switching and diode recovery times

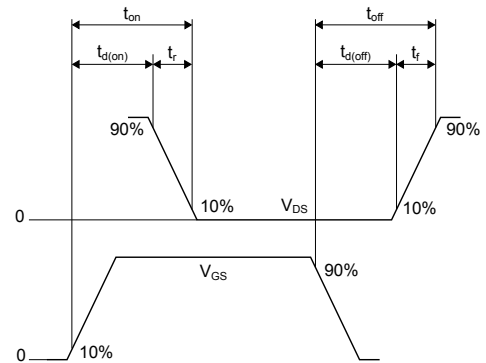

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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


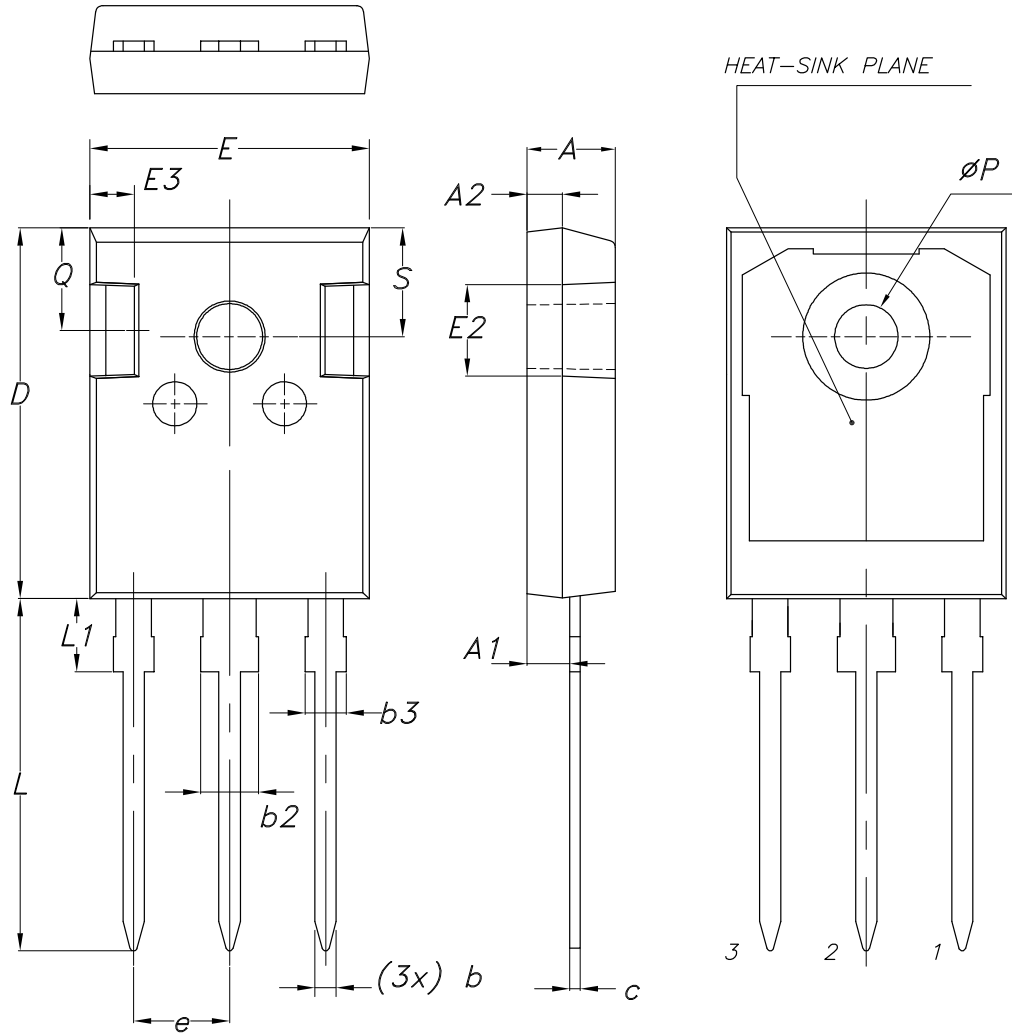
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline



8463846_2_F

Table 8. TO-247 long leads package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.90 | 5.00 | 5.10 |
| A1 | 2.31 | 2.41 | 2.51 |
| A2 | 1.90 | 2.00 | 2.10 |
| b | 1.16 | | 1.26 |
| b2 | | | 3.25 |
| b3 | | | 2.25 |
| c | 0.59 | | 0.66 |
| D | 20.90 | 21.00 | 21.10 |
| E | 15.70 | 15.80 | 15.90 |
| E2 | 4.90 | 5.00 | 5.10 |
| E3 | 2.40 | 2.50 | 2.60 |
| e | 5.34 | 5.44 | 5.54 |
| L | 19.80 | 19.92 | 20.10 |
| L1 | | | 4.30 |
| P | 3.50 | 3.60 | 3.70 |
| Q | 5.60 | | 6.00 |
| S | 6.05 | 6.15 | 6.25 |

Revision history

Table 9. Document revision history

| Date | Version | Changes |
|-------------|---------|--|
| 07-Aug-2018 | 1 | Initial release. The document status is production data. |

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