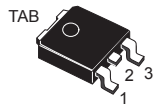
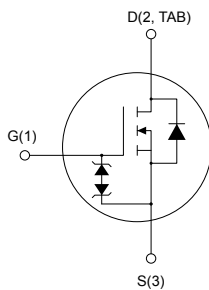


## N-channel 800 V, 13 $\Omega$ typ., 1 A SuperMESH Power MOSFET in a DPAK package



DPAK



AM01476v1\_tab

### Features

Order codes	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD1NK80ZT4	800 V	16 $\Omega$	1

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of  $dv/dt$  capability for the most demanding applications.



#### Product status link

[STD1NK80ZT4](#)

#### Product summary

Order code	STD1NK80ZT4
Marking	D1NK80Z
Package	DPAK
Packing	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	800	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	1	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.63	
$I_{DM}^{(1)}$	Drain current (pulsed)	5	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	1	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 1\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	2.78	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	50	mJ

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified.

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}^{(1)}$			50	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3.0	3.8	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 0.5\text{ A}$		13	16	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	160	-	pF
$C_{oss}$	Output capacitance		-	26	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	6.7	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }640\text{ V}$	-	9.5	-	pF
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}$ , $I_D = 1.1\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	7.7	-	nC
$Q_{gs}$	Gate-source charge		-	1.4	-	nC
$Q_{gd}$	Gate-drain charge		-	4.5	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as the constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 0.55\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	7	-	ns
$t_r$	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time	see (Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	18	-	ns
$t_f$	Fall time		-	28	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		5	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	365		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50 \text{ V}$	-	802		nC
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4.4		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	389		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	891		nC
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

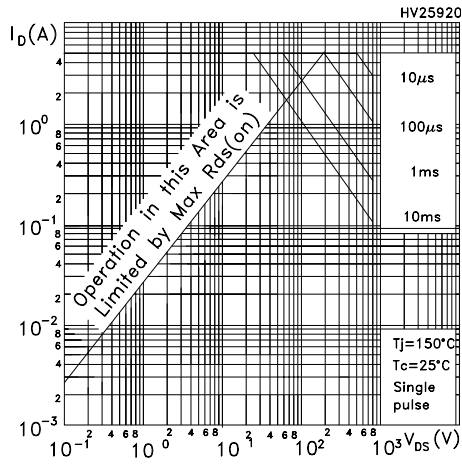


Figure 2. Normalized transient thermal impedance

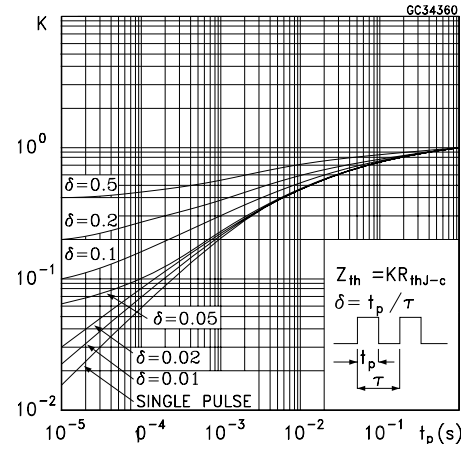


Figure 3. Typical output characteristics

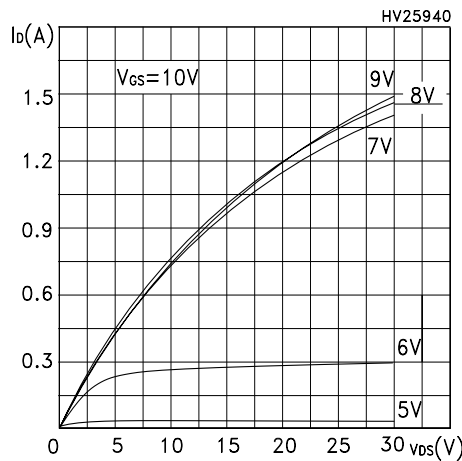


Figure 4. Typical transfer characteristics

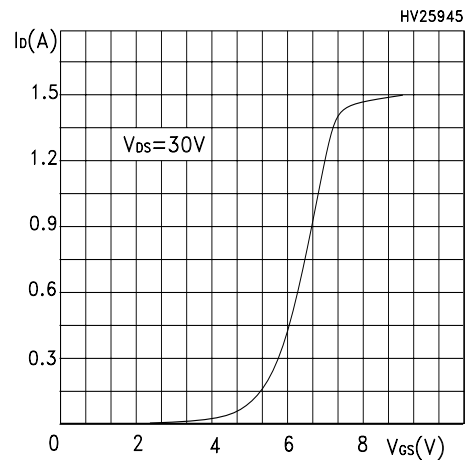


Figure 5. Typical drain-source on-resistance

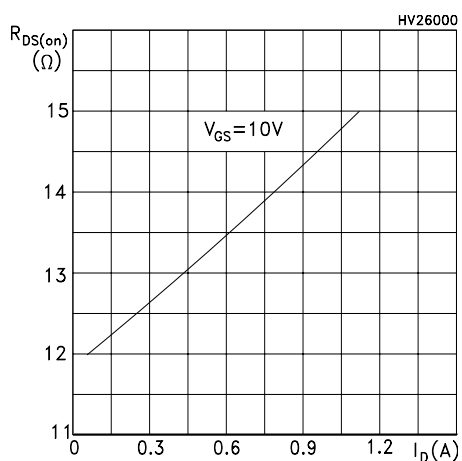
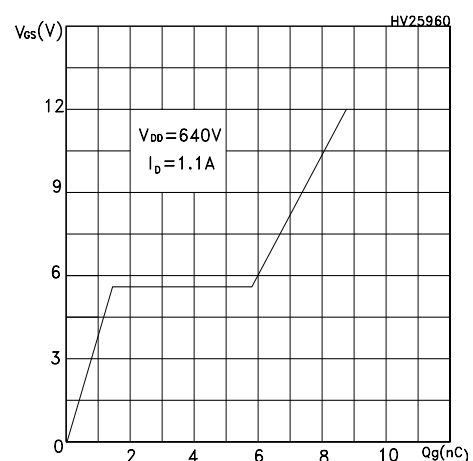
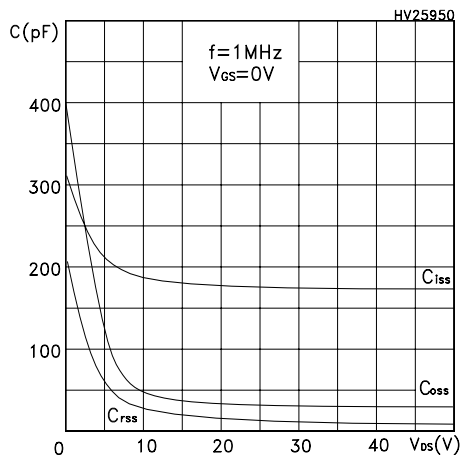


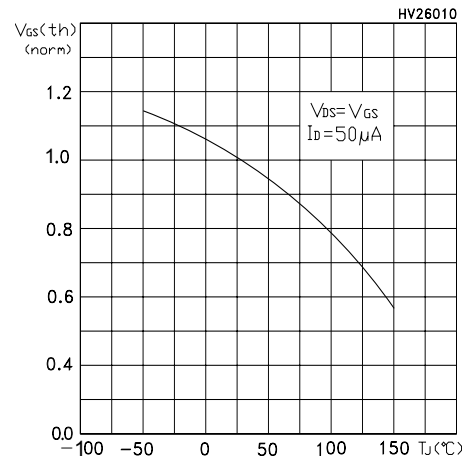
Figure 6. Typical gate charge characteristics



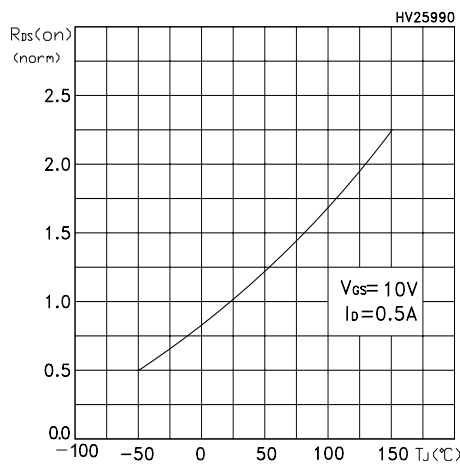
**Figure 7. Typical capacitance characteristics**



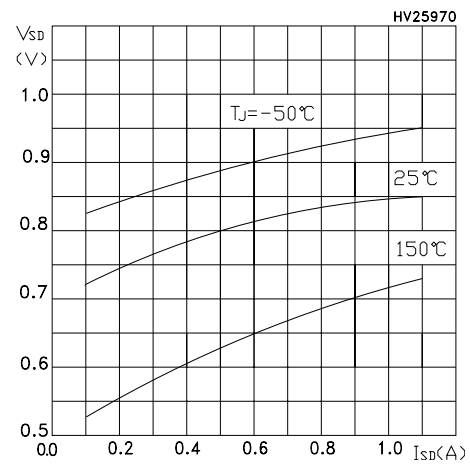
**Figure 8. Normalized gate threshold vs temperature**



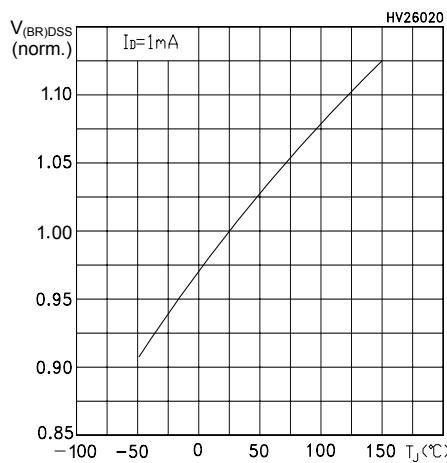
**Figure 9. Normalized on-resistance vs temperature**



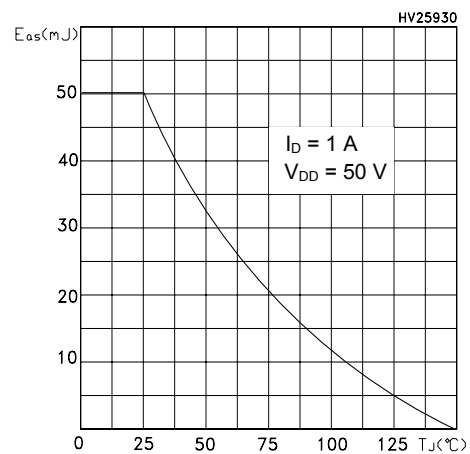
**Figure 10. Typical reverse diode forward characteristics**



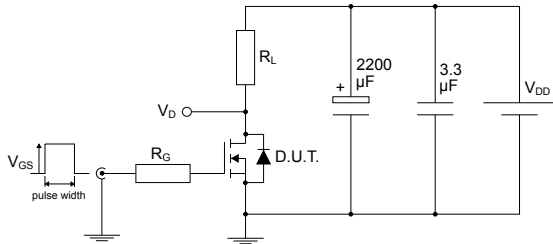
**Figure 11. Normalized breakdown voltage vs temperature**



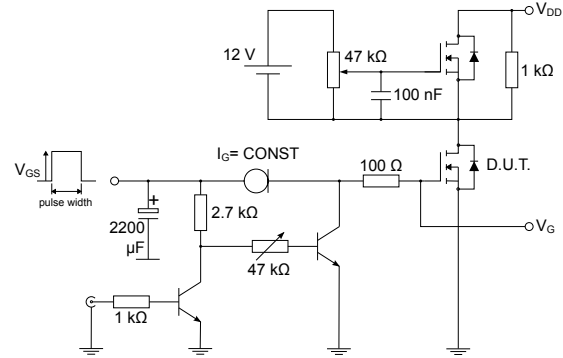
**Figure 12. Maximum avalanche energy vs temperature**



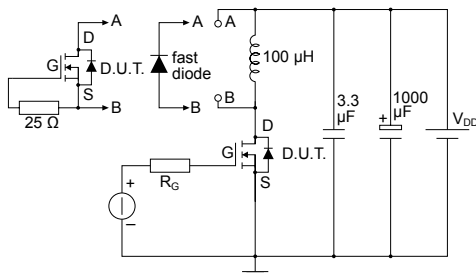
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


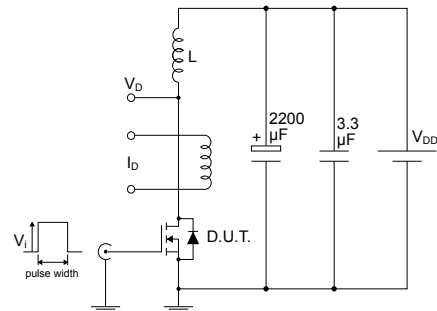
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


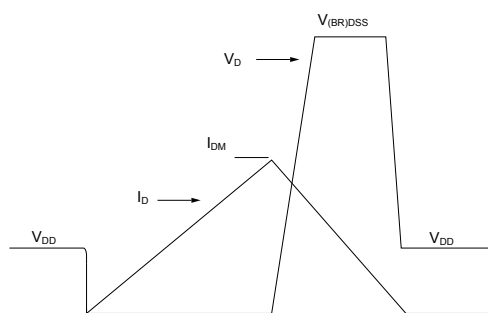
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


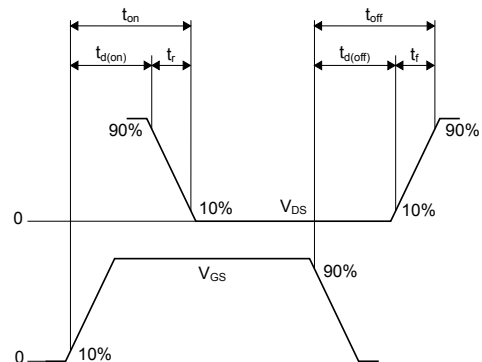
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


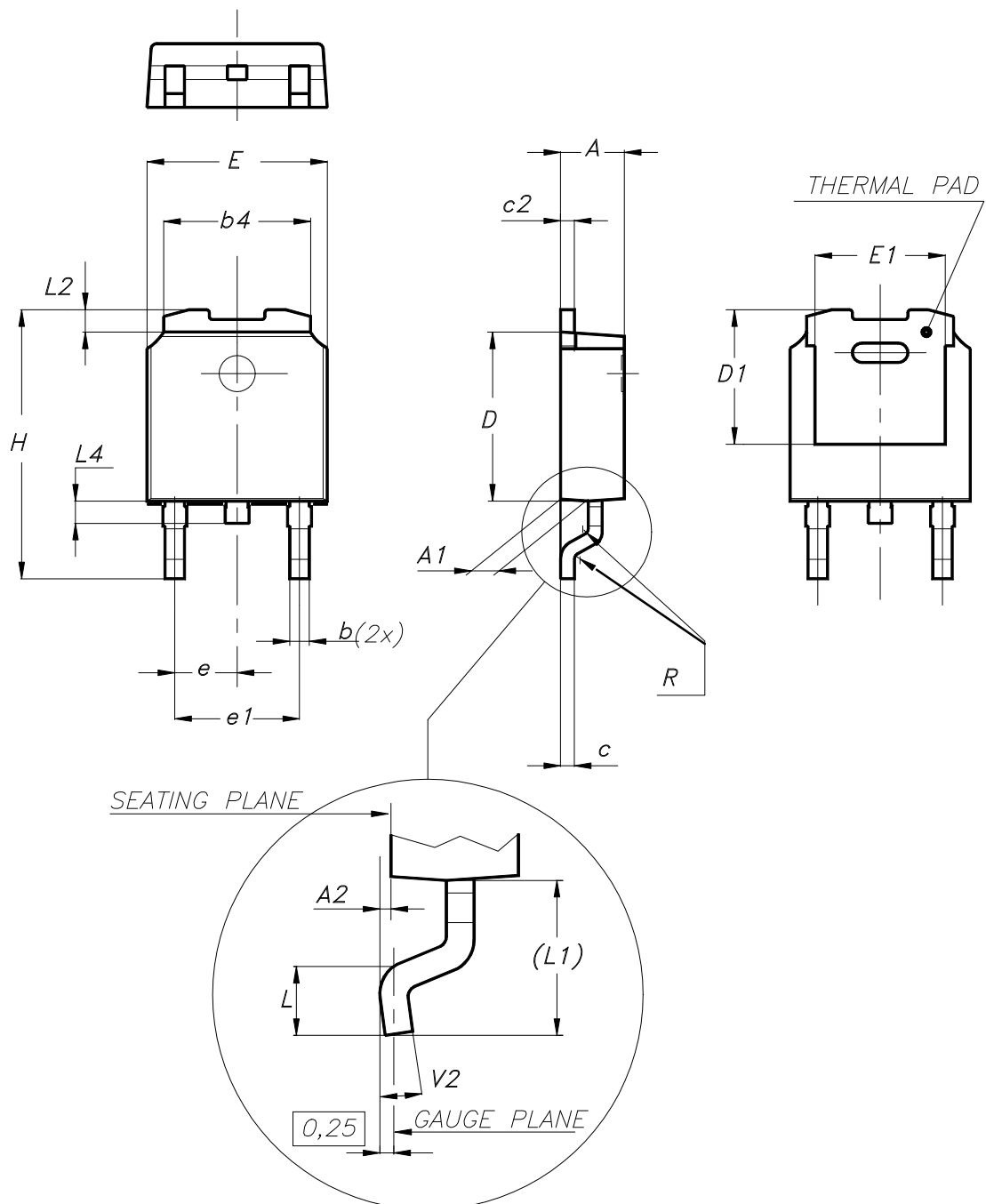
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) package information

Figure 19. DPAK (TO-252) type A package outline



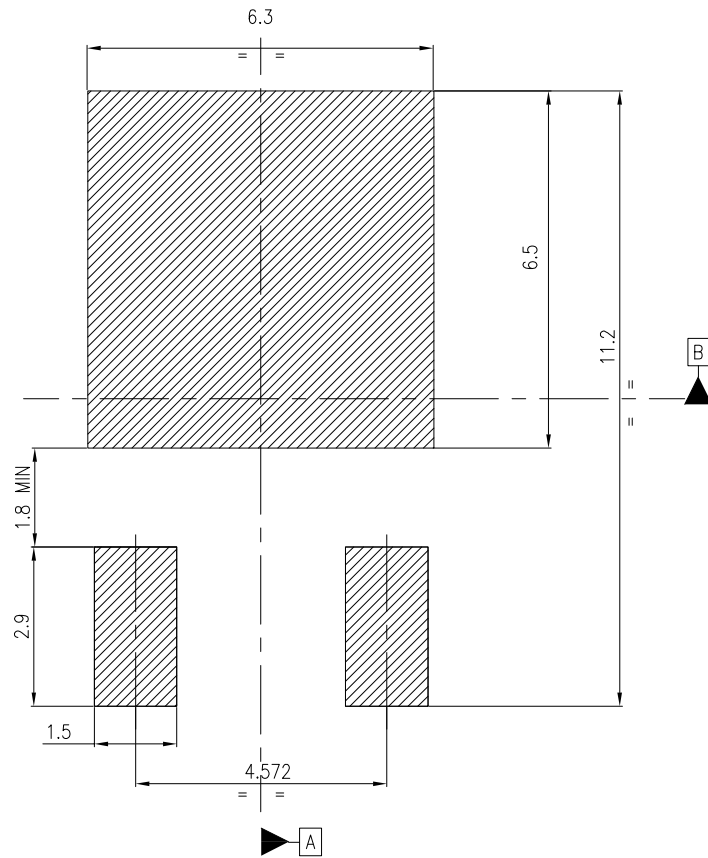
0068772\_A\_33



**Table 8. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



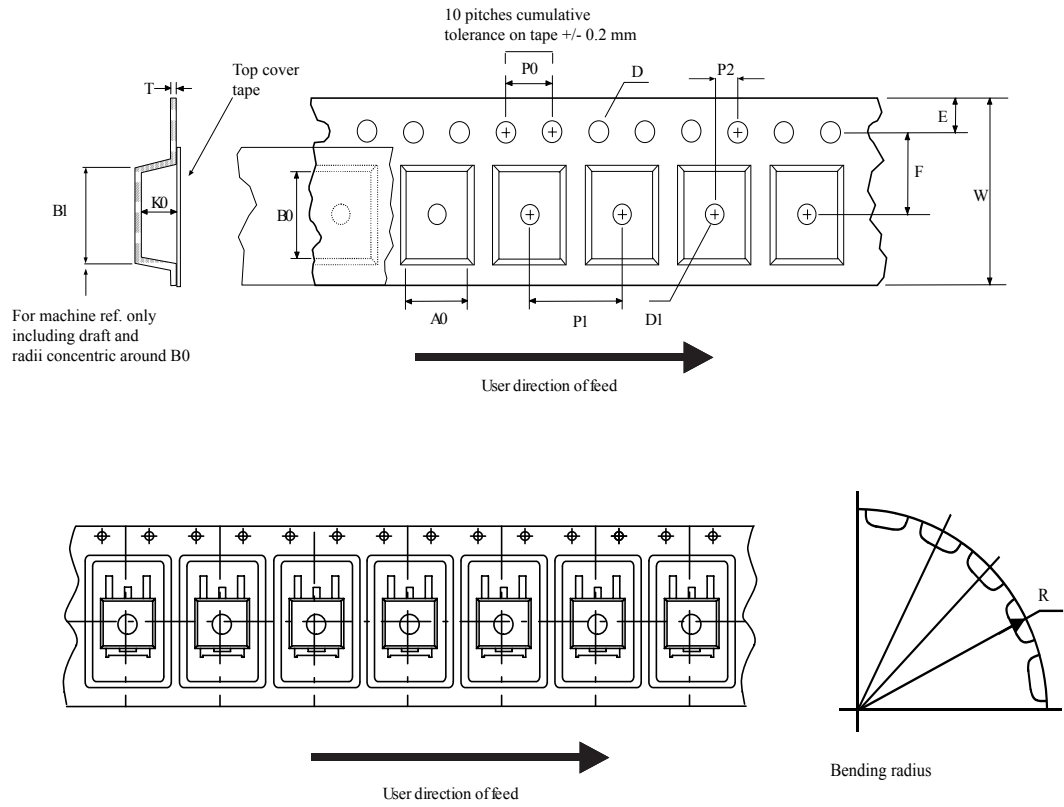
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within  $\boxed{\oplus 0.05 \text{ A B}}$

FP\_0068772\_33

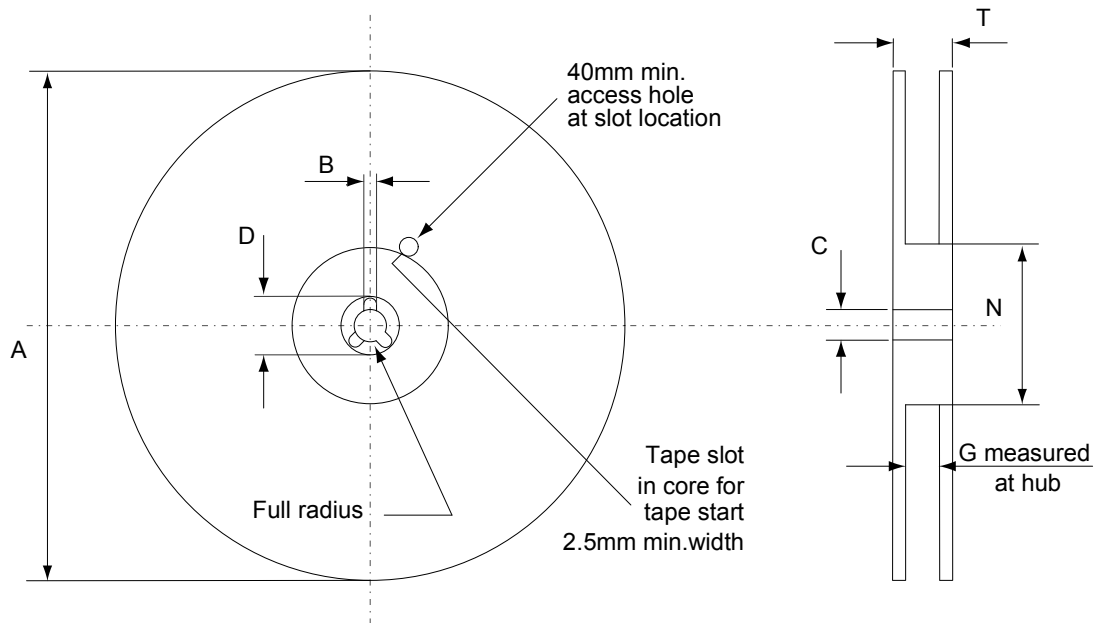
## 4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
08-Jun-2005	1	First release.
06-Sep-2005	2	Inserted Ecopack indication
16-Jan-2006	3	Corrected value on <i>Table 3</i>
13-Mar-2023	4	The part numbers STN1NK80Z and STQ1NK80ZR-AP have been moved to a separate datasheet and the document has been updated accordingly.

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