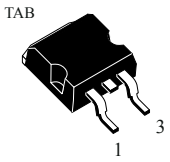
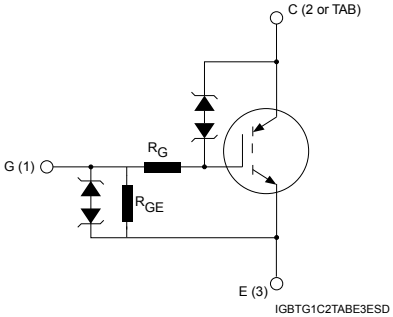
STGB18N40LZT4

Datasheet

Automotive-grade 390 V internally clamped IGBT E_{SCIS} 180 mJ



D²PAK



Features

- AEC-Q101 qualified
- SCIS energy of 180 mJ @ T_C = 150 °C, L = 3 mH
- Parts are 100% tested in SCIS
- ESD gate-emitter protection
- Gate-collector high voltage clamping
- Logic level gate drive
- Very low saturation voltage
- High pulsed current capability
- Gate and gate-emitter resistor

Applications

- Pencil coil electronic ignition driver

Description

This application-specific IGBT utilizes the most advanced PowerMESH technology optimized for coil driving in the harsh environment of automotive ignition systems. The device show very low on-state voltage and very high SCIS energy capability over a wide operating temperature range. Moreover, ESD-protected logic level gate input and an integrated gate resistor means no external protection circuitry is required.

Product status link
STGB18N40LZT4

Product summary	
Order code	STGB18N40LZT4
Marking	GB18N40LZ
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	$V_{CES(clamped)}$	V
V_{ECS}	Emitter-collector voltage (V_{GE} = 0 V)	20	V
I_C	Continuous collector current at T_C = 100 °C	30	A
I_{CP} (1)	Pulsed collector current	40	A
V_{GE}	Gate-emitter voltage	$V_{GE(clamped)}$	V
P_{TOT}	Total power dissipation at T_C = 25 °C	150	W
E_{SCIS} (2)	Single pulse energy T_C = 25 °C, L = 3 mH, V_{CC} = 50 V	300	mJ
	Single pulse energy T_C = 150 °C, L = 3 mH, V_{CC} = 50 V	180	mJ
ESD	Human body model, R = 1.5 kΩ, C = 100 pF	8	kV
	Machine model, R = 0, C = 100 pF	800	V
	Charged device model	2	kV
T_{STG}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by max. junction temperature.*
2. *For E_{SCIS} test circuit refer to Figure 14. Test circuit for inductive load switching with A and B not connected.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CES(clamped)}$	Collector-emitter clamped voltage	I_C = 2 mA, V_{GE} = 0 V, T_J= - 40 °C to 175 °C	360	390	420	V
$V_{(BR)ECS}$	Emitter-collector break-down voltage	V_{GE} = 0 V, I_C = 75 mA	20	28		V
$V_{GE(clamped)}$	Gate-emitter clamped voltage	I_G = ±2 mA	12		16	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 4.5 V, I_C = 10 A		1.35	1.7	V
		V_{GE} = 4.5 V, I_C = 10 A, T_J = 150 °C		1.30		V
		V_{GE} = 3.8 V, I_C = 6 A		1.30		V
$V_{GE(th)}$	Gate-threshold voltage	V_{GE} = V_{CE}, I_C = 1 mA, T_J = -40 °C	1.4			V
		V_{GE} = V_{CE}, I_C = 1 mA	1.2	1.6	2.3	V
		V_{GE} = V_{CE}, I_C = 1 mA, T_J = 150 °C (1)	0.7			V
I_{CES}	Collector cut-off current	V_{CE} = 15 V, V_{GE} = 0 V, T_J = 150 °C (1)			10	µA
		V_{CE} = 200 V, V_{GE} = 0 V, T_J = 150 °C (1)			100	µA
I_{GES}	Gate-emitter leakage current	V_{GE} = ±10 V, V_{CE} = 0 V	450	625	830	µA
R_{GE}	Gate emitter resistance		12	16	22	kΩ
R_G	Gate resistance			1.6		kΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	490	-	pF
C_{oes}	Output capacitance		-	90	-	
C_{res}	Reverse transfer capacitance		-	5	-	
Q_g	Total gate charge	V_{CE} = 280 V, I_C = 10 A, V_{GE} = 0 to 5 V	-	29	-	nC

Table 5. Resistive load switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 14 V, V_{GE} = 5 V,	-	0.65	-	µs
t_r	Current rise time	R_L = 1 Ω	-	3.5	-	µs
$t_{d(on)}$	Turn-on delay time	V_{CC} = 14 V, V_{GE} = 5 V,	-	0.65	-	µs
t_r	Current rise time	R_L= 1 Ω, T_J = 150 °C	-	3.8	-	µs

Table 6. Inductive load switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	V_{CC} = 300 V, L = 1 mH,	-	13.5	-	µs
t_f	Current fall time	I_C = 10 A, V_{GE} = 5 V,	-	5.5	-	µs
dV/dt	Turn-off voltage slope		-	105	-	V/µs
$t_{d(off)}$	Turn-off delay time	V_{CC} = 300 V, L = 1 mH,	-	14.2	-	µs
t_f	Current fall time	I_C = 10 A, V_{GE} = 5 V,	-	8	-	µs
dV/dt	Turn-off voltage slope	T_J = 150 °C	-	97	-	V/µs

2.1 Electrical characteristics (curves)

Figure 1. Collector-emitter on voltage vs temperature

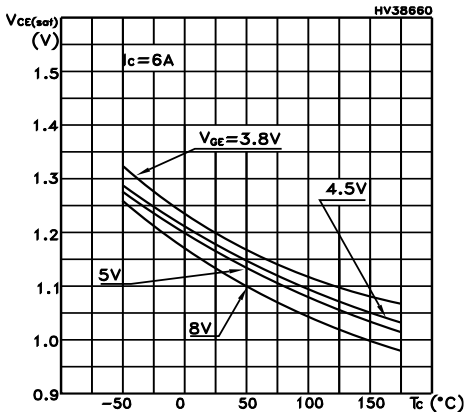


Figure 2. Collector-emitter on voltage vs temperature

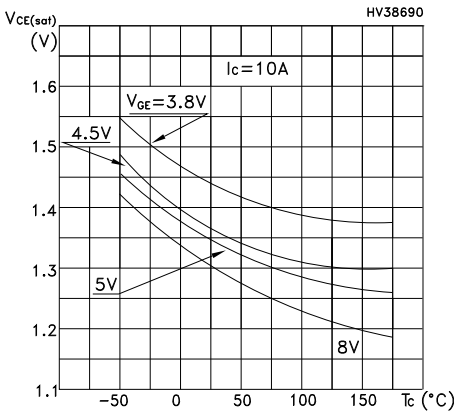


Figure 3. Collector-emitter on voltage vs temperature

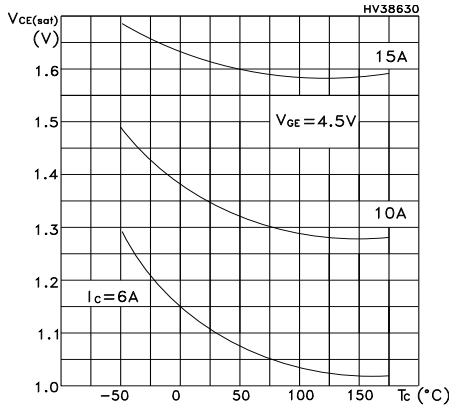


Figure 4. Self clamped inductive switch

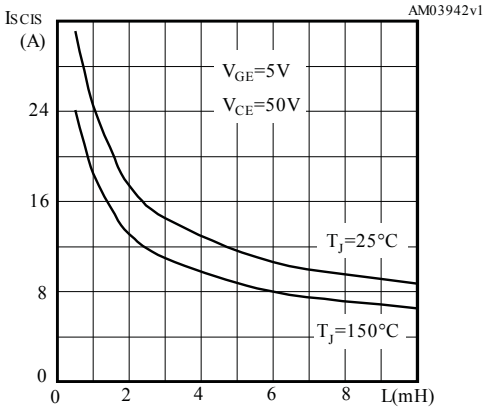


Figure 5. Output characteristics at 25 °C

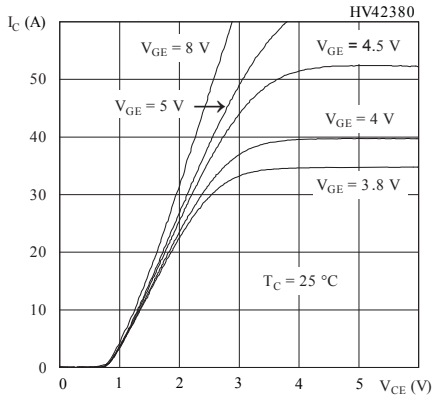


Figure 6. Output characteristics at -40 °C

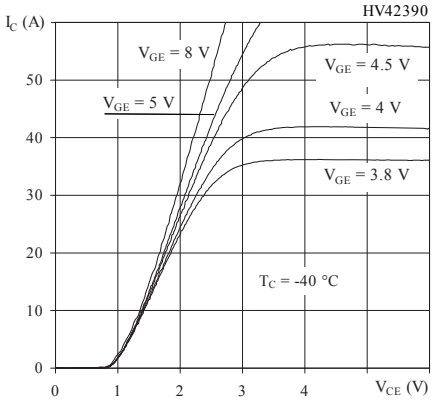


Figure 7. Output characteristics at 175 °C

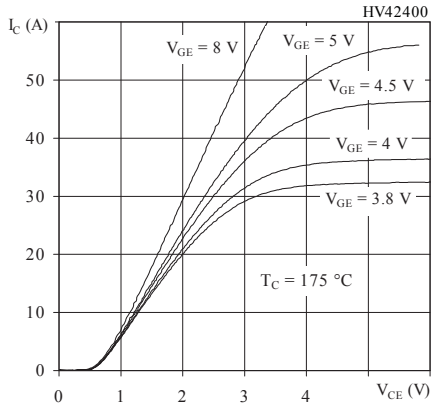


Figure 8. Transfer characteristics

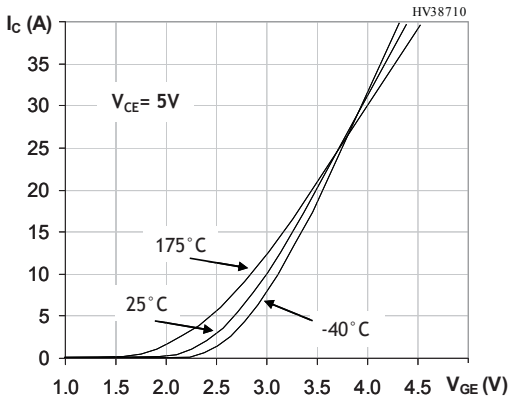


Figure 9. Collector cut-off current vs temperature

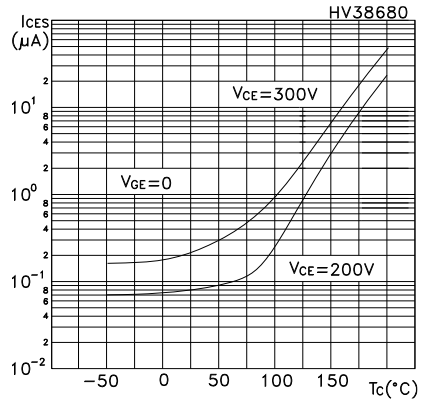


Figure 10. Normalized collector emitter voltage vs temperature

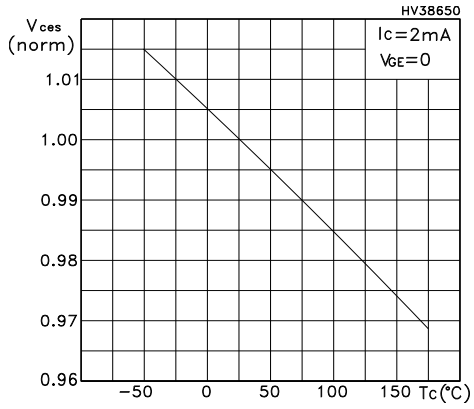


Figure 11. Normalized gate threshold voltage vs temperature

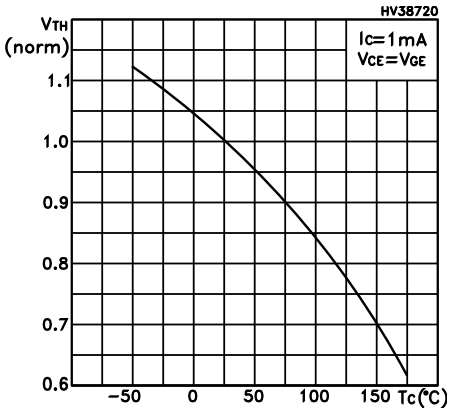


Figure 12. Normalized collector emitter on voltage vs temperature

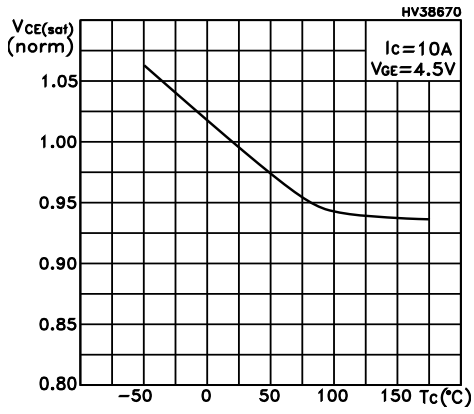
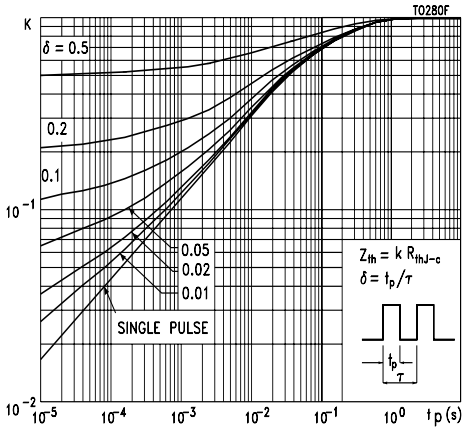


Figure 13. **Thermal impedance**



3 Test circuits

Figure 14. Test circuit for inductive load switching

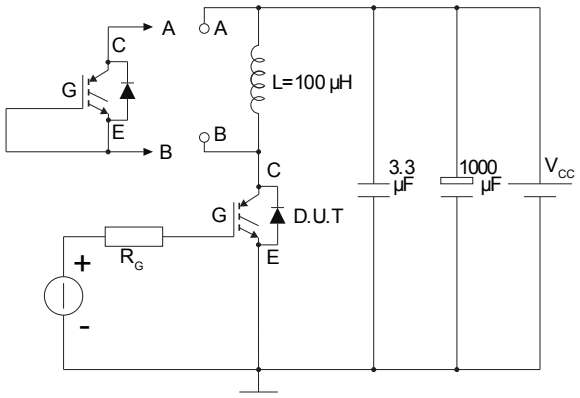


Figure 15. Test circuit for resistive load switching

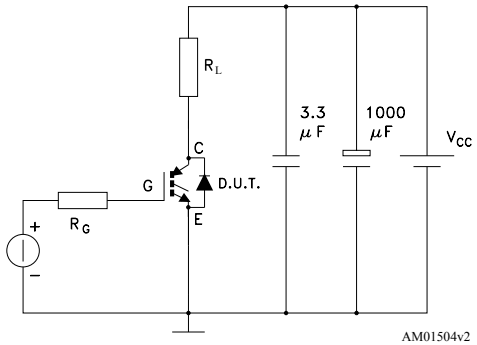


Figure 16. Gate charge test circuit

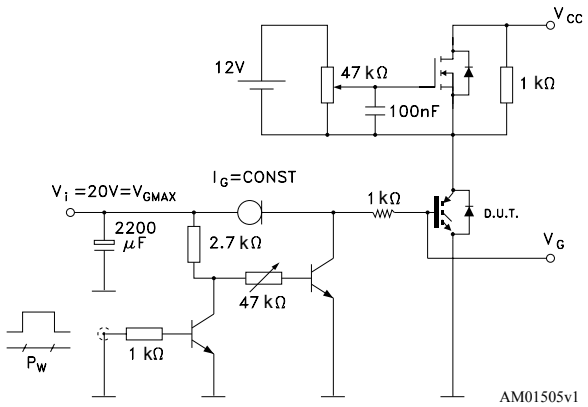
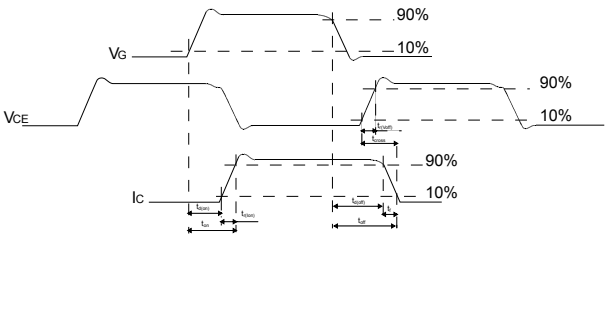


Figure 17. Switching waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 18. **D²PAK (TO-263) type A package outline**

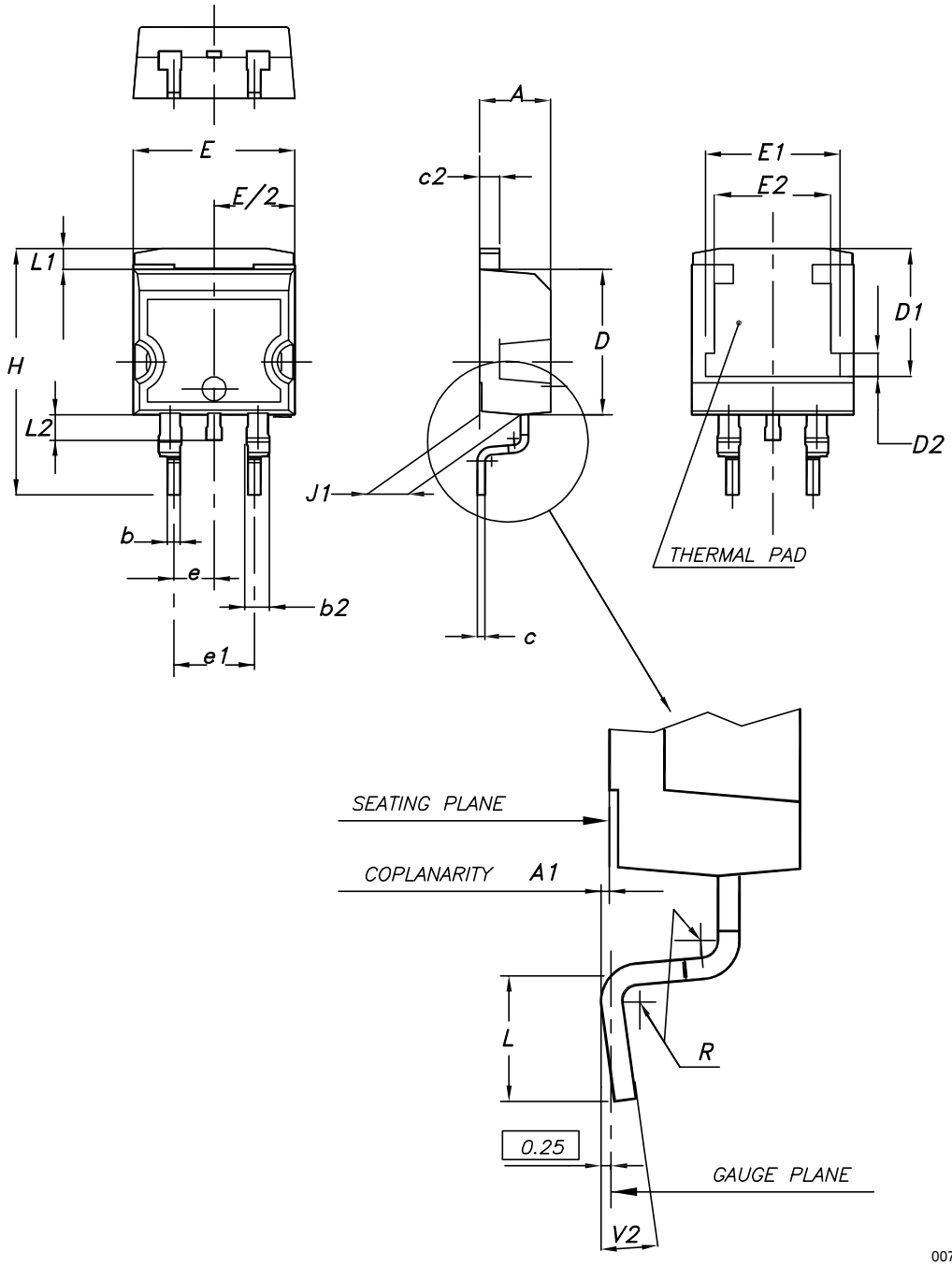
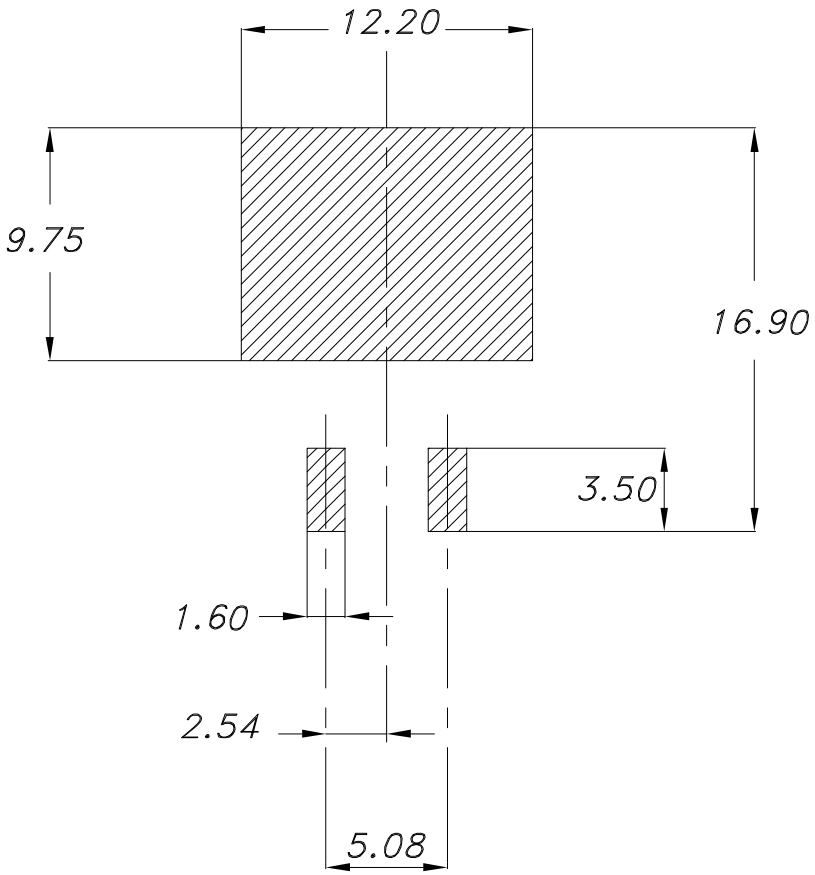


Table 7. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 19. **D²PAK (TO-263) recommended footprint (dimensions are in mm)**



4.2 D²PAK packing information

Figure 20. D²PAK tape outline

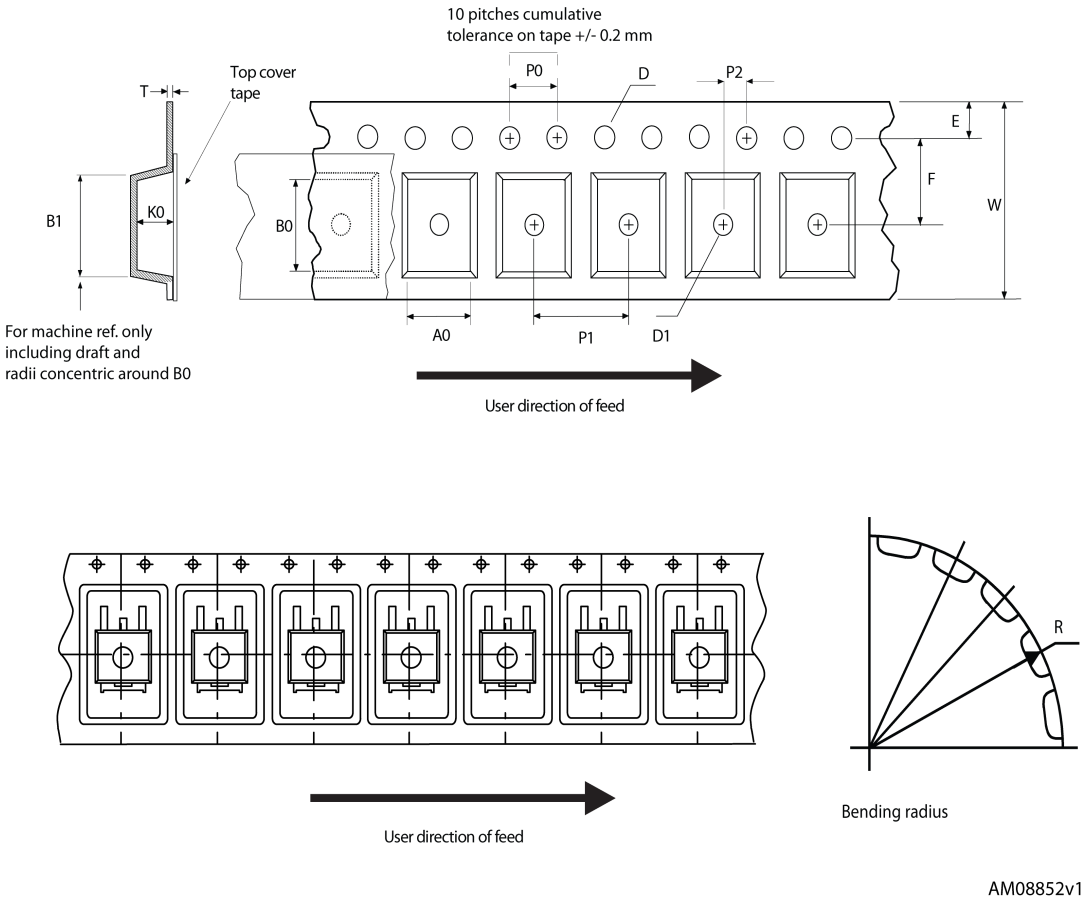


Figure 21. **D²PAK reel outline**

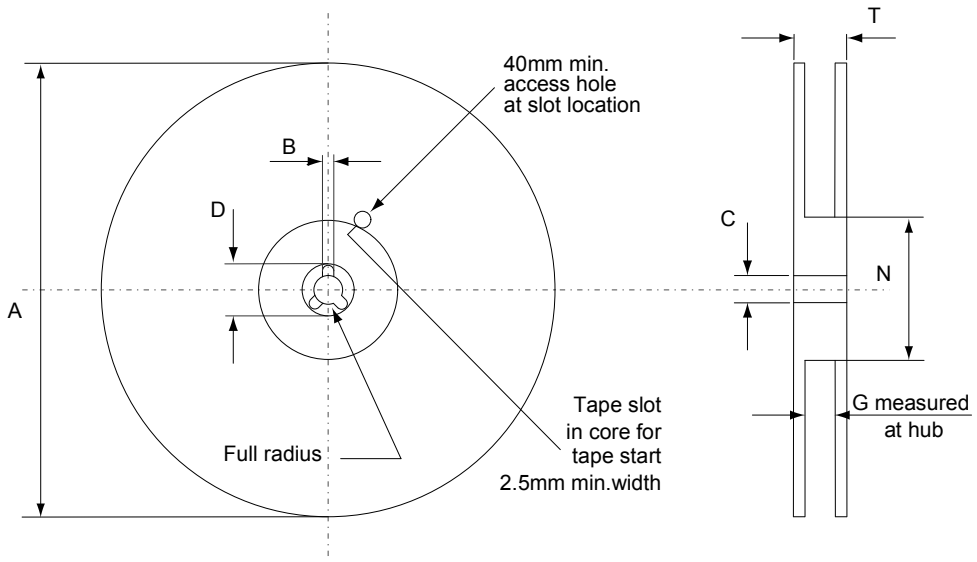


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Table 8. **D²PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
18-Jan-2008	1	Initial release.
07-Mar-2008	2	Modified *Figure 7, Figure 8, Figure 10*.
07-May-2008	3	Modified *Figure 9*
31-Mar-2009	4	Added new package, mechanical data: TO-220
18-May-2009	5	Modified *Figure 5*
12-Nov-2014	6	Updated *Table 1: Device summary, Table 2: Absolute maximum ratings* and *Table 3: Thermal data* Updated *3: Test circuits* Updated *Section 4: Package mechanical data* Updated *Section 5: Packaging mechanical data* Minor text changes
11-Jan-2021	7	The part numbers STGD18N40LZ and STGP18N40LZT4 have been removed. Minor text changes

Contents

单击下面可查看定价，库存，交付和生命周期等信息

>>STMicro(意法半导体)