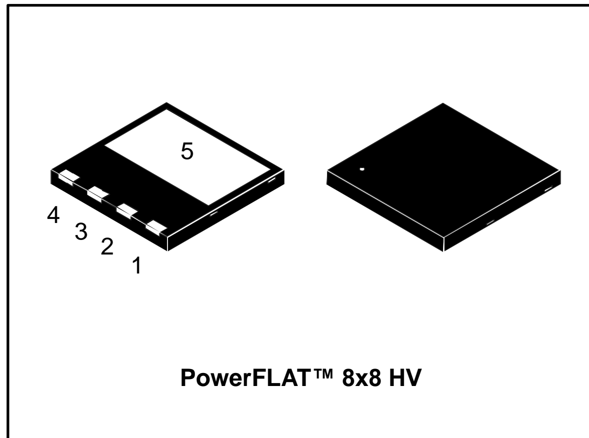
STL33N60DM2

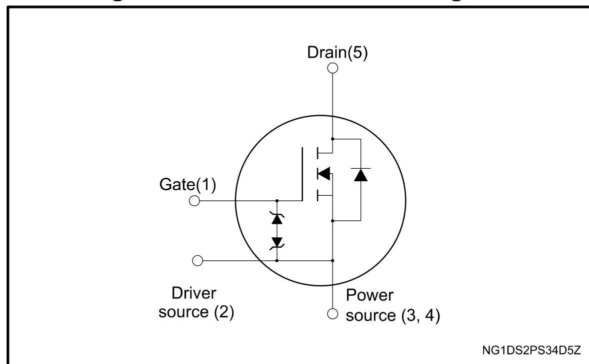
N-channel 600 V, 0.115 Ω typ., 21 A MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$max	I_D
STL33N60DM2	650 V	0.140 Ω	21 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL33N60DM2	33N60DM2	PowerFLAT™ 8x8 HV	Tape and reel

This is information on a product in full production. www.st.com

Downloaded From Oneyac.com

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuits 8

4 Package mechanical data 9

4.1 PowerFLAT™ 8x8 HV package mechanical data 10

4.2 PowerFLAT™ 8x8 HV packing information 12

5 Revision history 14

Downloaded From Oneyac.com

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	21	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	15	A
I_{DM} (1), (2)	Drain current (pulsed)	84	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	150	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	570	mJ
dv/dt (3)	Peak diode recovery voltage slope	50	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)The value is rated according to $R_{thj\text{-}case}$ and limited by package.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 21 A, di/dt ≤ 900 A/μs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V.

(4)V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient max	45	°C/W

Notes:

(1)When mounted on FR-4 board of inch², 2oz Cu.

Downloaded From Oneyac.com

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C=125 °C[(1)]			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 10.5 A		0.115	0.140	Ω

Notes:

[(1)]Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1870	-	pF
C_{oss}	Output capacitance		-	87	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$[(1)]	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	157	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	4.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 21 A V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	43	-	nC
Q_{gs}	Gate-source charge		-	9.8	-	nC
Q_{gd}	Gate-drain charge		-	21.4	-	nC

Notes:

[(1)]Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% V_{DSS}.

Downloaded From Oneyac.com

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 10.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"*)	-	17	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	62	-	ns
t_f	Fall time		-	9	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		21	A
I_{SDM} (1)(2)	Source-drain current (pulsed)		-		84	A
V_{SD} (3)	Forward on voltage	I_{SD} = 21 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	120		ns
Q_{rr}	Reverse recovery charge		-	0.53		µC
I_{RRM}	Reverse recovery current		-	8.8		A
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	316		ns
Q_{rr}	Reverse recovery charge		-	2.85		µC
I_{RRM}	Reverse recovery current		-	18		A

Notes:

(1)The value is rated according to $R_{thj\text{-}case}$ and limited by package.

(2)Pulse width limited by safe operating area

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±250 µA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

Downloaded From Oneyac.com

2.2 Electrical characteristics (curves)

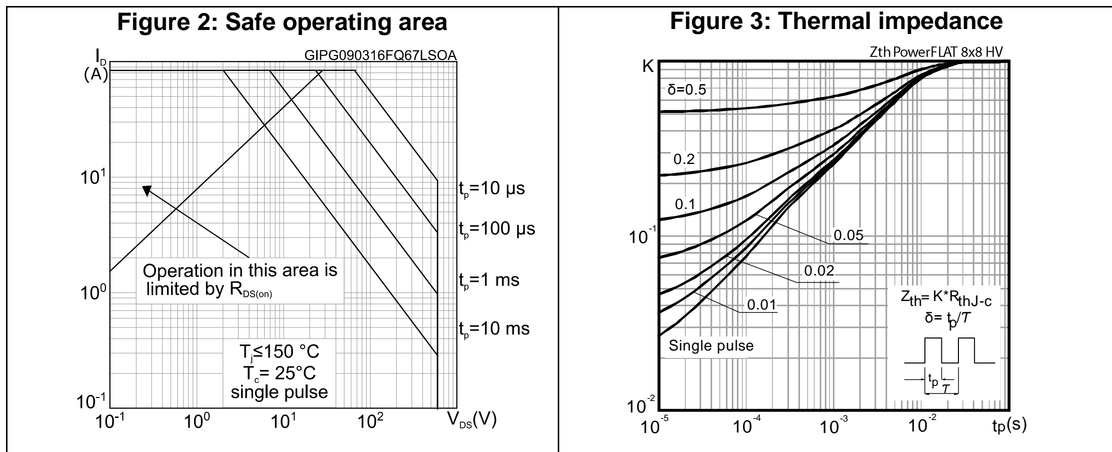


Figure 2: Safe operating area

Figure 3: Thermal impedance

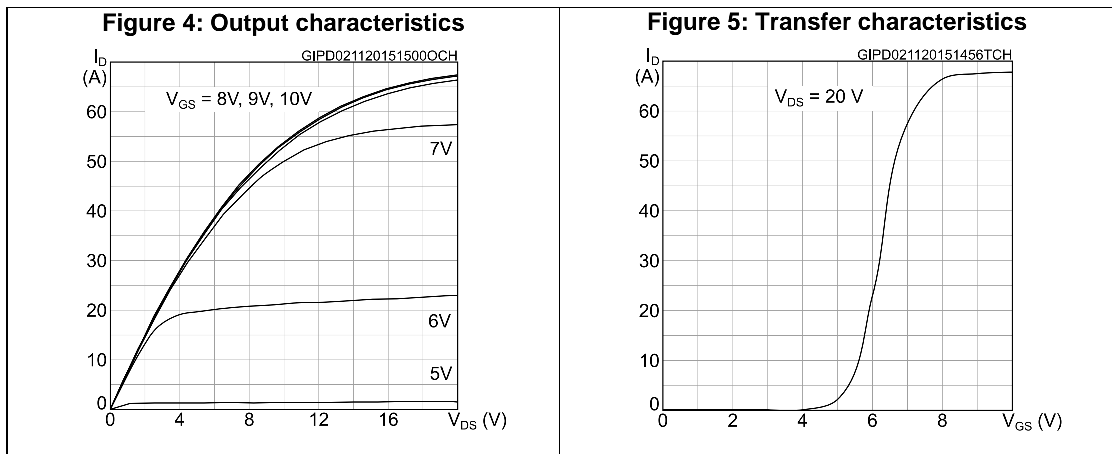


Figure 4: Output characteristics

Figure 5: Transfer characteristics

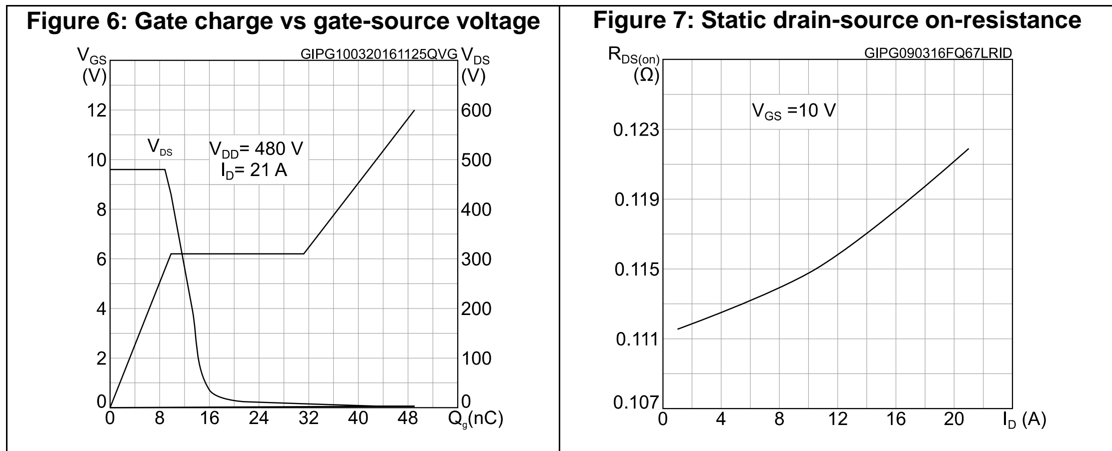


Figure 6: Gate charge vs gate-source voltage

Figure 7: Static drain-source on-resistance

Downloaded From Oneyac.com

Figure 8: Capacitance variations

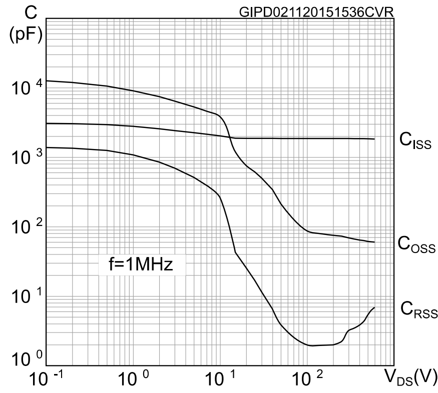


Figure 9: Normalized gate threshold voltage vs temperature

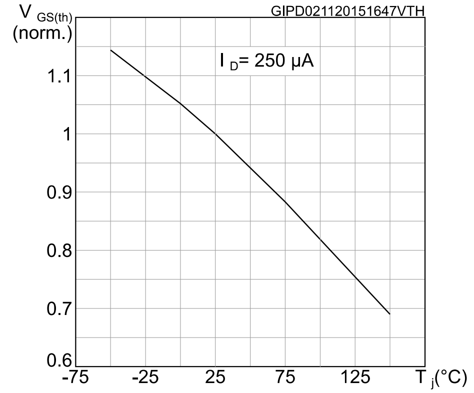


Figure 10: Normalized on-resistance vs temperature

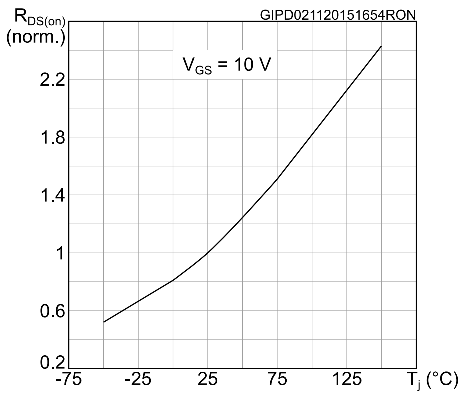


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

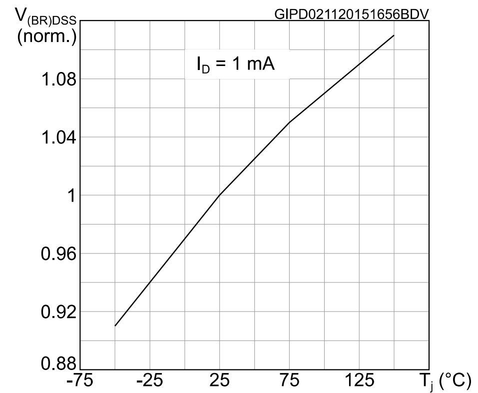


Figure 12: Output capacitance stored energy

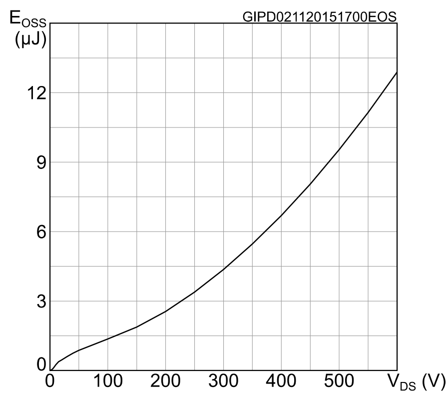
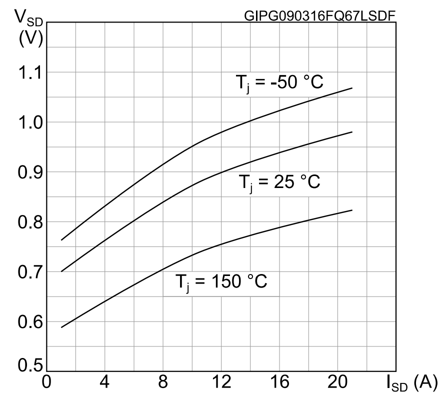


Figure 13: Source- drain diode forward characteristics



Downloaded From Oneyac.com

3 Test circuits

Figure 14: Switching times test circuit for resistive load

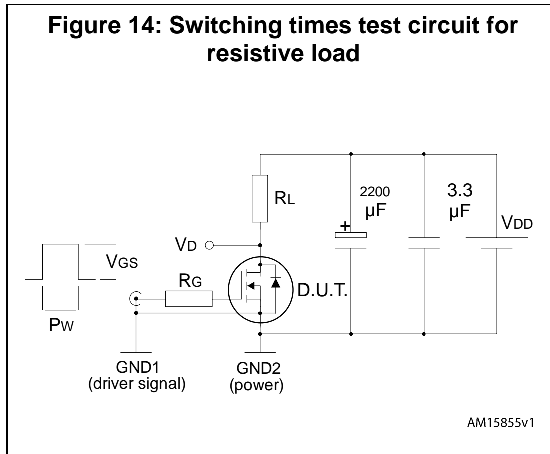


Figure 15: Gate charge test circuit

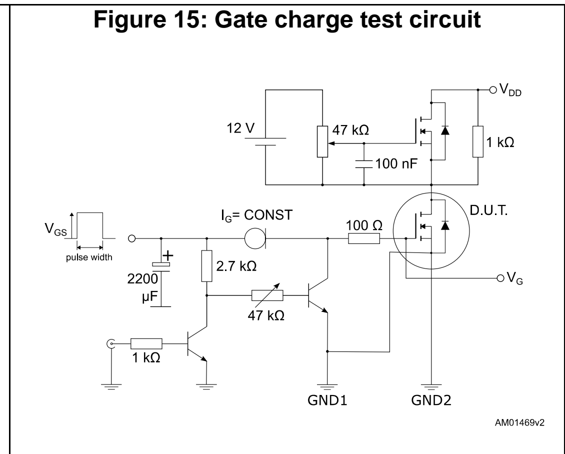


Figure 16: Test circuit for inductive load switching and diode recovery times

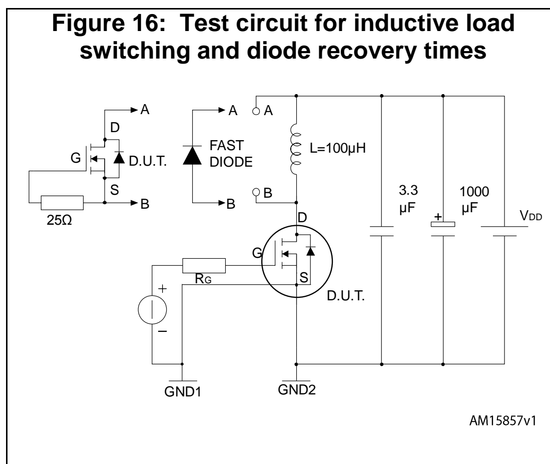


Figure 17: Unclamped inductive load test circuit

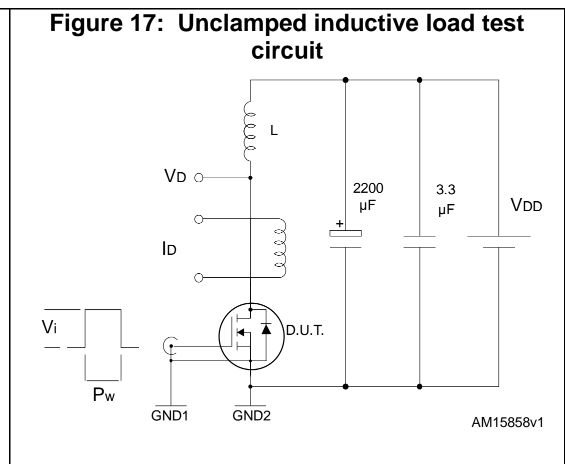


Figure 18: Unclamped inductive waveform

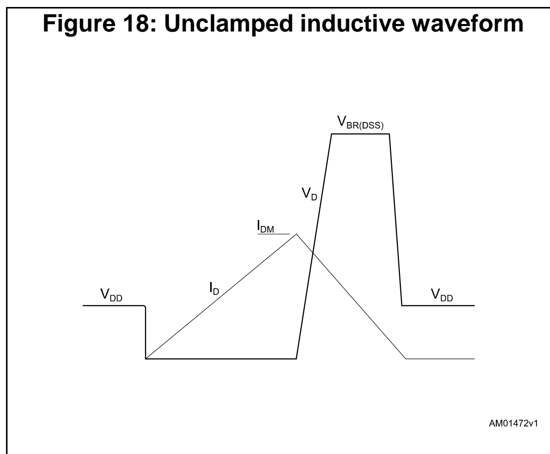
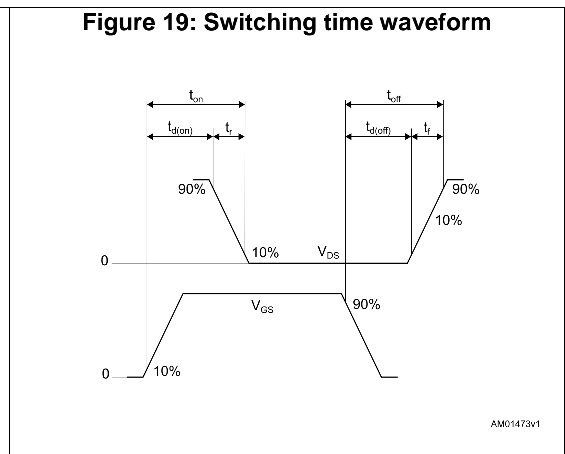


Figure 19: Switching time waveform



Downloaded From Oneyac.com

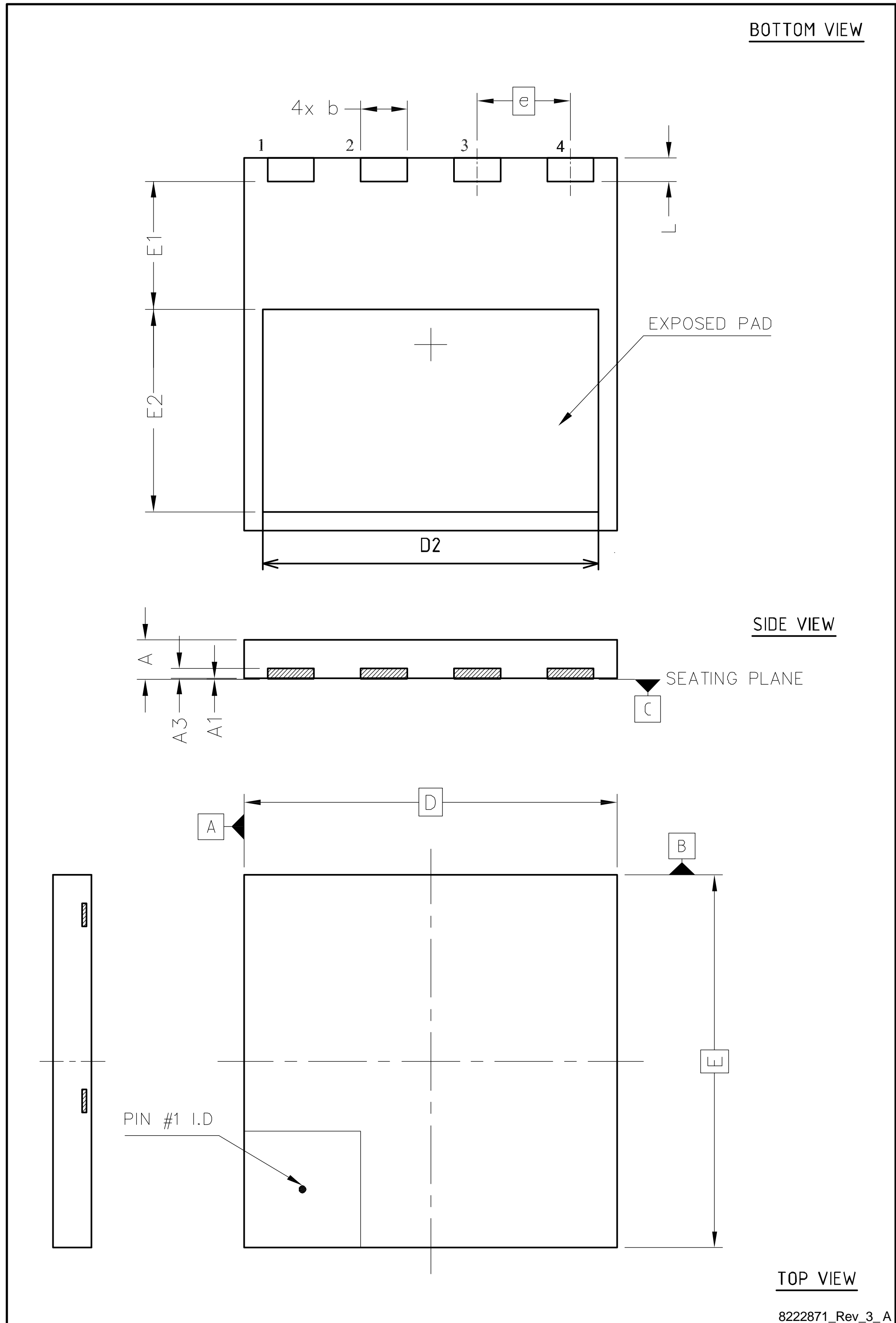
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

Downloaded From Oneyac.com

4.1 PowerFLAT™ 8x8 HV package mechanical data

Figure 20: PowerFLAT™ 8x8 HV package outline

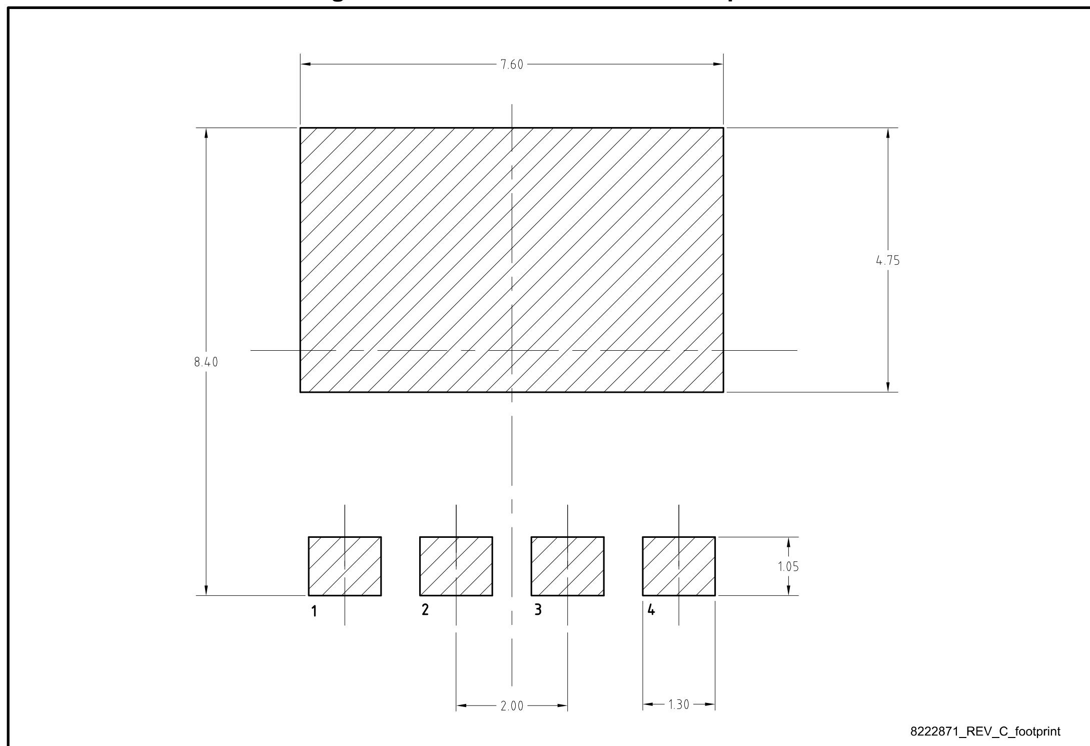


Downloaded From Oneyac.com

Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

Downloaded From Oneyac.com

4.2 PowerFLAT™ 8x8 HV packing information

Figure 22: PowerFLAT™ 8x8 HV tape

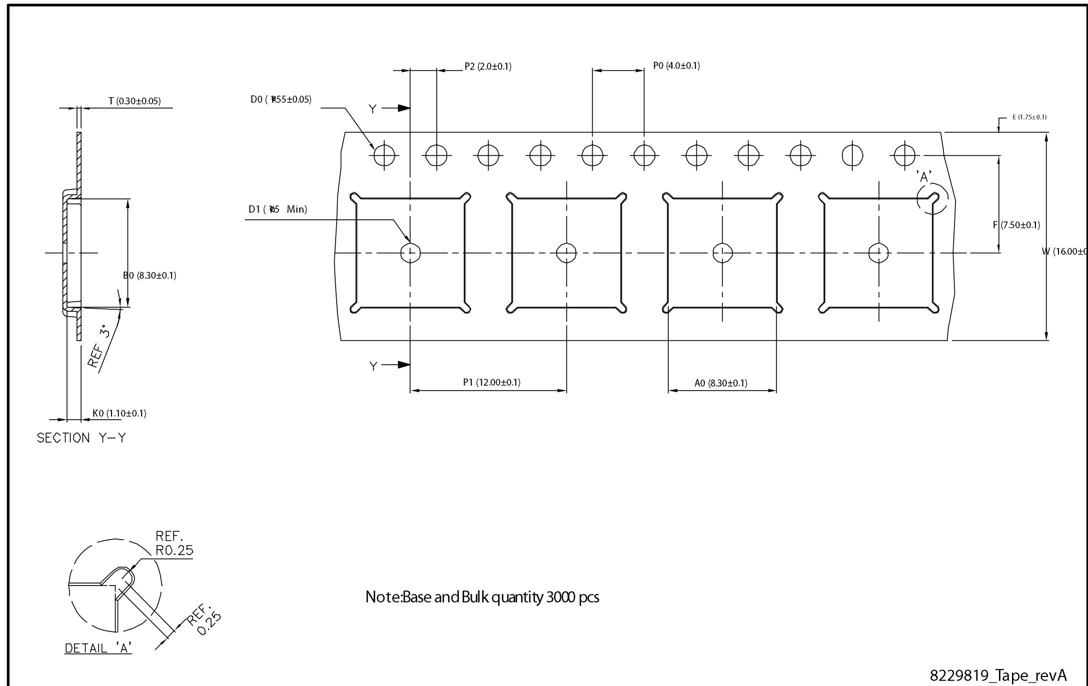
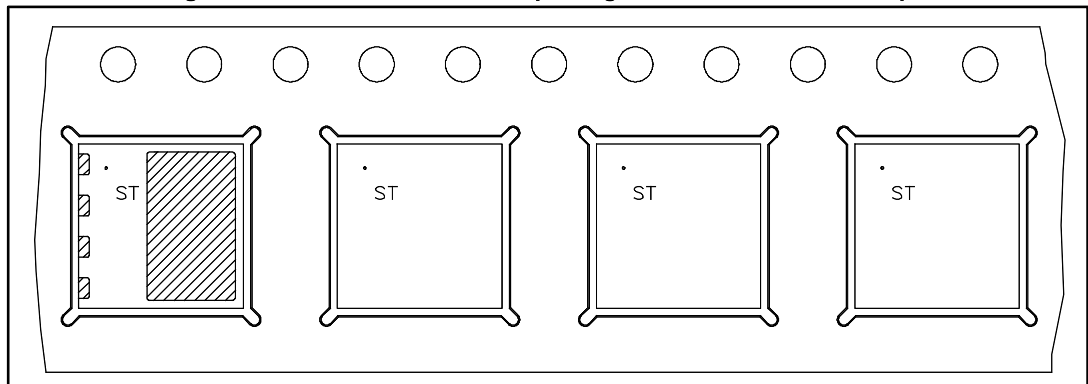
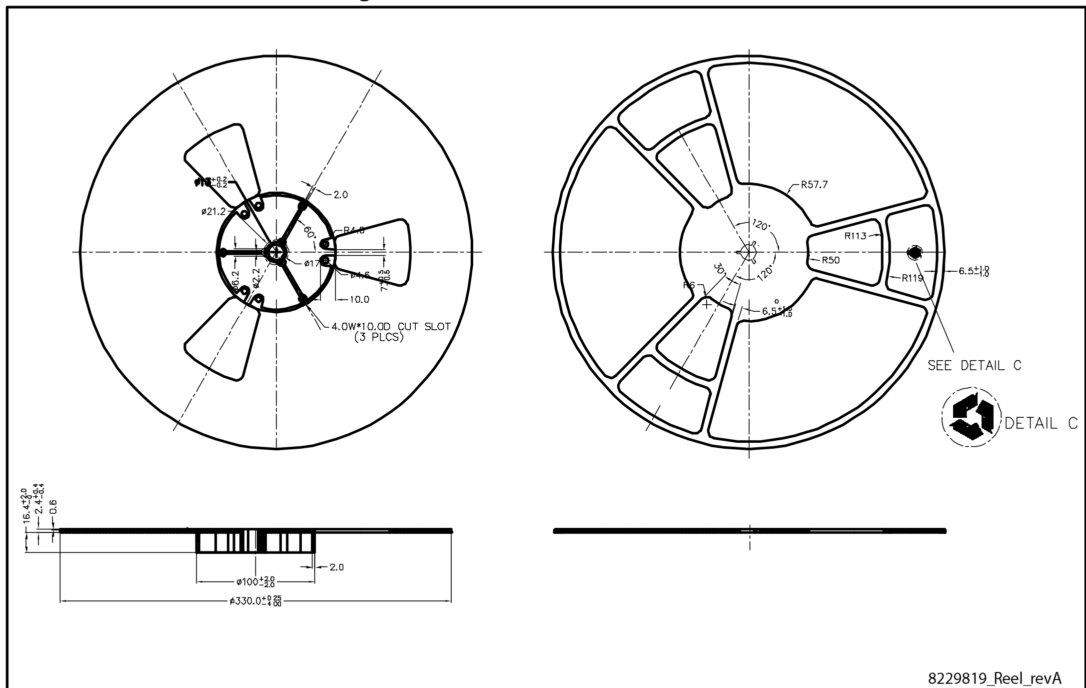


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape



Downloaded From Oneyac.com

Figure 24: PowerFLAT™ 8x8 HV reel



Downloaded From Oneyac.com

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
08-Aug-2014	1	First release.
09-Mar-2016	2	Updated title and internal schematic in cover page. Document status promoted from preliminary data to production data. Modified: *Table 2: "Absolute maximum ratings"*, *Table 4: "On /off states"*, *Table 5: "Dynamic"*, *Table 6: "Switching times"* and *Table 7: "Source drain diode"* Added: *Section 4.1: "Electrical characteristics (curves)"* Updated: *Section 6.1: "PowerFLAT™ 8x8 HV package mechanical data"* Minor text changes

Downloaded From Oneyac.com

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved

Downloaded From Oneyac.com

单击下面可查看定价，库存，交付和生命周期等信息

>>STMicro(意法半导体)

Downloaded From Oneyac.com