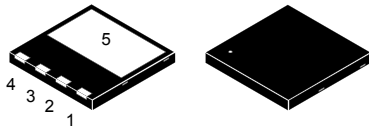
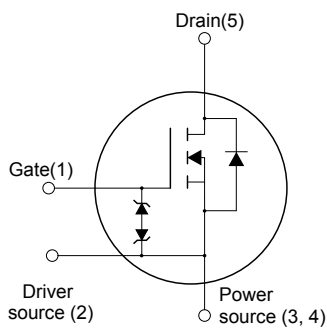


## N-channel 600 V, 91 mΩ typ., 25 A MDmesh™ M6 Power MOSFET in a PowerFLAT™ 8x8 HV package



PowerFLAT™ 8x8 HV



NG1DS2PS34D5Z

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL36N60M6	600 V	110 mΩ	25 A

- Reduced switching losses
- Lower R<sub>DS(on)</sub> x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

### Applications

- Switching applications
- LLC converters
- Boost PFC converters

### Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

#### Product status link

[STL36N60M6](#)

#### Product summary

<b>Order code</b>	STL36N60M6
<b>Marking</b>	36N60M6
<b>Package</b>	PowerFLAT™ 8x8 HV
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	25	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	15.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	100	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	160	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 25\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.78	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	°C/W

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ )	750	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$		91	110	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1960	-	pF
$C_{oss}$	Output capacitance		-	93	-	pF
$C_{riss}$	Reverse transfer capacitance		-	6	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	332	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	1.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 30\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	44.3	-	nC
$Q_{gs}$	Gate-source charge		-	10.1	-	nC
$Q_{gd}$	Gate-drain charge		-	25	-	nC

1.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 15\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	15.2	-	ns
$t_r$	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.2	-	ns
$t_f$	Fall time		-	7.3	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		25	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		100	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 25\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 30\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	340		ns
$Q_{rr}$	Reverse recovery charge		-	5.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	31		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 30\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	430		ns
$Q_{rr}$	Reverse recovery charge		-	7.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	36		A

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

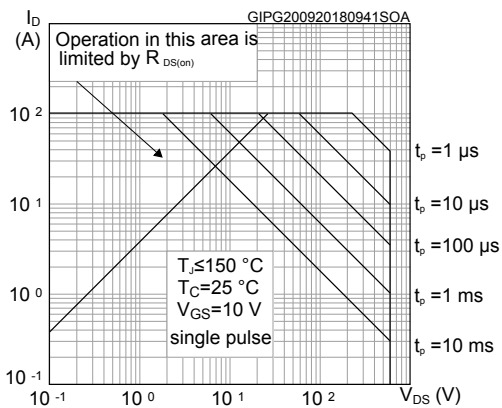


Figure 2. Thermal impedance

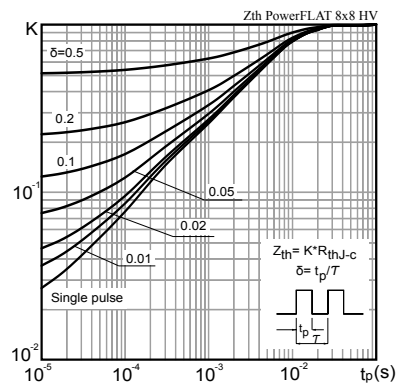


Figure 3. Output characteristics

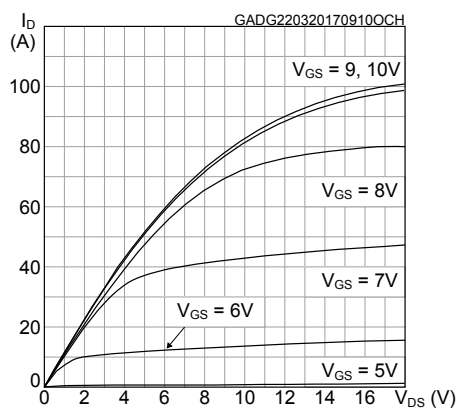


Figure 4. Transfer characteristics

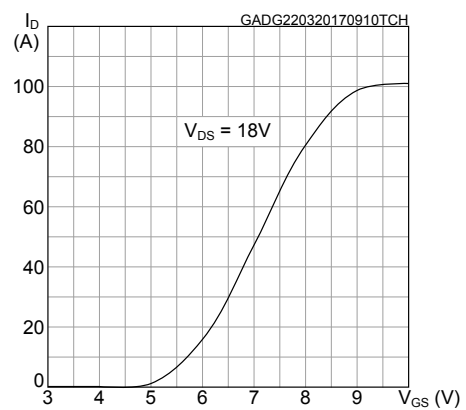


Figure 5. Gate charge vs gate-source voltage

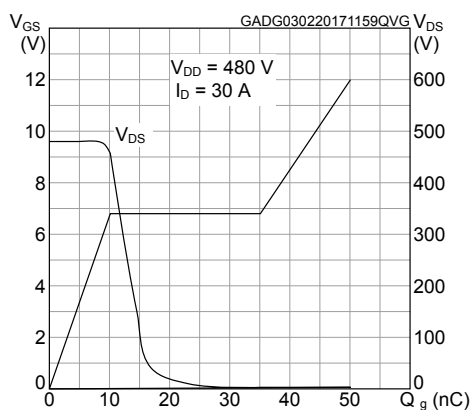


Figure 6. Static drain-source on-resistance

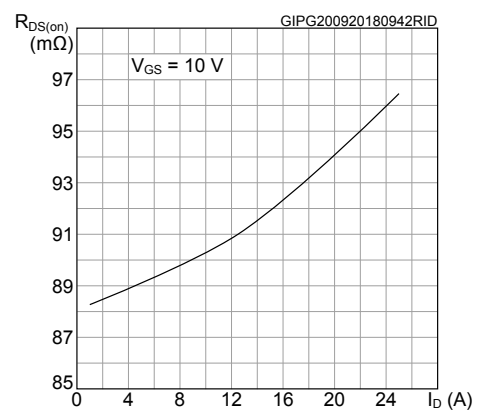


Figure 7. Capacitance variations

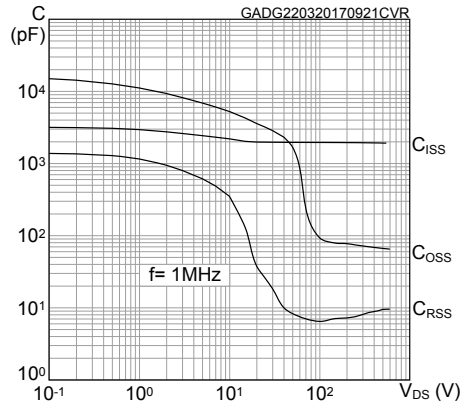


Figure 8. Normalized gate threshold voltage vs temperature

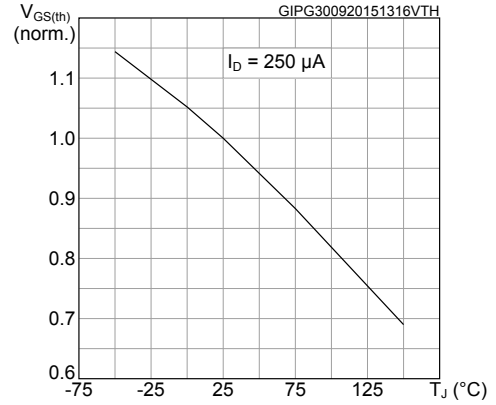


Figure 9. Normalized on-resistance vs temperature

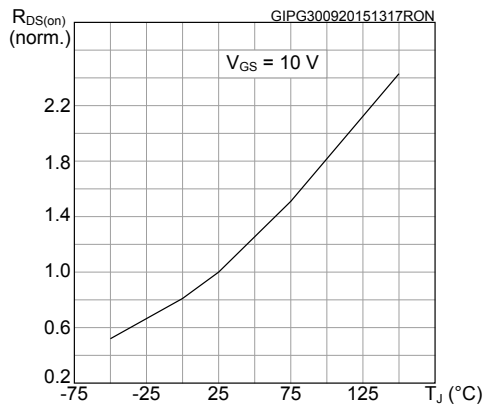


Figure 10. Normalized V<sub>(BR)DSS</sub> vs temperature

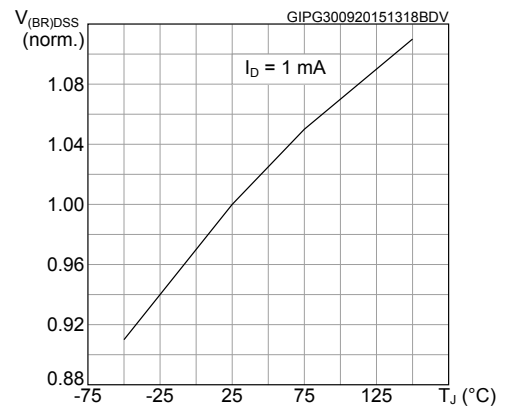


Figure 11. Output capacitance stored energy

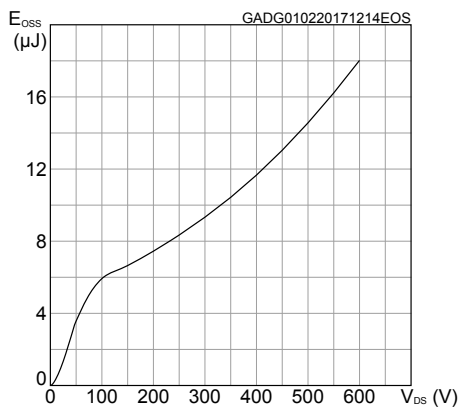
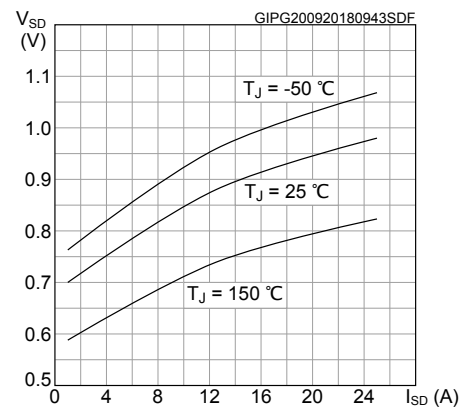
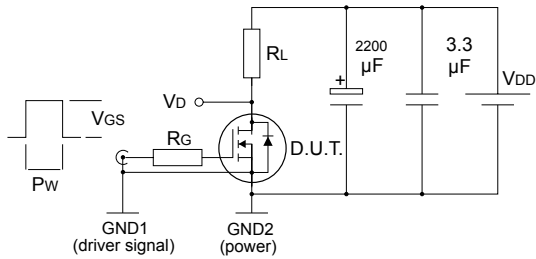


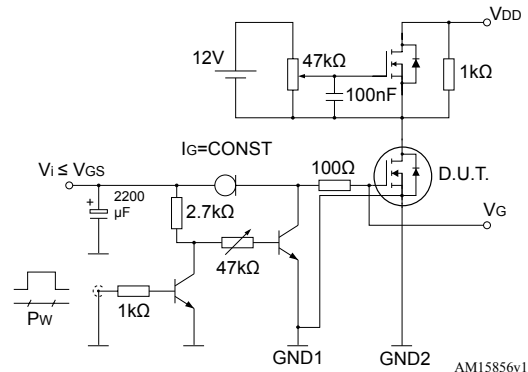
Figure 12. Source-drain diode forward characteristics



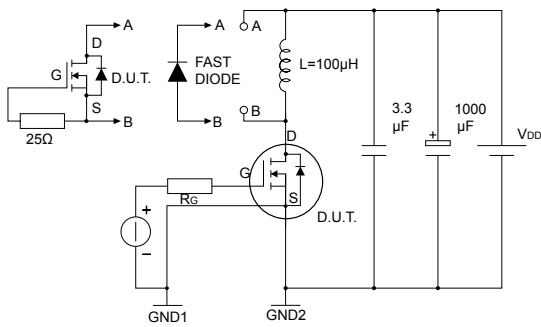
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**


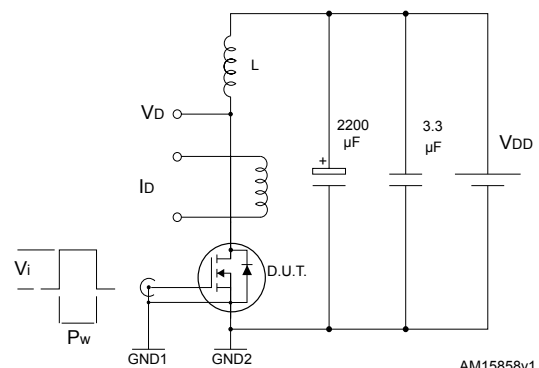
AM15855v1

**Figure 14. Test circuit for gate charge behavior**


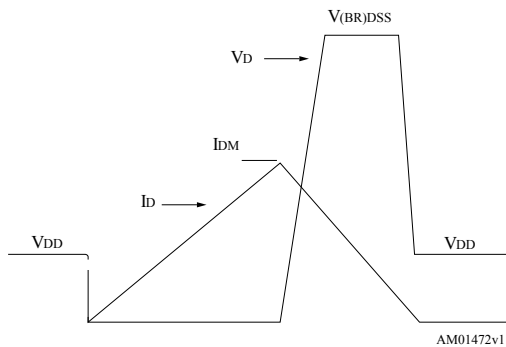
AM15856v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


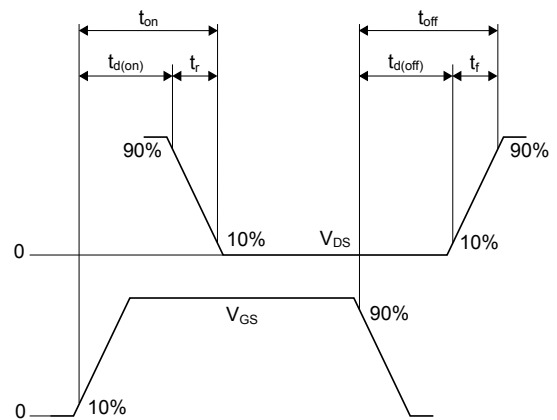
AM15857v1

**Figure 16. Unclamped inductive load test circuit**


AM15858v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

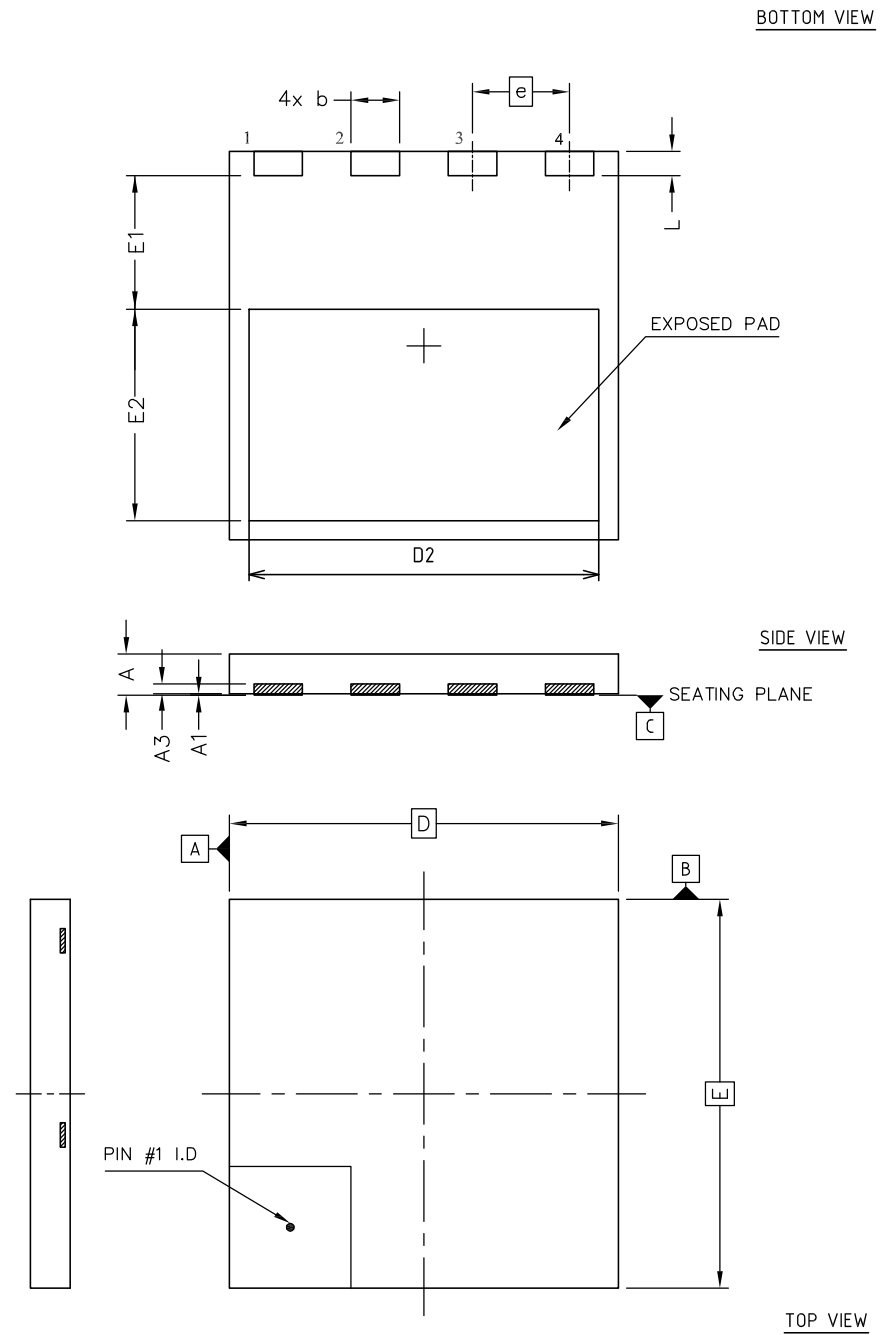
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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



## 4.1 PowerFLAT™ 8x8 HV package information

Figure 19. PowerFLAT™ 8x8 HV package outline

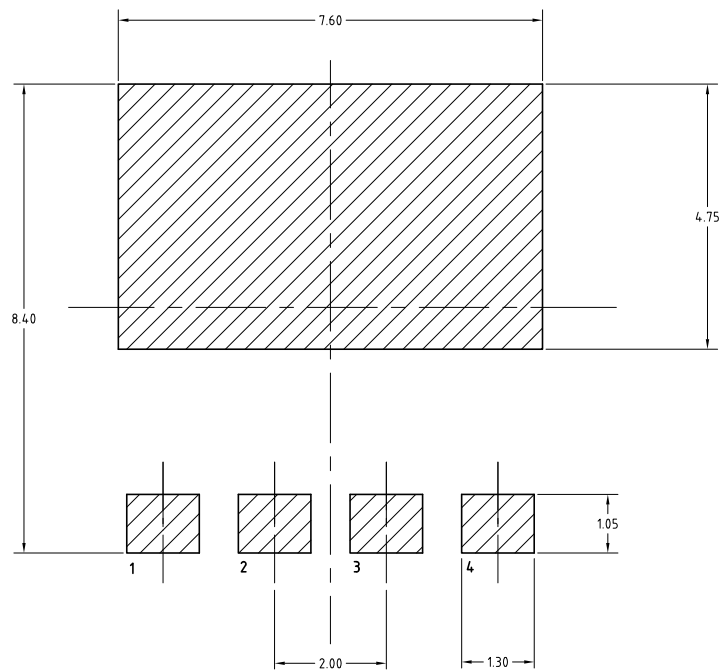


8222871\_Rev\_4

**Table 8. PowerFLAT™ 8x8 HV mechanical data**

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

**Figure 20. PowerFLAT™ 8x8 HV footprint**

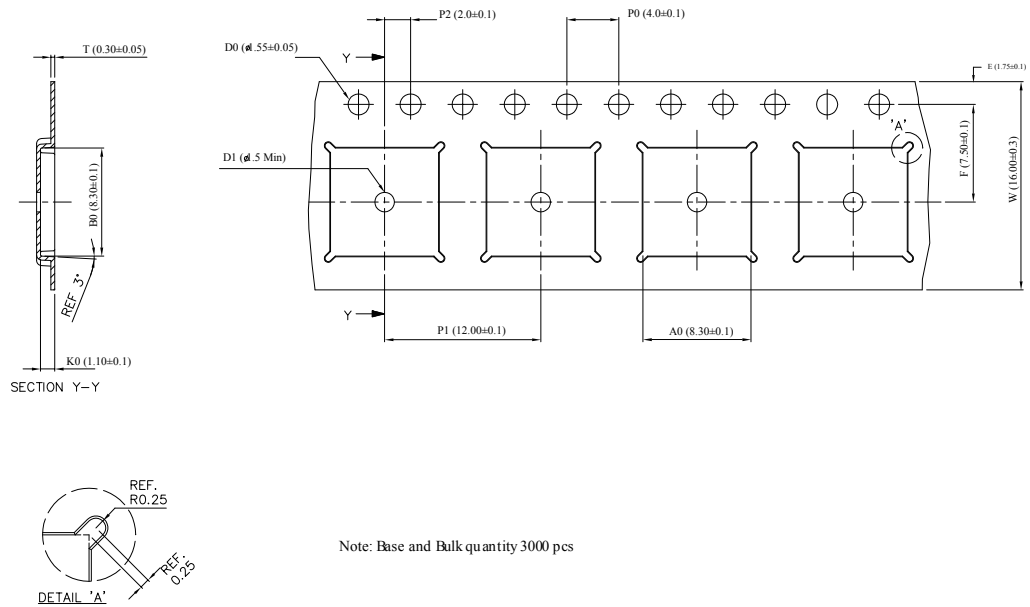


8222871\_REV\_4\_footprint

*Note: All dimensions are in millimeters.*

## 4.2 PowerFLAT™ 8x8 HV packing information

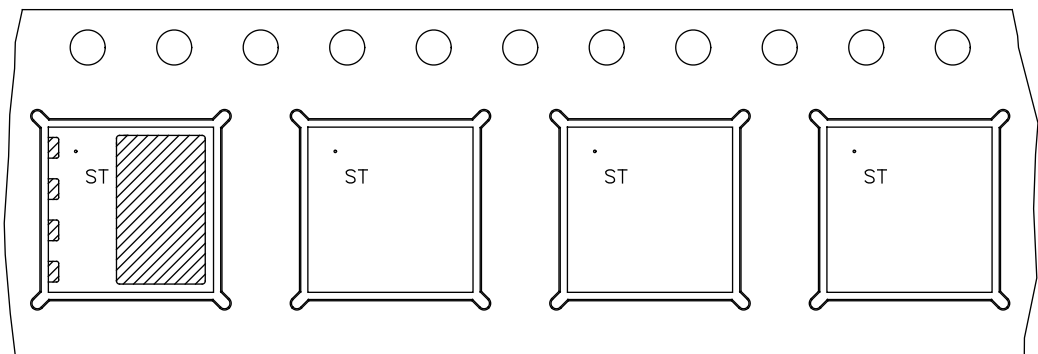
Figure 21. PowerFLAT™ 8x8 HV tape



8229819\_Tape\_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape





## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
03-Jul-2015	1	First release.
09-Jul-2015	2	Updated <i>Figure 1: "Internal schematic diagram" in cover page.</i>
07-Aug-2015	3	Text and formatting changes throughout document. Datasheet promoted from preliminary data to production data. On cover page: - updated title description and package silhouette In section Electrical ratings: - updated table <i>Avalanche characteristics</i> In section Electrical characteristics: - updated <i>tables On/off states, Dynamic, Switching times and Source drain diode</i> Added <i>section Electrical characteristics (curves)</i>
20-Sep-2018	4	Modified features table on cover page. Modified <a href="#">Table 4. On/off states</a> , <a href="#">Table 5. Dynamic</a> , <a href="#">Table 6. Switching times</a> and <a href="#">Table 7. Source-drain diode</a> . Modified <a href="#">Section 2.1 Electrical characteristics (curves)</a> . Minor text changes.

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