

# **BTA06 and BTB06 Series**

**6A TRIACs** 

SNUBBERLESS™, LOGIC LEVEL & STANDARD

**Table 1: Main Features** 

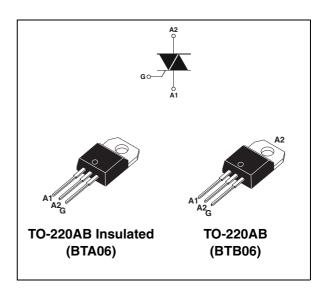
Symbol	Value	Unit
I <sub>T(RMS)</sub>	6	Α
V <sub>DRM</sub> /V <sub>RRM</sub>	600 and 800	V
I <sub>GT (Q₁)</sub>	5 to 50	mA

#### **DESCRIPTION**

Available either in through-hole or surface-mount packages, the **BTA06** and **BTB06** triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers,...

The snubberless and logic level versions (BTA/BTB...W) are specially recommended for use on inductive loads, thanks to their high commutation performances.

By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at  $2500V_{RMS}$ ) complying with UL standards (File ref.: E81734).



**Table 2: Order Codes** 

Part Number	Marking
BTA06-xxxxxRG	See page table 8 on
BTB06-xxxxxRG	page 6

**Table 3: Absolute Maximum Ratings** 

Symbol	Paramet	Parameter				
I=	RMS on-state current (full sine	TO-220AB $T_c = 110^{\circ}C$		6	Α	
I <sub>T(RMS)</sub>	wave)	TO-220AB Ins.	$T_{c} = 105^{\circ}C$	0	A	
Ітом	Non repetitive surge peak on-state	F = 50 Hz	t = 20 ms	60	Α	
ITSM	current (full cycle, T <sub>j</sub> initial = 25°C)	F = 60 Hz	t = 16.7 ms	63	^	
l <sup>2</sup> t	I <sup>2</sup> t Value for fusing	t <sub>p</sub> = 10 ms		21	A <sup>2</sup> s	
dl/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r \le 100 \text{ ns}$	F = 120 Hz	T <sub>j</sub> = 125°C	50	A/µs	
I <sub>GM</sub>	Peak gate current	t <sub>p</sub> = 20 μs	T <sub>j</sub> = 125°C	4	Α	
P <sub>G(AV)</sub>	Average gate power dissipation	1	W			
T <sub>stg</sub> T <sub>j</sub>	Storage junction temperature range Operating junction temperature range	- 40 to + 150 - 40 to + 125	°C			

February 2006 REV. 6 1/7

**Tables 4: Electrical Characteristics** ( $T_j = 25$ °C, unless otherwise specified)

# ■ SNUBBERLESS and Logic Level (3 quadrants)

Symbol	mbol Test Conditions				BTA06	BTB06		Unit
Syllibol	rest conditions	Quadrant		TW	SW	CW	BW	Offic
I <sub>GT</sub> (1)	$V_{D} = 12 \text{ V } R_{I} = 30 \Omega$	1 - 11 - 111	MAX.	5	10	35	50	mA
V <sub>GT</sub>	VD = 12 V 11[ = 50 52	1 - 11 - 111	MAX.		1	.3		V
V <sub>GD</sub>	$V_D = V_{DRM}$ $R_L = 3.3 \text{ k}\Omega$ $T_j = 125^{\circ}\text{C}$	1 - 11 - 111	MIN.		0	.2		V
I <sub>H</sub> (2)	I <sub>T</sub> = 100 mA		MAX.	10	15	35	50	mA
I <sub>I</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	I - III	MAX.	10	25	50	70	mA
'L	II III	IVI/A/X.	15	30	60	80	ША	
dV/dt (2)	$V_D = 67 \text{ %}V_{DRM}$ gate open $T_j = 125 \text{°}C$		MIN.	20	40	400	1000	V/µs
	$(dV/dt)c = 0.1 V/\mu s$ $T_j = 125^{\circ}C$			2.7	3.5	-	-	
(dl/dt)c (2)	$(dV/dt)c = 10 V/\mu s$ $T_j = 125$ °C		MIN.	1.2	2.4	-	-	A/ms
	Without snubber $T_j = 125^{\circ}C$	;		-	-	3.5	5.3	

### ■ Standard (4 quadrants)

Symbol	Test Conditions	Quadrant		BTA06	Unit		
Symbol	rest conditions	Quadrant		С	В	Oille	
I <sub>GT</sub> (1)		I - II - III	MAX.	25	50	mA	
·GI (·/	$V_D = 12 V$ $R_L = 30 \Omega$	IV	WIAX.	50	100	ША	
V <sub>GT</sub>		ALL	MAX.	1	.3	V	
$V_{GD}$	$V_D = V_{DRM}$ $R_L = 3.3 \text{ k}\Omega$ $T_j = 125^{\circ}\text{C}$	ALL	MIN.	0.2		V	
I <sub>H</sub> (2)	I <sub>T</sub> = 500 mA		MAX.	25	50	mA	
Ι <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	I - III - IV	MAX.	40	50	mA	
, <u>,</u>	- G G	II	WIAX.	80	100		
dV/dt (2)	$V_D = 67 \text{ %V}_{DRM}$ gate open $T_j = 125 \text{°C}$		MIN.	200	400	V/µs	
(dV/dt)c (2)	$(dI/dt)c = 2.7 \text{ A/ms}$ $T_j = 125^\circ$	C	MIN.	5	10	V/µs	

**Table 5: Static Characteristics** 

Symbol	Test C	Test Conditions				
V <sub>TM</sub> (2)	$I_{TM} = 8.5 \text{ A}$ $t_p = 380  \mu\text{s}$	T <sub>j</sub> = 25°C	MAX.	1.55	V	
V <sub>t0</sub> (2)	Threshold voltage	T <sub>j</sub> = 125°C	MAX.	0.85	V	
R <sub>d</sub> (2)	Dynamic resistance	T <sub>j</sub> = 125°C	MAX.	60	mΩ	
I <sub>DRM</sub>	$V_{DRM} = V_{RRM}$ $T_j = 25^{\circ}C$ MAX.		MAY	5	μA	
$I_{RRM}$	VDRM — VRRM	T <sub>j</sub> = 125°C	IVIAA.	1	mA	

Note 1: minimum I<sub>GT</sub> is guaranted at 5% of I<sub>GT</sub> max.

Note 2: for both polarities of A2 referenced to A1.

**577** 

**Table 6: Thermal resistance** 

Symbol	Parame	Value	Unit	
<b>D</b>	lunction to coop (AC)	TO-220AB	1.8	°C/W
R <sub>th(j-c)</sub> Junction to case (AC)	TO-220AB Insulated	2.7	- C/VV	
R <sub>th(j-a)</sub>	Junction to ambient	TO-220AB TO-220AB Insulated	60	°C/W

Figure 1: Maximum power dissipation versus RMS on-state current (full cycle)

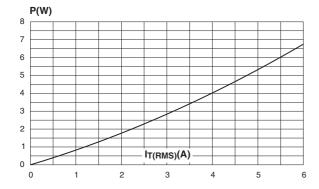


Figure 3: Relative variation of thermal impedance versus pulse duration

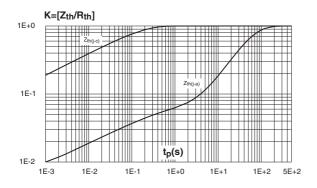


Figure 2: RMS on-state current versus case temperature (full cycle)

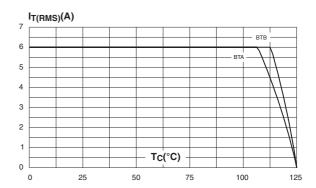
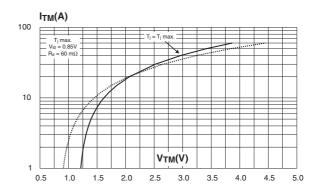


Figure 4: On-state characteristics (maximum values)



577

Figure 5: Surge peak on-state current versus number of cycles

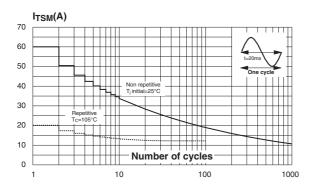


Figure 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

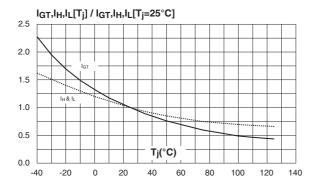


Figure 9: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (Standard types)

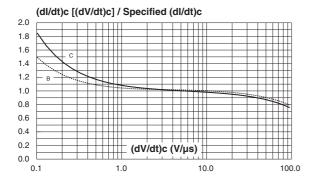


Figure 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10 \text{ ms}$  and corresponding value of  $l^2t$ 

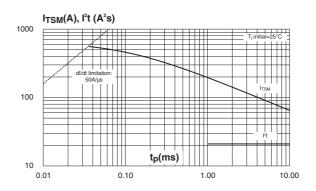


Figure 8: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (Snubberless & logic level types)

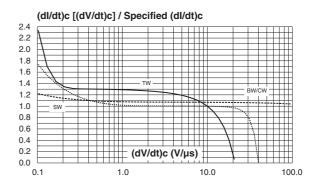
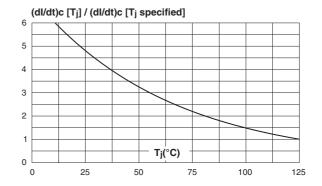
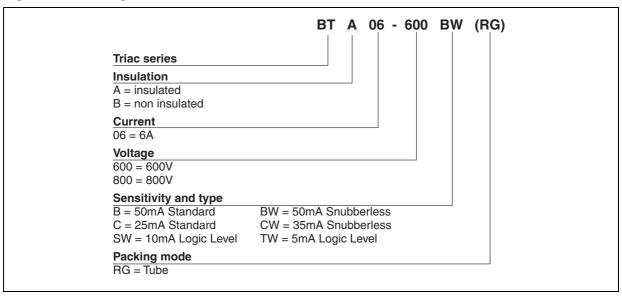


Figure 10: Relative variation of critical rate of decrease of main current versus junction temperature



4/7

Figure 11: Ordering Information Scheme

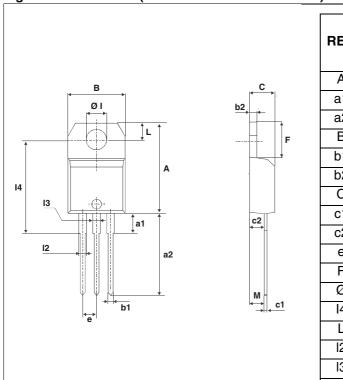


**Table 7: Product Selector** 

Part Number	Voltag	e (xxx)	Sensitivity	Туре	
rait Nullibei	600 V	800 V	- Sensitivity	туре	Package
BTA/BTB06-xxxB	Х	Х	50 mA	Standard	TO-220AB
BTA/BTB06-xxxBW	Х	Х	50 mA	Snubberless	TO-220AB
BTA/BTB06-xxxC	Х	Х	25 mA	Standard	TO-220AB
BTA/BTB06-xxxCW	Х	Х	35 mA	Snubberless	TO-220AB
BTA/BTB06-xxxSW	Х	Х	10 mA	Logic level	TO-220AB
BTA/BTB06-xxxTW	Х	Х	5 mA	Logic Level	TO-220AB

BTB: non insulated TO-220AB package

Figure 12: TO-220AB (insulated and non insulated) Package Mechanical Data



			DIMEN	SIONS	<u> </u>	
REF.	Mi	Ilimete	rs		Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
В	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
С	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
е	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
ØI	3.75		3.85	0.147		0.151
14	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
12	1.14		1.70	0.044		0.066
13	1.14		1.70	0.044		0.066
М		2.60			0.102	

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: <a href="https://www.st.com">www.st.com</a>.

**Table 8: Ordering Information** 

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
BTA/BTB06-xxxyzRG	BTA/BTB06-xxxyz	TO-220AB	2.3 g	50	Tube

**Note:** xxx = voltage, yy = sensitivity, z = type

**Table 9: Revision History** 

Date	Revision	Description of Changes
Apr-2002	5A	Last update.
13-Feb-2006	6	TO-220AB delivery mode changed from bulk to tube. ECOPACK statement added.

6/7

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

© 2006 STMicroelectronics - All rights reserved

#### STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America www.st.com



7/7

单击下面可查看定价,库存,交付和生命周期等信息

>>STMicroelectronics(意法半导体)