

N-channel 600 V, 0.28 Ω typ., 11 A MDmesh™ II
Power MOSFETs in D²PAK and DPAK packages

Datasheet — production data

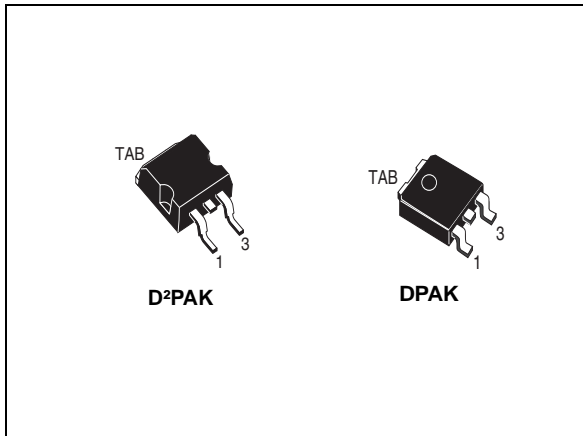
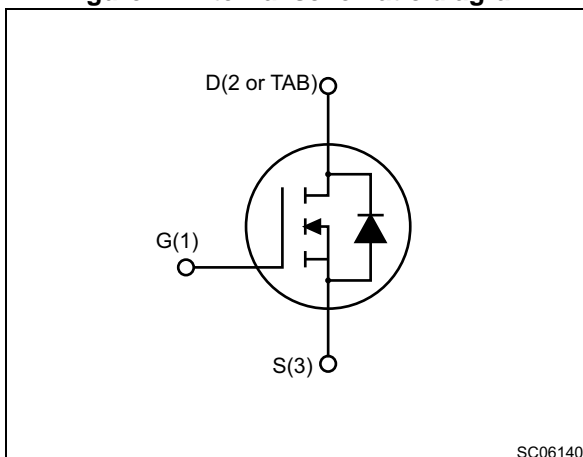


Figure 1. Internal schematic diagram



Features

Order code	V _{DS} (@T _{jmax})	R _{DS(on)} max	I _D
STB13NM60N	650 V	0.36 Ω	11 A
STD13NM60N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB13NM60N	13NM60N	D ² PAK	Tape and reel
STD13NM60N		DPAK	

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves) 6
- 3 Test circuits 9**
- 4 Package information 10**
 - 4.1 D²PAK package information 10
 - 4.2 DPAK package information 15
- 5 Packing information 20**
- 6 Revision history 23**



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.93	A
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
$R_{thj\text{-case}}$	Thermal resistance junction-case max	1.39		$^\circ\text{C}/\text{W}$
$R_{thj\text{-pcb}}$	Thermal resistance junction-pcb max	30	50	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	200	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			± 0.1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$		0.28	0.36	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$	-	790	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance		-	3.6	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	135	-	pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 11\text{ A}, V_{GS} = 10\text{ V},$ (see Figure 16)	-	27	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	14	-	nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	4.7	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 5.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 15)	-	3	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Fall time		-	10	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see Figure 17)	-	230		ns
Q_{rr}	Reverse recovery charge		-	2		μC
I_{RRM}	Reverse recovery current		-	18		A
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17)	-	290		ns
Q_{rr}	Reverse recovery charge		-	2.5		μC
I_{RRM}	Reverse recovery current		-	17		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

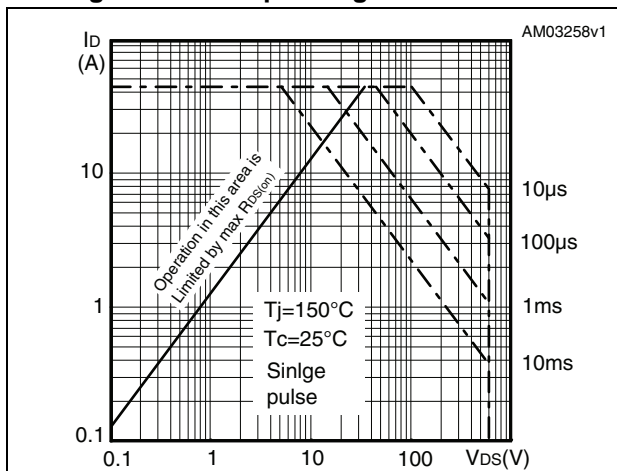


Figure 3. Thermal impedance for D²PAK

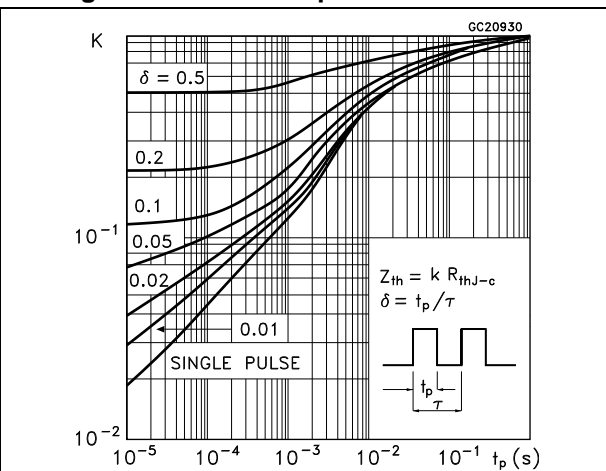


Figure 4. Safe operating area for DPAK

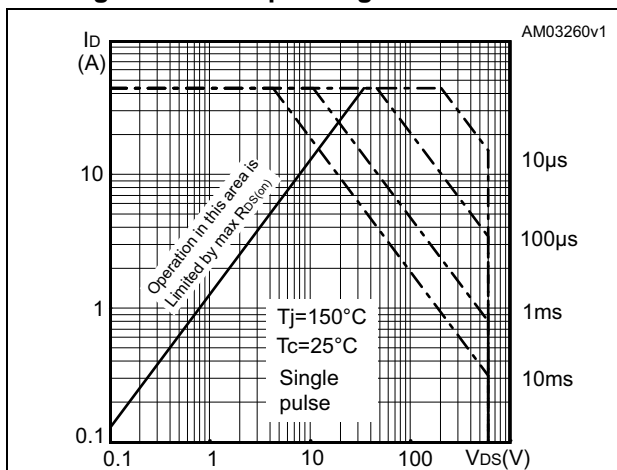


Figure 5. Thermal impedance for DPAK

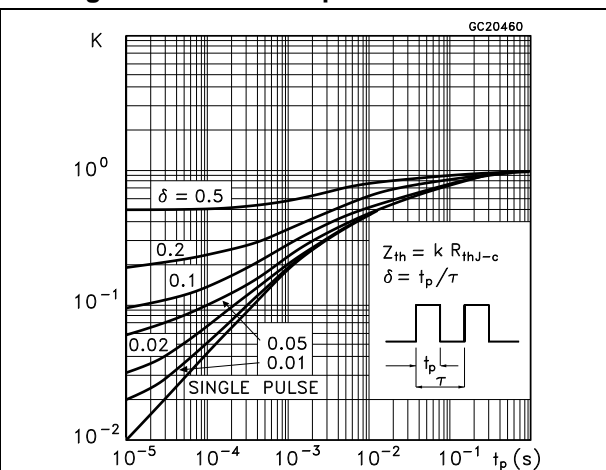


Figure 6. Output characteristics

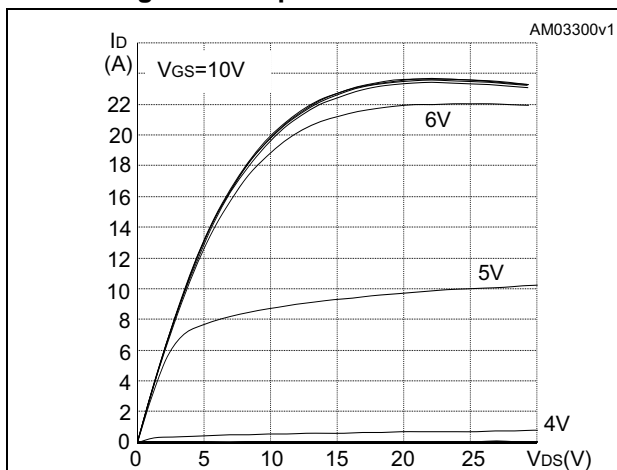


Figure 7. Transfer characteristics

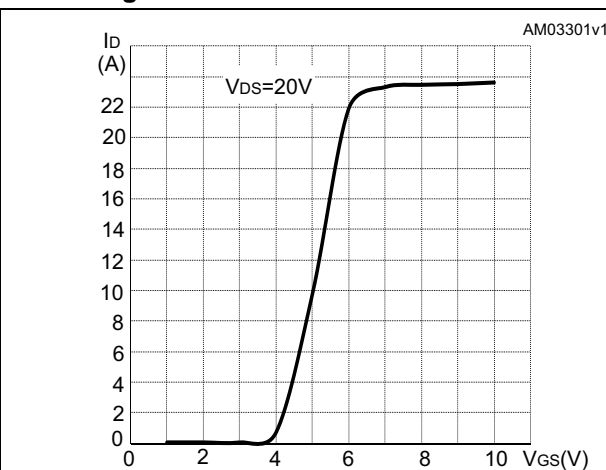


Figure 8. Normalized $V_{(BR)DSS}$ vs temperature

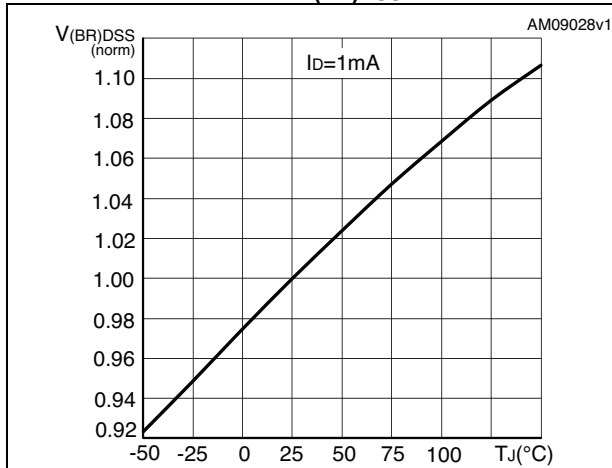


Figure 9. Static drain-source on-resistance

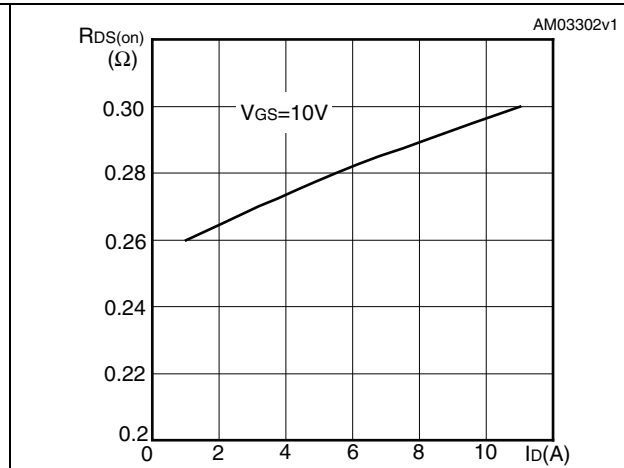


Figure 10. Gate charge vs gate-source voltage

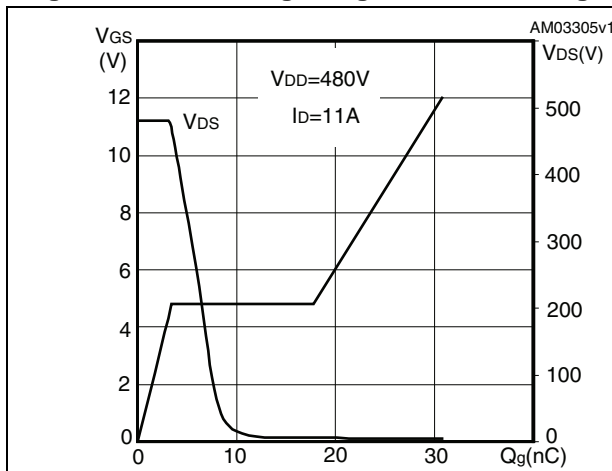


Figure 11. Capacitance variations

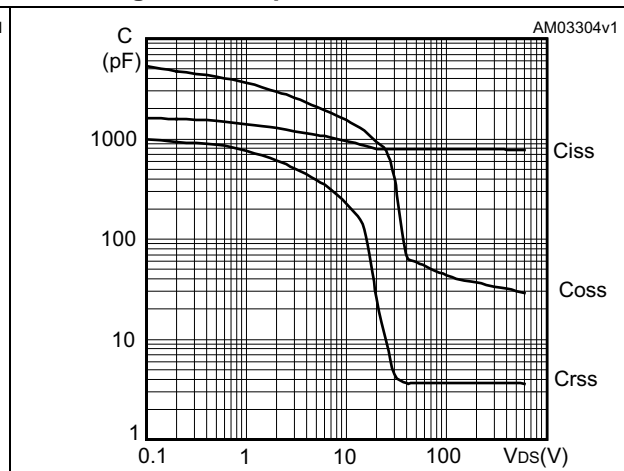


Figure 12. Normalized gate threshold voltage vs temperature

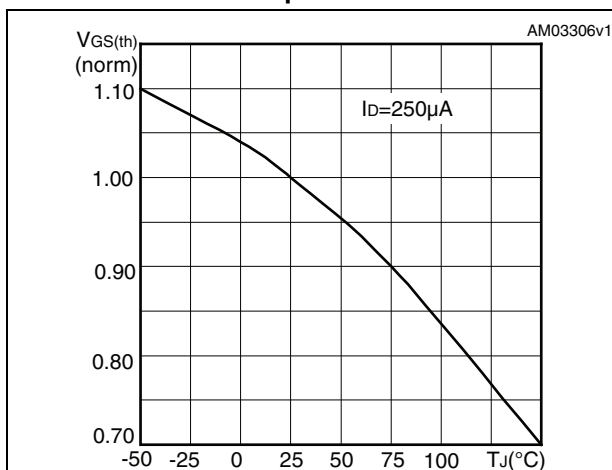


Figure 13. Normalized on-resistance vs temperature

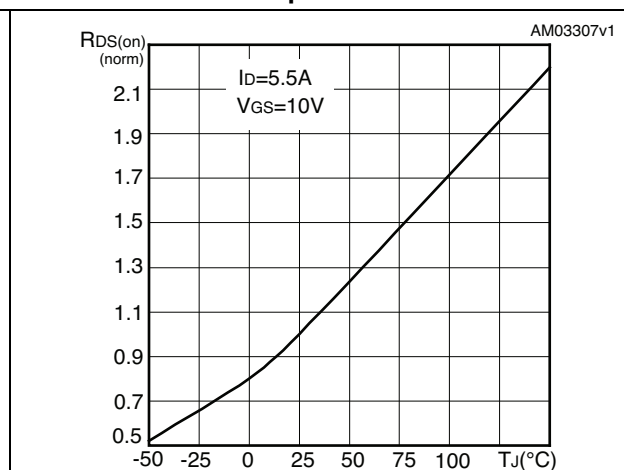
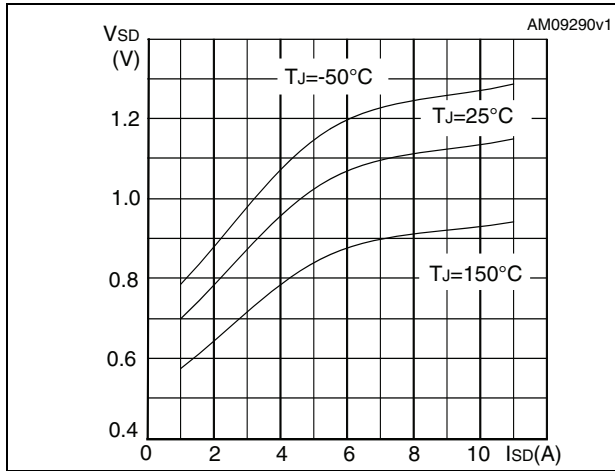


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit

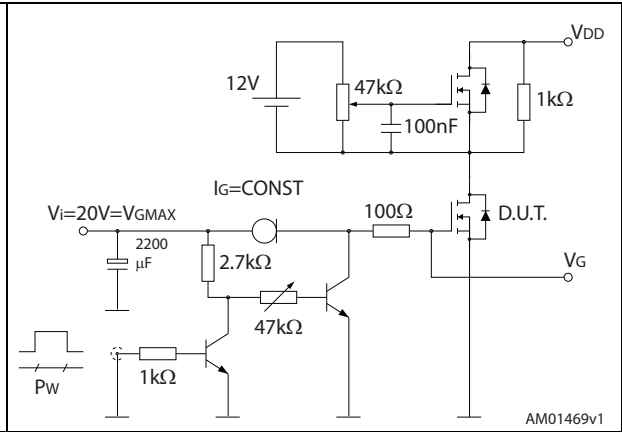


Figure 17. Test circuit for inductive load switching and diode recovery times

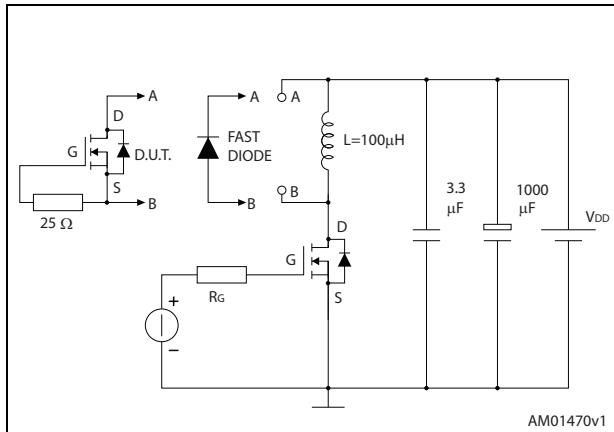


Figure 18. Unclamped inductive load test circuit

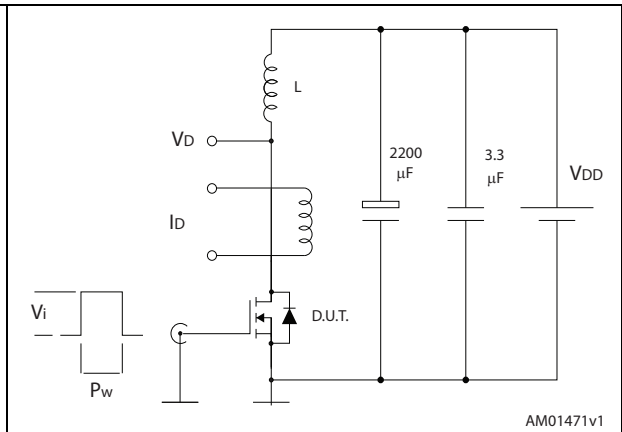


Figure 19. Unclamped inductive waveform

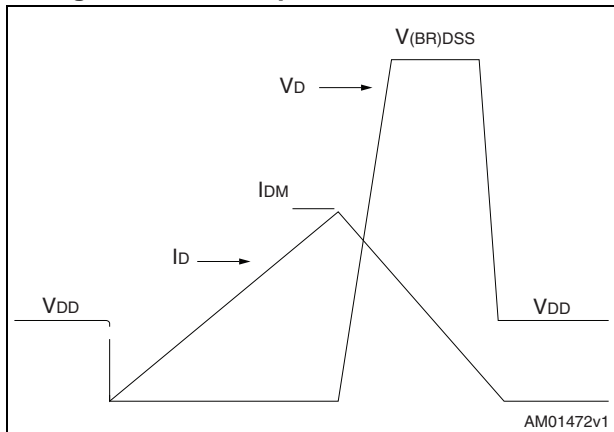
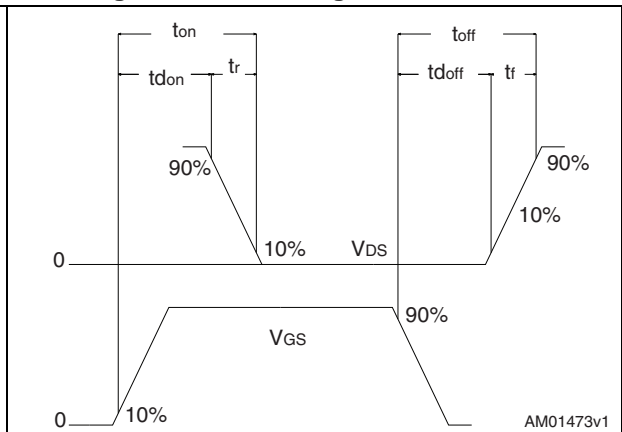


Figure 20. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK package information

Figure 21. D²PAK (TO-263) type A package outline

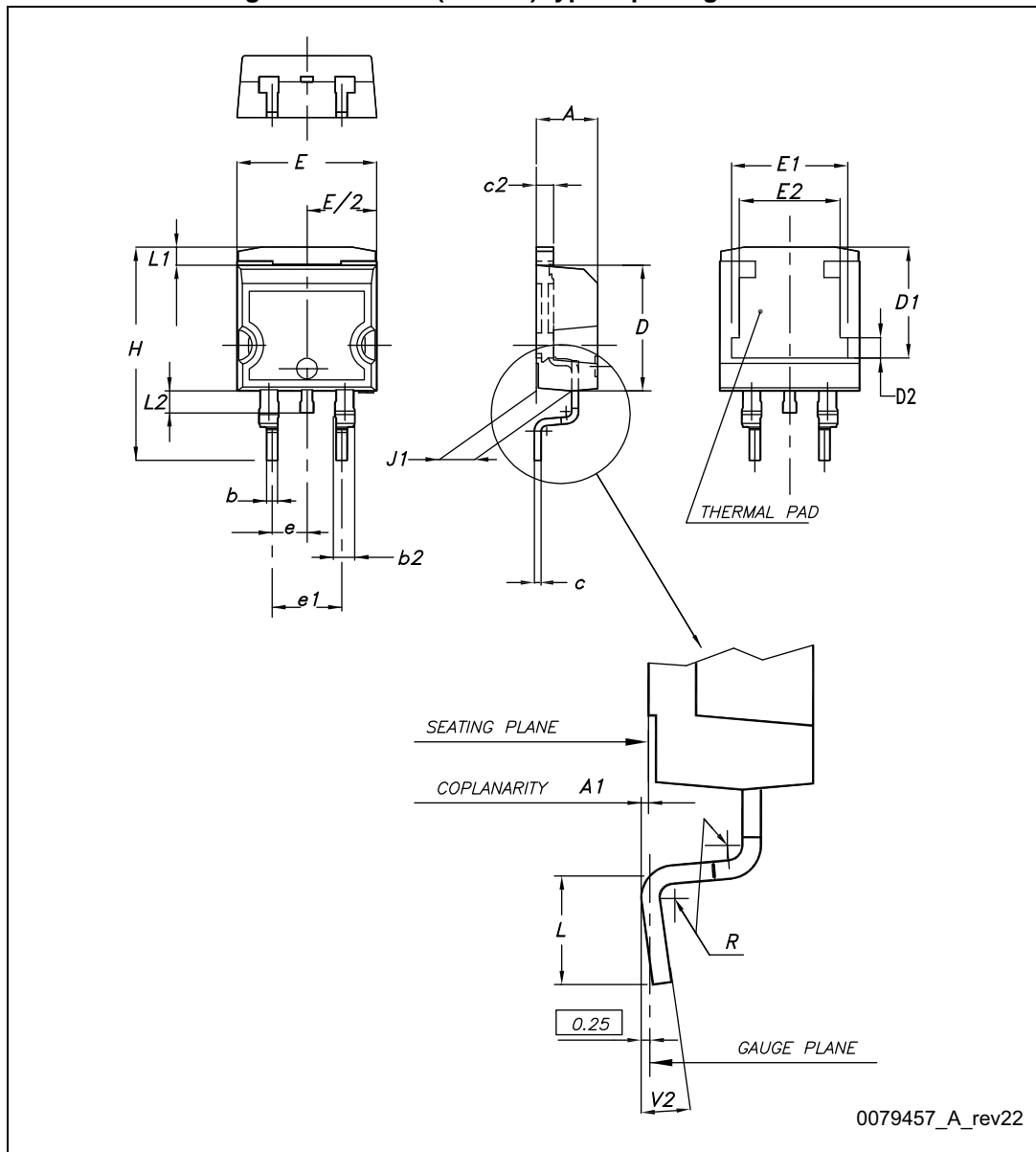


Table 9. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22. D²PAK (TO-263) type B package outline

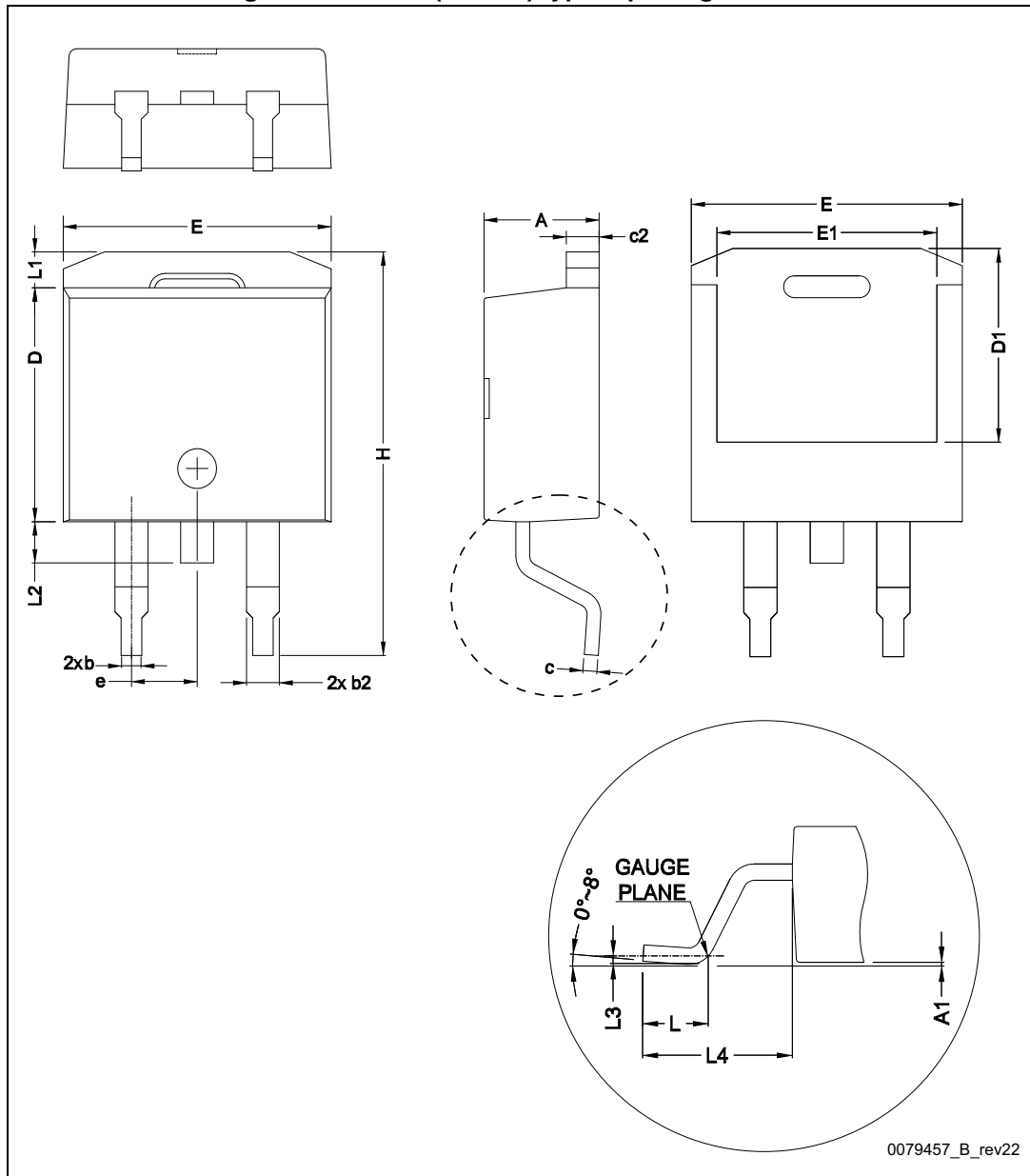
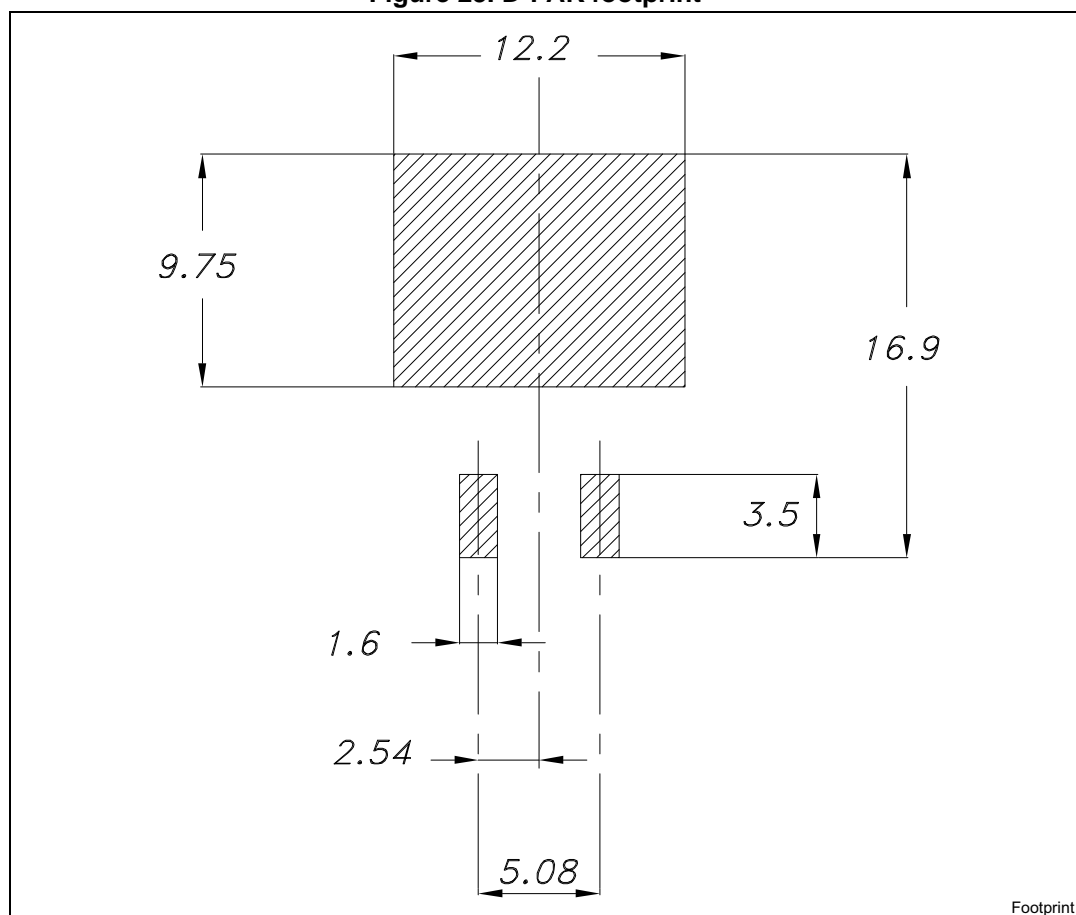


Table 10. D²PAK (TO-263) type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.60
A1	0		0.25
b	0.70		0.93
b2	1.14		1.70
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.36
D	8.6		9.35
D1	6.9		
E	10		10.55
E1	8.1		
e		2.54	
H	15		15.85
L	1.9		2.79
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 23. D²PAK footprint^(a)



a. All dimension are in millimeters

4.2 DPAK package information

Figure 24. DPAK (TO-252) type A2 package outline

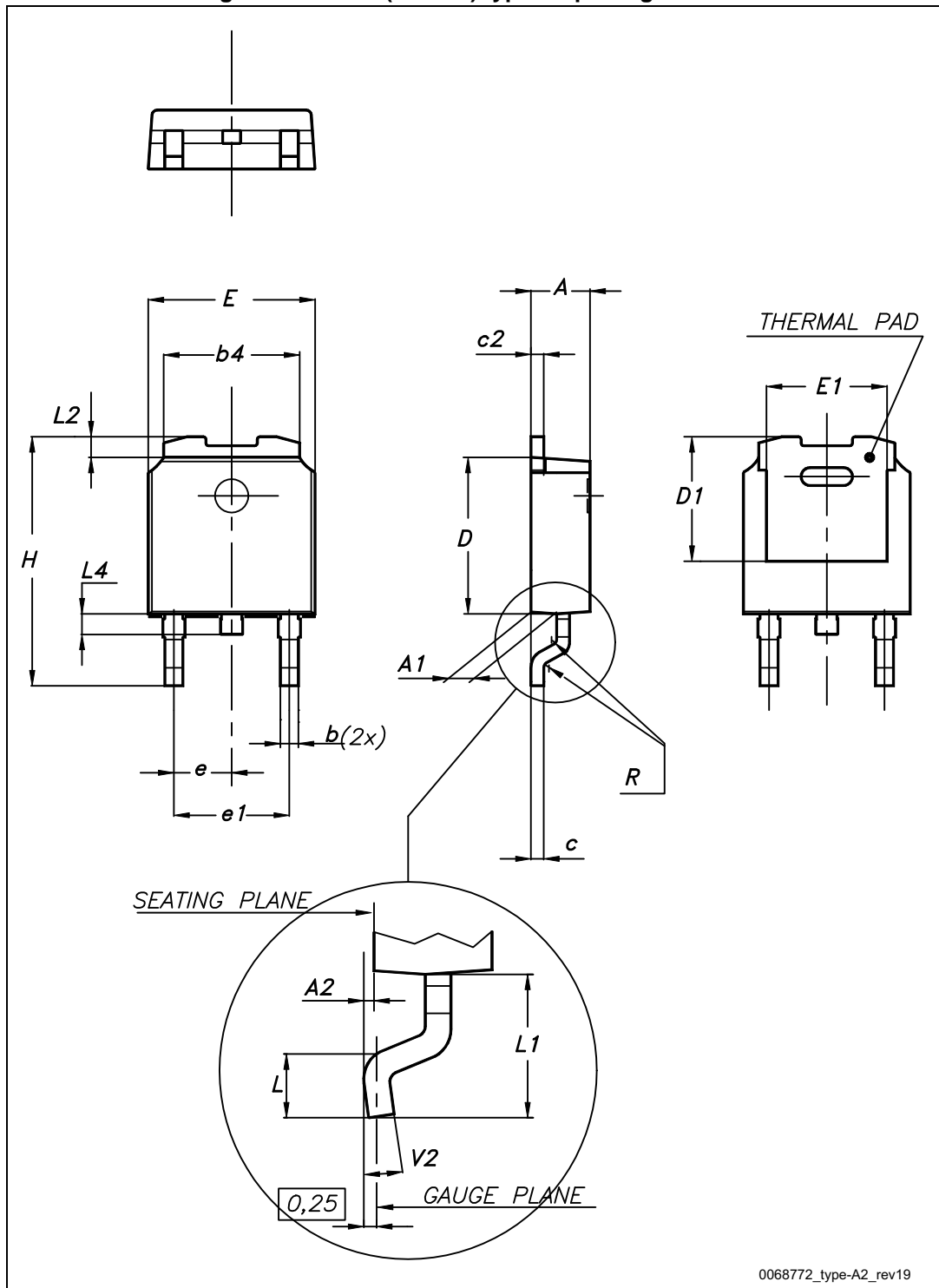


Table 11. DPAK (TO-252) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) type C2 outline

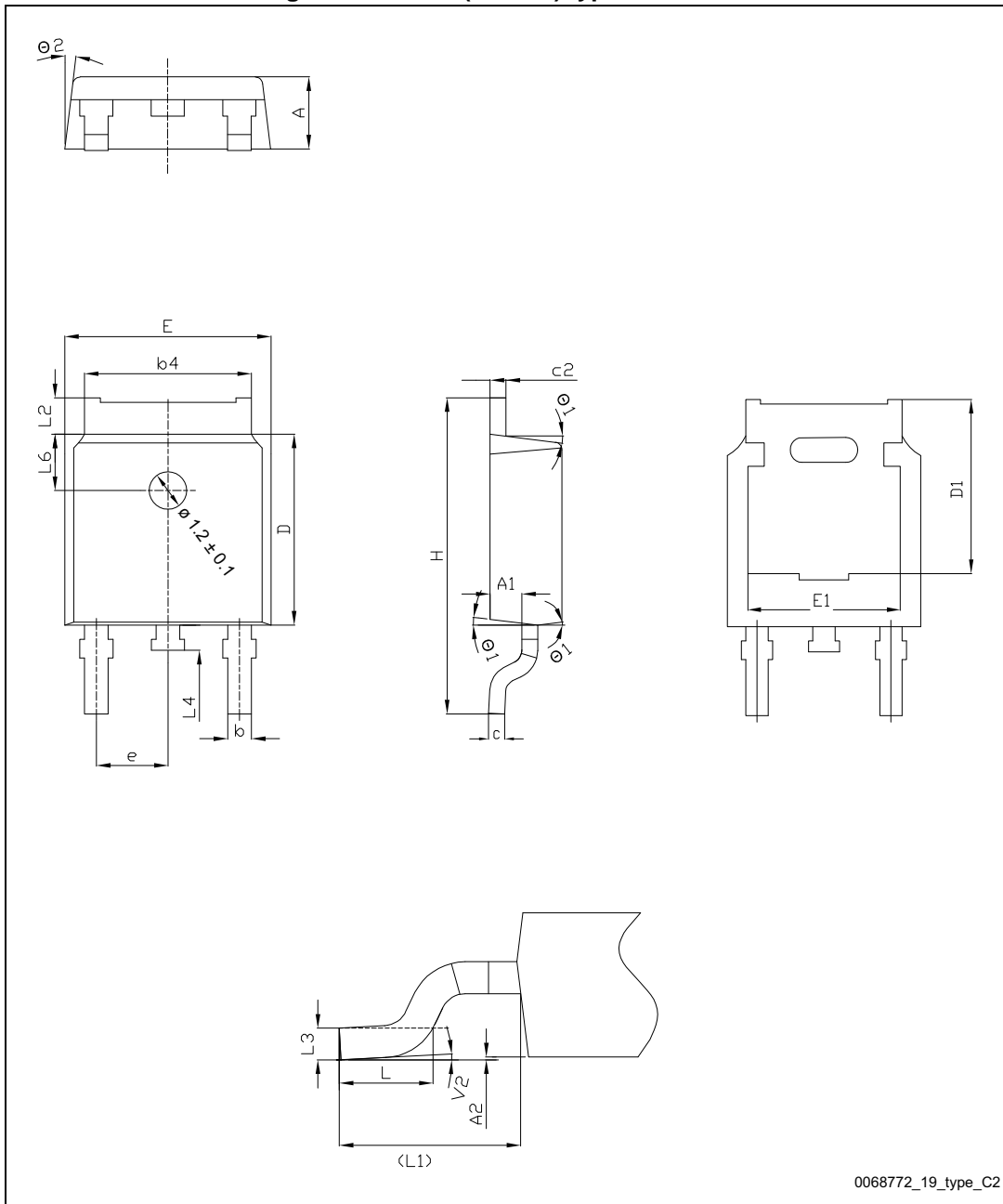
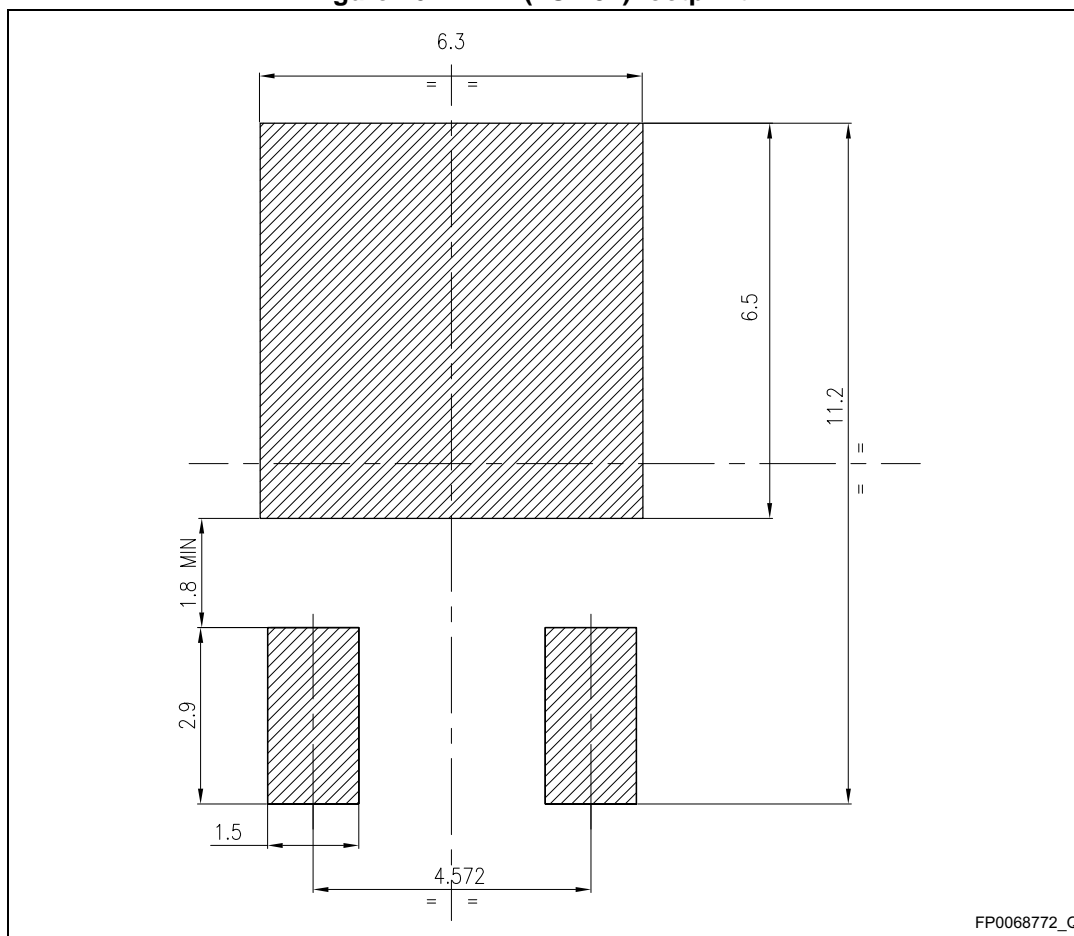


Table 12. DPAK (TO-252) type C2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25	-	-
E	6.50	6.60	6.70
E1	5.20	-	-
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90	-	1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 26. DPAK (TO-252) footprint (b)



b. All dimensions are in millimeters

5 Packing information

Figure 27. Tape

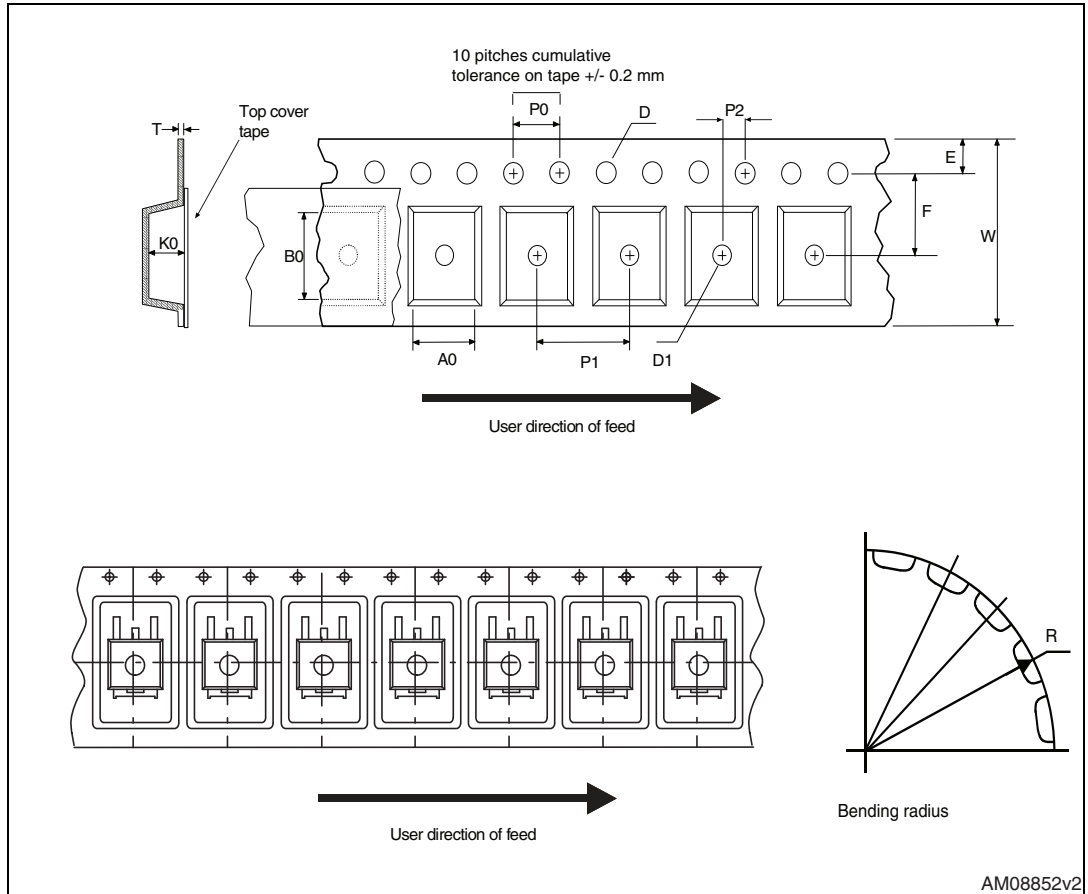


Figure 28. Reel

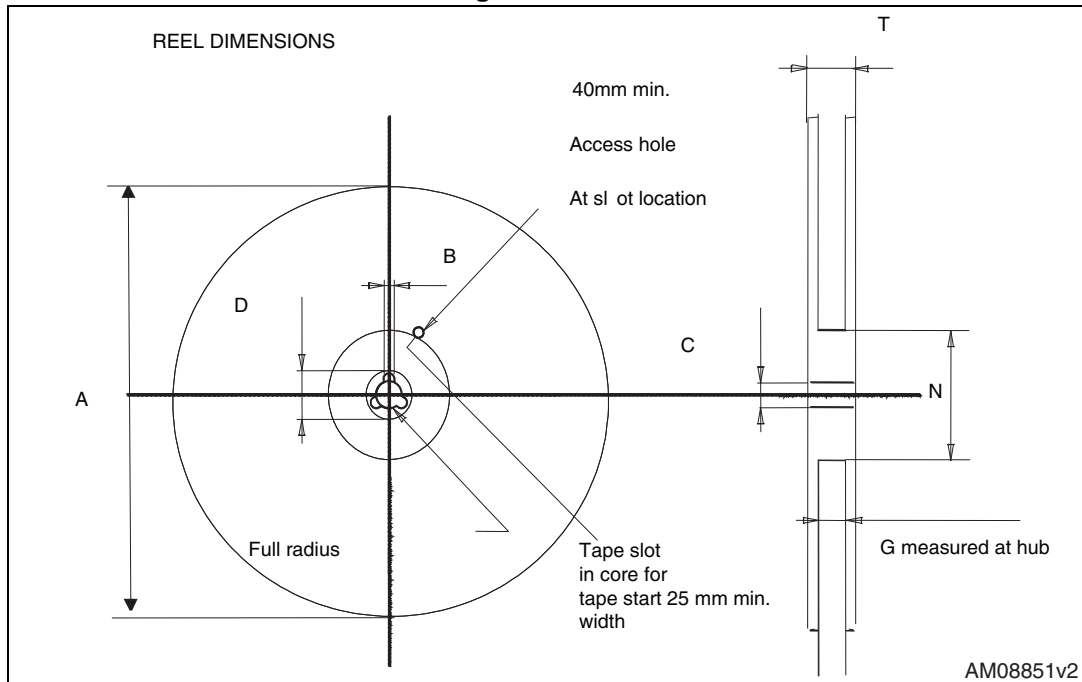


Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 15. Document revision history

Date	Revision	Changes
18-Dec-2012	1	First release
10-Jul-2014	2	– Updated: Section 3: Test circuits – Updated: Section 4: Package information – Minor text changes
19-Jun-2015	3	– Updated 4: Package information – Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

单击下面可查看定价，库存，交付和生命周期等信息

[>>STMicroelectronics\(意法半导体\)](#)