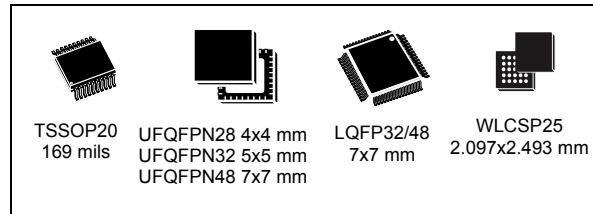


Access line ultra-low-power 32-bit MCU Arm[®]-based Cortex[®]-M0+, 32KB Flash, 8KB SRAM, 1KB EEPROM, ADC, AES

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - -40 to 125 °C temperature range
 - 0.23 µA Standby mode (2 wakeup pins)
 - 0.35 µA Stop mode (16 wakeup lines)
 - 0.6 µA Stop mode + RTC + 8 KB RAM retention
 - Down to 76 µA/MHz in Run mode
 - 5 µs wakeup time (from Flash memory)
 - 41 µA 12-bit ADC conversion at 10 ksp/s
- Core: Arm[®] 32-bit Cortex[®]-M0+
 - From 32 kHz up to 32 MHz max.
 - 0.95 DMIPS/MHz
- Reset and supply management
 - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
 - Ultralow power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 25 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High speed internal 16 MHz factory-trimmed RC (+/- 1%)
 - Internal low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz RC
 - PLL for CPU clock
- Pre-programmed bootloader
 - USART, SPI supported
- Development support
 - Serial wire debug supported
- Up to 38 fast I/Os (31 I/Os 5V tolerant)
- Memories
 - 32 KB Flash with ECC
 - 8 KB RAM
 - 1 KB of data EEPROM with ECC
 - 20-byte backup register
 - Sector protection against R/W operation



- Rich Analog peripherals
 - 12-bit ADC 1.14 Msps up to 10 channels (down to 1.65 V)
 - 2x ultra-low-power comparators (window mode and wake up capability, down to 1.65 V)
- 7-channel DMA controller, supporting ADC, SPI, I2C, USART, Timers, AES
- 5x peripherals communication interface
- 1x USART (ISO 7816, IrDA), 1x UART (low power)
- Up to 2 SPI interfaces, up to 16 Mbits/s
- 1x I2C (SMBus/PMBus)
- 8x timers: 1x 16-bit with up to 4 channels, 2x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC and 2x watchdogs (independent/window)
- CRC calculation unit, 96-bit unique ID
- Hardware Encryption Engine AES 128-bit
- All packages are ECOPACK[®]2

Table 1. Device summary

Reference	Part number
STM32L041x6	STM32L041G6, STM32L041K6, STM32L041C6, STM32L041F6, STM32L041E6

Contents

1	Introduction	9
2	Description	10
2.1	Device overview	11
2.2	Ultra-low-power device continuum	13
3	Functional overview	14
3.1	Low-power modes	14
3.2	Interconnect matrix	18
3.3	Arm® Cortex®-M0+ core	19
3.4	Reset and supply management	20
3.4.1	Power supply schemes	20
3.4.2	Power supply supervisor	20
3.4.3	Voltage regulator	21
3.4.4	Boot modes	21
3.5	Clock management	22
3.6	Low-power real-time clock and backup registers	24
3.7	General-purpose inputs/outputs (GPIOs)	24
3.8	Memories	25
3.9	Direct memory access (DMA)	25
3.10	Analog-to-digital converter (ADC)	25
3.11	Temperature sensor	26
3.11.1	Internal voltage reference (V_{REFINT})	26
3.12	Ultra-low-power comparators and reference voltage	27
3.13	System configuration controller	27
3.14	AES	27
3.15	Timers and watchdogs	28
3.15.1	General-purpose timers (TIM2, TIM21 and TIM22)	28
3.15.2	Low-power Timer (LPTIM)	29
3.15.3	SysTick timer	29
3.15.4	Independent watchdog (IWDG)	29
3.15.5	Window watchdog (WWDG)	29

3.16	Communication interfaces	30
3.16.1	I2C bus	30
3.16.2	Universal synchronous/asynchronous receiver transmitter (USART)	31
3.16.3	Low-power universal asynchronous receiver transmitter (LPUART)	31
3.16.4	Serial peripheral interface (SPI)	32
3.17	Cyclic redundancy check (CRC) calculation unit	32
3.18	Serial wire debug port (SW-DP)	32
4	Pin descriptions	33
5	Memory mapping	46
6	Electrical characteristics	47
6.1	Parameter conditions	47
6.1.1	Minimum and maximum values	47
6.1.2	Typical values	47
6.1.3	Typical curves	47
6.1.4	Loading capacitor	47
6.1.5	Pin input voltage	47
6.1.6	Power supply scheme	48
6.1.7	Current consumption measurement	48
6.2	Absolute maximum ratings	49
6.3	Operating conditions	51
6.3.1	General operating conditions	51
6.3.2	Embedded reset and power control block characteristics	52
6.3.3	Embedded internal reference voltage	54
6.3.4	Supply current characteristics	55
6.3.5	Wakeup time from low-power mode	65
6.3.6	External clock source characteristics	67
6.3.7	Internal clock source characteristics	71
6.3.8	PLL characteristics	73
6.3.9	Memory characteristics	74
6.3.10	EMC characteristics	76
6.3.11	Electrical sensitivity characteristics	77
6.3.12	I/O current injection characteristics	78
6.3.13	I/O port characteristics	79
6.3.14	NRST pin characteristics	83

6.3.15	12-bit ADC characteristics	84
6.3.16	Temperature sensor characteristics	87
6.3.17	Comparators	88
6.3.18	Timer characteristics	89
6.3.19	Communications interfaces	90
7	Package information	96
7.1	LQFP48 package information	96
7.2	UFQFPN48 package information	100
7.3	LQFP32 package information	102
7.4	UFQFPN32 package information	105
7.5	UFQFPN28 package information	107
7.6	WLCSP25 package information	110
7.7	TSSOP20 package information	113
7.8	Thermal characteristics	116
7.8.1	Reference document	117
8	Ordering information	118
9	Revision history	119

List of tables

Table 1.	Device summary	1
Table 2.	Ultra-low-power STM32L041x4/x6 device features and peripheral counts	11
Table 3.	Functionalities depending on the operating power supply range	16
Table 4.	CPU frequency range depending on dynamic voltage scaling	16
Table 5.	Functionalities depending on the working mode (from Run/active down to standby)	16
Table 6.	STM32L0xx peripherals interconnect matrix	18
Table 7.	Temperature sensor calibration values	26
Table 8.	Internal voltage reference measured values	26
Table 9.	Timer feature comparison	28
Table 10.	Comparison of I2C analog and digital filters	30
Table 11.	STM32L041x6 I ² C implementation	30
Table 12.	USART implementation	31
Table 13.	SPI implementation	32
Table 14.	Legend/abbreviations used in the pinout table	37
Table 15.	Pin definitions	38
Table 16.	Alternate functions	44
Table 17.	Voltage characteristics	49
Table 18.	Current characteristics	50
Table 19.	Thermal characteristics	50
Table 20.	General operating conditions	51
Table 21.	Embedded reset and power control block characteristics	52
Table 22.	Embedded internal reference voltage calibration values	54
Table 23.	Embedded internal reference voltage	54
Table 24.	Current consumption in Run mode, code with data processing running from Flash memory	56
Table 25.	Current consumption in Run mode vs code type, code with data processing running from Flash memory	56
Table 26.	Current consumption in Run mode, code with data processing running from RAM	58
Table 27.	Current consumption in Run mode vs code type, code with data processing running from RAM	58
Table 28.	Current consumption in Sleep mode	59
Table 29.	Current consumption in Low-power run mode	60
Table 30.	Current consumption in Low-power Sleep mode	61
Table 31.	Typical and maximum current consumptions in Stop mode	62
Table 32.	Typical and maximum current consumptions in Standby mode	63
Table 33.	Average current consumption during wakeup	63
Table 34.	Peripheral current consumption in Run or Sleep mode	64
Table 35.	Peripheral current consumption in Stop and Standby mode	65
Table 36.	Low-power mode wakeup timings	66
Table 37.	High-speed external user clock characteristics	67
Table 38.	Low-speed external user clock characteristics	68
Table 39.	HSE oscillator characteristics	69
Table 40.	LSE oscillator characteristics	70
Table 41.	16 MHz HSI16 oscillator characteristics	71
Table 42.	LSI oscillator characteristics	72
Table 43.	MSI oscillator characteristics	72
Table 44.	PLL characteristics	73



Table 45.	RAM and hardware registers	74
Table 46.	Flash memory and data EEPROM characteristics	74
Table 47.	Flash memory and data EEPROM endurance and retention	75
Table 48.	EMS characteristics	76
Table 49.	EMI characteristics	77
Table 50.	ESD absolute maximum ratings	77
Table 51.	Electrical sensitivities	78
Table 52.	I/O current injection susceptibility	78
Table 53.	I/O static characteristics	79
Table 54.	Output voltage characteristics	81
Table 55.	I/O AC characteristics	82
Table 56.	NRST pin characteristics	83
Table 57.	ADC characteristics	84
Table 58.	R_{AIN} max for $f_{ADC} = 16$ MHz	86
Table 59.	ADC accuracy	86
Table 60.	Temperature sensor calibration values	87
Table 61.	Temperature sensor characteristics	88
Table 62.	Comparator 1 characteristics	88
Table 63.	Comparator 2 characteristics	89
Table 64.	TIMx characteristics	89
Table 65.	I2C analog filter characteristics	90
Table 66.	SPI characteristics in voltage Range 1	91
Table 67.	SPI characteristics in voltage Range 2	92
Table 68.	SPI characteristics in voltage Range 3	93
Table 69.	LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data	97
Table 70.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data	101
Table 71.	LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package mechanical data	103
Table 72.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data	105
Table 73.	UFQPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data	107
Table 74.	WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data	110
Table 75.	WLCSP25 recommended PCB design rules	111
Table 76.	TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data	113
Table 77.	Thermal characteristics	116
Table 78.	STM32L041x6 ordering information scheme	118
Table 79.	Document revision history	119

List of figures

Figure 1.	STM32L041x6 block diagram	12
Figure 2.	Clock tree	23
Figure 3.	STM32L041x6 UFQFPN48.	33
Figure 4.	STM32L041x6 LQFP48	34
Figure 5.	STM32L041x6 LQFP32 pinout	34
Figure 6.	STM32L041x6 UFQFPN32 pinout	35
Figure 7.	STM32L041x6 UFQFPN28 pinout	35
Figure 8.	STM32L041G6UxS UFQFPN28 pinout	36
Figure 9.	STM32L041x6 TSSOP20 pinout	36
Figure 10.	STM32L041x6 WLCSP25 pinout	37
Figure 11.	Pin loading conditions.	47
Figure 12.	Pin input voltage	47
Figure 13.	Power supply scheme.	48
Figure 14.	Current consumption measurement scheme	48
Figure 15.	ID _D vs V _{DD} , at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE = 16 MHz, 1WS	57
Figure 16.	ID _D vs V _{DD} , at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS	57
Figure 17.	ID _D vs V _{DD} , at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS	61
Figure 18.	ID _D vs V _{DD} , at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive	62
Figure 19.	ID _D vs V _{DD} , at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off	62
Figure 20.	High-speed external clock source AC timing diagram	67
Figure 21.	Low-speed external clock source AC timing diagram	68
Figure 22.	HSE oscillator circuit diagram.	69
Figure 23.	Typical application with a 32.768 kHz crystal	70
Figure 24.	HSI16 minimum and maximum value versus temperature	71
Figure 25.	VIH/VIL versus V _{DD} (CMOS I/Os)	80
Figure 26.	VIH/VIL versus V _{DD} (TTL I/Os)	80
Figure 27.	I/O AC characteristics definition	83
Figure 28.	Recommended NRST pin protection	84
Figure 29.	ADC accuracy characteristics.	87
Figure 30.	Typical connection diagram using the ADC	87
Figure 31.	SPI timing diagram - slave mode and CPHA = 0	94
Figure 32.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	94
Figure 33.	SPI timing diagram - master mode ⁽¹⁾	95
Figure 34.	LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline	96
Figure 35.	LQFP48 recommended footprint	98
Figure 36.	Example of LQFP48 marking (package top view)	99
Figure 37.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.	100
Figure 38.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint	101
Figure 39.	LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package outline	102
Figure 40.	LQFP32 recommended footprint	103
Figure 41.	Example of LQFP32 marking (package top view)	104

Figure 42.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline.	105
Figure 43.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint	106
Figure 44.	Example of UFQFPN32 marking (package top view)	106
Figure 45.	UFQFN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.	107
Figure 46.	UFQFN28 recommended footprint.	108
Figure 47.	Example of UFQFN28 marking (package top view)	109
Figure 48.	WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale package outline.	110
Figure 49.	WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale recommended footprint.	111
Figure 50.	Example of WLCSP25 marking (package top view)	112
Figure 51.	TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline.	113
Figure 52.	TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint	114
Figure 53.	Example of TSSOP20 marking (package top view)	115
Figure 54.	Thermal resistance	117

1 Introduction

The ultra-low-power STM32L041x6 family includes devices in 6 different packages from 20 to 48 pins. The description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L041x6 microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L041x6 datasheet should be read in conjunction with the STM32L0x1 reference manual (RM0377).

For information on the Arm[®] Cortex[®]-M0+ core please refer to the Cortex[®]-M0+ Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family..



2 Description

The access line ultra-low-power STM32L041x6 family incorporates the high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (32 Kbytes of Flash program memory, 1 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L041x6 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L041x6 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L041x6 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L041x6 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L041x6 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

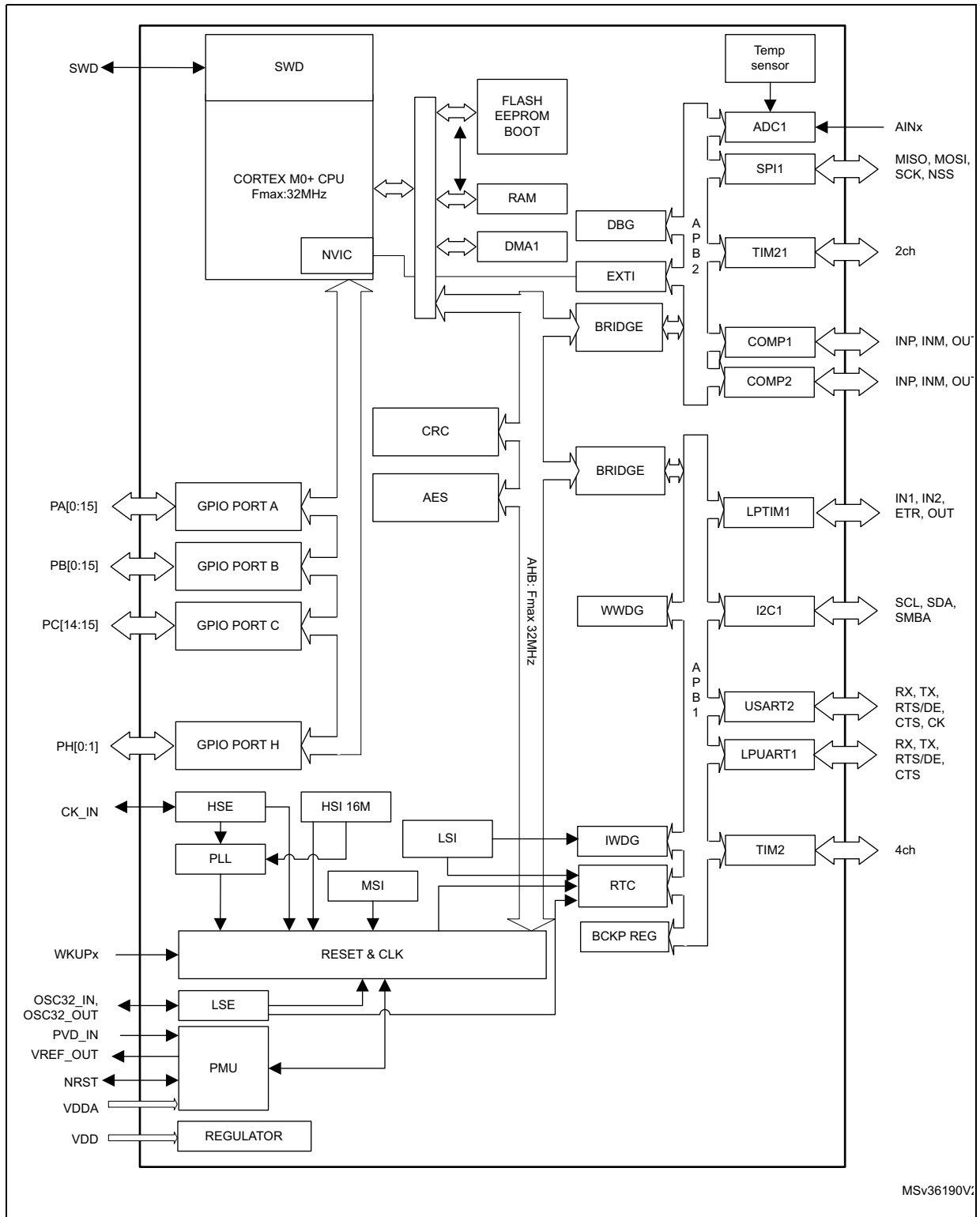
2.1 Device overview

Table 2. Ultra-low-power STM32L041x4/x6 device features and peripheral counts

Peripheral		STM32 L041F6	STM32 L041E6	STM32 L041G6	STM32 L041K6	STM32 L041C6
Flash (Kbytes)		32				
Data EEPROM (Kbytes)		1				
RAM (Kbytes)		8				
AES		1				
Timers	General-purpose	3				
	LPTIMER	1				
RTC/SYSTICK/IWDG/ WWDG		1/1/1/1				
Communication interfaces	SPI	2(1) ⁽¹⁾				
	I ² C	1				
	USART	1				
	LPUART	1				
GPIOs		15	20	21(23) ⁽²⁾	27 ⁽³⁾	38
Clocks: HSE ⁽⁴⁾ /LSE/HSI/MSI/LSI		1/1/1/1/1				
12-bit synchronized ADC Number of channels		1 10				
Comparators		2				
Max. CPU frequency		32 MHz				
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option				
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C				
Packages		TSSOP 20	WLCSP 25	UFQFPN28	LQFP32, UFQFPN32	LQFP48, UFQFPN48

1. 1 SPI interface is a USART operating in SPI master mode.
2. 23 GPIOs are available only on STM32L041G6UxS part number.
3. LQFP32 has two GPIOs, less than UFQFPN32 (27).
4. HSE external quartz connexion available only on LQFP48.

Figure 1. STM32L041x6 block diagram



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to Arm® Cortex®-M4, including Arm® Cortex®-M3 and Arm® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L041x6 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

(if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range ⁽¹⁾	Functionalities depending on the operating power supply range	
	ADC operation	Dynamic voltage scaling range
V _{DD} = 1.65 to 1.71 V	Conversion time up to 570 ksps	Range 2 or range 3
V _{DD} = 1.71 to 2.0 V ⁽²⁾	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3
V _{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3
V _{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3

1. GPIO speed depends on V_{DD} voltage range. Refer to [Table 55: I/O AC characteristics](#) for more information about I/O speed.
2. CPU frequency changes from initial to final must respect the condition: $f_{CPU\ initial} < 4f_{CPU\ final}$. It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) ⁽¹⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
CPU	Y	--	Y	--	--	--	--	--
Flash memory	O	O	O	O	--	--	--	--
RAM	Y	Y	Y	Y	Y	--	--	--
Backup registers	Y	Y	Y	Y	Y	Y	Y	Y
EEPROM	O	O	O	O	--	--	--	--
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--	--	--	--



Table 5. Functionalities depending on the working mode (from Run/active down to standby)⁽¹⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(2)		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
USART	O	O	O	O	O ⁽³⁾	O	--	
LPUART	O	O	O	O	O ⁽³⁾	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	--	--	O ⁽⁴⁾	O	--	
ADC	O	O	--	--	--		--	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins



Table 5. Functionalities depending on the working mode (from Run/active down to standby)⁽¹⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Wakeup time to Run mode	0 μs	0.36 μs	3 μs	32 μs	3.5 μs	65 μs
Consumption V _{DD} =1.8 to 3.6 V (Typ)	Down to 115 μA/MHz (from Flash)	Down to 25 μA/MHz (from Flash)	Down to 6.5 μA	Down to 3.2 μA	0.35 μA (No RTC) V _{DD} =1.8 V	0.23 μA (No RTC) V _{DD} =1.8 V
					0.6 μA (with RTC) V _{DD} =1.8 V	0.39 μA (with RTC) V _{DD} =1.8 V
					0.38 μA (No RTC) V _{DD} =3.0 V	0.26 μA (No RTC) V _{DD} =3.0 V
					0.8 μA (with RTC) V _{DD} =3.0 V	0.57 μA (with RTC) V _{DD} =3.0 V

- Legend:
 "Y" = Yes (enable).
 "O" = Optional, can be enabled/disabled by software
 "-" = Not available
- Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
- UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
- I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2, TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-



Table 6. STM32L0xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 Arm® Cortex®-M0+ core

The Cortex-M0+ processor is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded Arm core, the STM32L041x6 are compatible with all Arm tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L041x6 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- $V_{SSA}, V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.4.2 Power supply supervisor

The devices feature an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the

internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7), USART2 (PA2, PA3) or USART2 (PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**

Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**

To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**

Three different clock sources can be used to drive the master clock SYSCLK:

 - 1-25 MHz high-speed external (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source**

Two ultra-low-power clock sources that can be used to drive the real-time clock:

 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC clock sources**

The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.
- **Startup clock**

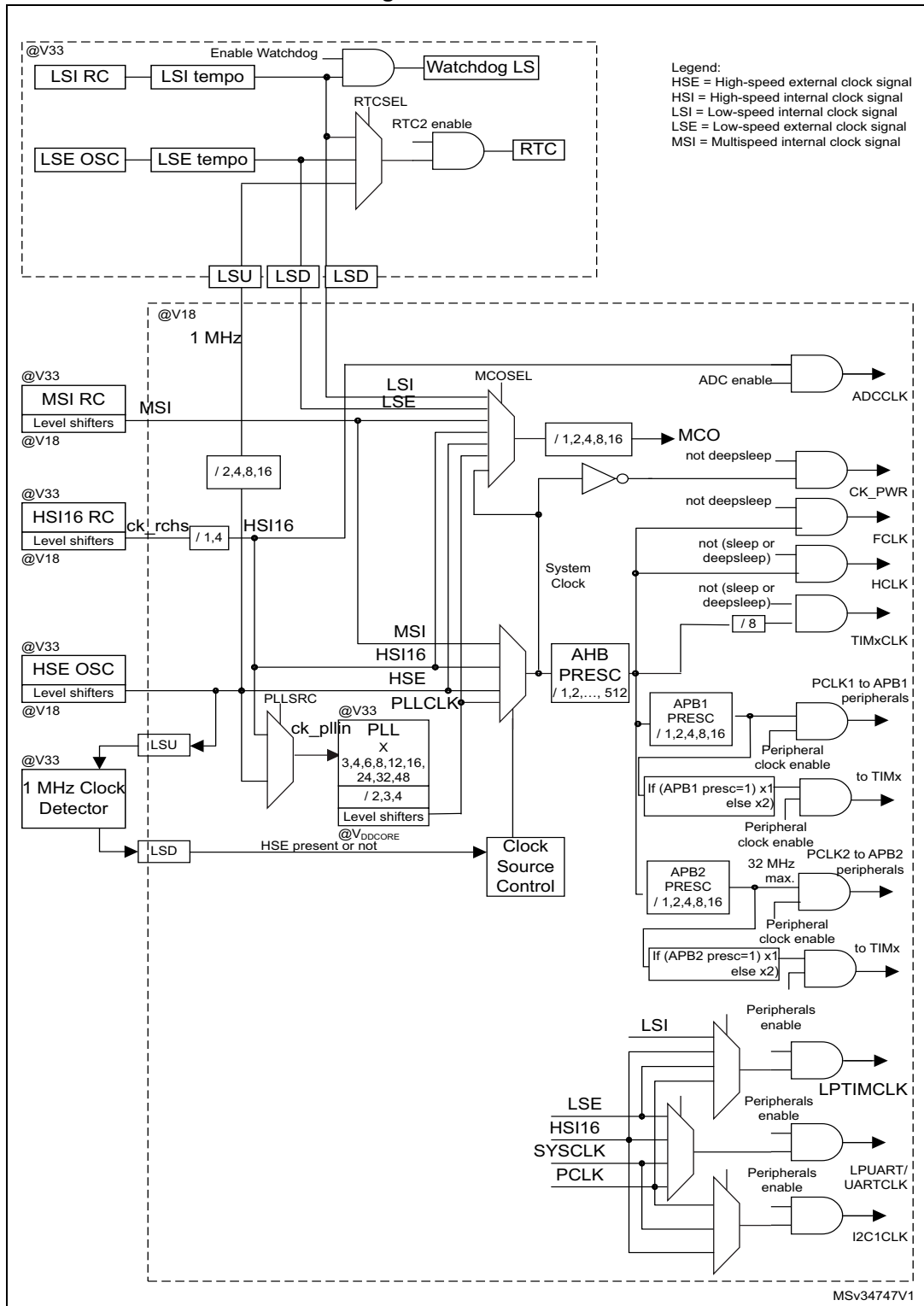
After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**

This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**

It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Figure 2. Clock tree



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIMER or comparator events.

3.8 Memories

The STM32L041x6 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 32 Kbytes of embedded Flash program memory
 - 1 Kbytes of data EEPROM
 - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0:** no protection
- **Level 1:** memory readout protected.
The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2:** chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: AES, SPI, I²C, USART, LPUART, general-purpose timers, and ADC.

3.10 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L041x6 devices. It has up to 10 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels are fast channels, PA0, PA4 and PA5, while the others are standard channels.

It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 μ A at 10 kSPS, ~200 μ A at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.11 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3 V$	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C, $V_{DDA} = 3 V$	0x1FF8 007E - 0x1FF8 007F

3.11.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (since no external voltage, V_{REF+} , is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C $V_{DDA} = 3 V$	0x1FF8 0078 - 0x1FF8 0079

3.12 Ultra-low-power comparators and reference voltage

The STM32L041x6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
 - External I/O pins
 - Internal reference voltage (V_{REFINT})
 - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 μ A typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT} .

3.14 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26):

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

The AES can be served by the DMA controller.

3.15 Timers and watchdogs

The ultra-low-power STM32L041x6 devices include three general-purpose timers, one low-power timer (LPTM), two watchdog timers and the SysTick timer.

[Table 9](#) compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

3.15.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L041x6 devices (see [Table 9](#) for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.15.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
 - Internal clock source: LSE, LSI, HSI or APB clock
 - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.15.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches '0'.

3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

One I²C interface (I2C1) can operate in multimaster or slave modes. The I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

The I²C interface supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 10. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Refer to [Table 11](#) for the supported modes and features of I2C interface.

Table 11. STM32L041x6 I²C implementation

I2C features ⁽¹⁾	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X ⁽²⁾
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.
2. See [Table 15: Pin definitions on page 38](#) for the list of I/Os that feature Fast Mode Plus capability

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

[Table 12](#) for the supported modes and features of USART interface.

Table 12. USART implementation

USART modes/features ⁽¹⁾	USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode ⁽²⁾	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.

2. This mode allows using the USART as an SPI master.

3.16.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while

having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.16.4 Serial peripheral interface (SPI)

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

The SPI can be served by the DMA controller.

Refer to [Table 13](#) for the supported modes and features of SPI interface.

Table 13. SPI implementation

SPI features ⁽¹⁾	SPI1
Hardware CRC calculation	X
I2S mode	-
TI mode	X

1. X = supported.

3.17 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

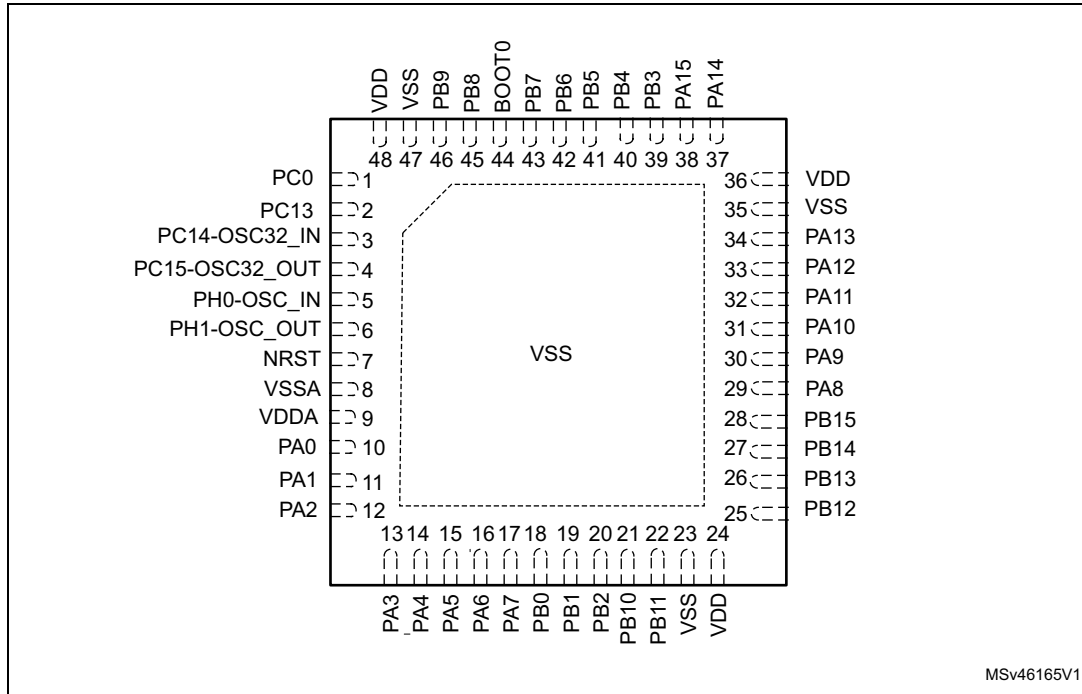
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.18 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pin descriptions

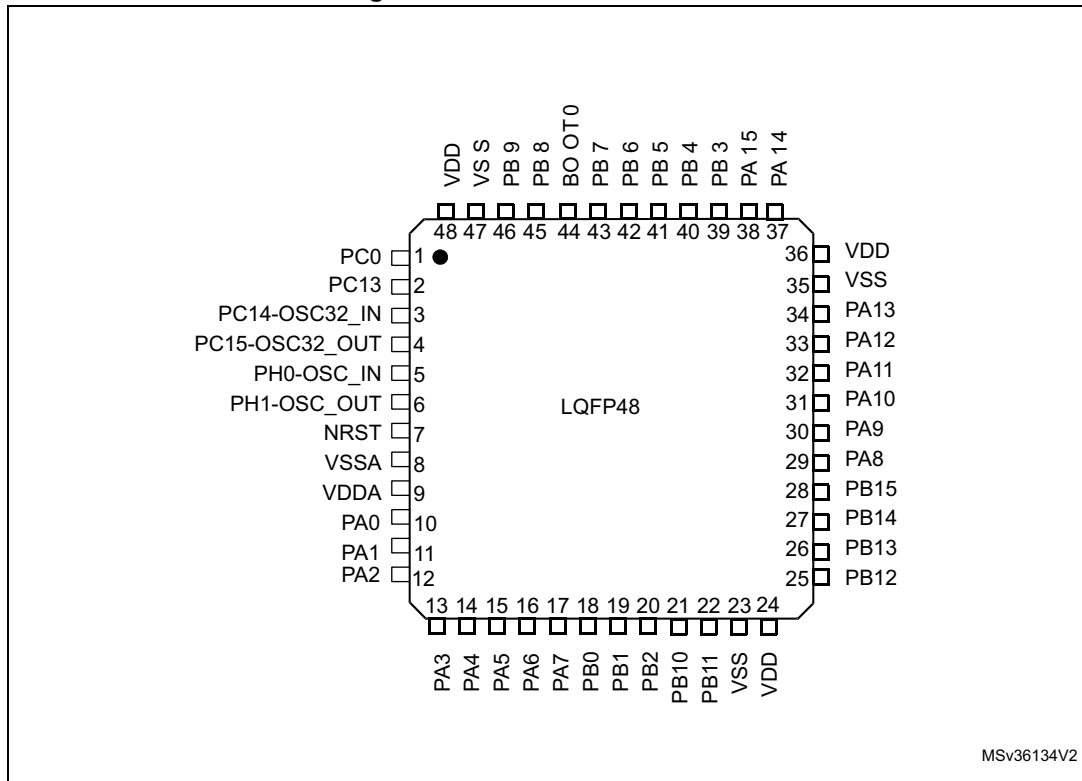
Figure 3. STM32L041x6 UFQFPN48



MSv46165V1

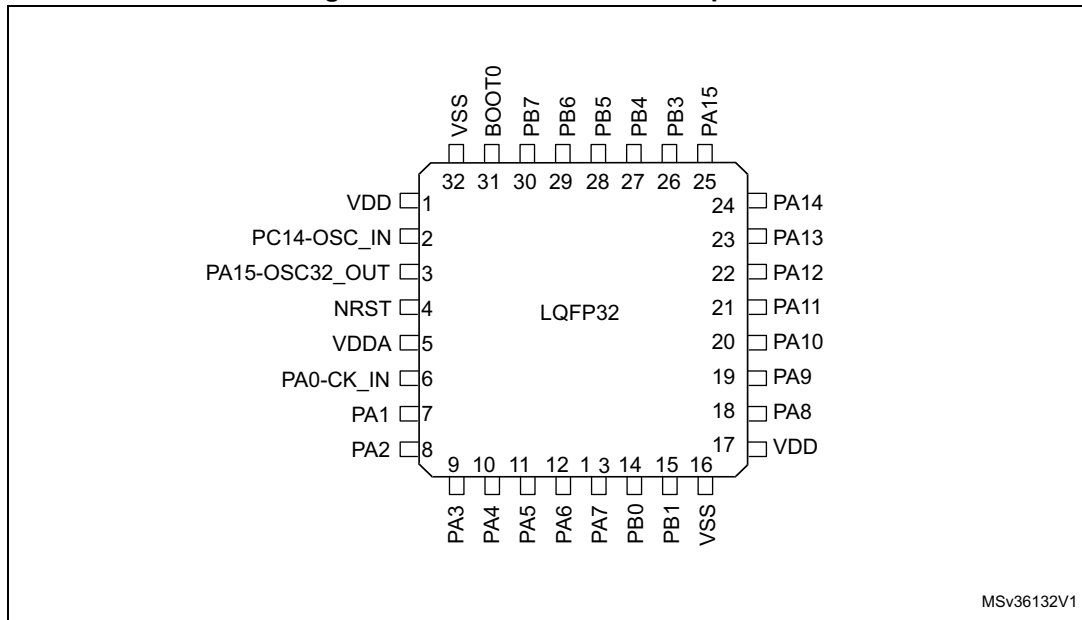
1. The above figure shows the package top view.

Figure 4. STM32L041x6 LQFP48



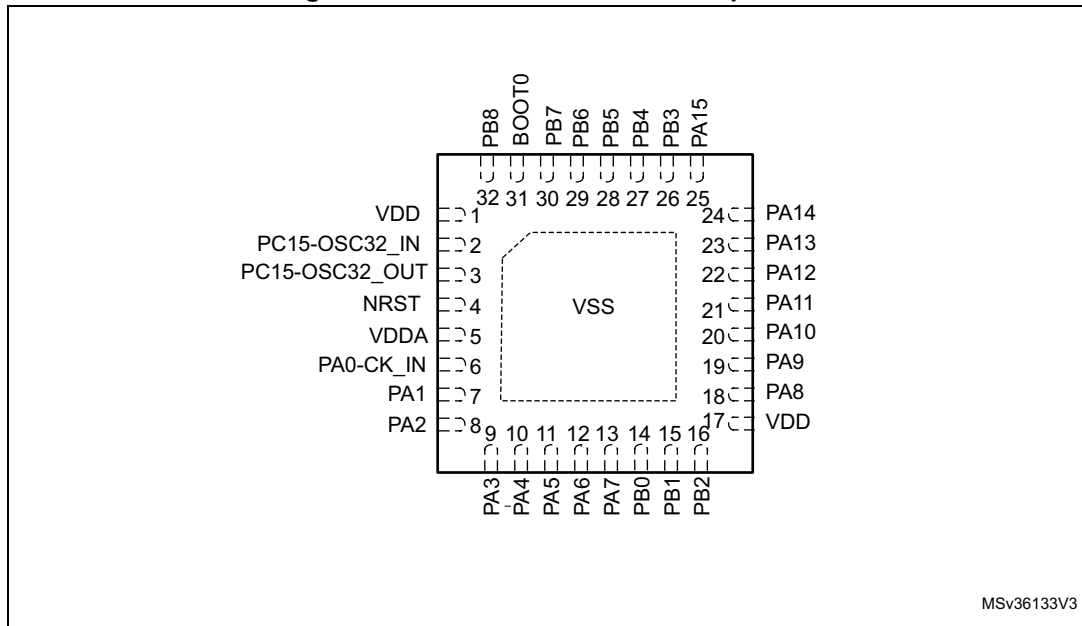
1. The above figure shows the package bump view.

Figure 5. STM32L041x6 LQFP32 pinout



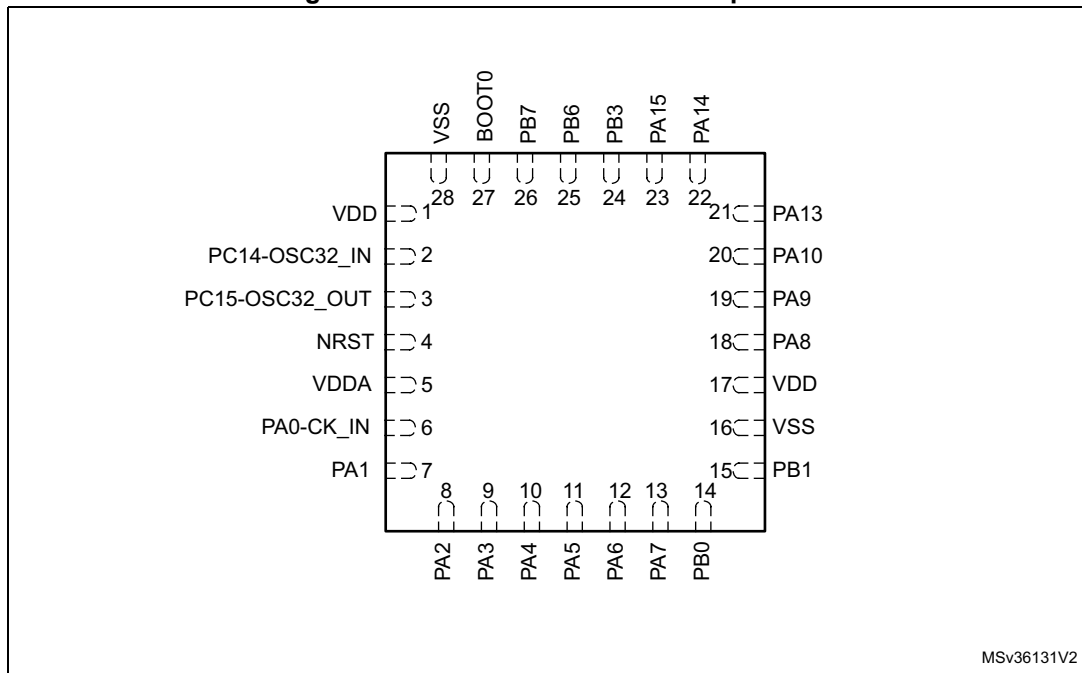
1. The above figure shows the package top view.

Figure 6. STM32L041x6 UFQFPN32 pinout



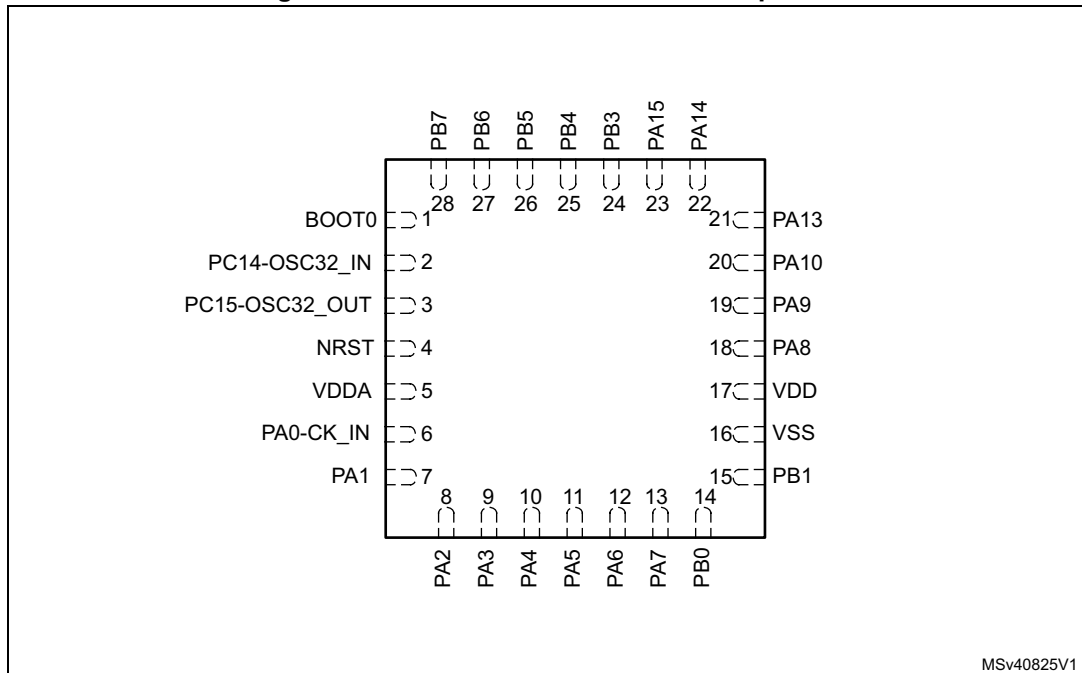
1. The above figure shows the package top view.

Figure 7. STM32L041x6 UFQFPN28 pinout



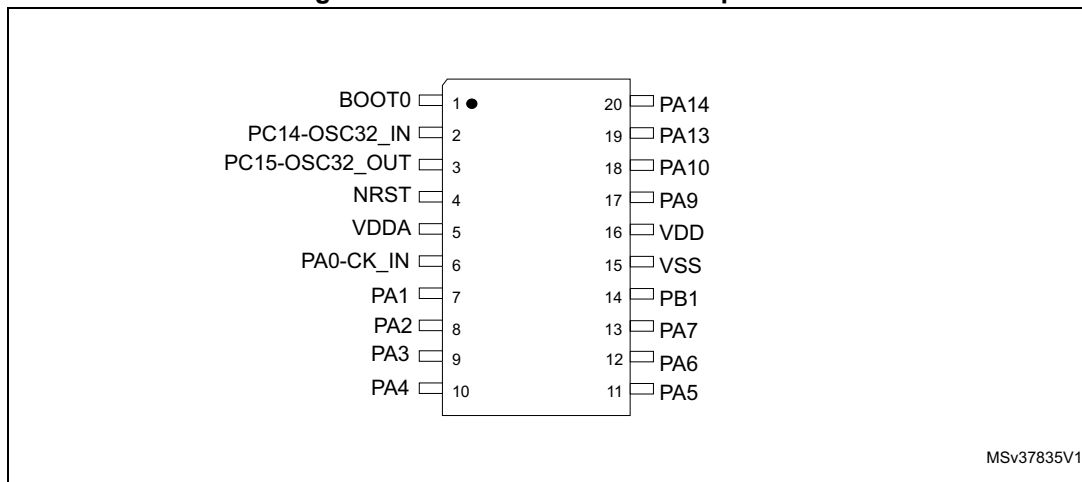
1. The above figure shows the package top view.
2. This pinout applies to all part numbers except for STM32L041G6UxS.

Figure 8. STM32L041G6UxS UFQFPN28 pinout



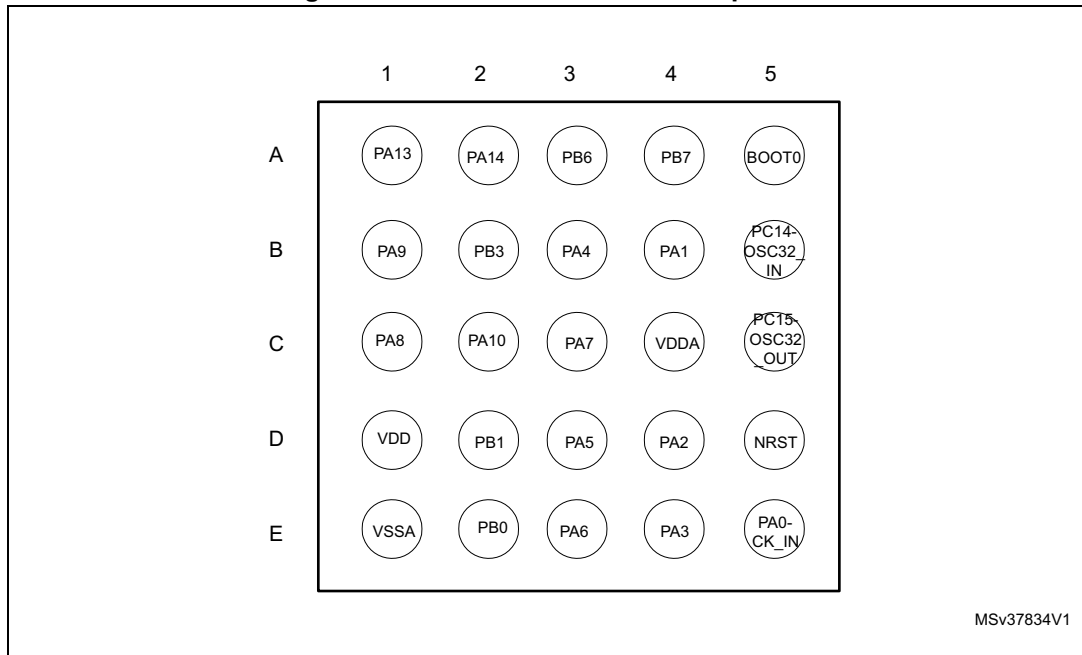
1. The above figure shows the package top view.
2. This pinout applies only to STM32L041G6UxS part number.

Figure 9. STM32L041x6 TSSOP20 pinout



1. The above figure shows the package top view.

Figure 10. STM32L041x6 WLCSP25 pinout



1. The above figure shows the package top view.

Table 14. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, FM+ capable
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

Table 15. Pin definitions

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041G6UxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	UFQFPN48						
-	-	-	-	-	-	2	2	PC13- ANTI_TAMP	I/O	FT	-	-	TAMP1/WKUP2
2	B5	2	2	2	2	3	3	PC14- OSC32_IN	I/O	TC	-	-	OSC32_IN
3	C5	3	3	3	3	4	4	PC15- OSC32_ OUT	I/O	TC	-	-	OSC32_OUT
-	-	-	-	-	-	5	5	PH0- OSC_IN	I/O	TC	-	-	-
-	-	-	-	-	-	6	6	PH1- OSC_OUT	I/O	TC	-	-	-
4	D5	4	4	4	4	7	7	NRST	I/O	-	-	-	-
-	-	-	-	-	-	1	1	PC0	I/O	FT	-	LPTIM1_IN1, EVENTOUT, LPUART1_RX	-
-	E1	-	-	-	"0"	8	8	VSSA	S	-	-	-	-
5	C4	5	5	5	5	9	9	VDDA	S	-	-	-	-
6	E5	6	6	6	6	-	-	PA0-CK_IN	I/O	TC	-	LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, COMP1_OUT	COMP1_INM6, ADC_IN0, RTC_TAMP2/WKUP1
-	-	-	-	-	-	10	10	PA0	I/O	TC	-	LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, COMP1_OUT	COMP1_INM6, ADC_IN0, RTC_TAMP2/WKUP1



Table 15. Pin definitions (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041G6UxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	UFQFPN48						
7	B4	7	7	7	7	11	11	PA1	I/O	FT	-	EVENTOUT, LPTIM1_IN2, TIM2_CH2, I2C1_SMBA, USART2_RTS/ USART2_DE, TIM21_ETR	COMP1_INP, ADC_IN1
8	D4	8	8	8	8	12	12	PA2	I/O	TC	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM6, ADC_IN2, RTC_TAMP3/RTC_TS /RTC_OUT/WKUP3
9	E4	9	9	9	9	13	13	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
10	B3	10	10	10	10	14	14	PA4	I/O	TC	-	SPI1_NSS, LPTIM1_IN1, USART2_CK, TIM22_ETR	COMP1_INM4, COMP2_INM4, ADC_IN4
11	D3	11	11	11	11	15	15	PA5	I/O	TC	-	SPI1_SCK, LPTIM1_IN2, TIM2_ETR, TIM2_CH1	COMP1_INM5, COMP2_INM5, ADC_IN5
12	E3	12	12	12	12	16	16	PA6	I/O	FT	-	SPI1_MISO, LPTIM1_ETR, LPUART1_CTS , TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6



Table 15. Pin definitions (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041G6UxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	UFQFPN48						
13	C3	13	13	13	13	17	17	PA7	I/O	FT	-	SPI1_MOSI, LPTIM1_OUT, USART2_CTS, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	E2	14	14	14	14	18	18	PB0	I/O	FT	-	EVENTOUT, SPI1_MISO, USART2_RTS/ USART2_DE, TIM2_CH3	ADC_IN8, VREF_OUT
14	D2	15	15	15	15	19	19	PB1	I/O	FT	-	USART2_CK, SPI1_MOSI, LPUART1_RTS /LPUART1_DE, TIM2_CH4	ADC_IN9, VREF_OUT
-	-	-	-	-	-	16	20	PB2	I/O	FT	-	LPTIM1_OUT	-
-	-	-	-	-	-	-	21	PB10	I/O	FT	-	TIM2_CH3, LPUART1_TX	-
-	-	-	-	-	-	-	22	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, LPUART1_RX	-
15	-	16	16	16	-	23	23	VSS	S	-	-	-	-
16	-	17	17	17	17	24	24	VDD	S	-	-	-	-
-	-	-	-	-	-	-	25	PB12	I/O	FT	-	SPI1_NSS, EVENTOUT	-

Table 15. Pin definitions (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041G6UxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	UFQFPN48						
-	-	-	-	-	-	26	26	PB13	I/O	FT	-	SPI1_SCK, MCO, TIM21_CH1, LPUART1_CTS	-
-	-	-	-	-	-	27	27	PB14	I/O	FT	-	SPI1_MISO, RTC_OUT, TIM21_CH2, LPUART1_RTS /LPUART1_DE	-
-	-	-	-	-	-	28	28	PB15	I/O	FT	-	SPI1_MOSI, RTC_REFIN	-
-	C1	18	18	18	18	29	29	PA8	I/O	FT	-	MCO, LPTIM1_IN1, EVENTOUT, USART2_CK, TIM2_CH1	-
17	B1	19	19	19	19	30	30	PA9	I/O	FT f	-	MCO, I2C1_SCL, USART2_TX, TIM22_CH1	-
18	C2	20	20	20	20	31	31	PA10	I/O	FT f	-	I2C1_SDA, USART2_RX, TIM22_CH2	-
-	-	-	-	21	21	32	32	PA11	I/O	FT	-	SPI1_MISO, EVENTOUT, USART2_CTS, TIM21_CH2, COMP1_OUT	-



Table 15. Pin definitions (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041G6UxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	UFQFPN48						
-	-	-	-	22	22	33	33	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART2_RTS/ USART2_DE, COMP2_OUT	-
19	A1	21	21	23	23	34	34	PA13	I/O	FT	-	SWDIO, LPTIM1_ETR, LPUART1_RX	-
-	-	-	-	-	-	35	35	VSS	S	-	-	-	-
-	D1	-	-	-	-	36	36	VDD	S	-	-	-	-
20	A2	22	22	24	24	37	37	PA14	I/O	FT	-	SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, LPUART1_TX	-
-	-	23	23	25	25	38	38	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	--
-	B2	24	24	26	26	39	39	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT	COMP2_INN
-	-	-	25	27	27	40	40	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TIM22_CH1	COMP2_INP

Table 15. Pin definitions (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25	UFQFPN28	UFQFPN28 (STM32L041G6UxS only)	LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	UFQFPN48						
-	-	-	26	28	28	41	41	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
-	A3	25	27	29	29	42	42	PB6	I/O	FT f	-	USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM21_CH1	COMP2_INP
-	A4	26	28	30	30	43	43	PB7	I/O	FT f	-	USART2_RX, I2C1_SDA, LPTIM1_IN2	COMP2_INP, VREF_PVD_IN
1	A5	27	1	31	31	44	44	BOOT0	I	-	-	-	-
-	-	-	-	-	32	45	45	PB8	I/O	FT f	-	I2C1_SCL	-
-	-	-	-	-	-	46	46	PB9	I/O	FT f	-	EVENTOUT, I2C1_SDA	-
-	-	28	-	32	-	47	47	VSS	S	-	-	-	-
-	-	1	-	1	1	48	48	VDD	S	-	-	-	-

1. VSS pins are connected to the exposed pad (see [Figure 42: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline](#)).

Table 16. Alternate functions

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port A	PA0	-	LPTIM1_IN1	TIM2_CH1	-	USART2_CTS	TIM2_ETR	-	COMP1_OUT
	PA1	EVENTOUT	LPTIM1_IN2	TIM2_CH2	I2C1_SMBA	USART2_RTS/ USART2_DE	TIM21_ETR	-	-
	PA2	TIM21_CH1	-	TIM2_CH3	-	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2	-	TIM2_CH4	-	USART2_RX	-	LPUART1_RX	
	PA4	SPI1_NSS	LPTIM1_IN1	-	-	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	LPTIM1_IN2	TIM2_ETR	-	-	TIM2_CH1	-	-
	PA6	SPI1_MISO	LPTIM1_ETR	-	-	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	LPTIM1_OUT	-	-	USART2_CTS	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	-	LPTIM1_IN1	EVENTOUT	USART2_CK	TIM2_CH1	-	-
	PA9	MCO	I2C1_SCL	-	-	USART2_TX	TIM22_CH1	-	-
	PA10	-	I2C1_SDA	-	-	USART2_RX	TIM22_CH2	-	-
	PA11	SPI1_MISO	-	EVENTOUT	-	USART2_CTS	TIM21_CH2	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	-	USART2_RTS/ USART2_DE	-	-	COMP2_OUT
	PA13	SWDIO	LPTIM1_ETR	-	-	-	-	LPUART1_RX	-
	PA14	SWCLK	LPTIM1_OUT	-	I2C1_SMBA	USART2_TX	-	LPUART1_TX	-
PA15	SPI1_NSS	-	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	-	-	



Table 16. Alternate functions (continued)

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port B	PB0	EVENTOUT	SPI1_MISO	-	-	USART2_RTS/ USART2_DE	TIM2_CH3	-	-
	PB1	USART2_CK	SPI1_MOSI	-	-	LPUART1_RTS /LPUART1_DE	TIM2_CH4	-	-
	PB2	-	-	LPTIM1_OUT	-	-	-	-	-
	PB3	SPI1_SCK	-	TIM2_CH2	-	EVENTOUT	-	-	-
	PB4	SPI1_MISO	-	EVENTOUT	-	TIM22_CH1	-	-	-
	PB5	SPI1_MOSI	-	LPTIM1_IN1	I2C1_SMBA	TIM22_CH2	-	-	-
	PB6	USART2_TX	I2C1_SCL	LPTIM1_ETR	-	-	TIM21_CH1	-	-
	PB7	USART2_RX	I2C1_SDA	LPTIM1_IN2	-	-	-	-	-
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	-	EVENTOUT	-	I2C1_SDA	-	-	-
	PB10	-	-	TIM2_CH3	-	-	-	LPUART1_TX	-
	PB11	EVENTOUT	-	TIM2_CH4	-	-	-	LPUART1_RX	-
	PB12	SPI1_NSS	-	-	-	-	-	EVENTOUT	-
	PB13	SPI1_SCK	-	MCO	-	-	TIM21_CH1	LPUART1_CTS	-
	PB14	SPI1_MISO	-	RTC_OUT	-	-	TIM21_CH2	LPUART1_RTS /LPUART1_DE	-
PB15	SPI1_MOSI	-	RTC_REFIN	-	-	-	-	-	
Port C	PC0	LPTIM1_IN1	-	EVENTOUT	-	-	-	LPUART1_RX	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 3.6\text{ V}$ (for the $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

6.1.3 Typical curves

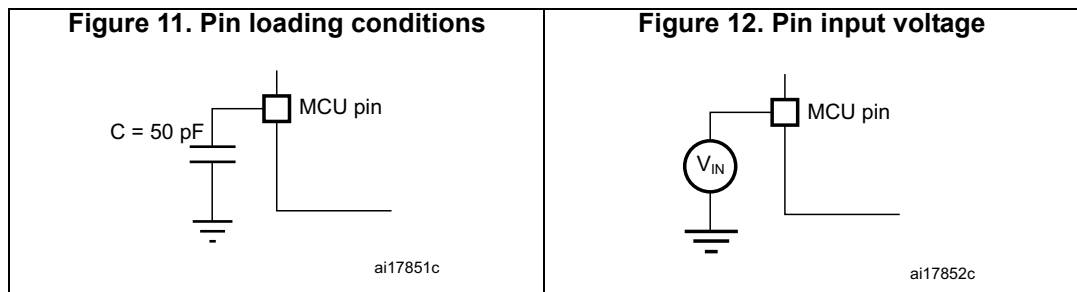
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 11](#).

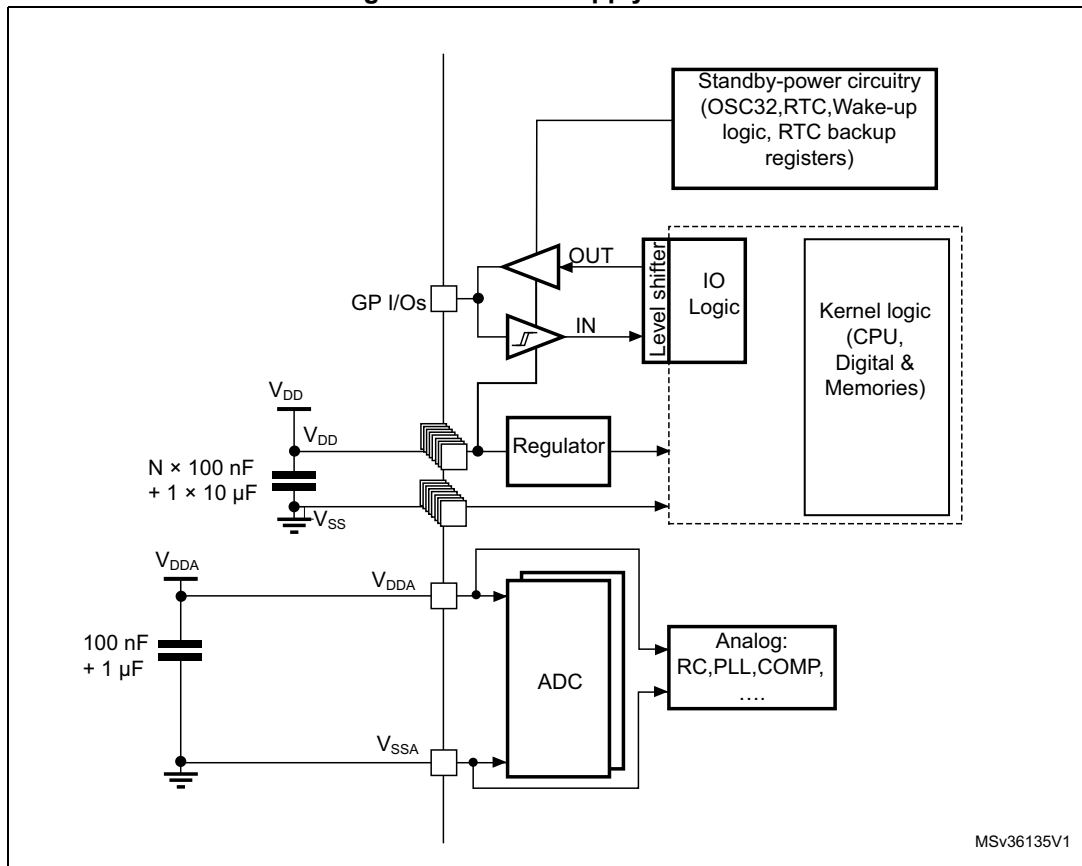
6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 12](#).



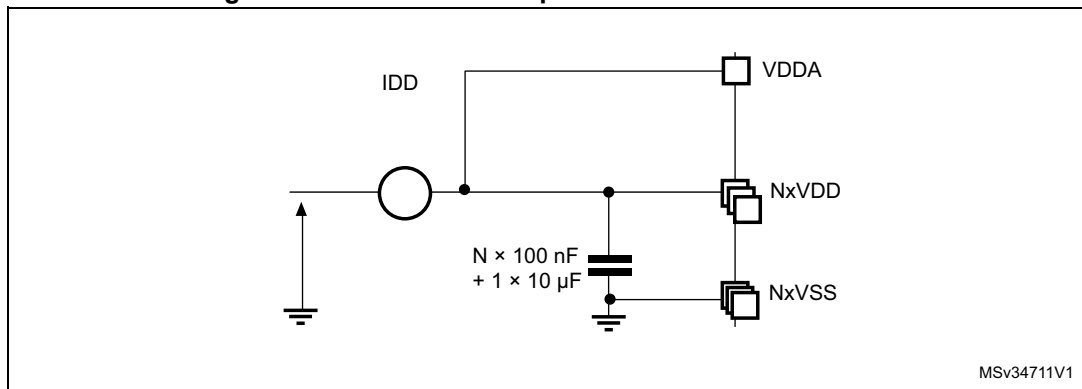
6.1.6 Power supply scheme

Figure 13. Power supply scheme



6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 17: Voltage characteristics](#), [Table 18: Current characteristics](#), and [Table 19: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 17. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} , V_{DD}) ⁽¹⁾	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS}-0.3$	$V_{DD}+4.0$	
	Input voltage on TC pins	$V_{SS}-0.3$	4.0	
	Input voltage on BOOT0	V_{SS}	$V_{DD}+4.0$	
	Input voltage on any other pin	$V_{SS}-0.3$	4.0	
$ \Delta V_{DD} $	Variations between different V_{DDx} power pins	-	50	mV
$ V_{DDA}-V_{DDx} $	Variations between any V_{DDx} and V_{DDA} power pins ⁽³⁾	-	300	
$ \Delta V_{SS} $	Variations between all different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.11		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 18](#) for maximum allowed injected current values.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation.

Table 18. Current characteristics

Symbol	Ratings	Max.	Unit
$\Sigma I_{VDD}^{(2)}$	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	105	mA
$\Sigma I_{VSS}^{(2)}$	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	105	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}^{(3)}$	Total output current sunk by sum of all IOs and control pins ⁽⁴⁾	45	
	Total output current sourced by sum of all IOs and control pins ⁽⁴⁾	-45	
$\Sigma I_{IO(PIN)}^{(5)}$	Total output current sunk by sum of all IOs and control pins ⁽²⁾	90	
	Total output current sourced by sum of all IOs and control pins ⁽²⁾	-90	
$I_{INJ(PIN)}$	Injected current on FT, FFf, RST and B pins	-5/+0 ⁽⁶⁾	
	Injected current on TC pin	± 5 ⁽⁷⁾	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁸⁾	± 25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. These values apply only to STM32L041G6UxS part number
4. This current consumption must be correctly distributed over all I/Os and control pins. In particular, it must be located the closest possible to the couple of supply and ground, and distributed on both sides.
5. These values apply to all part numbers except for STM32L041G6UxS
6. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 17](#) for maximum allowed input voltage values.
7. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 17: Voltage characteristics](#) for the maximum allowed input voltage values.
8. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C



6.3 Operating conditions

6.3.1 General operating conditions

Table 20. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}	Analog operating voltage (all features)	Must be the same voltage as V_{DD} ⁽¹⁾	1.65	3.6	V
V_{IN}	Input voltage on FT, FTf and RST pins ⁽²⁾	$2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-0.3	5.5	V
		$1.65\text{ V} \leq V_{DD} \leq 2.0\text{ V}$	-0.3	5.2	
	Input voltage on BOOT0 pin	-	0	5.5	
	Input voltage on TC pin	-	-0.3	$V_{DD}+0.3$	
P_D	Power dissipation at $T_A = 85\text{ °C}$ (range 6) or $T_A = 105\text{ °C}$ (range 7) ⁽³⁾	LQFP48 package	-	351	mW
		UFQFPN48 package	-	625	
		LQFP32 package	-	333	
		UFQFPN32 package	-	513	
		UFQFPN28 package	-	167	
		WLCSP25 package	-	286	
		TSSOP20 package	-	333	
	Power dissipation at $T_A = 125\text{ °C}$ (range 3) ⁽³⁾	LQFP48 package	-	88	
		UFQFPN48 package	-	156	
		LQFP32 package	-	83	
		UFQFPN32 package	-	128	
		UFQFPN28 package	-	42	
		WLCSP25 package	-	71	
		TSSOP20 package	-	83	

Table 20. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T _A	Temperature range	Maximum power dissipation (range 6)	-40	85	°C
		Maximum power dissipation (range 7)	-40	105	
		Maximum power dissipation (range 3)	-40	125	
T _J	Junction temperature range (range 6)	-40 °C ≤ T _A ≤ 85 °	-40	105	
	Junction temperature range (range 7)	-40 °C ≤ T _A ≤ 105 °C	-40	125	
	Junction temperature range (range 3)	-40 °C ≤ T _A ≤ 125 °C	-40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see [Table 19: Thermal characteristics on page 50](#)).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in [Table 20](#).

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{VDD} ⁽¹⁾	V _{DD} rise time rate	BOR detector enabled	0	-	∞	μs/V
		BOR detector disabled	0	-	1000	
	V _{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
T _{RSTTEMPO} ⁽¹⁾	Reset temporization	V _{DD} rising, BOR enabled	-	2	3.3	ms
		V _{DD} rising, BOR disabled ⁽²⁾	0.4	0.7	1.6	
V _{POR/PDR}	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V _{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V _{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V _{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

Table 21. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	V
		Rising edge	2.54	2.66	2.7	
V _{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V _{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V _{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V _{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V _{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V _{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V _{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V _{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V _{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in [Table 23](#) are based on characterization results, unless otherwise specified.

Table 22. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C, V _{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 23. Embedded internal reference voltage⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{REFINT_out} ⁽²⁾	Internal reference voltage	-40 °C < T _J < +125 °C	1.202	1.224	1.242	V
T _{VREFINT}	Internal reference startup time	-	-	2	3	ms
V _{VREF_MEAS}	V _{DDA} voltage during V _{REFINT} factory measure	-	2.99	3	3.01	V
A _{VREF_MEAS}	Accuracy of factory-measured V _{REFINT} value ⁽³⁾	Including uncertainties due to ADC and V _{DDA} values	-	-	±5	mV
T _{Coef} ⁽⁴⁾	Temperature coefficient	-40 °C < T _J < +125 °C	-	25	100	ppm/°C
A _{Coef} ⁽⁴⁾	Long-term stability	1000 hours, T = 25 °C	-	-	1000	ppm
V _{DDCoef} ⁽⁴⁾	Voltage coefficient	3.0 V < V _{DDA} < 3.6 V	-	-	2000	ppm/V
T _{S_vrefint} ⁽⁴⁾⁽⁵⁾	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T _{ADC_BUF} ⁽⁴⁾	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I _{BUF_ADC} ⁽⁴⁾	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I _{VREF_OUT} ⁽⁴⁾	VREF_OUT output current ⁽⁶⁾	-	-	-	1	µA
C _{VREF_OUT} ⁽⁴⁾	VREF_OUT output load	-	-	-	50	pF
I _{LPBUF} ⁽⁴⁾	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V _{REFINT_DIV1} ⁽⁴⁾	1/4 reference voltage	-	24	25	26	% V _{REFINT}
V _{REFINT_DIV2} ⁽⁴⁾	1/2 reference voltage	-	49	50	51	
V _{REFINT_DIV3} ⁽⁴⁾	3/4 reference voltage	-	74	75	76	

1. Refer to [Table 35: Peripheral current consumption in Stop and Standby mode](#) for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in [Figure 14: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20: General operating conditions](#) unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to OSCI_IN input (LQFP48 package) and to CK_IN (other packages). It follows the characteristic specified in [Table 37: High-speed external user clock characteristics](#)
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in [Table 44](#), [Table 20](#) and [Table 21](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 24. Current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL on) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	140	200	μA
				2 MHz	245	310	
				4 MHz	460	540	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10,	4 MHz	0.56	0.63	mA
				8 MHz	1.1	1.2	
				16 MHz	2.1	2.3	
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4		
			16 MHz	2.5	2.7		
			32 MHz	5	5.6		
		HSI clock	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10,	16 MHz	2.1	2.4	
				Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	5.1	5.7
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	34.5	110	μA
524 kHz	86			150			
4.2 MHz	505			570			

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 25. Current consumption in Run mode vs code type, code with data processing running from Flash memory

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Unit	
I _{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash memory	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽¹⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	460	μA
				CoreMark		455	
				Fibonacci		330	
				while(1)		305	
				while(1), prefetch OFF		320	
		Range 1, VOS[1:0]=01, V _{CORE} =1.8 V	Dhrystone	32 MHz	5	mA	
			CoreMark		5.15		
			Fibonacci		5		
			while(1)		4.35		
			while(1), prefetch OFF		3.85		

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).



Figure 15. I_{DD} vs V_{DD} , at $T_A = 25/55/85/105^\circ\text{C}$, Run mode, code running from Flash memory, Range 2, HSE = 16 MHz, 1WS

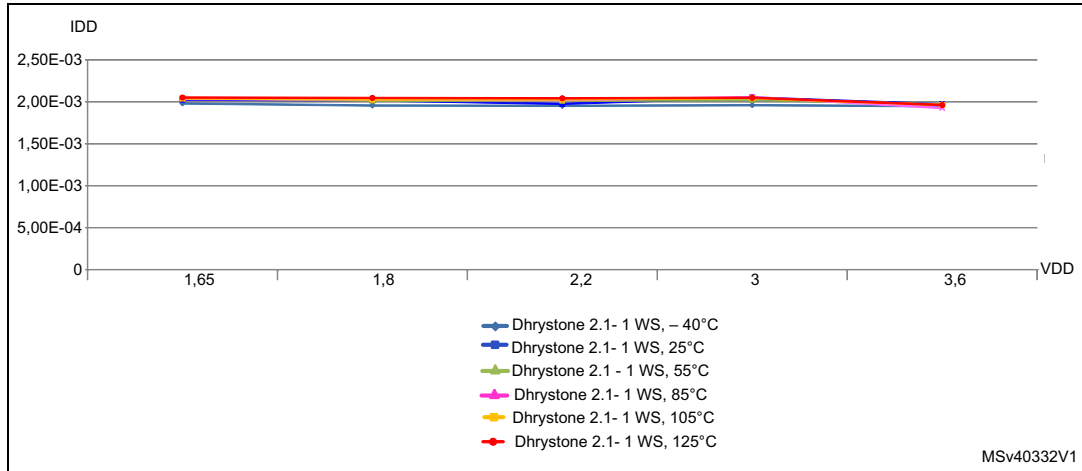


Figure 16. I_{DD} vs V_{DD} , at $T_A = 25/55/85/105^\circ\text{C}$, Run mode, code running from Flash memory, Range 2, HSI16, 1WS

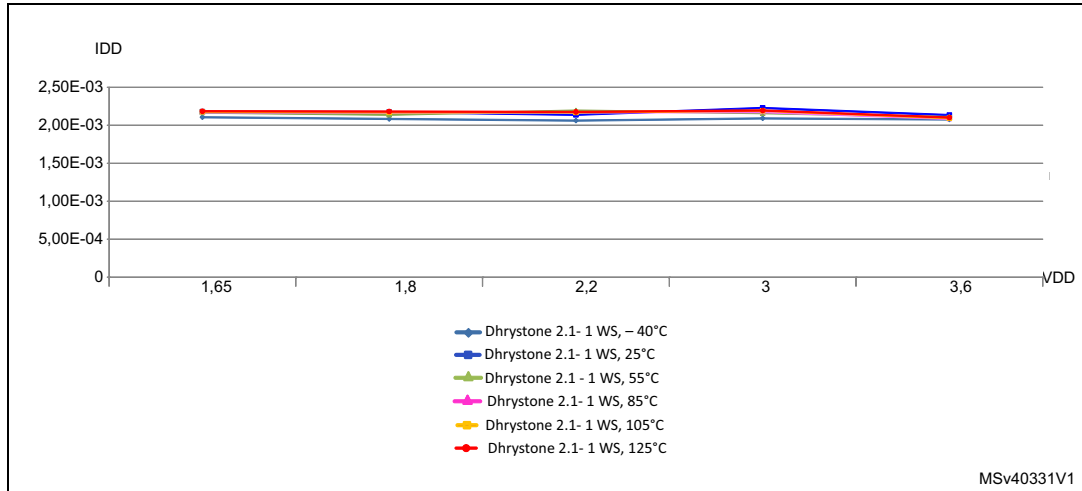


Table 26. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched OFF	f _{HSE} = f _{HCLK} up to 16 MHz, included f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	115	170	μA
				2 MHz	210	250	
				4 MHz	385	420	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	0.48	0.6	mA
				8 MHz	0.935	1.1	
				16 MHz	1.8	2	
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	1.1	1.3	mA	
			16 MHz	2.1	2.3		
			32 MHz	4.5	4.7		
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	22	52	μA
				524 kHz	70.5	91	
				4.2 MHz	420	450	
HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	1.95	2.2	mA		
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	4.7		5.1	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 27. Current consumption in Run mode vs code type, code with data processing running from RAM⁽¹⁾

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Unit	
I _{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched OFF	f _{HSE} = f _{HCLK} up to 16 MHz, included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	385	μA
				CoreMark		395	
				Fibonacci		360	
				while(1)		265	
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	4.5	mA	
			CoreMark		4.65		
			Fibonacci		4.2		
			while(1)		3.05		

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).



Table 28. Current consumption in Sleep mode

Symbol	Parameter	Conditions	f _{HCLK}	Typ	Max ⁽¹⁾	Unit	
I _{DD} (Sleep)	Supply current in Sleep mode, Flash memory OFF	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	36.5	87	μA
				2 MHz	58	100	
				4 MHz	100	170	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	125	190	
				8 MHz	230	310	
				16 MHz	450	540	
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	275	360		
			16 MHz	555	650		
			32 MHz	1350	1600		
		HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	585	690	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	17	43	
	524 kHz			28	55		
	4.2 MHz			115	190		
	Supply current in Sleep mode, Flash memory ON	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	49	160	
				2 MHz	69	190	
				4 MHz	115	230	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	135	200	
				8 MHz	240	320	
				16 MHz	460	550	
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	290	370		
			16 MHz	565	670		
			32 MHz	1350	1600		
		HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	600	700	
Range 1, V _{CORE} =1.8 V, VOS[1:0]=01			32 MHz	1500	1700		
MSI clock		Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	28	55		
	524 kHz		39.5	67			
	4.2 MHz		125	200			

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).



Table 29. Current consumption in Low-power run mode

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit	
I _{DD} (LP Run)	Supply current in Low-power run mode	All peripherals off, code executed from RAM, Flash memory OFF, V _{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f _{HCLK} = 32 kHz	T _A = -40 °C to 25 °C	6.3	8.4	μA
				T _A = 85 °C	9.15	13	
				T _A = 105 °C	12.5	19	
				T _A = 125 °C	20.5	36	
			MSI clock, 65 kHz f _{HCLK} = 65 kHz	T _A = -40 °C to 25 °C	9.45	12	
				T _A = 85 °C	12.5	15	
				T _A = 105 °C	16	22	
				T _A = 125 °C	24	38	
			MSI clock, 131 kHz f _{HCLK} = 131 kHz	T _A = -40 °C to 25 °C	17	20	
				T _A = 55 °C	19	21	
				T _A = 85 °C	20.5	24	
				T _A = 105 °C	23.5	28	
		All peripherals off, code executed from Flash memory, V _{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f _{HCLK} = 32 kHz	T _A = -40 °C to 25 °C	18.5	23	
				T _A = 85 °C	23	27	
				T _A = 105 °C	27	33	
				T _A = 125 °C	36	52	
			MSI clock, 65 kHz f _{HCLK} = 65 kHz	T _A = -40 °C to 25 °C	22.5	26	
				T _A = 85 °C	27.5	31	
				T _A = 105 °C	31	38	
				T _A = 125 °C	40.5	56	
			MSI clock, 131 kHz f _{HCLK} = 131 kHz	T _A = -40 °C to 25 °C	32	36	
				T _A = 55 °C	35	37	
				T _A = 85 °C	37.5	42	
				T _A = 105 °C	41	47	
		T _A = 125 °C	50	65			

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.



Figure 17. I_{DD} vs V_{DD} , at $T_A = 25/55/ 85/105/125$ °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

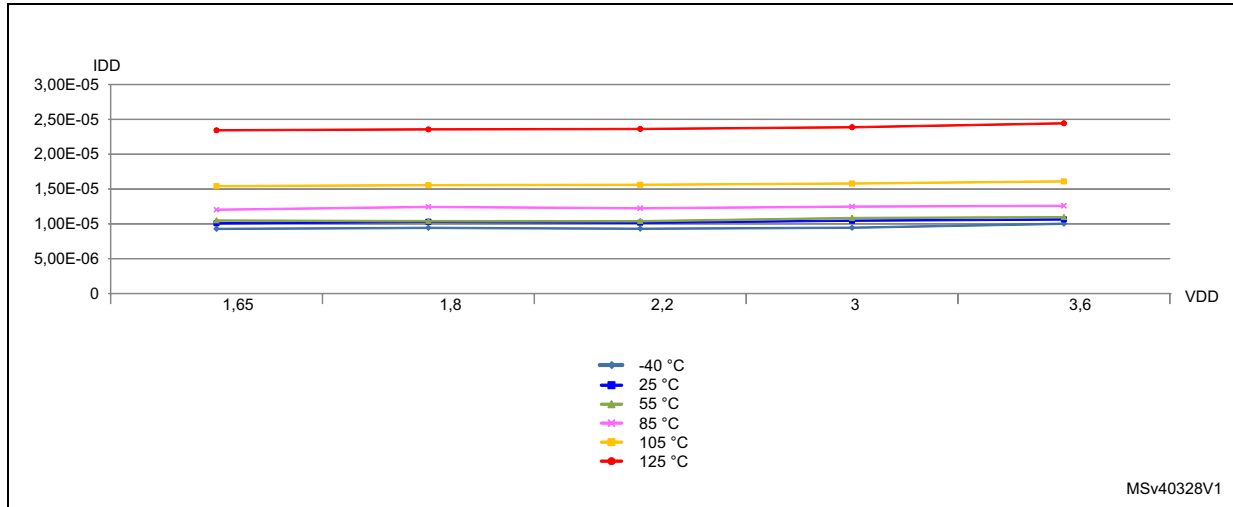


Table 30. Current consumption in Low-power Sleep mode

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit	
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals off, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz Flash memory OFF	$T_A = -40$ °C to 25 °C	3.2 ⁽²⁾	-	μA
				$T_A = -40$ °C to 25 °C	13	19	
			MSI clock, 65 kHz $f_{HCLK} = 32$ kHz Flash memory ON	$T_A = 85$ °C	16	21	
				$T_A = 105$ °C	18.5	24	
				$T_A = 125$ °C	23.5	32	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz, Flash memory ON	$T_A = -40$ °C to 25 °C	13.5	19	
				$T_A = 85$ °C	16.5	21	
				$T_A = 105$ °C	18.5	24	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz, Flash memory ON	$T_A = 125$ °C	24	33	
				$T_A = -40$ °C to 25 °C	15.5	21	
				$T_A = 55$ °C	17.5	22	
				$T_A = 85$ °C	18.5	23	
				$T_A = 105$ °C	21	26	
$T_A = 125$ °C	26	35					

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly 12 μA) is the same whatever the clock frequency.

Table 31. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
I _{DD} (Stop)	Supply current in Stop mode	T _A = -40°C to 25°C	0.38	0.99	μA
		T _A = 55°C	0.54	1.9	
		T _A = 85°C	1.35	4.2	
		T _A = 105°C	3.1	9	
		T _A = 125°C	7.55	19	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Figure 18. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

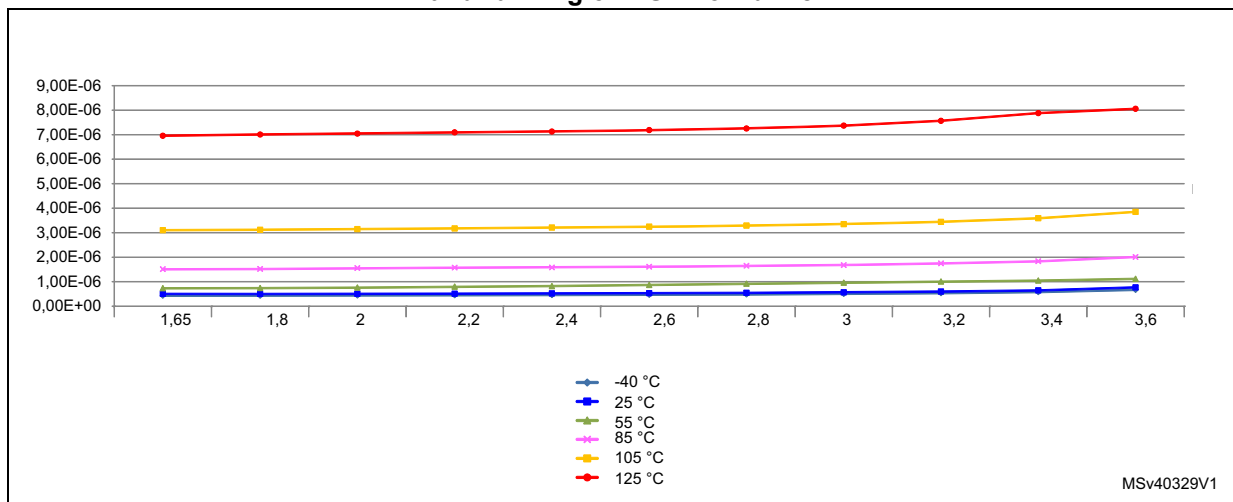


Figure 19. I_{DD} vs V_{DD}, at T_A= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off

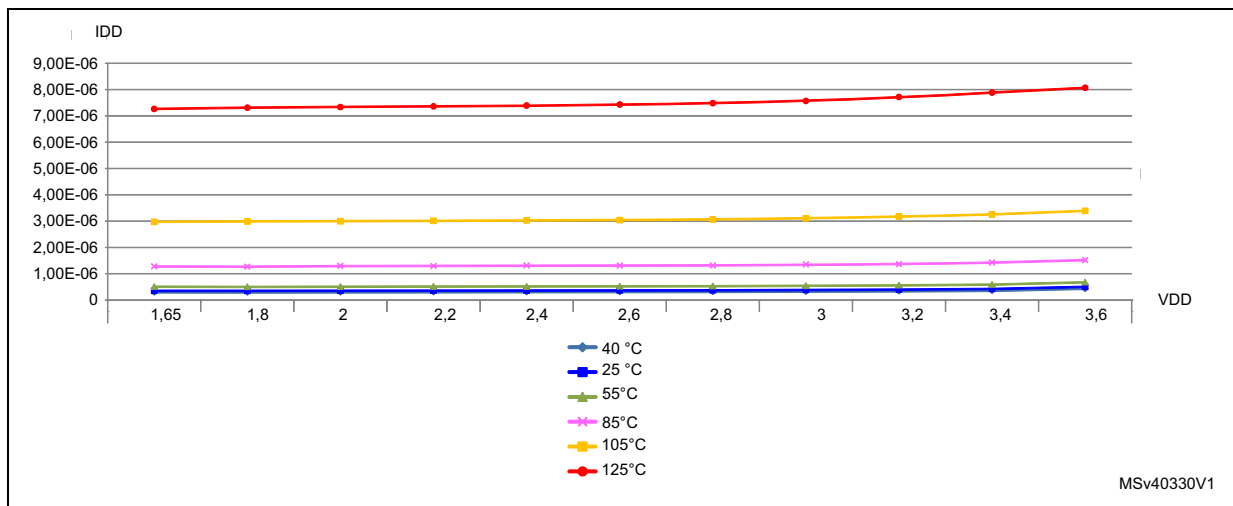


Table 32. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
I _{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	T _A = -40 °C to 25 °C	0.8	1.6	μA
			T _A = 55 °C	0.9	1.8	
			T _A = 85 °C	1	2	
			T _A = 105 °C	1.3	3	
			T _A = 125 °C	2.15	7	
		Independent watchdog and LSI off	T _A = -40 °C to 25 °C	0.255	0.6	
			T _A = 55 °C	0.28	0.7	
			T _A = 85 °C	0.405	1	
			T _A = 105 °C	0.7	1.7	
			T _A = 125 °C	1.55	5	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

Table 33. Average current consumption during wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I _{DD} (WU from Stop)	Supply current during wakeup from Stop mode	HSI	1	mA
		HSI/4	0.7	
		MSI 4,2 MHz	0.7	
		MSI 1,05 MHz	0.4	
		MSI 65 KHz	0.1	
I _{DD} (Reset)	Reset pin pulled down	-	0.21	
I _{DD} (Power Up)	BOR on	-	0.23	
I _{DD} (WU from StandBy)	With Fast wakeup set	MSI 2,1 MHz	0.5	
	With Fast wakeup disabled	MSI 2,1 MHz	0.12	

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on

Table 34. Peripheral current consumption in Run or Sleep mode⁽¹⁾

Peripheral		Typical consumption, $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$				Unit
		Range 1, $V_{CORE}=1.8\text{ V}$ $VOS[1:0] = 01$	Range 2, $V_{CORE}=1.5\text{ V}$ $VOS[1:0] = 10$	Range 3, $V_{CORE}=1.2\text{ V}$ $VOS[1:0] = 11$	Low-power sleep and run	
APB1	WWDG	3	2	2	2	$\mu\text{A}/\text{MHz}$ (f_{HCLK})
	LPUART1	8	6.5	5.5	6	
	I2C1	11	9.5	7.5	9	
	LPTIM1	10	8.5	6.5	8	
	TIM2	10.5	8.5	7	9	
	USART2	14.5	12	9.5	11	
APB2	ADC1 ⁽²⁾	5.5	5	3.5	4	$\mu\text{A}/\text{MHz}$ (f_{HCLK})
	SPI1	4	3	3	2.5	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	$\mu\text{A}/\text{MHz}$ (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	$\mu\text{A}/\text{MHz}$ (f_{HCLK})
	FLASH	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	
	AES	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	
	DMA1	10	8	6.5	8.5	
All enabled		101	83	66	85	
PWR		2.5	2	2	1	$\mu\text{A}/\text{MHz}$ (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: $f_{HCLK} = 32\text{ MHz}$ (range 1), $f_{HCLK} = 16\text{ MHz}$ (range 2), $f_{HCLK} = 4\text{ MHz}$ (range 3), $f_{HCLK} = 64\text{ kHz}$ (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.



2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 μA .

Table 35. Peripheral current consumption in Stop and Standby mode⁽¹⁾

Symbol	Peripheral	Typical consumption, $T_A = 25\text{ }^\circ\text{C}$		Unit
		$V_{DD}=1.8\text{ V}$	$V_{DD}=3.0\text{ V}$	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	μA
I_{REFINT}	-	1.3	1.4	
-	LSE Low drive ⁽²⁾	0.1	0.1	
-	LSI	0.27	0.31	
-	IWDG	0.2	0.3	
-	LPTIM1, Input 100 Hz	0.01	0.01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0.2	0.2	
-	RTC (LSE in Bypass mode)	0.2	0.2	

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	$f_{HCLK} = 32 \text{ MHz}$	7	8	Number of clock cycles
$t_{WUSLEEP_LP}$	Wakeup from Low-power sleep mode, $f_{HCLK} = 262 \text{ kHz}$	$f_{HCLK} = 262 \text{ kHz}$ Flash memory enabled	7	8	
		$f_{HCLK} = 262 \text{ kHz}$ Flash memory switched OFF	9	10	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	5.0	8	μs
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	7.3	13	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	13	23	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	28	38	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	51	65	
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	100	120	
		$f_{HCLK} = \text{MSI} = 65 \text{ kHz}$	200	260	
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
		Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	
$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	7.9		10		
$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	4.7		8		
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	$f_{HCLK} = \text{MSI} = 2.1 \text{ MHz}$	65	130	ms
	Wakeup from Standby mode FWU bit = 0	$f_{HCLK} = \text{MSI} = 2.1 \text{ MHz}$	2.2	3	

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

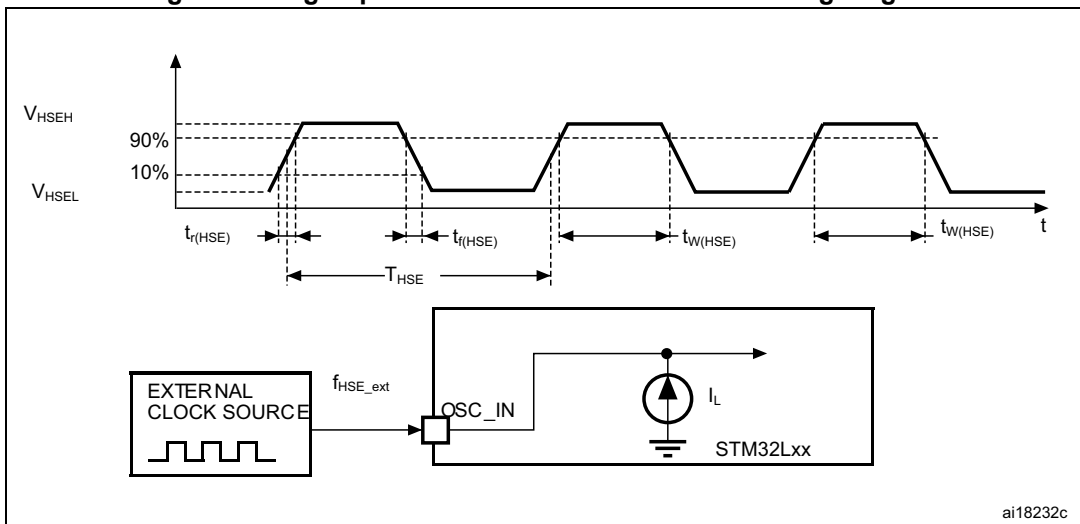
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.12](#). However, the recommended clock input waveform is shown in [Figure 20](#).

Table 37. High-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN/CK_IN ⁽²⁾ input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN/CK_IN ⁽²⁾ input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN/CK_IN ⁽²⁾ high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN/CK_IN ⁽²⁾ rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN/CK_IN ⁽²⁾ input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN/CK_IN ⁽²⁾ Input leakage current		$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1

1. Guaranteed by design.
2. HSE external user clock is applied to OSC_IN on LQFP48 package and to CK_IN on other packages.

Figure 20. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

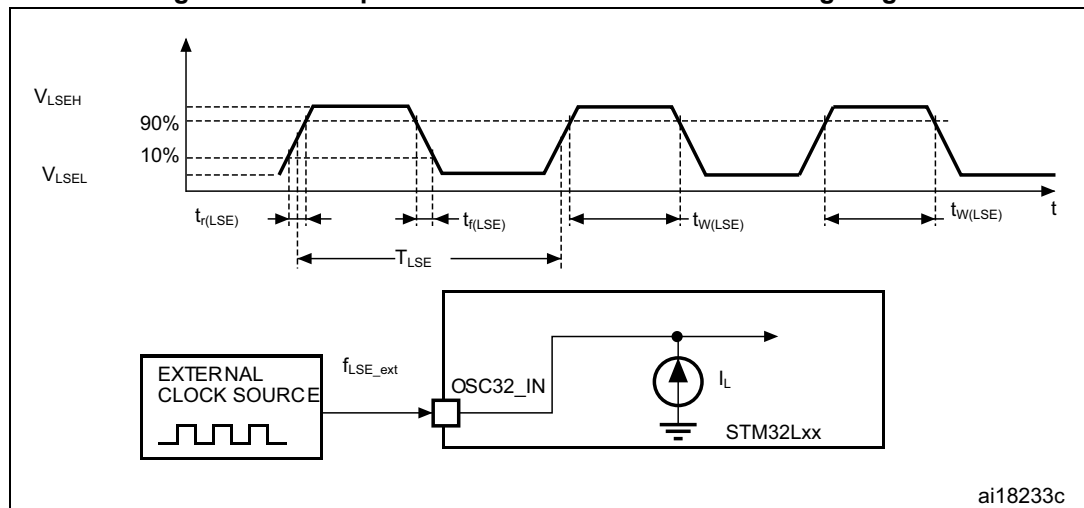
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 20](#).

Table 38. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency		1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{r(LSE)}$	OSC32_IN rise or fall time	-	-	10		
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy(LSE)$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator (LQFP48 package only). All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 39](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

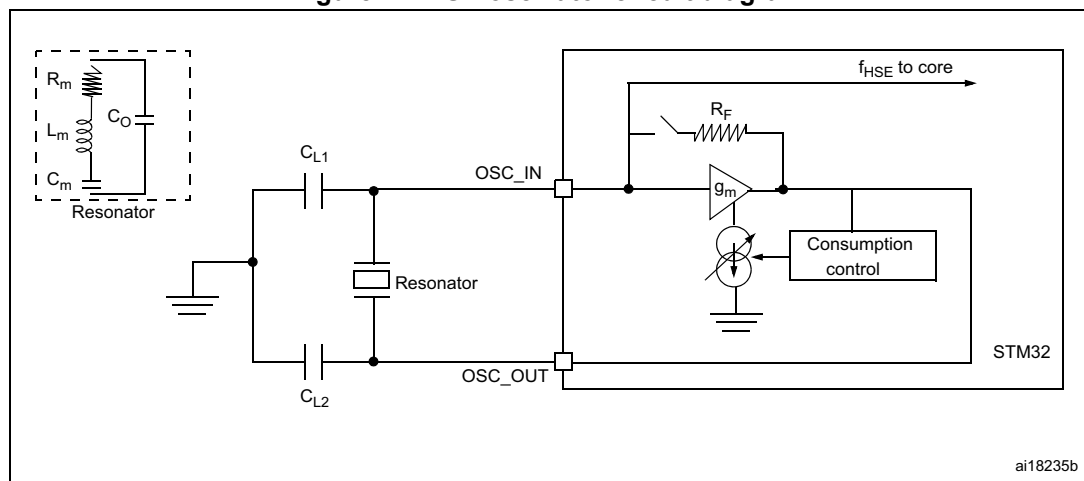
Table 39. HSE oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		25	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
G_m	Maximum critical crystal transconductance	Startup	-	-	700	$\mu A/V$
$t_{SU(HSE)}^{(2)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 22](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 22. HSE oscillator circuit diagram



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

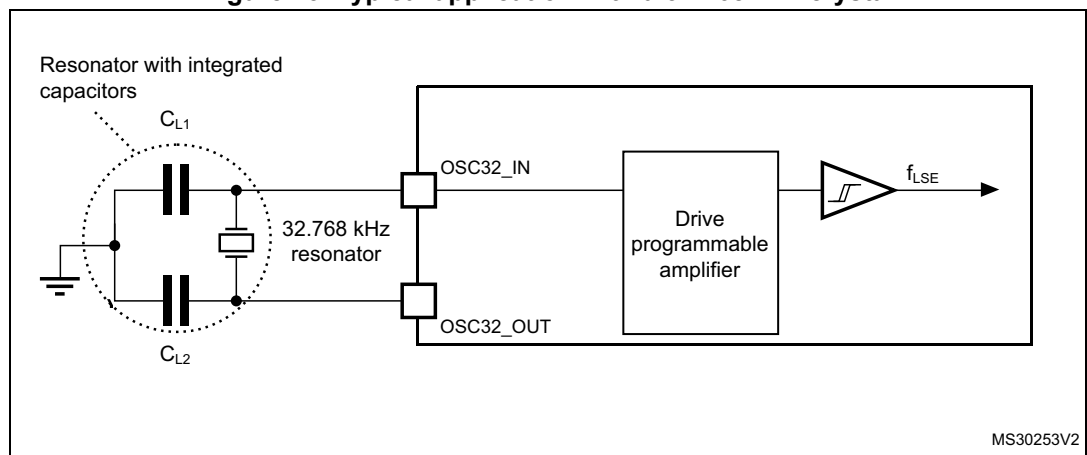
Table 40. LSE oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min ⁽²⁾	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	$\mu A/V$
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$ ⁽³⁾	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 23. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between $OSC32_IN$ and $OSC32_OUT$ and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in [Table 41](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

High-speed internal 16 MHz (HSI16) RC oscillator

Table 41. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	$V_{DD} = 3.0\text{ V}$	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$ACC_{HSI16}^{(2)}$	Accuracy of the factory-calibrated HSI16 oscillator	$V_{DDA} = 3.0\text{ V}, T_A = 25\text{ }^\circ\text{C}$	-1 ⁽³⁾	-	1 ⁽³⁾	%
		$V_{DDA} = 3.0\text{ V}, T_A = 0\text{ to }55\text{ }^\circ\text{C}$	-1.5	-	1.5	%
		$V_{DDA} = 3.0\text{ V}, T_A = -10\text{ to }70\text{ }^\circ\text{C}$	-2	-	2	%
		$V_{DDA} = 3.0\text{ V}, T_A = -10\text{ to }85\text{ }^\circ\text{C}$	-2.5	-	2	%
		$V_{DDA} = 3.0\text{ V}, T_A = -10\text{ to }105\text{ }^\circ\text{C}$	-4	-	2	%
		$V_{DDA} = 1.65\text{ V to }3.6\text{ V}, T_A = -40\text{ to }125\text{ }^\circ\text{C}$	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	μs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	μA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 24. HSI16 minimum and maximum value versus temperature



Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift $0^{\circ}C \leq T_A \leq 85^{\circ}C$	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	μs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 43. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at $V_{DD} = 3.3 V$ and $T_A = 25^{\circ}C$	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	MHz
		MSI range 4	1.05	-	
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	± 0.5	-	%
$D_{TEMP(MSI)}^{(1)}$	MSI oscillator frequency drift $0^{\circ}C \leq T_A \leq 85^{\circ}C$	-	± 3	-	%
$D_{VOLT(MSI)}^{(1)}$	MSI oscillator frequency drift $1.65 V \leq V_{DD} \leq 3.6 V, T_A = 25^{\circ}C$	-	-	2.5	%/V
$I_{DD(MSI)}^{(2)}$	MSI oscillator power consumption	MSI range 0	0.75	-	μA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	

Table 43. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
t _{SU(MSI)}	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
t _{STAB(MSI)} ⁽²⁾	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
f _{OVER(MSI)}	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.8 PLL characteristics

The parameters given in [Table 44](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 44. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f _{PLL_IN}	PLL input clock ⁽²⁾	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%



Table 44. PLL characteristics (continued)

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f _{PLL_OUT}	PLL output clock	2	-	32	MHz
t _{LOCK}	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-		±600	ps
I _{DDA} (PLL)	Current consumption on V _{DDA}	-	220	450	µA
I _{DD} (PLL)	Current consumption on V _{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

RAM memory

Table 45. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 46. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V _{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t _{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I _{DD}	Average current during the whole programming / erase operation	T _A = 25 °C, V _{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 47. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N _{CYC} ⁽²⁾	Cycling (erase / write) Program memory	T _A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T _A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	
t _{RET} ⁽²⁾	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T _{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T _{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 105 °C			
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T _{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T _A = 125 °C			

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 48](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, LQFP48, $T_A = +25\text{ °C}$, $f_{HCLK} = 32\text{ MHz}$ conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, LQFP48, $T_A = +25\text{ °C}$, $f_{HCLK} = 32\text{ MHz}$ conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. f_{osc}/f_{CPU}	Unit
				8 MHz/32 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, LQFP48 package conforming to IEC61967-2	0.1 to 30 MHz	-10	dBµV
			30 to 130 MHz	5	
			130 MHz to 1GHz	-5	
			EMI Level	1.5	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin



These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T _A = +125 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the [Table 52](#).

Table 52. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I _{INJ}	Injected current on BOOT0	-0	NA ⁽¹⁾	mA
	Injected current on PA0, PA2, PA4, PA5, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT and FTf pin	-5 ⁽²⁾	NA ⁽¹⁾	
	Injected current on any other pin	-5 ⁽²⁾	+5	

1. Current injection is not possible.
2. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.



6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 53](#) are derived from tests performed under the conditions summarized in [Table 20](#). All I/Os are CMOS and TTL compliant.

Table 53. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	$0.3V_{DD}$	V
		BOOT0 pin	-	-	$0.14V_{DD}^{(1)}$	
V_{IH}	Input high level voltage	All I/Os	$0.7 V_{DD}$	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis ⁽²⁾	Standard I/Os	-	$10\% V_{DD}^{(3)}$	-	
		BOOT0 pin	-	0.01	-	
I_{lkg}	Input leakage current ⁽⁴⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ All I/Os except PA11, PA12, BOOT0 and FTf I/Os	-	-	± 50	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA11 and P12 I/Os	-	-	-50/+250	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ FTf I/Os	-	-	± 100	
		$V_{DD} \leq V_{IN} \leq 5 V$ All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	200	
		$V_{DD} \leq V_{IN} \leq 5 V$ FTf I/Os	-	-	500	
		$V_{DD} \leq V_{IN} \leq 5 V$ PA11, PA12 and BOOT0	-	-	10	μA
R_{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	25	45	65	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	25	45	65	k Ω
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by characterization.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 200 mV. Guaranteed by characterization results.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 25. V_{IH}/V_{IL} versus V_{DD} (CMOS I/Os)

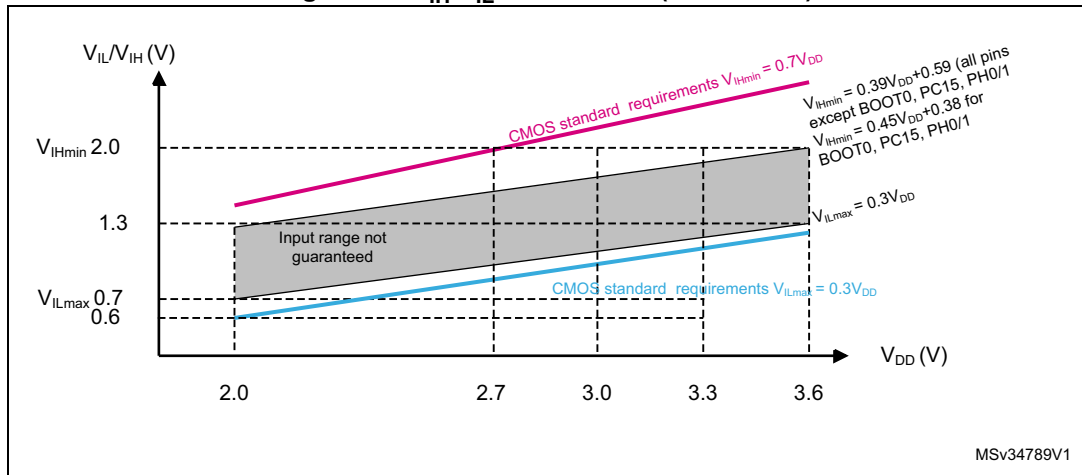
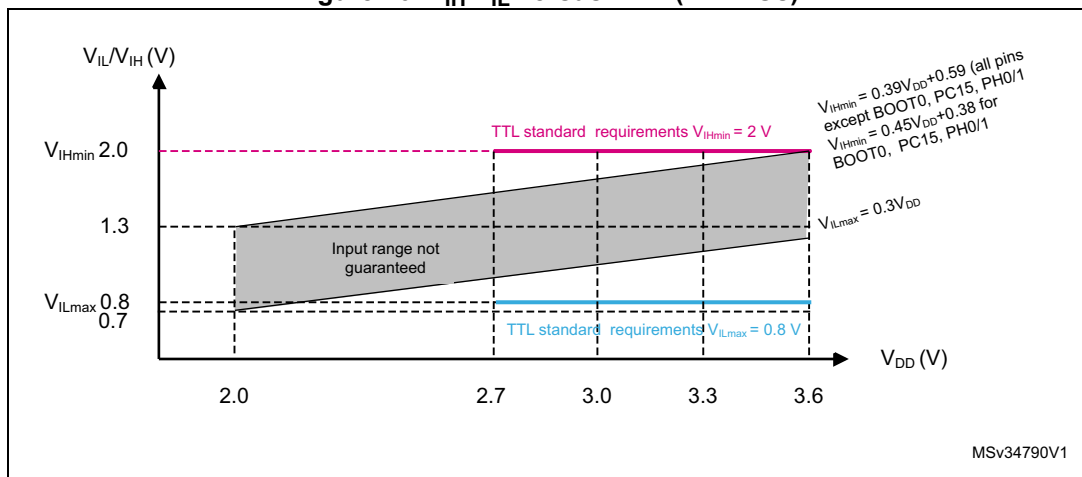


Figure 26. V_{IH}/V_{IL} versus V_{DD} (TTL I/Os)



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 15 mA with the non-standard V_{OL}/V_{OH} specifications given in [Table 54](#).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see [Table 18](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see [Table 18](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#). All I/Os are CMOS and TTL compliant.

Table 54. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = -6 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} < 3.6 \text{ V}$	-	0.45	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-0.45$	-	
$V_{OLFM+}^{(1)(4)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$I_{IO} = 20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
		$I_{IO} = 10 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 18](#). The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 18](#). The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 27](#) and [Table 55](#), respectively.

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

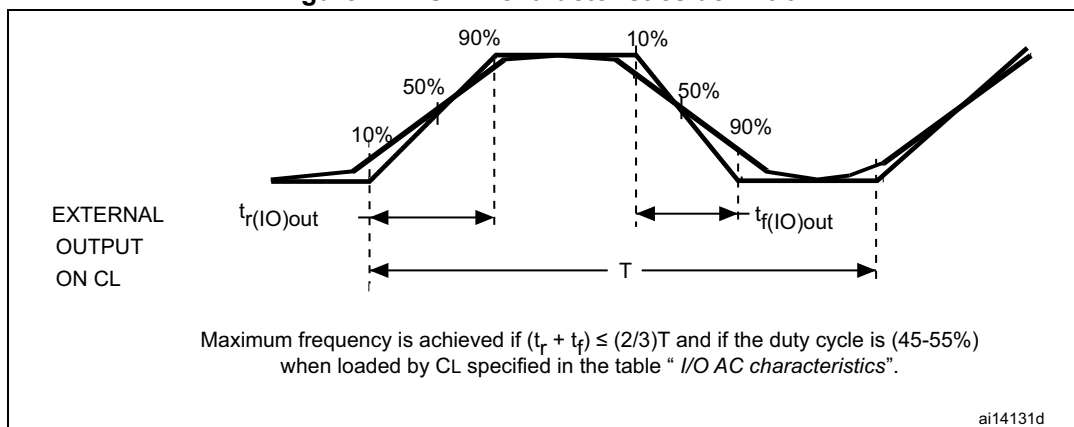
Table 55. I/O AC characteristics⁽¹⁾

OSPEEDRx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	400	kHz
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	100	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	125	ns
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	320	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	2	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	0.6	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	30	ns
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	65	
10	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	10	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	2	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	13	ns
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	28	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	35	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	10	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	6	ns
			$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	17	
Fm+ configuration ⁽⁴⁾	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.5 \text{ V to } 3.6 \text{ V}$	-	1	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	10	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	30	
	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 3.6 \text{ V}$	-	350	KHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	15	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	60	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in [Figure 27](#).
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the line reference manual for a detailed description of Fm+ I/O configuration.



Figure 27. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see [Table 56](#)).

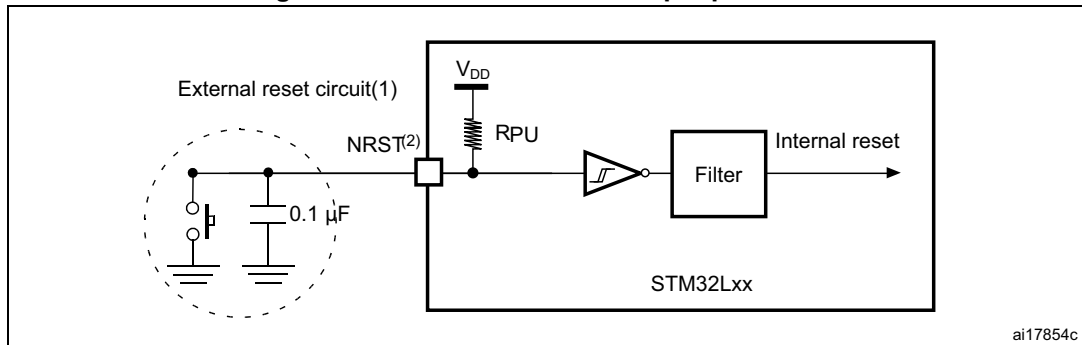
Unless otherwise specified, the parameters given in [Table 56](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 56. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}^{(1)}$	NRST output low level voltage	$I_{OL} = 2\text{ mA}$ $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	0.4	
		$I_{OL} = 1.5\text{ mA}$ $1.65\text{ V} < V_{DD} < 2.7\text{ V}$	-	-		
$V_{hys(NRST)}^{(1)}$	NRST Schmitt trigger voltage hysteresis	-	-	$10\%V_{DD}^{(2)}$	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	25	45	65	k Ω
$V_{F(NRST)}^{(1)}$	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}^{(1)}$	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 28. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 56](#). Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 57](#) are values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 20: General operating conditions](#).

Note: It is recommended to perform a calibration after each power-up.

Table 57. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC on	Fast channel	1.65	-	3.6	V
		Standard channel	1.75 ⁽¹⁾	-	3.6	
I_{DDA} (ADC)	Current consumption of the ADC on V_{DDA}	1.14 Msps	-	200	-	μA
		10 ksps	-	40	-	
	Current consumption of the ADC on V_{DD} ⁽²⁾	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
f_{ADC}	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
f_S ⁽³⁾	Sampling rate		0.05	-	1.14	MHz
f_{TRIG} ⁽³⁾	External trigger frequency	$f_{ADC} = 16$ MHz	-	-	941	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0	-	V_{DDA}	V
R_{AIN} ⁽³⁾	External input impedance	See Equation 1 and Table 58 for details	-	-	50	k Ω
R_{ADC} ⁽³⁾⁽⁴⁾	Sampling switch resistance		-	-	1	k Ω
C_{ADC} ⁽³⁾	Internal sample and hold capacitor		-	-	8	pF

Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{CAL} ⁽³⁾	Calibration time	f _{ADC} = 16 MHz	5.2			µs
			83			1/f _{ADC}
W _{LATENCY}	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f _{PCLK} cycles	-	1.5 ADC cycles + 3 f _{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f _{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f _{PCLK} cycle
t _{iatr} ⁽³⁾	Trigger conversion latency	f _{ADC} = f _{PCLK} /2 = 16 MHz	0.266			µs
		f _{ADC} = f _{PCLK} /2	8.5			1/f _{PCLK}
		f _{ADC} = f _{PCLK} /4 = 8 MHz	0.516			µs
		f _{ADC} = f _{PCLK} /4	16.5			1/f _{PCLK}
		f _{ADC} = f _{HSI16} = 16 MHz	0.252	-	0.260	µs
Jitter _{ADC}	ADC jitter on trigger conversion	f _{ADC} = f _{HSI16}	-	1	-	1/f _{HSI16}
t _S ⁽³⁾	Sampling time	f _{ADC} = 16 MHz	0.093	-	10.03	µs
			1.5	-	239.5	1/f _{ADC}
t _{STAB} ⁽³⁾	Power-up time		0	0	1	µs
t _{ConV} ⁽³⁾	Total conversion time (including sampling time)	f _{ADC} = 16 MHz	0.875		10.81	µs
			14 to 173 (t _S for sampling + 12.5 for successive approximation)			1/f _{ADC}

- V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to [Table 58: RAIN max for fADC = 16 MHz](#).
- A current consumption proportional to the APB clock frequency has to be added (see [Table 34: Peripheral current consumption in Run or Sleep mode](#)).
- Guaranteed by design.
- Standard channels have an extra protection resistance which depends on supply voltage. Refer to [Table 58: RAIN max for fADC = 16 MHz](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 58. R_{AIN} max for $f_{ADC} = 16 \text{ MHz}^{(1)}$

T_s (cycles)	t_s (μs)	R_{AIN} max for fast channels ($k\Omega$)	R_{AIN} max for standard channels ($k\Omega$)						
			$V_{DD} > 2.7 \text{ V}$	$V_{DD} > 2.4 \text{ V}$	$V_{DD} > 2.0 \text{ V}$	$V_{DD} > 1.8 \text{ V}$	$V_{DD} > 1.75 \text{ V}$	$V_{DD} > 1.65 \text{ V}$ and $T_A > -10 \text{ }^\circ\text{C}$	$V_{DD} > 1.65 \text{ V}$ and $T_A > 25 \text{ }^\circ\text{C}$
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 59. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	$1.65 \text{ V} < V_{DDA} < 3.6 \text{ V}$, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256) ⁽⁴⁾		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256) ⁽⁴⁾		70	76	-	
THD	Total harmonic distortion	-	-85	-73		

- ADC DC accuracy values are measured after internal calibration.
- ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.12](#) does not affect the ADC accuracy.
- Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.
- This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 29. ADC accuracy characteristics

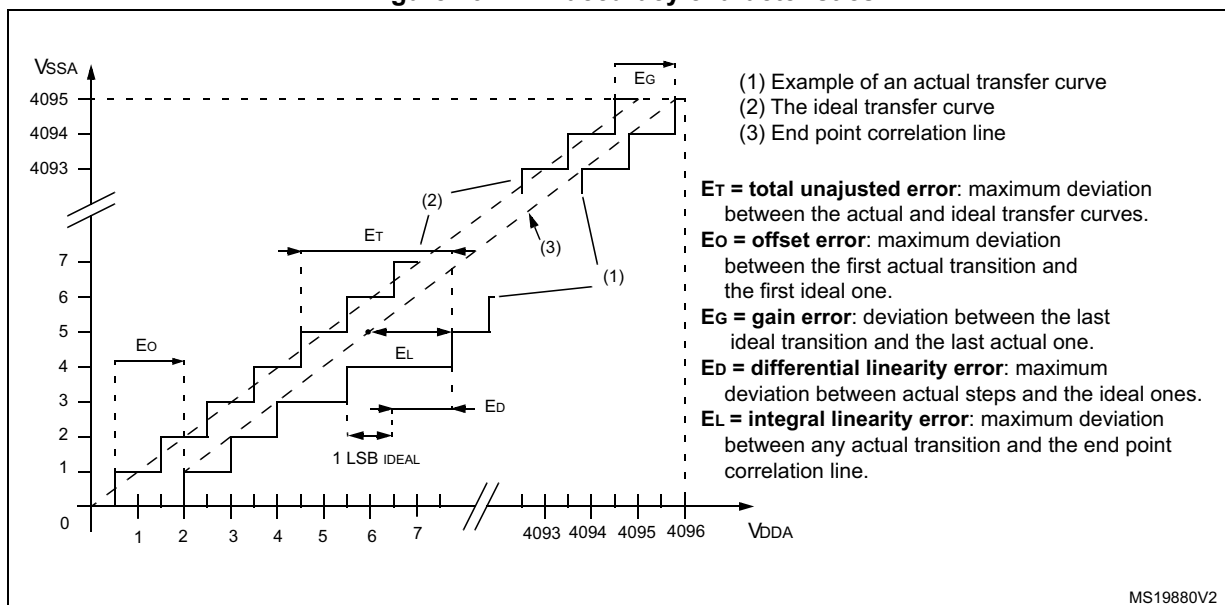
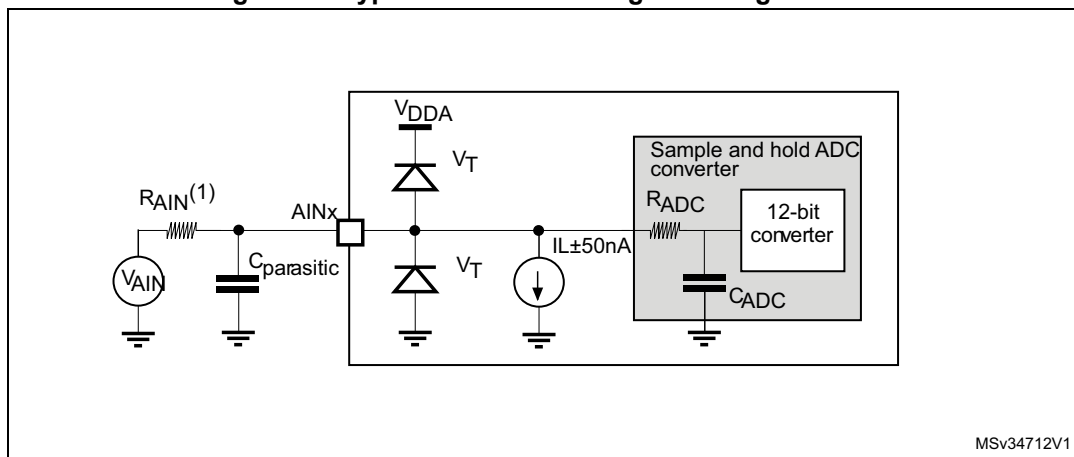


Figure 30. Typical connection diagram using the ADC



1. Refer to [Table 57: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 Temperature sensor characteristics

Table 60. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3\text{ V}$	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C $V_{DDA} = 3\text{ V}$	0x1FF8 007E - 0x1FF8 007F

Table 61. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}C$
Avg_Slope ⁽¹⁾	Average slope	1.48	1.61	1.75	mV/ $^{\circ}C$
V_{130}	Voltage at 130 $^{\circ}C \pm 5^{\circ}C^{(2)}$	640	670	700	mV
$I_{DDA(TEMP)}^{(3)}$	Current consumption	-	3.4	6	μA
$t_{START}^{(3)}$	Startup time	-	-	10	μs
$T_{S_temp}^{(4)(3)}$	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at $V_{DD} = 3 V \pm 10 mV$. V_{130} ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.17 Comparators

Table 62. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	k Ω
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	μs
t_d	Propagation delay ⁽²⁾	-	-	3	10	
Voffset	Comparator offset	-	-	± 3	± 10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6 V$ $V_{IN+} = 0 V$ $V_{IN-} = V_{REFINT}$ $T_A = 25^{\circ}C$	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption ⁽³⁾	-	-	160	260	nA

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 63. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V _{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V _{IN}	Comparator 2 input voltage range	-	0	-	V _{DDA}	V
t _{START}	Comparator startup time	Fast mode	-	15	20	μs
		Slow mode	-	20	25	
t _{d slow}	Propagation delay ⁽²⁾ in slow mode	1.65 V ≤ V _{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V _{DDA} ≤ 3.6 V	-	2.5	6	
t _{d fast}	Propagation delay ⁽²⁾ in fast mode	1.65 V ≤ V _{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V _{DDA} ≤ 3.6 V	-	1.2	4	
V _{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient	V _{DDA} = 3.3V T _A = 0 to 50 °C V ₋ = V _{REFINT} , 3/4 V _{REFINT} , 1/2 V _{REFINT} , 1/4 V _{REFINT} .	-	15	30	ppm /°C
I _{COMP2}	Current consumption ⁽³⁾	Fast mode	-	3.5	5	μA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.18 Timer characteristics

TIM timer characteristics

The parameters given in the [Table 64](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 64. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t _{res(TIM)}	Timer resolution time		1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	31.25	-	ns
f _{EXT}	Timer external clock frequency on CH1 to CH4		0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 32 MHz	0	16	MHz
Res _{TIM}	Timer resolution	-		16	bit

Table 64. TIMx⁽¹⁾ characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
t _{COUNTER}	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	0.0312	2048	μs
t _{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM21, and TIM22 timers.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to [Section 6.3.13: I/O port characteristics](#) for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see [Table 65](#) for the analog filter characteristics).

The analog spike filter is compliant with I²C timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V ≤ V_{DD} ≤ 3.6 V and voltage scaling Range 1
- Fast mode:
 - 2 V ≤ V_{DD} ≤ 3.6 V and voltage scaling Range 1 or Range 2.
 - V_{DD} < 2 V, voltage scaling Range 1 or Range 2, C_{load} < 200 pF.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 65. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t _{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50 ⁽²⁾	100 ⁽³⁾	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.

2. Spikes with widths below t_{AF(min)} are filtered.

- Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 20](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 66. SPI characteristics in voltage Range 1 ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver	-	-	16	
		Slave mode Transmitter $1.71 < V_{DD} < 3.6V$	-	-	12 ⁽²⁾	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$	-	-	16 ⁽²⁾	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_h(NSS)$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_w(SCKH)$ $t_w(SCKL)$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	8.5	-	-	
$t_{su(SI)}$		Slave mode	8.5	-	-	
$t_h(MI)$	Data input hold time	Master mode	6	-	-	
$t_h(SI)$		Slave mode	1	-	-	
$t_a(SO)$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_v(SO)$	Data output valid time	Slave mode $1.71 < V_{DD} < 3.6V$	-	29	41	
		Slave mode $2.7 < V_{DD} < 3.6V$	-	22	28	
$t_v(MO)$		Master mode	-	10	17	
$t_h(SO)$	Data output hold time	Slave mode	9	-	-	
$t_h(MO)$		Master mode	3	-	-	

- Guaranteed by characterization results.
- The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while $Duty_{(SCK)} = 50\%$.

Table 67. SPI characteristics in voltage Range 2 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65 < V_{DD} < 3.6V$			8	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$			8 ⁽²⁾	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_w(SCKH)$ $t_w(SCKL)$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	12	-	-	
$t_{su(SI)}$		Slave mode	11	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_a(SO)$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_v(SO)$	Data output valid time	Slave mode	-	40	55	
		Master mode	-	16	26	
$t_v(MO)$	Data output hold time	Slave mode	12	-	-	
$t_h(SO)$		Master mode	4	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_v(SO)$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty(SCK) = 50%.

Table 68. SPI characteristics in voltage Range 3 ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			$2^{(2)}$	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{pclk}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{pclk}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{pclk} - 2$	T_{pclk}	$T_{pclk} + 2$	
$t_{su(MI)}$	Data input setup time	Master mode	28.5	-	-	
$t_{su(SI)}$		Slave mode	22	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	53	86	
		Master mode	-	30	54	
$t_{v(MO)}$	Data output hold time	Slave mode	18	-	-	
$t_{h(SO)}$		Master mode	8	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while $Duty_{(SCK)} = 50\%$.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

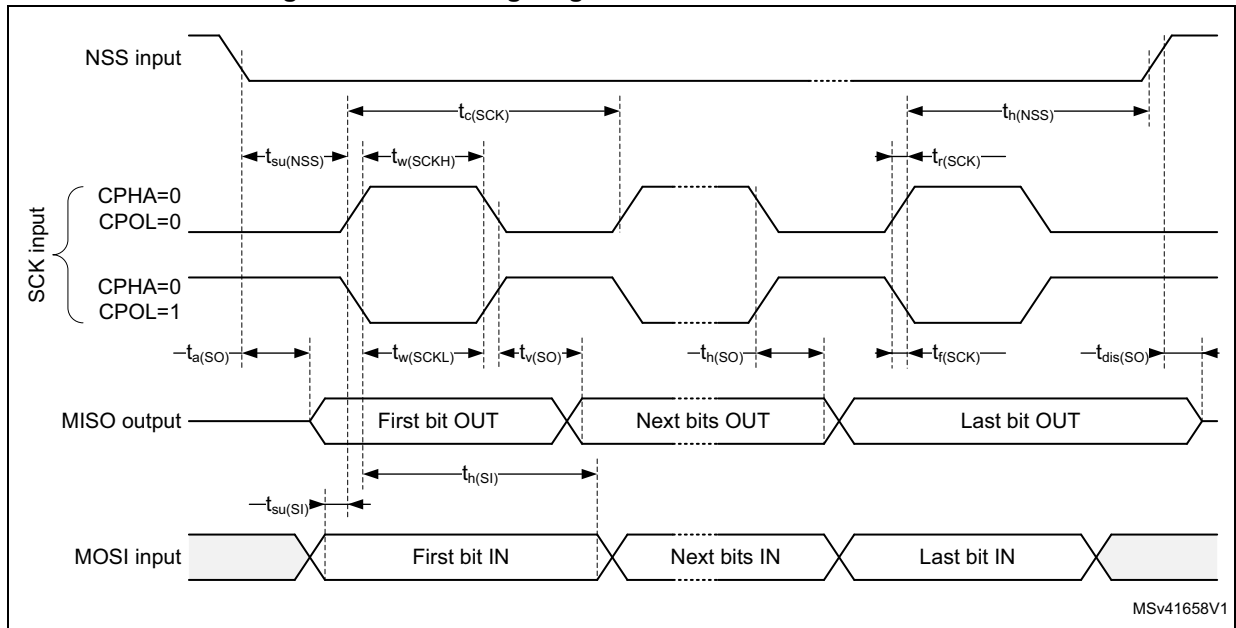
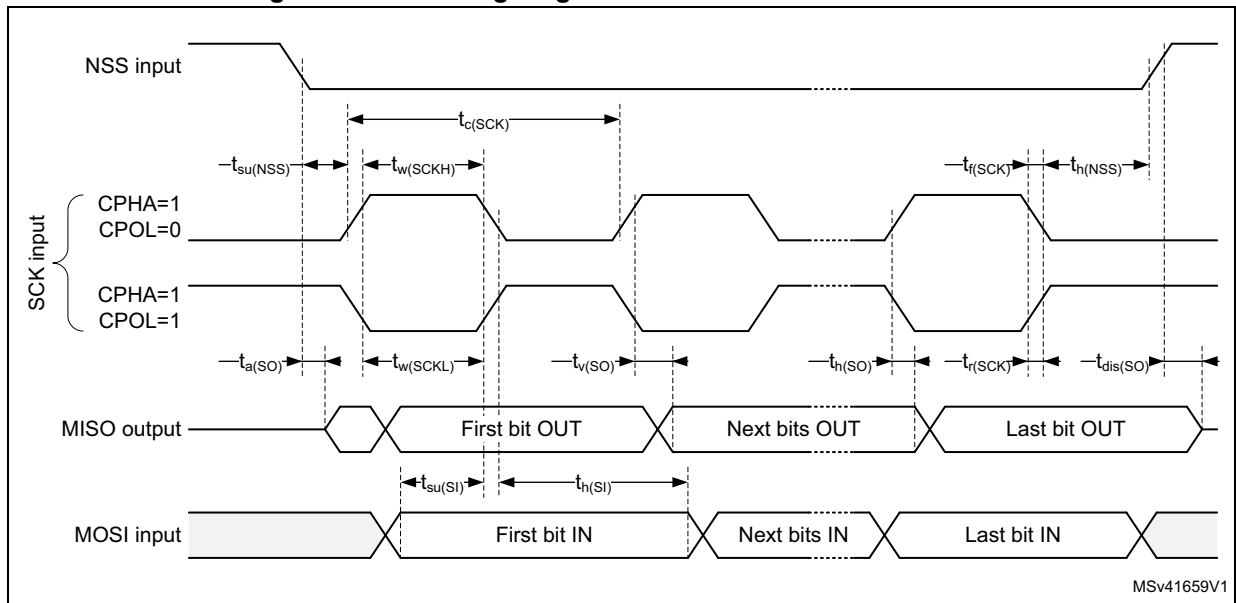
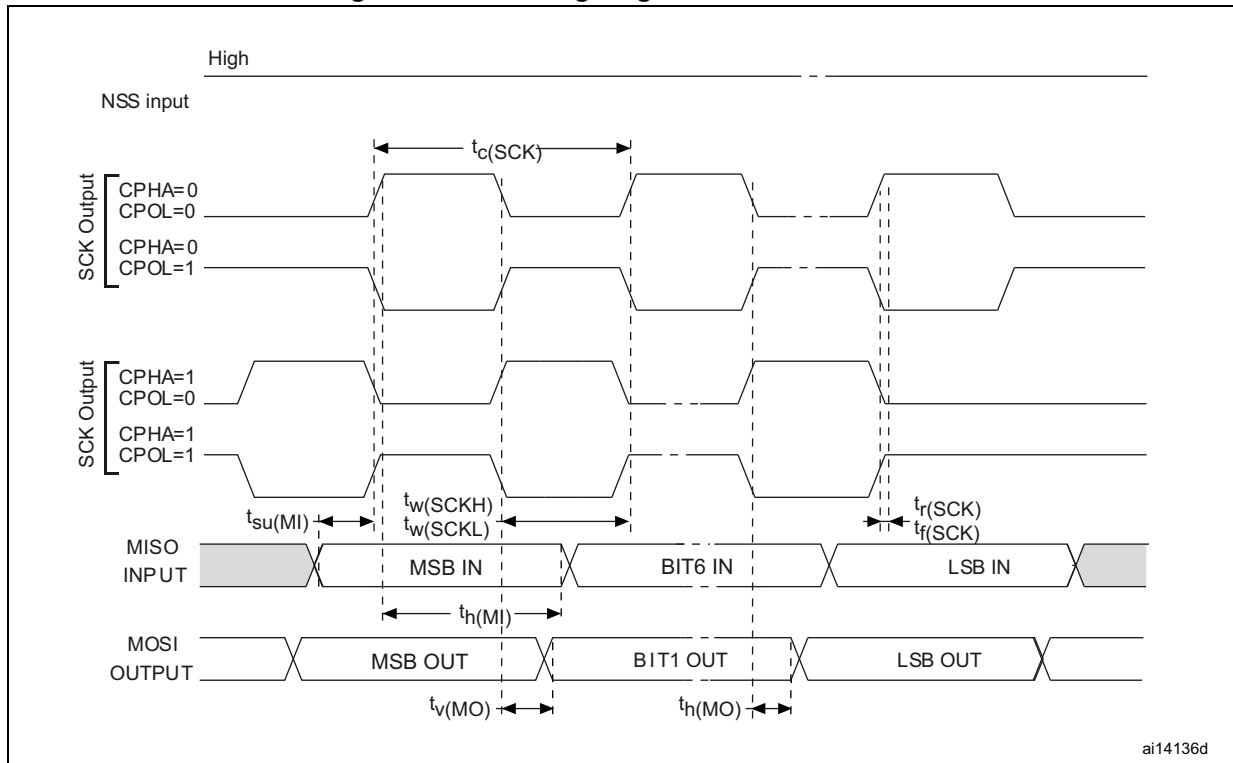


Figure 32. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 33. SPI timing diagram - master mode⁽¹⁾



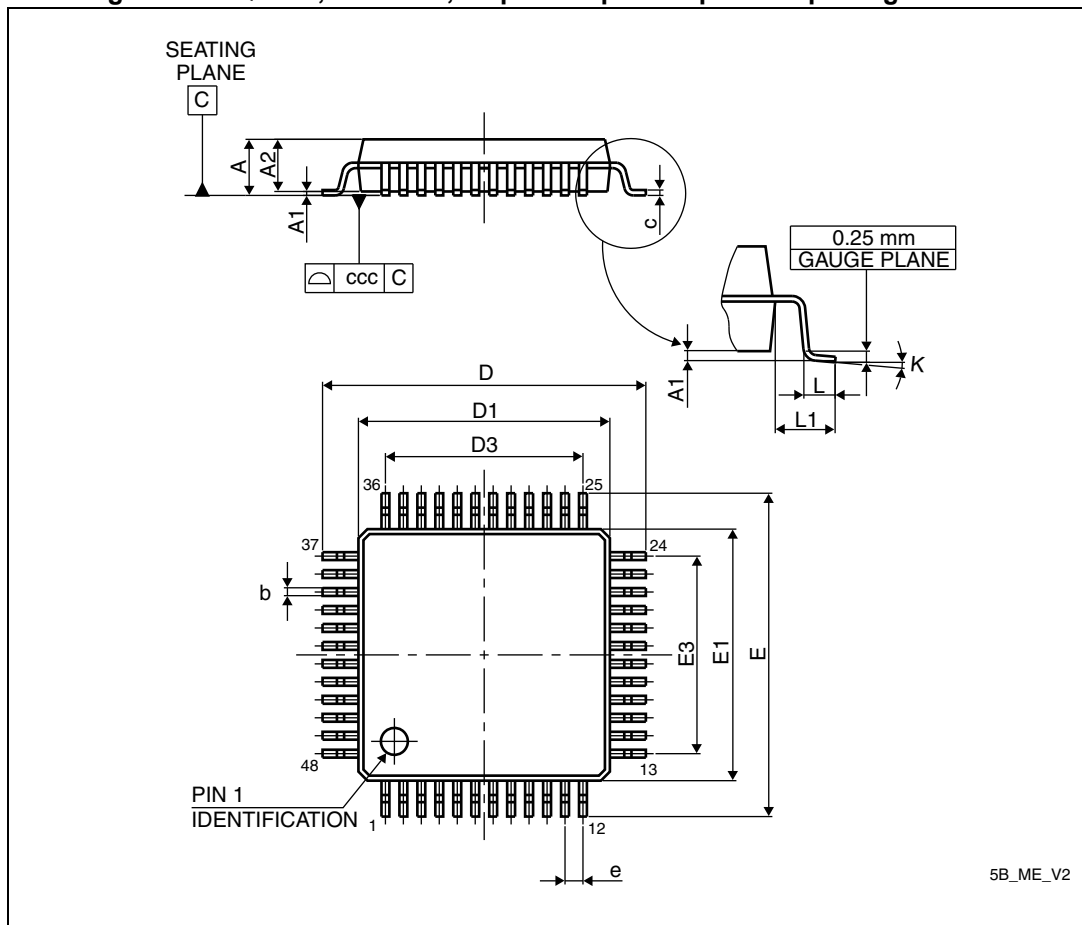
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at <http://www.st.com>. ECOPACK® is an ST trademark.

7.1 LQFP48 package information

Figure 34. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline



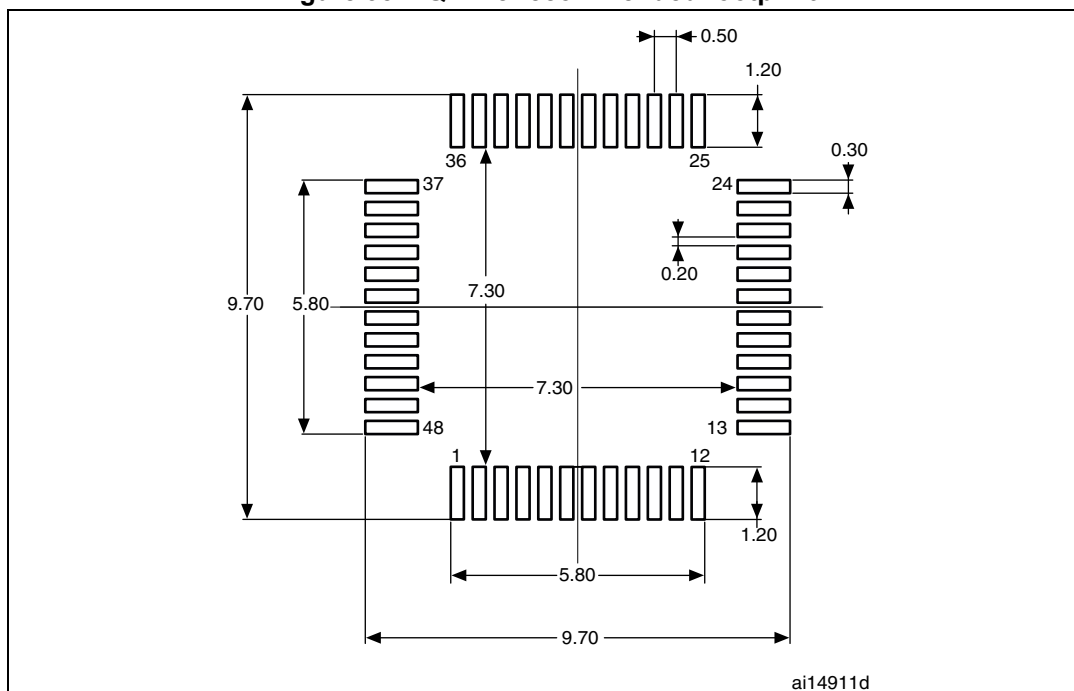
1. Drawing is not to scale.

Table 69. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP48 recommended footprint



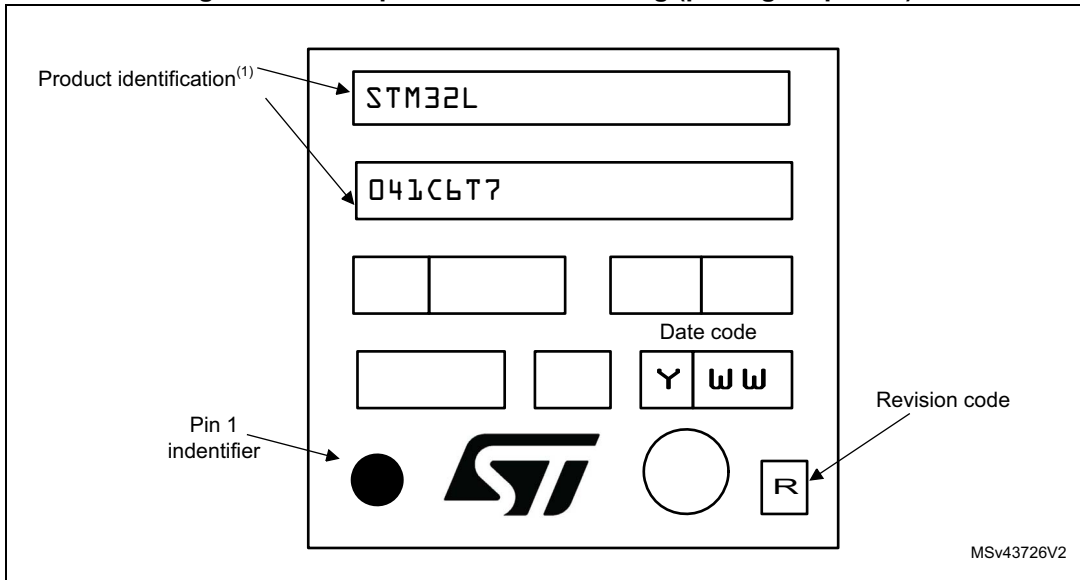
1. Dimensions are expressed in millimeters.

LQFP48 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

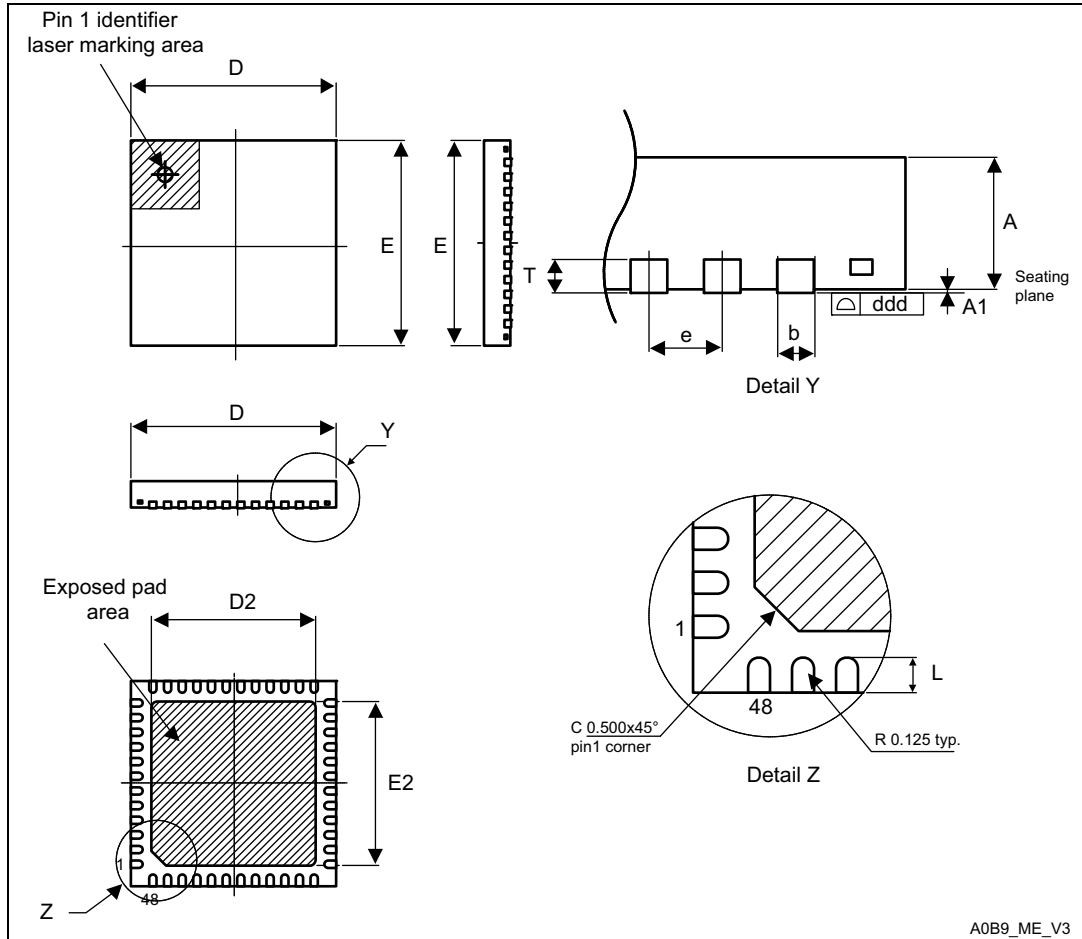
Figure 36. Example of LQFP48 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.2 UFQFPN48 package information

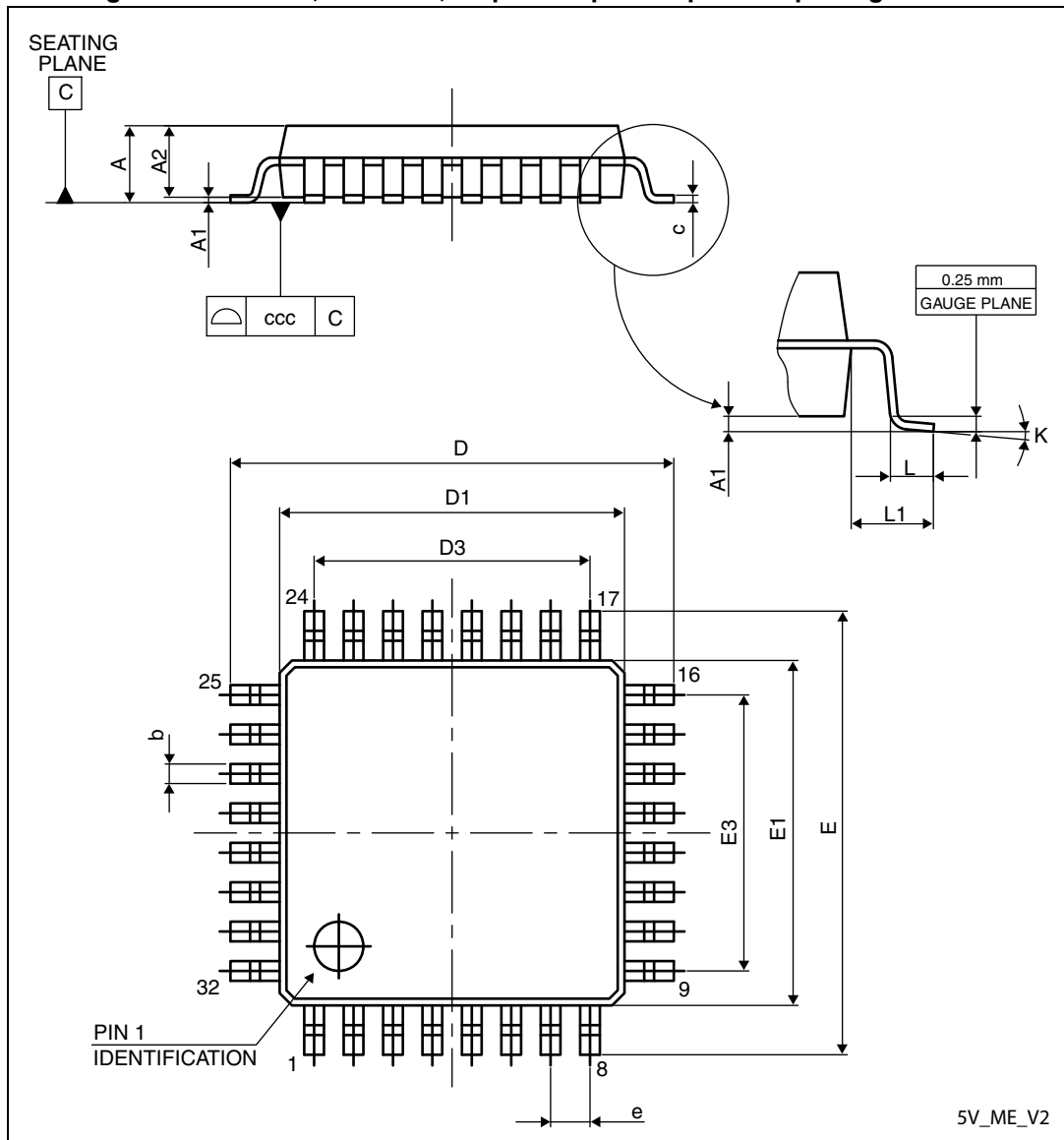
Figure 37. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

7.3 LQFP32 package information

Figure 39. LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package outline



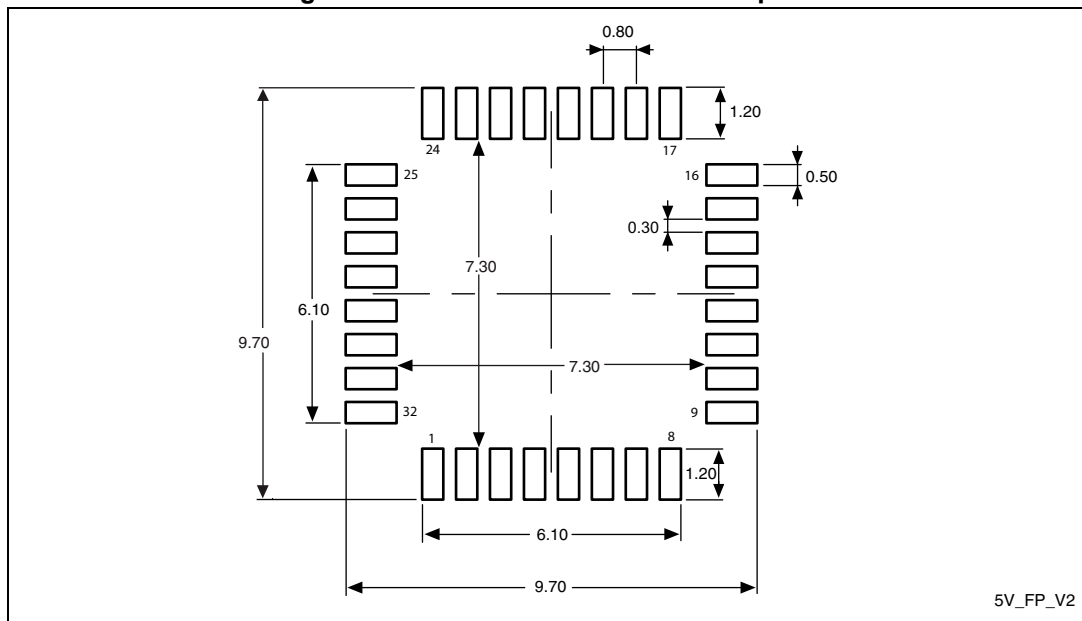
1. Drawing is not to scale.

Table 71. LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP32 recommended footprint



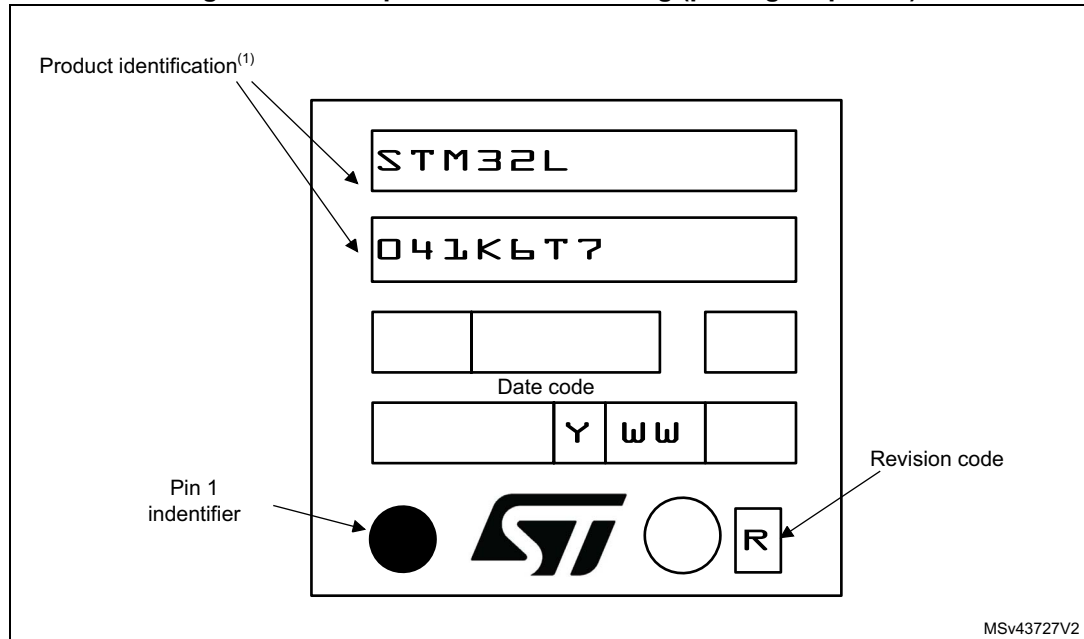
1. Dimensions are expressed in millimeters.

LQFP32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

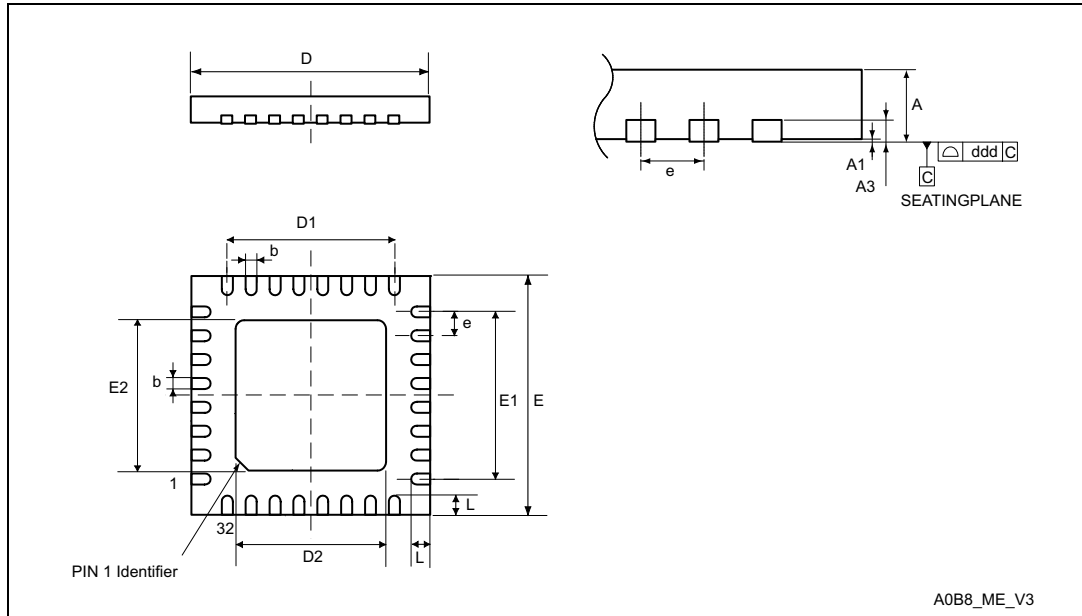
Figure 41. Example of LQFP32 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 UFQFPN32 package information

Figure 42. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



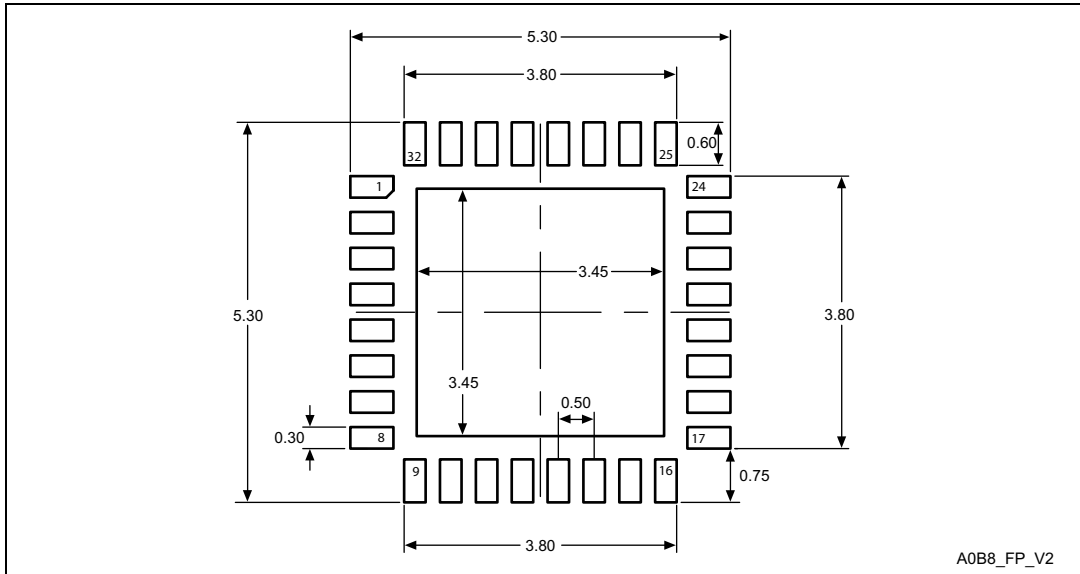
1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.

Table 72. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	-	0.050	-	-	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



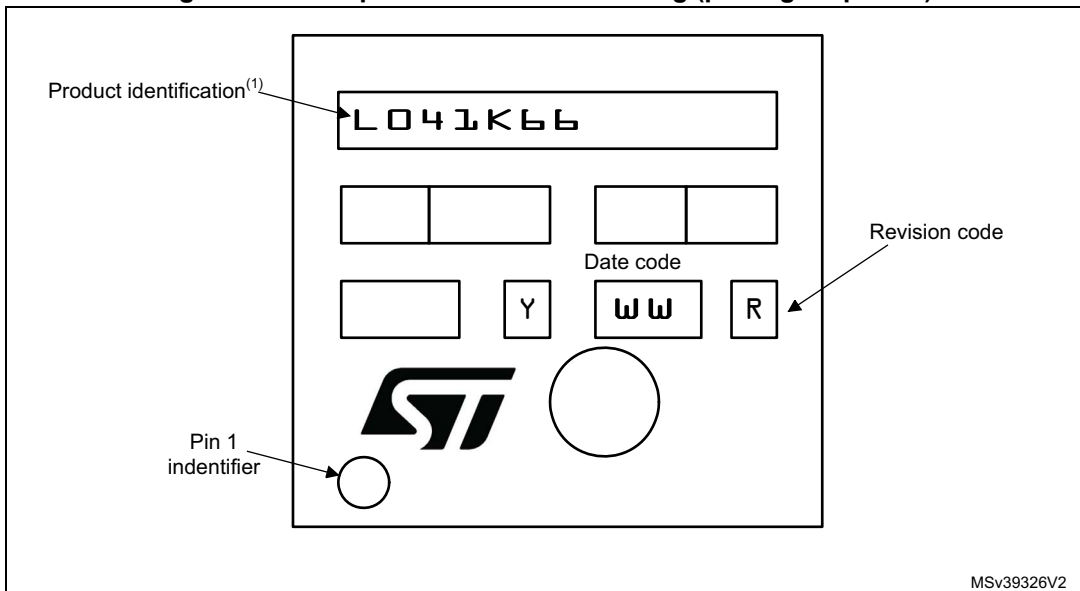
1. Dimensions are expressed in millimeters.

UFQFPN32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

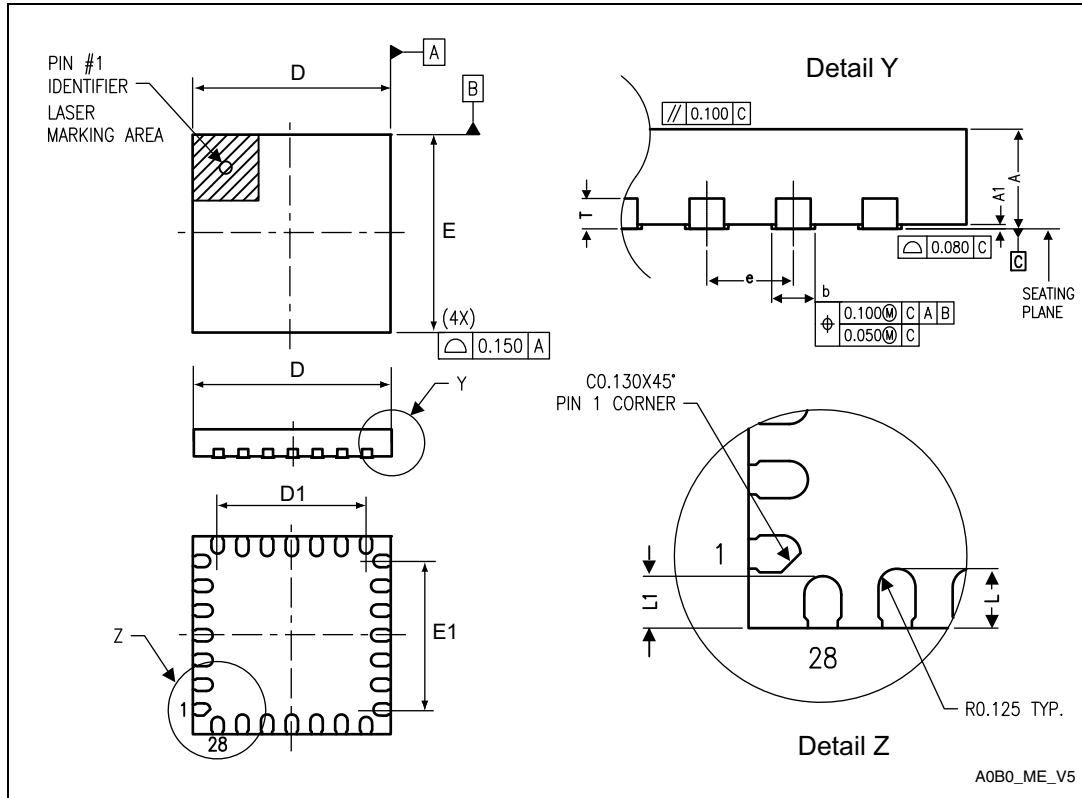
Figure 44. Example of UFQFPN32 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 UFQFPN28 package information

Figure 45. UFQPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Table 73. UFQPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data⁽¹⁾

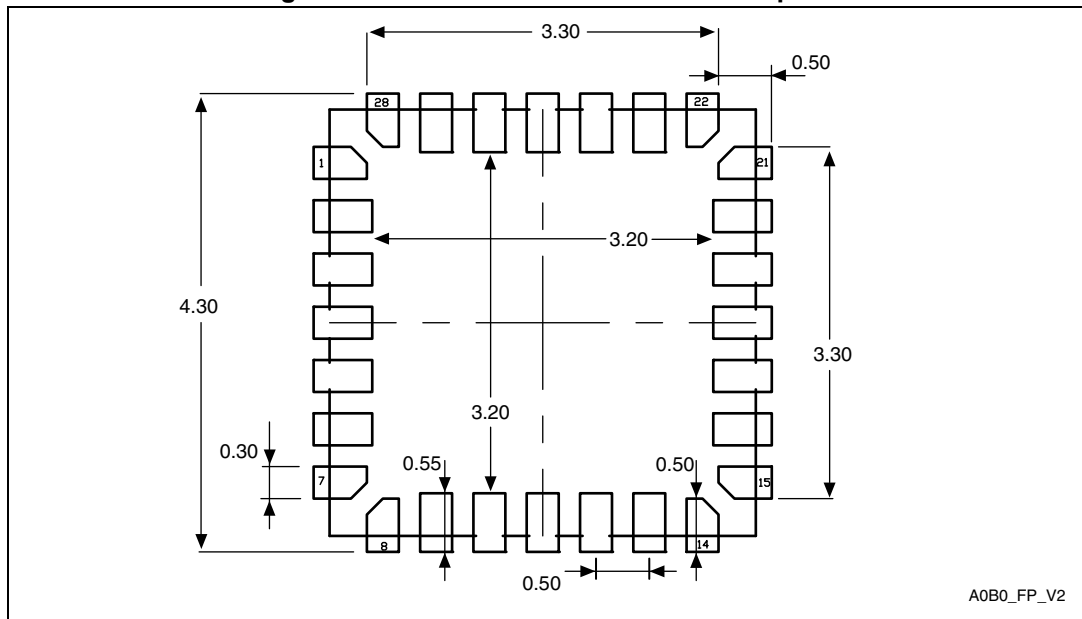
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-

Table 73. UFQPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data⁽¹⁾ (continued)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. UFQFPN28 recommended footprint



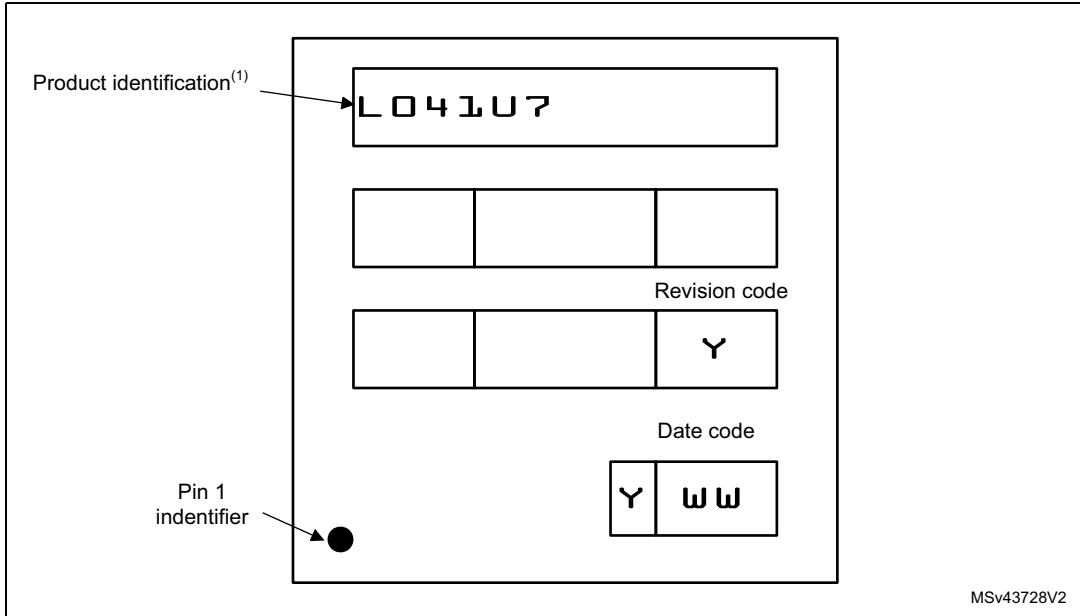
1. Dimensions are expressed in millimeters.

UFQFPN28 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 47. Example of UFQFPN28 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.6 WLCSP25 package information

Figure 48. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale package outline

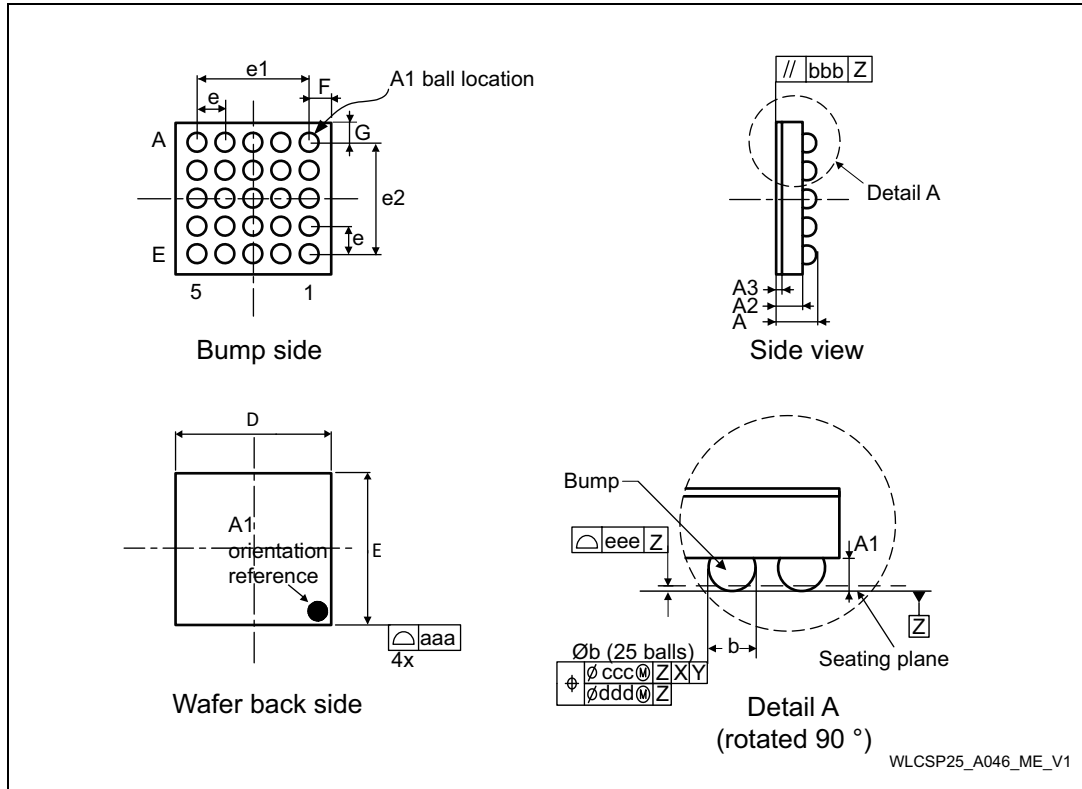


Table 74. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data

Symbol	Millimeters			Inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.062	2.097	2.132	0.0812	0.0826	0.0839
E	2.458	2.493	2.528	0.0968	0.0981	0.0995
e	-	0.400	-	-	0.0157	-
e1	-	1.600	-	-	0.0630	-
e2	-	1.600	-	-	0.0630	-
F	-	0.2485	-	-	0.0098	-
G	-	0.4465	-	-	0.0176	-

Table 74. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data (continued)

Symbol	Millimeters			Inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 49. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale recommended footprint

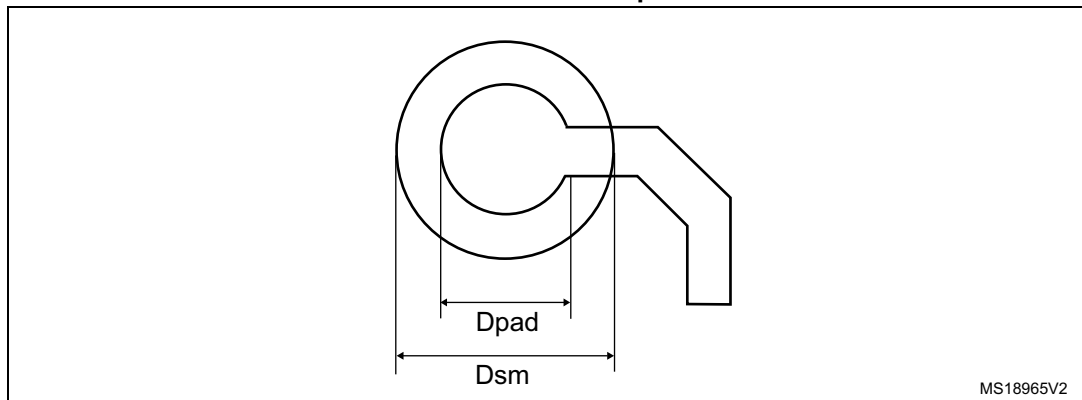


Table 75. WLCSP25 recommended PCB design rules

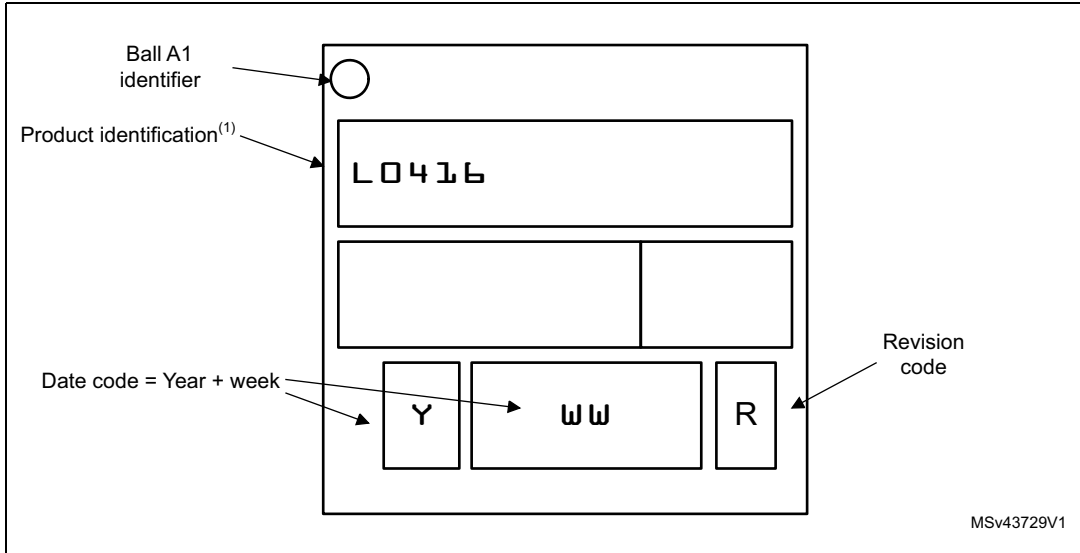
Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 μm max. (circular) 220 μm recommended
Dsm	300 μm min. (for 260 μm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

WLCSP25 device marking

The following figure gives an example of topside marking versus ball A1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

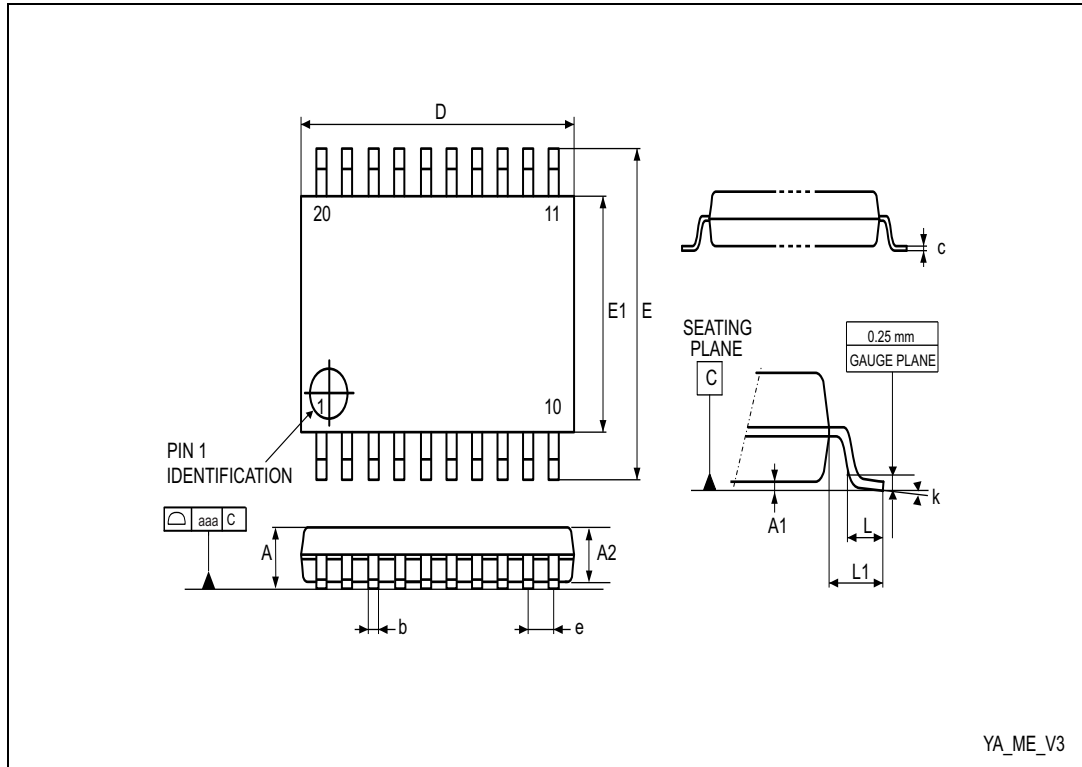
Figure 50. Example of WLCSP25 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 TSSOP20 package information

Figure 51. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 76. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data

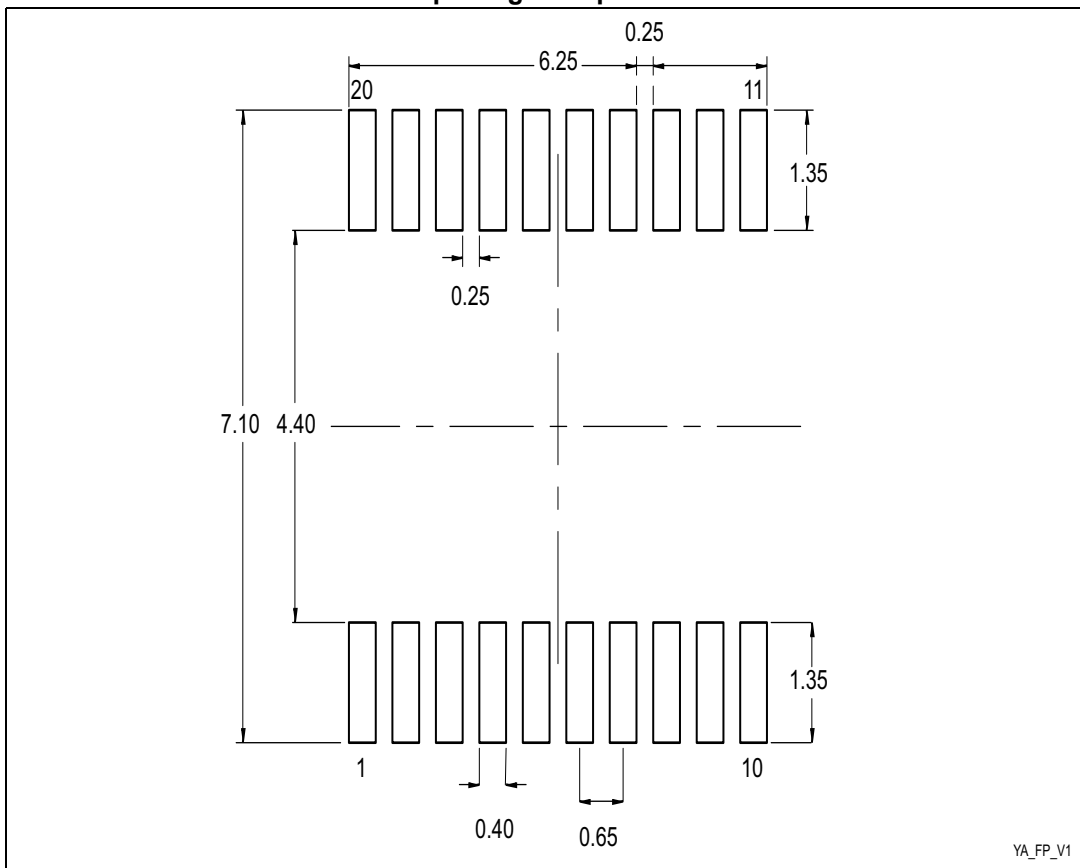
Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D ⁽²⁾	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1 ⁽³⁾	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 76. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 52. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



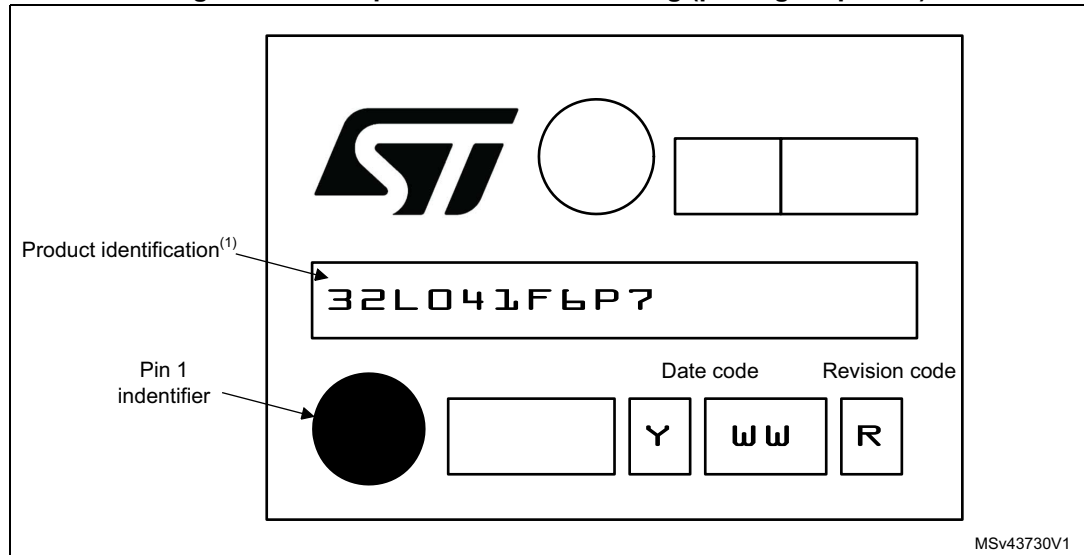
1. Dimensions are expressed in millimeters.

TSSOP20 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 53. Example of TSSOP20 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT \text{ max}}$ and $P_{I/O \text{ max}}$ ($P_D \text{ max} = P_{INT \text{ max}} + P_{I/O \text{ max}}$),
- $P_{INT \text{ max}}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O \text{ max}}$ represents the maximum power dissipation on output pins where:

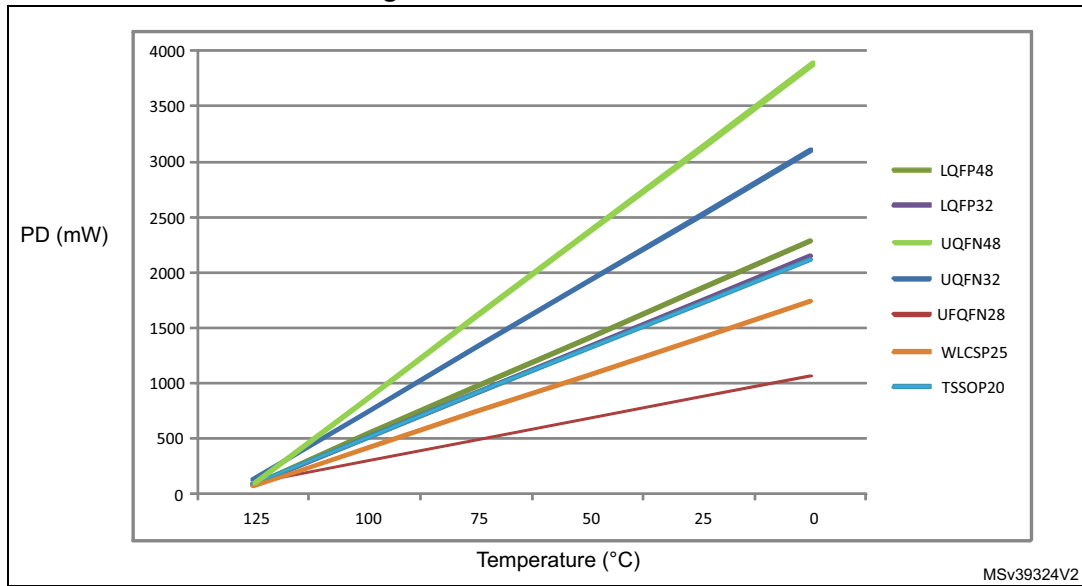
$$P_{I/O \text{ max}} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 77. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	57	°C/W
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	32	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm / 0.5 mm pitch	120	
	Thermal resistance junction-ambient WLCSP25 - 0.4 mm pitch	70	
	Thermal resistance junction-ambient TSSOP20 - 169 mils	60	

Figure 54. Thermal resistance



1. The above curves are valid for range 3. For range 7, the curves are shifted by 20 °C to the right.

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 78. STM32L041x6 ordering information scheme

Example:	STM32	L	041	K	6	T	6	D	TR
Device family	STM32 = Arm-based 32-bit microcontroller								
Product type	L = Low power								
Device subfamily	041 = Access line with AES								
Pin count	C = 48 pins K = 32 pins G = 28 pins E = 25 pins F = 20 pins								
Flash memory size	6 = 32 Kbytes								
Package	T = LQFP U = UFQFPN Y = WLCSP P = TSSOP								
Temperature range	6 = Industrial temperature range, -40 to 85 °C 7 = Industrial temperature range, -40 to 105 °C 3 = Industrial temperature range, -40 to 125 °C								
Number of UFQFPN28 power pairs	S = one power pair ⁽¹⁾ No character = Two power pairs								
Options	No character = V _{DD} range: 1.8 to 3.6 V and BOR enabled D = V _{DD} range: 1.65 to 3.6 V and BOR disabled								
Packing	TR = tape and reel No character = tray or tube								

1. This option is available only on STM32L041G6UxS part number. Contact your nearest ST sales office for availability.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



9 Revision history

Table 79. Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release.
14-Mar-2016	2	<p>Updated number of SPI interfaces on cover page and in Table 2: Ultra-low-power STM32L041x4/x6 device features and peripheral counts.</p> <p>Updated number of GPIOs for devices in UFQFPN28 in Table 2: Ultra-low-power STM32L041x4/x6 device features and peripheral counts.</p> <p>Updated Section 3.4.4: Boot modes.</p> <p>Updated Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART) and Section 3.16.4: Serial peripheral interface (SPI) to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces.</p> <p>Modified pin 2 in Figure 6: STM32L041x6 UFQFPN32 pinout.</p> <p>Added Figure 8: STM32L041G6UxS UFQFPN28 pinout.</p> <p>Table 15: Pin definitions:</p> <ul style="list-style-type: none"> – Added UFQFPN28 for STM32L041GxUxS part number. – Renamed PA0-WKUP-CK_IN into PA0-CK_IN – Renamed PA0-WKUP into PA0 <p>Updated Table 18: Current characteristics to add the total output current for STM32L031GxUxS.</p> <p>Added one power pair option in Table 78: STM32L041x6 ordering information scheme.</p>

Table 79. Document revision history

Date	Revision	Changes
12-Apr-2016	3	<p><i>Features:</i></p> <ul style="list-style-type: none"> – Change minimum comparator supply voltage to 1.65 V. – Updated current consumptions in Standby, Stop and Stop with RTC ON modes. <p>Removed note related to preliminary consumption values in Table 5: Functionalities depending on the working mode (from Run/active down to standby).</p> <p>Added number of fast and standard channels in Section 3.10: Analog-to-digital converter (ADC).</p> <p>Added baudrate allowing to wake up the MCU from Stop mode in Section 3.16.2: Universal synchronous/asynchronous receiver transmitter (USART) and Section 3.16.3: Low-power universal asynchronous receiver transmitter (LPUART).</p> <p>Changed V_{DDA} minimum value to 1.65 V in Table 20: General operating conditions.</p> <p>Added I_{REFINT} value for $V_{DD}=1.8$ V in Table 35: Peripheral current consumption in Stop and Standby mode.</p> <p>Section 6.3.15: 12-bit ADC characteristics:</p> <ul style="list-style-type: none"> – Table 57: ADC characteristics: <ul style="list-style-type: none"> Distinction made between V_{DDA} for fast and standard channels; added note 1. Added note 4, related to R_{ADC}. Updated t_S and t_{CONV}. – Updated Table 58: RAIN max for $f_{ADC} = 16$ MHz for $f_{ADC} = 16$ MHz and distinction made between fast and standard channels. <p>Added Table 66: USART/LPUART characteristics.</p>
01-Dec-2016	4	<p>Added STM32L041E6 part number.</p> <p>Added reference to optional marking or inset/upset marks in all package device marking sections.</p> <p>Removed note related to WLCSP25 preliminary ballout in Table 15: Pin definitions. Changed aaa, bbb, ccc, ddd and eee data from minimum to maximum values in Table 74: WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data.</p> <p>Added LQFP48 device marking, LQFP32 device marking, UFQFPN28 device marking and TSSOP20 device marking.</p>

Table 79. Document revision history

Date	Revision	Changes
26-Sep-2017	5	<p>Added UFQFPN48 package. Removed STM32L041x4 part numbers together with 16-Kbyte Flash memory density. Added AES in Table 2: Ultra-low-power STM32L041x4/x6 device features and peripheral counts. Removed column "I/O operation" from Table 3: Functionalities depending on the operating power supply range and added note related to GPIO speed. In Section 5: Memory mapping, replaced memory mapping schematic by reference to the reference manual. In Section 4: Pin descriptions, changed USARTx_RTS and LPUARTx_RTS into USARTx_RTS_DE and LPUARTx_RTS_DE, respectively. Updated introduction text in Section 6.2: Absolute maximum ratings to mention device mission profile and extended mission profiles. Added note in Table 52: I/O current injection susceptibility. Updated minimum and maximum values of I/O weak pull-up equivalent resistor (R_{PJ}) and weak pull-down equivalent resistor (R_{PD}) in Table 53: I/O static characteristics. Updated minimum and maximum values of NRST weak pull-up equivalent resistor (R_{PJ}) in Table 56: NRST pin characteristics. Added note 2. related to the position of the external capacitor below Figure 28: Recommended NRST pin protection. Updated Section : I2C interface characteristics. Updated Figure 31: SPI timing diagram - slave mode and CPHA = 0, Figure 32: SPI timing diagram - slave mode and CPHA = 1(1) and Figure 33: SPI timing diagram - master mode(1). Suppressed section USART/LPUART characteristics. Added reference to optional marking or inset/upset marks in all package device marking sections. Updated Figure 36: Example of LQFP48 marking (package top view) and Table 69: LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data. Updated Table 71: LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package mechanical data. Updated Figure 42: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline and Table 72: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data. Updated Table 74: WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data. Added notes related to D and E1 in Table 76: TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data. Updated Figure 54: Thermal resistance as well as the corresponding temperature range in the note below the figure. Renamed Section 8 into Ordering information.</p>

Table 79. Document revision history

Date	Revision	Changes
12-Feb-2018	6	<p>Added Arm logo in Section 1: Introduction and removed USB and Cortex logo from Section 2: Description.</p> <p>Updated I2C in Table 5: Functionalities depending on the working mode (from Run/active down to standby).</p> <p>Changed RTS into RTS/DE in Figure 1: STM32L041x6 block diagram. Changed USART2_RTS and USART2_RTS_DE into USART2_RTS/USART2_DE, and LPUART1_RTS and LPUART1_RTS_DE into LPUART1_RTS/LPUART1_DE in Table 15: Pin definitions and Table 16: Alternate functions.</p> <p>Updated Figure 36: Example of LQFP48 marking (package top view), Figure 41: Example of LQFP32 marking (package top view), Figure 44: Example of UFQFPN32 marking (package top view) and Figure 47: Example of UFQFPN28 marking (package top view). Removed UFQFPN48 marking example.</p> <p>Updated Table 72: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data.</p>

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