

Description

The VNL5160N3-E and VNL5160S5-E are monolithic devices, made using STMicroelectronics® VIPower® Technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short circuit. Output current limitation protects the devices in an overload condition. In the case of a long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

Features

Type	V _{clamp}	R _{DS(on)}	I _D
VNL5160N3-E	41 V	160 mΩ	3.5 A
VNL5160S5-E			

- Automotive qualified
- Drain current: 3.5A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC European directive
- Open drain status output (VNL5160S5-E only)
- Specially intended for R10W or 2x R5W automotive signal lamps

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	VNL5160N3-E	VNL5160N3TR-E
SO-8	VNL5160S5-E	VNL5160S5TR-E

Contents

1	Block diagrams and pins configurations	5
2	Absolute maximum rating	8
2.1	Absolute maximum ratings	8
2.2	Thermal data	9
3	Electrical characteristics	10
4	Application information	14
4.1	MCU I/O protection	15
5	Package and PC board thermal data	17
5.1	SOT-223 thermal data	17
5.2	SO-8 thermal data	19
6	Package and packing information	22
6.1	ECOPACK [®] packages	22
6.2	SOT-223 mechanical data	22
6.3	SO8 mechanical data	23
6.4	SOT-223 packing information	24
6.5	SO8 packing information	25
7	Revision history	26

List of tables

Table 1.	Device summary	1
Table 2.	Pin function	6
Table 3.	Suggested connections for unused and not connected pins	7
Table 4.	Absolute maximum ratings	8
Table 5.	Thermal data	9
Table 6.	PowerMOS section	10
Table 7.	Source drain diode	10
Table 8.	Input section	10
Table 9.	Status pin	10
Table 10.	Logic input	11
Table 11.	Open-load detection	11
Table 12.	Supply section	11
Table 13.	Switching characteristics ($V_{CC} = 13\text{ V}$)	12
Table 14.	Protection and diagnostics	12
Table 15.	Truth table	13
Table 16.	SOT-223 thermal parameter	19
Table 17.	SO-8 thermal parameter	21
Table 18.	Document revision history	26

List of figures

Figure 1.	VNL5160N3-E block diagram	5
Figure 2.	VNL5160S5-E block diagram	5
Figure 3.	VNL5160N3-E current and voltage conventions.	6
Figure 4.	VNL5160S5-E current and voltage conventions	6
Figure 5.	Configuration diagrams (top view)	7
Figure 6.	Switching characteristics	13
Figure 7.	VNL5160N3-E application schematic	14
Figure 8.	VNL5160S5-E application schematic	14
Figure 9.	Maximum demagnetization energy	16
Figure 10.	SOT-223 PC board	17
Figure 11.	SOT-223 Rthj-amb vs PCB copper area in open box free air condition	17
Figure 12.	SOT-223 thermal impedance junction ambient single pulse	18
Figure 13.	SOT-223 thermal fitting model	18
Figure 14.	SO-8 PC board	19
Figure 15.	SO-8 Rthj-amb vs PCB copper area in open box free air condition	20
Figure 16.	SO-8 thermal impedance junction ambient single pulse.	20
Figure 17.	SO-8 thermal fitting model	21
Figure 18.	SOT-223 mechanical data & package outline	22
Figure 19.	SO8 mechanical data & package outline	23
Figure 20.	SOT-223 tape and reel shipment (suffix "TR")	24
Figure 21.	SO-8 tube shipment (no suffix)	25
Figure 22.	SO-8 tape and reel shipment (suffix "TR")	25

1 Block diagrams and pins configurations

Figure 1. VNL5160N3-E block diagram

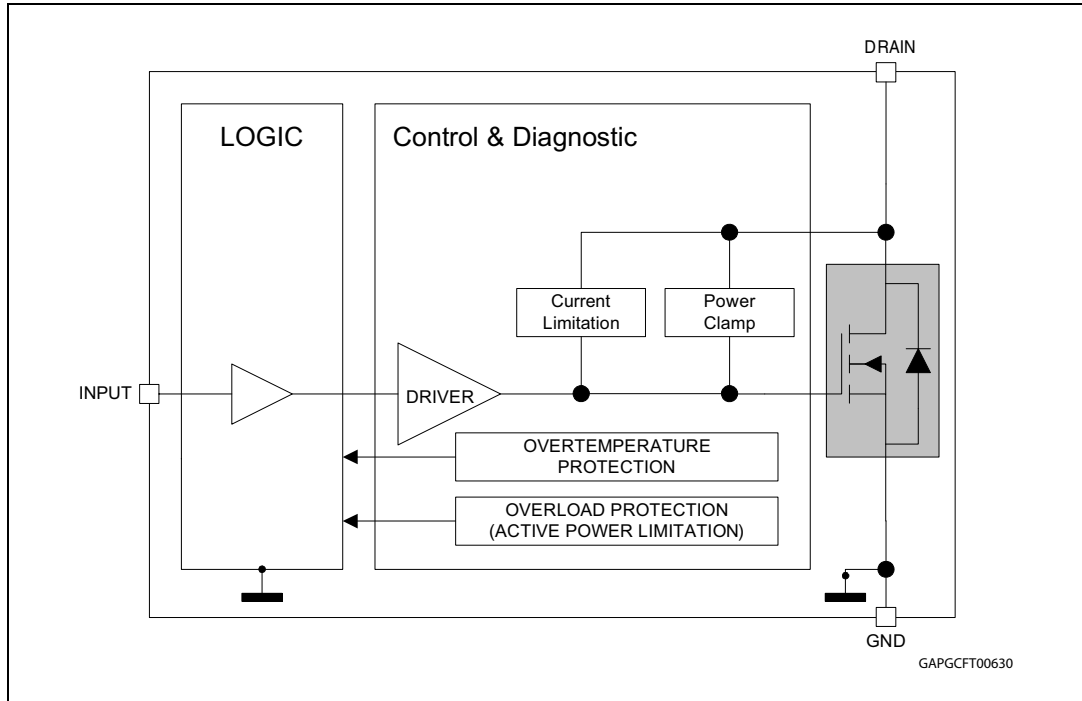


Figure 2. VNL5160S5-E block diagram

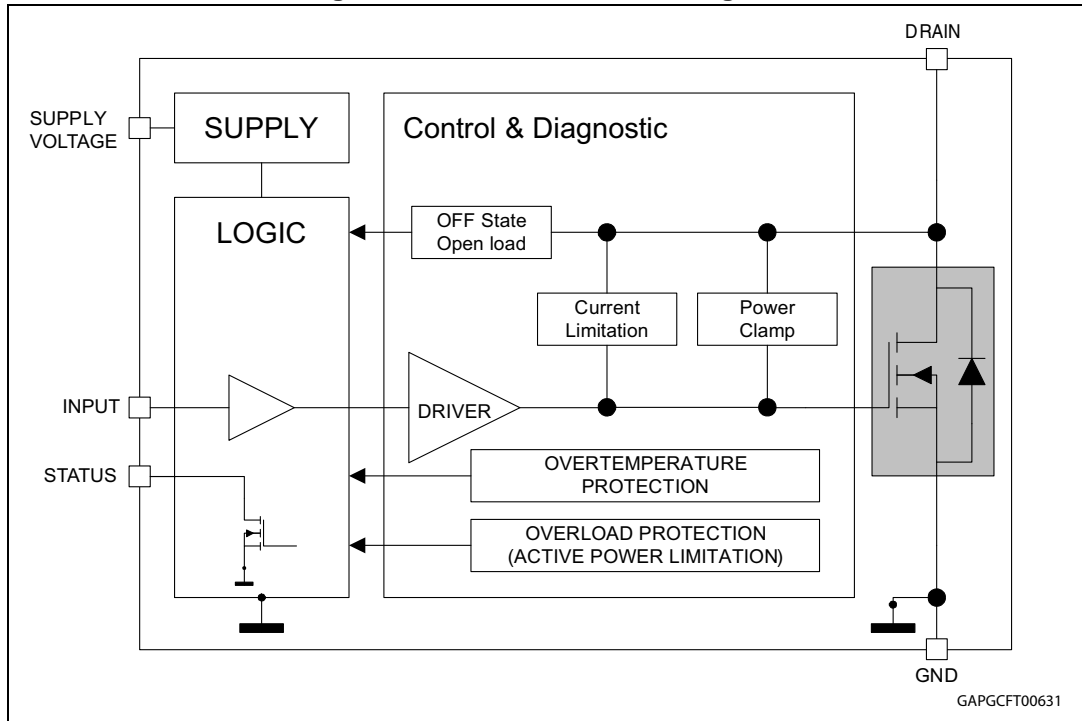


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state ⁽¹⁾
DRAIN	PowerMOS drain
SOURCE	PowerMOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5V)
STATUS	Open drain digital diagnostic pin ⁽²⁾

1. Internally connected to V_{supply} in the VNL5160N3-E.

2. Valid for VNL5160S5-E only.

Figure 3. VNL5160N3-E current and voltage conventions

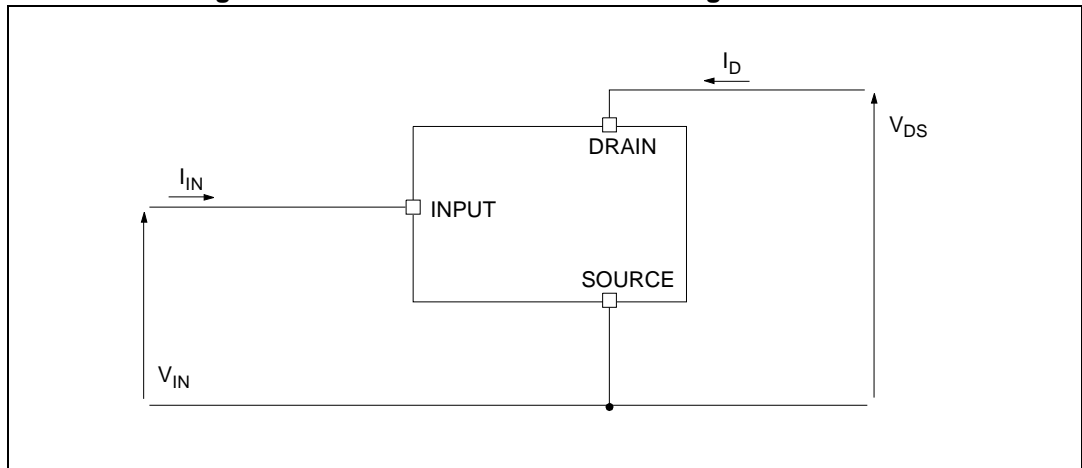


Figure 4. VNL5160S5-E current and voltage conventions

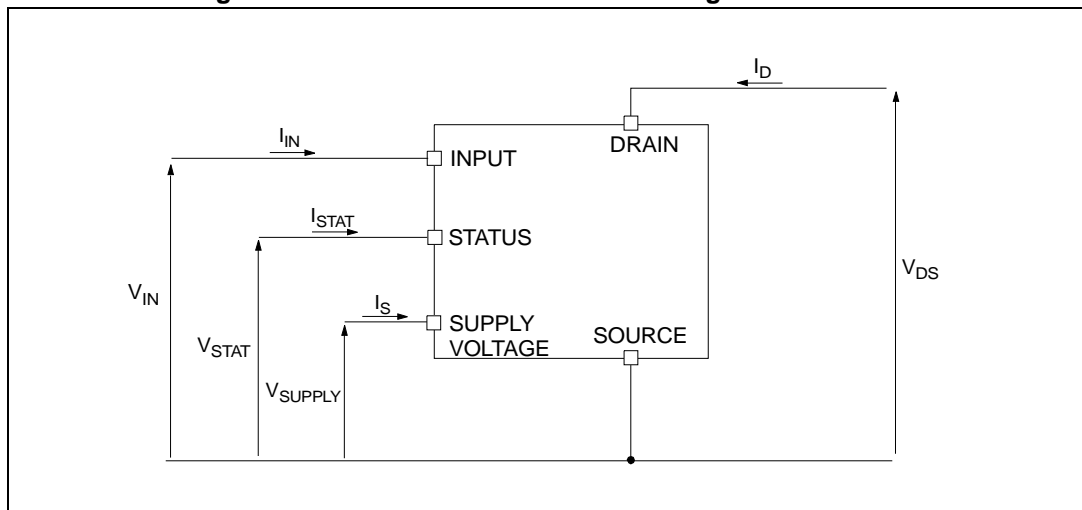


Figure 5. Configuration diagrams (top view)

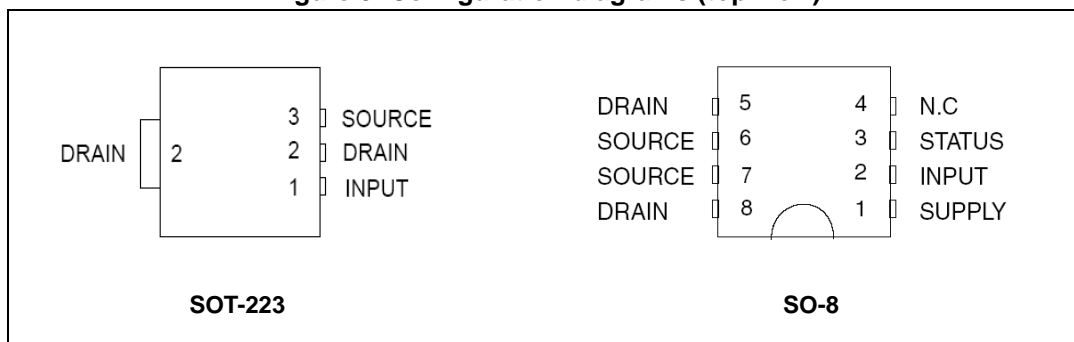


Table 3. Suggested connections for unused and not connected pins

Connection/pin	Status	N.C.	Input
Floating	X	X	X
To ground	Not allowed	X	Through 10kΩ resistor

2 Absolute maximum rating

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
V_{DS}	Drain-source voltage ($V_{IN}=0V$)	Internally clamped		V
I_D	DC drain current	Internally limited		A
$-I_D$	Reverse DC drain current	4		A
I_S	DC supply current	-	-1 to 10	mA
I_{IN}	DC input current	-1 to 10		mA
I_{STAT}	DC status current	-	-1 to 10	mA
V_{ESD1}	Electrostatic discharge ($R=1.5k\Omega$; $C=100pF$)			V
	- INPUT	4000		
	- STATUS	4000		
	- SUPPLY	4000		
	- DRAIN	5000		
V_{ESD2}	Electrostatic discharge on output pin only ($R=330\Omega$, $C=150pF$)	2000		V
T_j	Junction operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C
E_{as}	Single pulse avalanche energy $L = 8.5\text{ mH}$, $T_j = 150\text{ °C}$, $R_L = 0\ \Omega$, $V_{batt} = 13.5\text{ V}$, $I_{out} = I_{limL}$	37		mJ

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Maximum value		Unit
		SOT-223	SO-8	
R _{thj-amb}	Thermal resistance junction-ambient	146.8 ⁽¹⁾	103.1	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5cm² of Cu (at least 35 μm thick) connected to all DRAIN pins

3 Electrical characteristics

Values specified in this section are for $V_{IN} = V_{supply} = 4.5\text{ V to }5.5\text{ V}$, $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise stated.

Table 6. PowerMOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{supply}	Operating supply voltage		3.5	5	5.5	V
R_{ON}	On-state resistance	$V_{IN} = V_{supply} = 5\text{ V}; I_D = 1\text{ A}; T_j = 25\text{ °C}$		160	170	mΩ
		$V_{IN} = V_{supply} = 5\text{ V}; I_D = 1\text{ A}; T_j = 150\text{ °C}$			320	mΩ
V_{CLAMP}	Drain-source clamp voltage	$V_{IN} = 0\text{ V}; I_D = 1\text{ A}$	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	$V_{IN} = 0\text{ V}; I_D = 2\text{ mA}$	36			V
I_{DSS}	Off-state output current	$V_{IN} = 0\text{ V}; V_{DS} = 13\text{ V}; T_j = 25\text{ °C}$	0		3	μA
		$V_{IN} = 0\text{ V}; V_{DS} = 13\text{ V}; T_j = 125\text{ °C}$	0		5	μA

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	$I_D = 1\text{ A}; V_{IN} = 0\text{ V}$	—	0.8	—	V

Table 8. Input section⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	On-state $V_{IN} = V_{supply} = 5\text{ V}; V_{DS} = 0\text{ V}$		30	65	μA
V_{ICL}	Input clamp voltage	$I_S = 1\text{ mA}$	5.5		7	V
		$I_S = -1\text{ mA}$		-0.7		V
V_{INTH}	Input threshold voltage	$V_{DS} = V_{IN}; I_D = 1\text{ mA}$	1		3.5	V

1. Valid for VNL5160N3-E option (input & supply pins connected together).

Table 9. Status pin⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1\text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, $V_{STAT} = 5\text{ V}$			10	μA

Table 9. Status pin⁽¹⁾ (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF
V_{STCL}	Status clamp voltage	$I_{STAT} = 1\text{ mA}$	5.5		7	V
		$I_{STAT} = -1\text{ mA}$		-0.7		V

1. Valid for VNL5160S5-E option.

Table 10. Logic input⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.13			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V

1. Valid for VNL5160S5-E option.

Table 11. Open-load detection⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OI}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	0.6	1.2	1.7	V
$t_{d(oloff)}$	Delay between INPUT falling edge and STATUS falling edge in open-load condition	$I_{OUT} = 0\text{ A}$	45	425	1100	μs

1. Valid for VNL5160S5-E option.

Table 12. Supply section⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state $T_j = 25\text{ }^\circ\text{C}$; $V_{IN} = V_{DRAIN} = 0\text{ V}$		10	25	μA
		On-state $T_j = 25\text{ }^\circ\text{C}$; $V_{IN} = 5\text{ V}$; $V_{DS} = 0\text{ V}$		25	65	μA
V_{SCL}	Supply clamp voltage	$I_{SCL} = 1\text{ mA}$	5.5		7	V
		$I_{SCL} = -1\text{ mA}$		-0.7		V

1. Valid for VNL5160S5-E option.

Table 13. Switching characteristics ($V_{CC} = 13\text{ V}^{(1)}$)

Symbol	Parameter	Test conditions	SOT-223 ⁽²⁾			SO-8			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on delay time	$R_L = 13\Omega, V_{CC} = 13\text{V}^{(3)}$		8.9			8.9		μs
$t_{d(OFF)}$	Turn-off delay time	$R_L = 13\Omega, V_{CC} = 13\text{V}$		13.2			13.2		μs
t_r	Rise time	$R_L = 13\Omega, V_{CC} = 13\text{V}$		14.1			14.1		μs
t_f	Fall time	$R_L = 13\Omega, V_{CC} = 13\text{V}$		11.5			11.5		μs
W_{ON}	Switching energy losses at turn-on	$R_L = 13\Omega, V_{CC} = 13\text{V}$		34.3			34.3		μJ
W_{OFF}	Switching energy losses at turn-off	$R_L = 13\Omega, V_{CC} = 13\text{V}$		34.3			34.3		μJ

1. See [Figure 7: VNL5160N3-E application schematic](#) and [Figure 8: VNL5160S5-E application schematic](#).
2. $3.5\text{ V} < V_{S_{supply}} = V_{in} < 5.5\text{ V}$.
3. See [Figure 6: Switching characteristics](#).

Table 14. Protection and diagnostics

Symbol	Parameter	Test conditions ⁽¹⁾	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{DS} = 13\text{V}; V_{IN} = V_{supply} = 5\text{V}$	3.5	5	7.5	A
I_{limL}	Short circuit current during thermal cycling	$V_{DS} = 13\text{V}; T_R < T_j < T_{TSD}; V_{IN} = V_{supply} = 5\text{V}$		2.5		A
t_{dlim}	Step response current limit	$V_{DS} = 13\text{V}; V_{input} = 5\text{V}$		20		μs
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS}+1$	$T_{RS}+5$		$^{\circ}\text{C}$
$T_{RS}^{(2)}$	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$

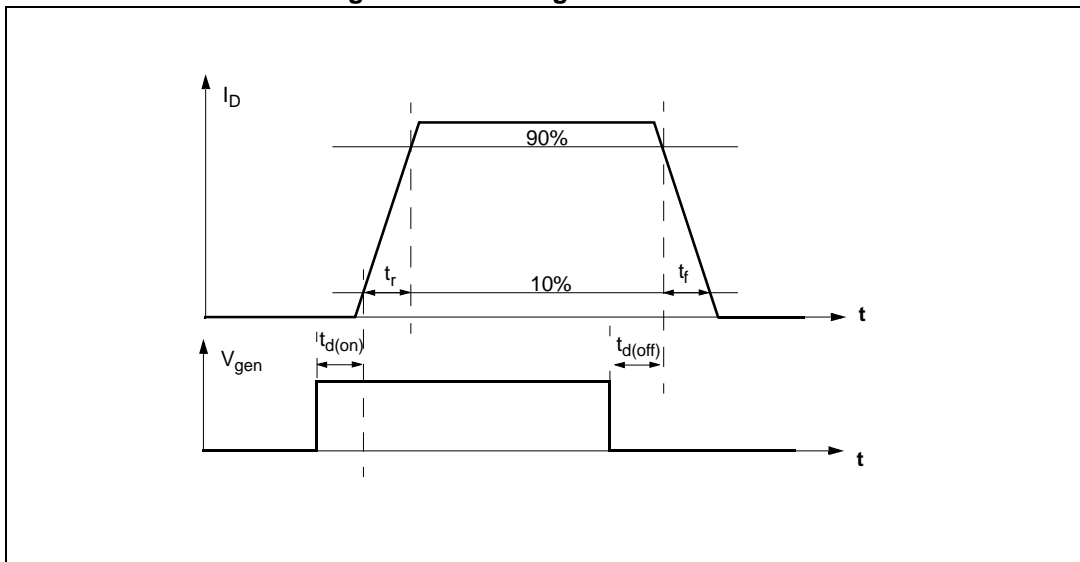
1. $V_{supply} = V_{input}$ in VNL5160N3-E version.
2. Valid for VNL5160S5-E option.

Table 15. Truth table (1)

Conditions	INPUT	DRAIN	STATUS
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Overtemperature	L	H	H
	H	H	L
Undervoltage	L	H	X
	H	H	X
Output voltage < V_{OL}	L	L	L
	H	L	H

1. Valid for VNL5160S5-E option

Figure 6. Switching characteristics



4 Application information

Figure 7. VNL5160N3-E application schematic

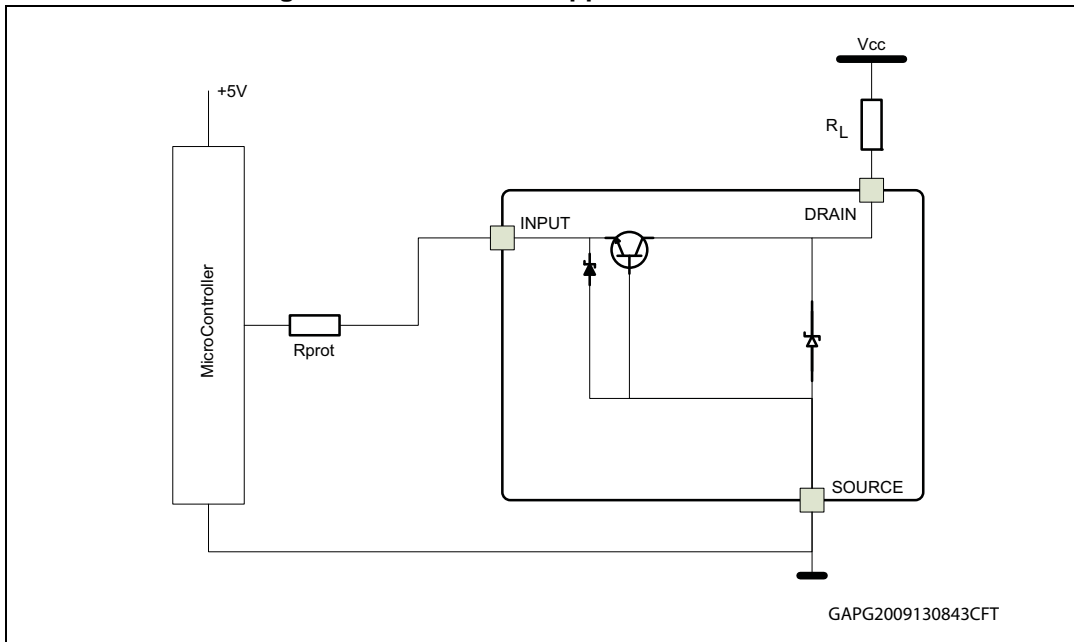
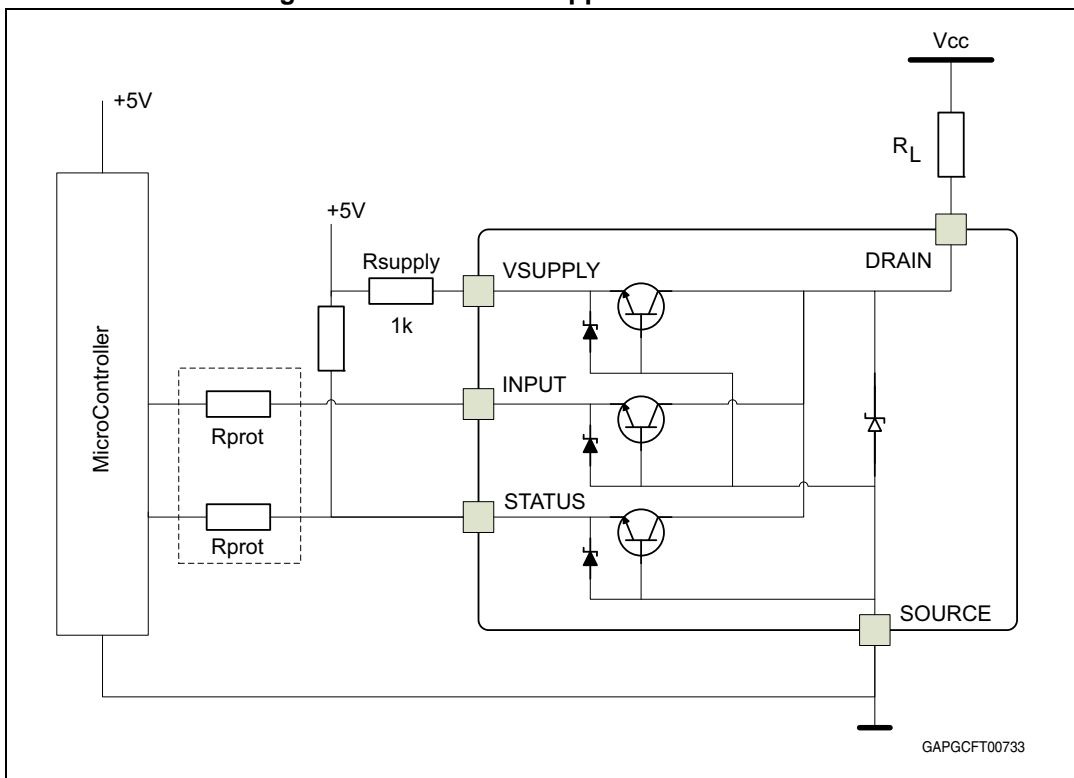


Figure 8. VNL5160S5-E application schematic



4.1 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/O pins from latching up^(a). The value of these resistors is a compromise between the leakage current of μC and the current required by the LSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os:

$$0.7/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For the following conditions:

$$I_{latchup} \geq 20mA$$

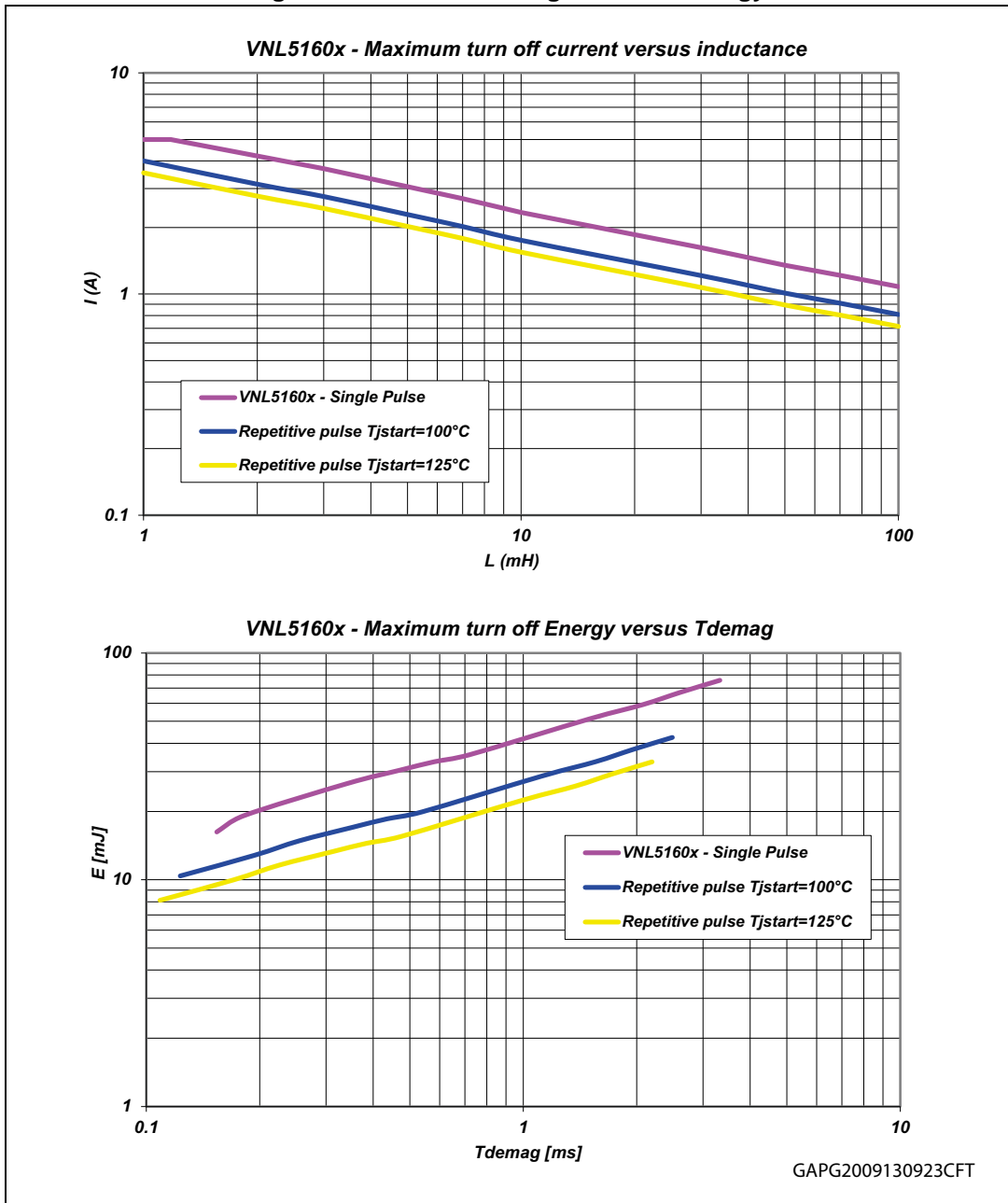
$$V_{OH\mu C} \geq 4.5V$$

$$35\Omega \leq R_{prot} \leq 100k\Omega.$$

Recommended value is $R_{prot} = 1 k\Omega$

a. In case of negative transient on the drain pin.

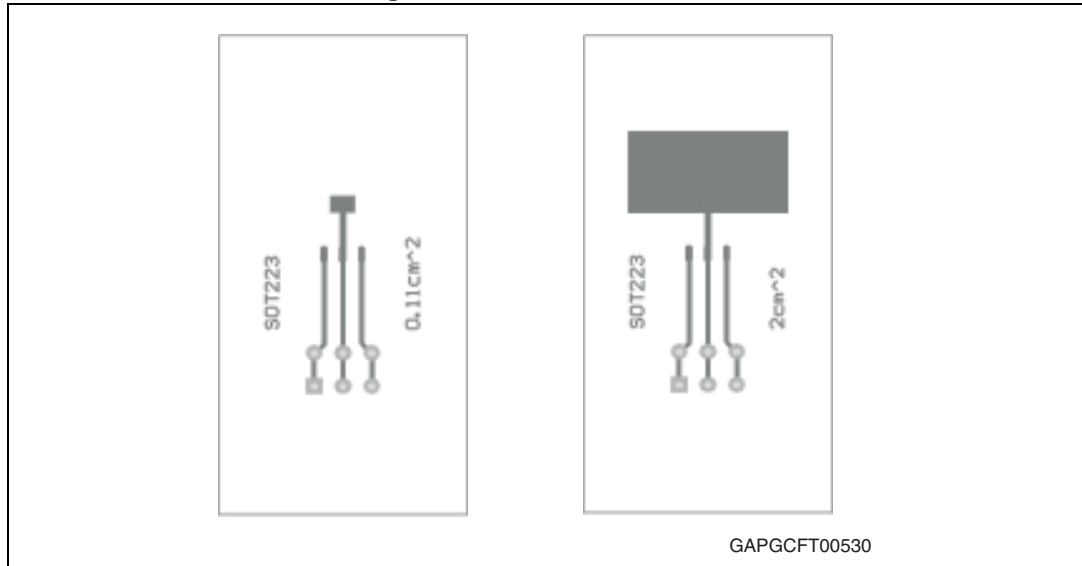
Figure 9. Maximum demagnetization energy



5 Package and PC board thermal data

5.1 SOT-223 thermal data

Figure 10. SOT-223 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 30 mm x 30 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad layout to 0.8 cm²).

Figure 11. SOT-223 $R_{thj-amb}$ vs PCB copper area in open box free air condition

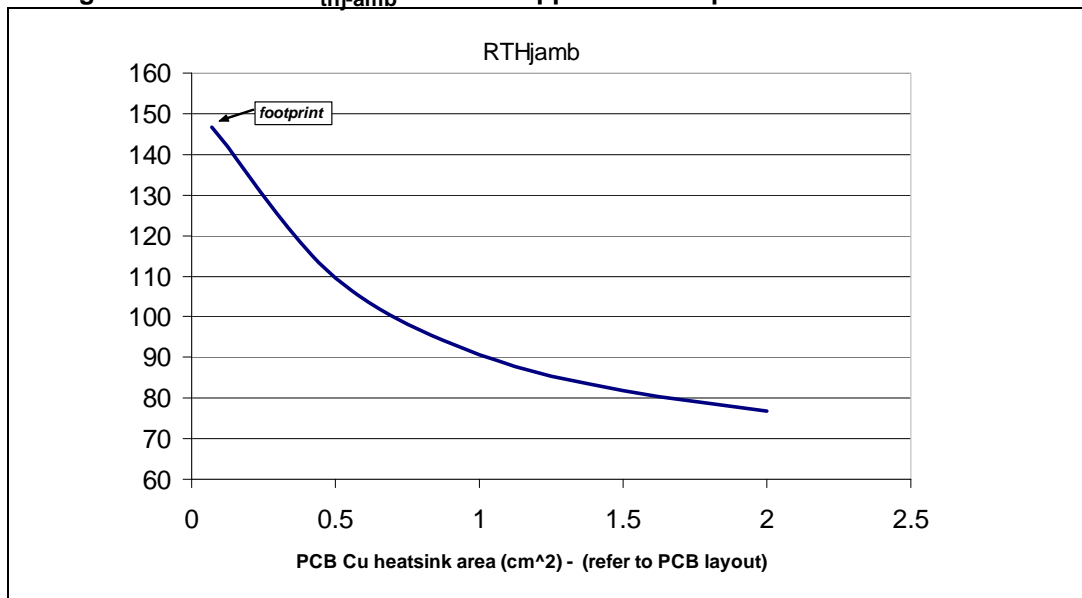
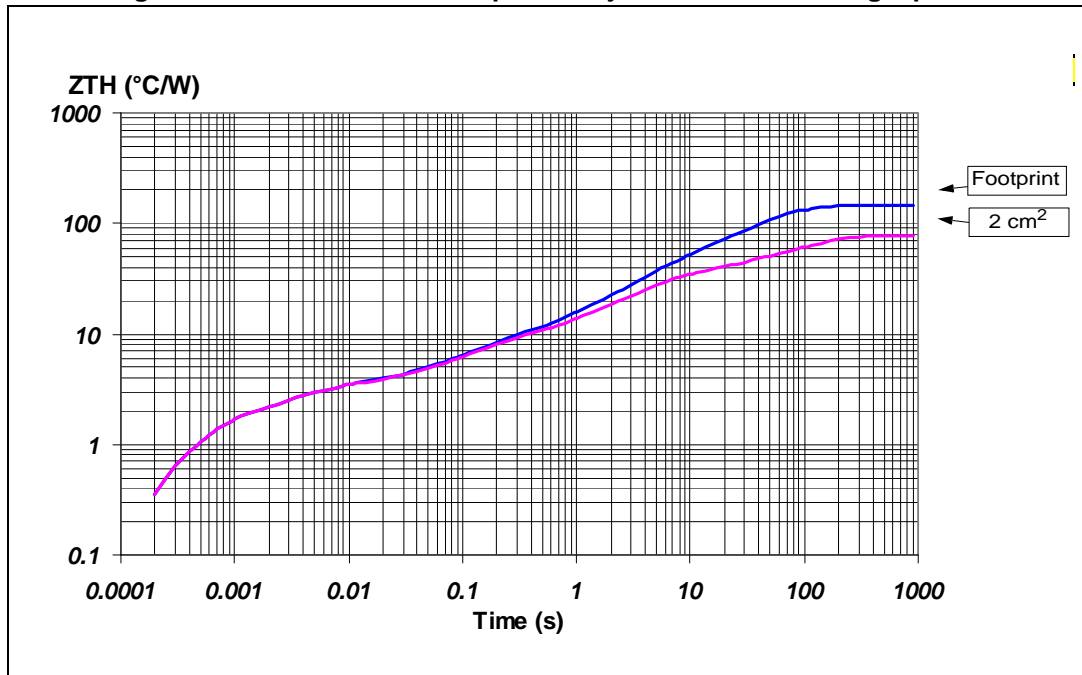


Figure 12. SOT-223 thermal impedance junction ambient single pulse

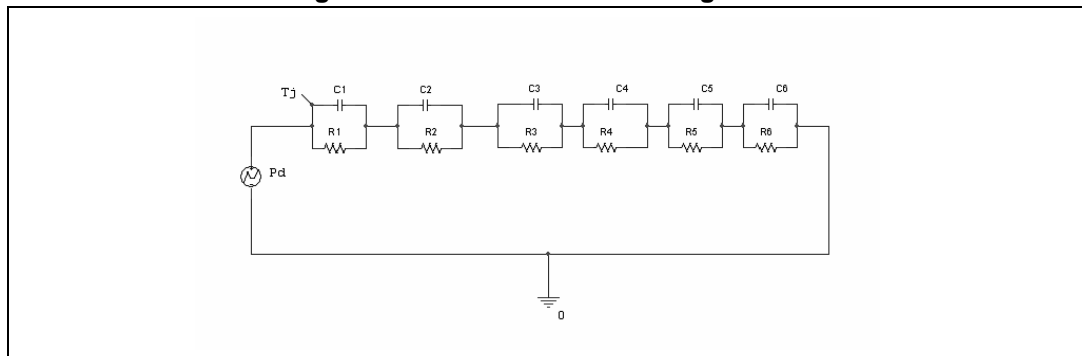


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 13. SOT-223 thermal fitting model



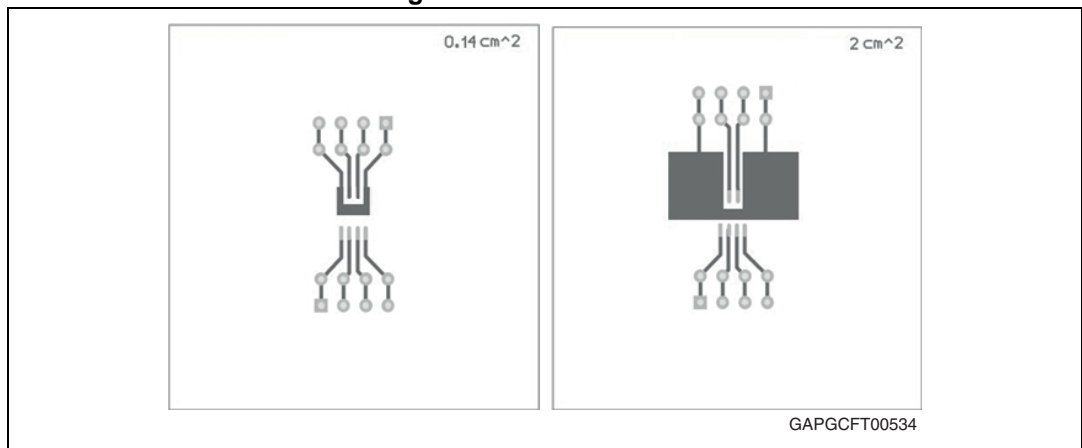
1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SOT-223 thermal parameter

Area/island (cm ²)	FP	2
R1 (°C/W)	1.4	
R2 (°C/W)	1.8	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	115	45
C1 (W·s/°C)	0.0003	
C2 (W·s/°C)	0.002	
C3 (W·s/°C)	0.03	
C4 (W·s/°C)	0.16	
C5 (W·s/°C)	1000	
C6 (W·s/°C)	0.4	2

5.2 SO-8 thermal data

Figure 14. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad layout to 2 cm²).

Figure 15. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition

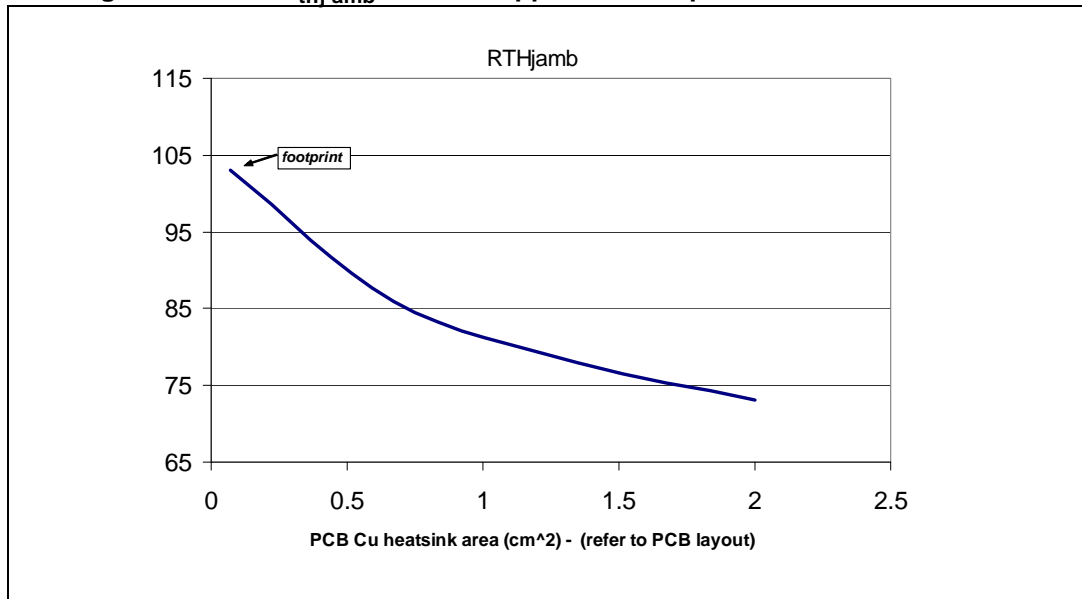
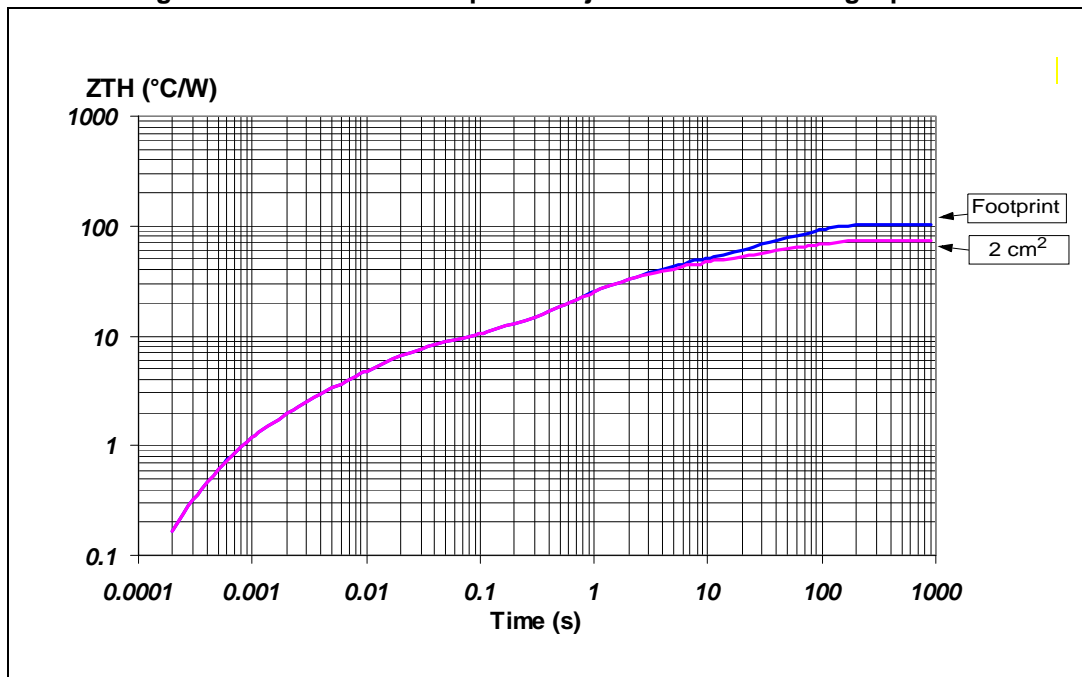


Figure 16. SO-8 thermal impedance junction ambient single pulse

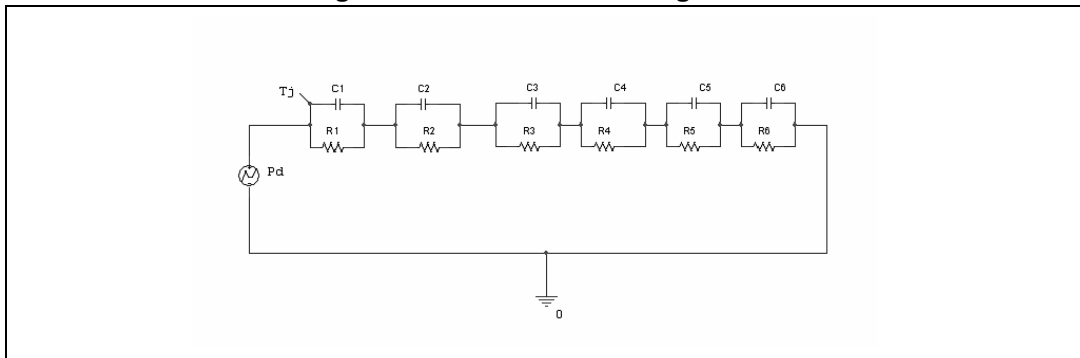


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 17. SO-8 thermal fitting model



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. SO-8 thermal parameter

Area/island (cm ²)	0.07	2
R1 (°C/W)	1.4	
R2 (°C/W)	3.2	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.0032	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

6 Package and packing information

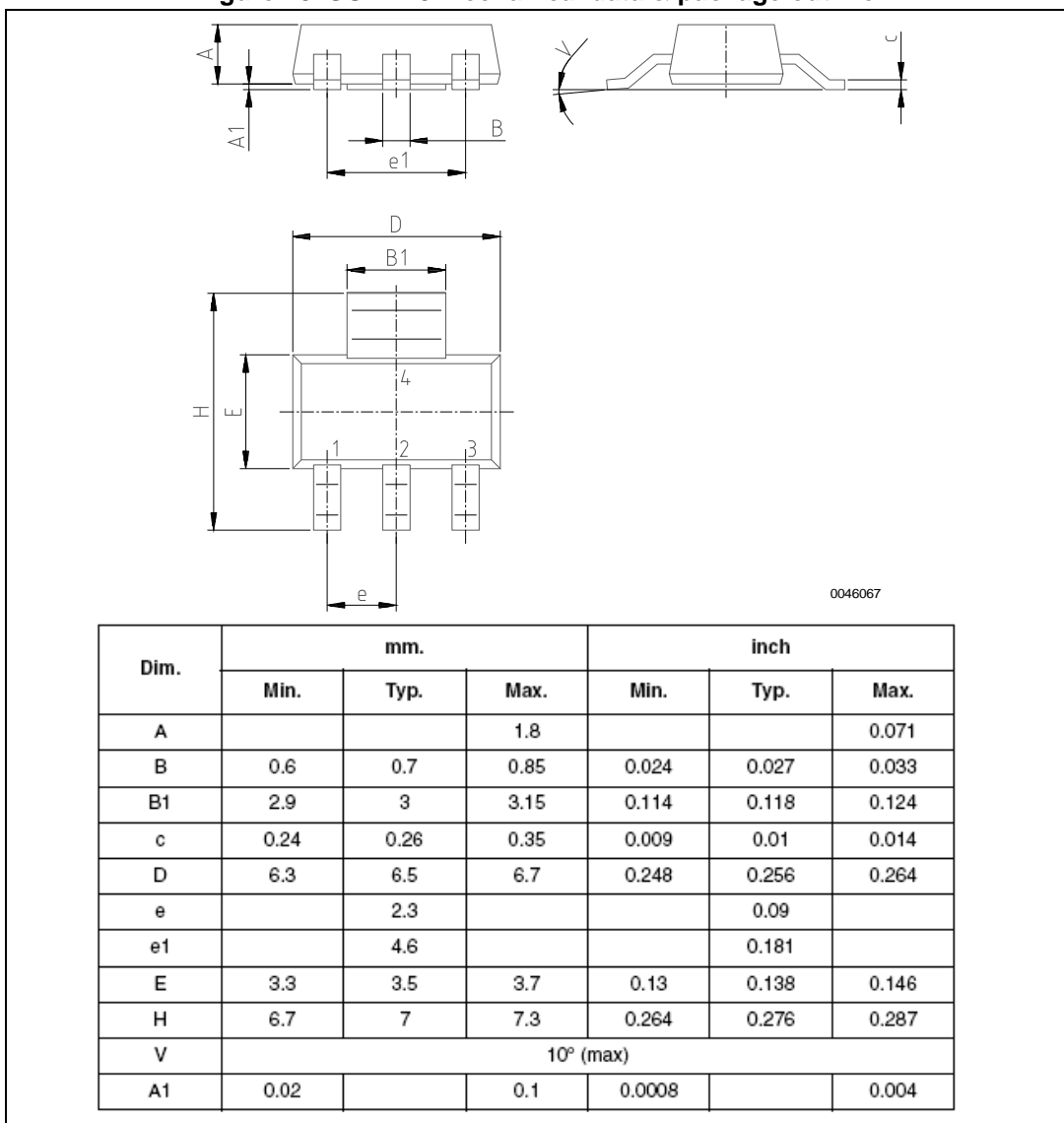
6.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

ECOPACK[®] is an ST trademark.

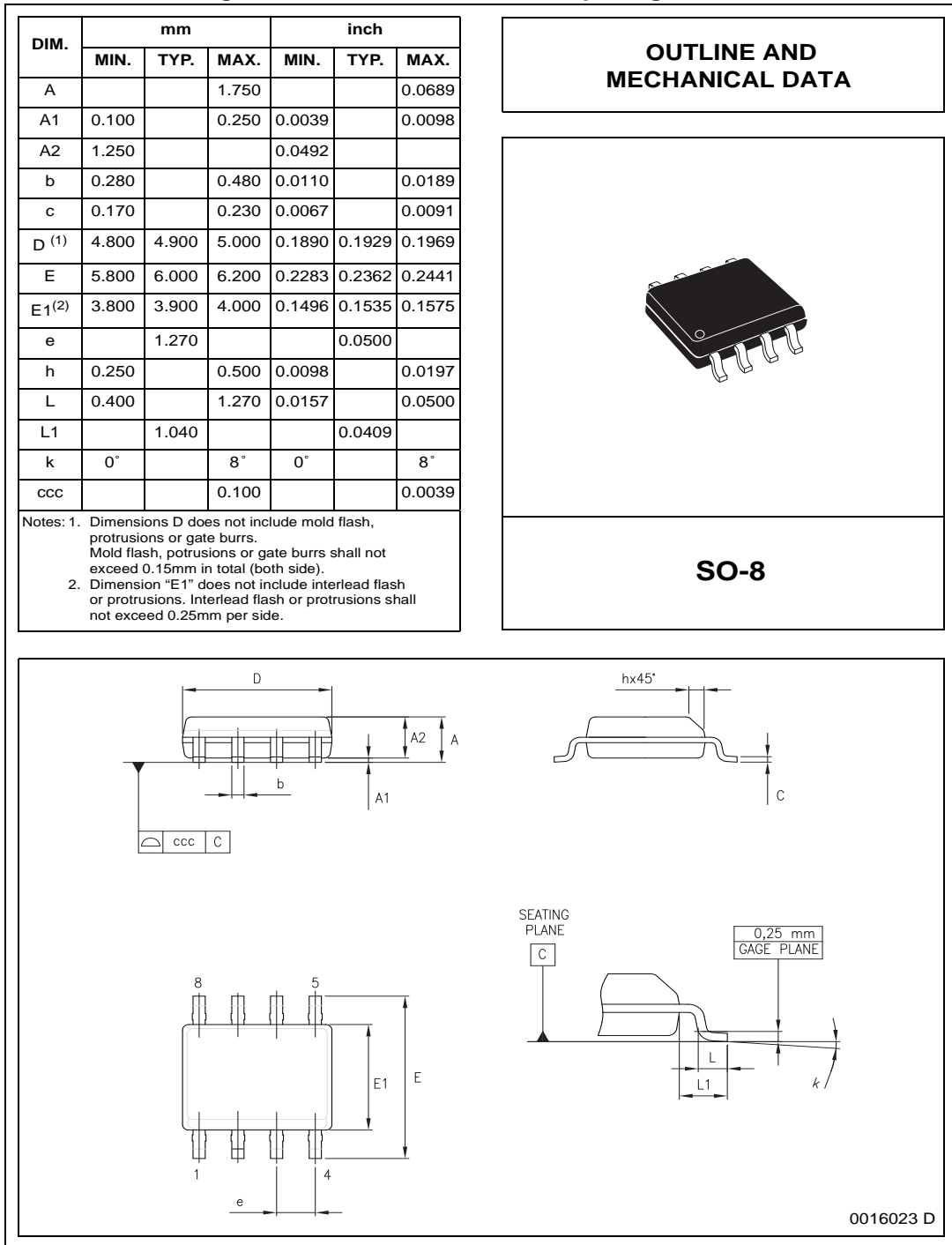
6.2 SOT-223 mechanical data

Figure 18. SOT-223 mechanical data & package outline



6.3 SO8 mechanical data

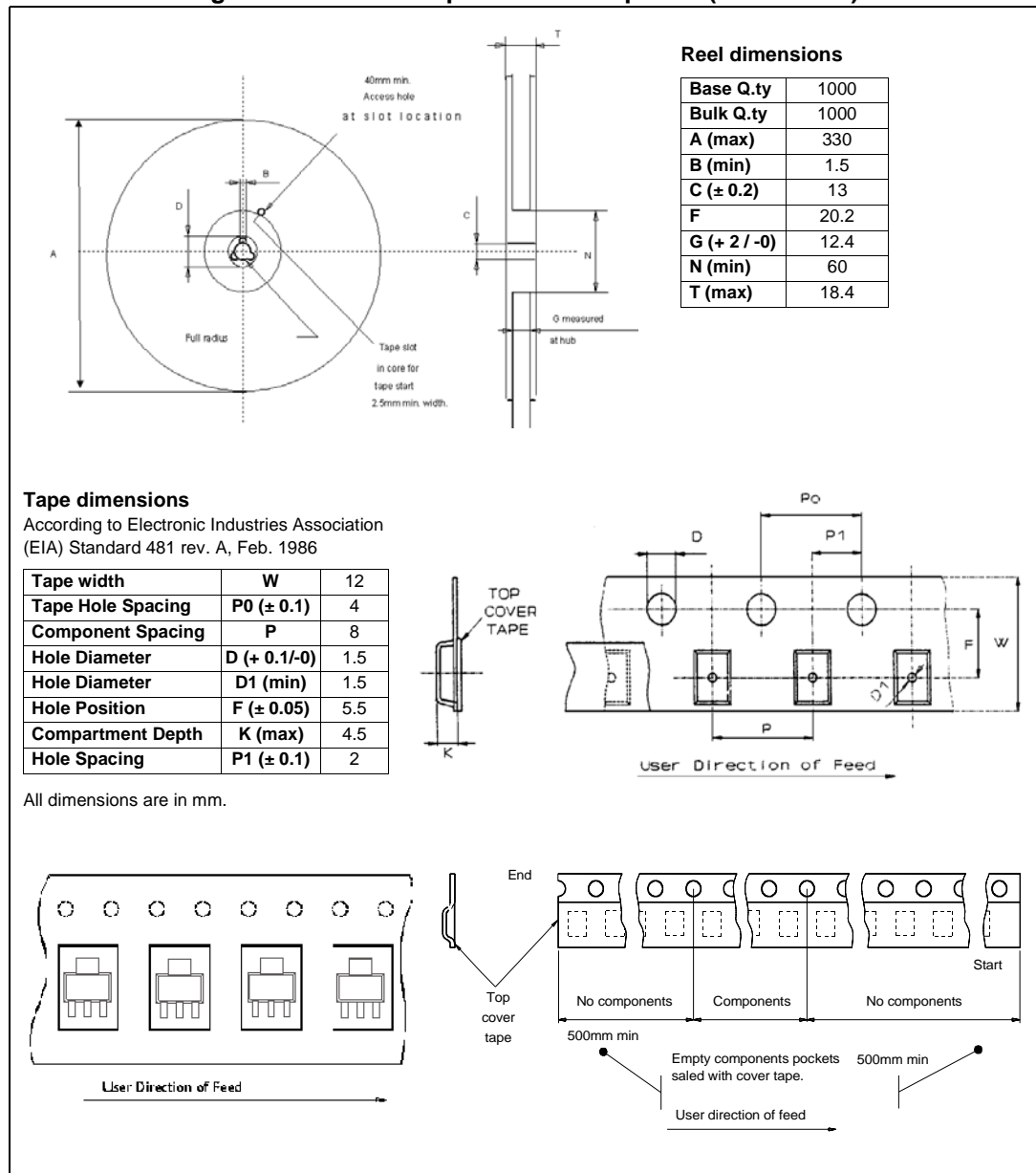
Figure 19. SO8 mechanical data & package outline



6.4 SOT-223 packing information

The devices can be packed in tube or tape and reel shipments (see the [Table 1: Device summary](#)).

Figure 20. SOT-223 tape and reel shipment (suffix "TR")



6.5 SO8 packing information

Figure 21. SO-8 tube shipment (no suffix)

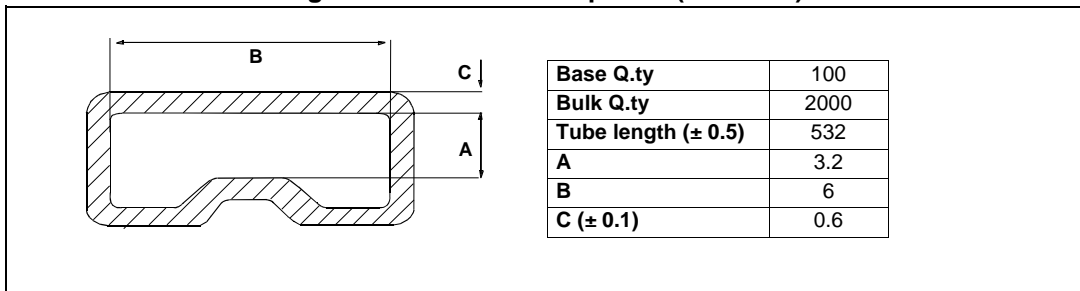
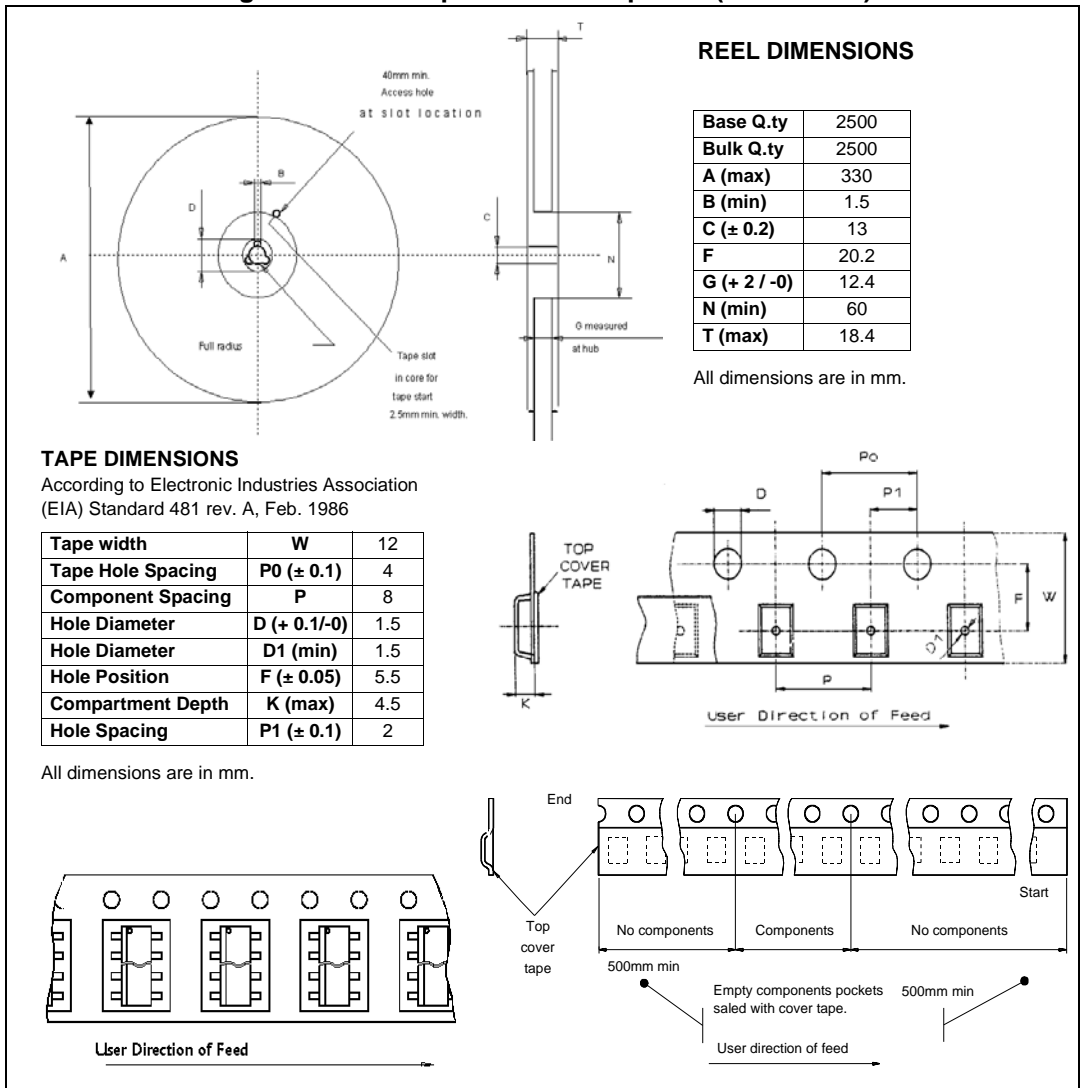


Figure 22. SO-8 tape and reel shipment (suffix "TR")



7 Revision history

Table 18. Document revision history

Date	Revision	Changes
17-Nov-2009	1	Initial release.
20-Feb-2012	2	Update the entire document in ST template. Update Section : Features in cover page.
20-Sep-2013	3	<p>Table 9: Status pin: – $-I_D$: updated value</p> <p>Table 9: Status pin: – I_{SS}: updated max value</p> <p>Table 13: Switching characteristics ($V_{CC} = 13 V$): – I_S: updated max value</p> <p>Updated Figure 8: VNL5160S5-E application schematic</p> <p>Updated Section 4.1: MCU I/O protection</p> <p>Updated Figure 9: Maximum demagnetization energy</p>

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com



单击下面可查看定价，库存，交付和生命周期等信息

[>>STMicroelectronics\(意法半导体\)](#)