DATASHEET

# 3A Rated µPOL™ Buck Regulator with Integrated Inductor and Digital Power System Management

## Features

- µPOL™ package with output inductor included
- Small size: 3.3mm x 3.3mm x 1.5mm
- Continuous 3A load capability
- Plug and play: no external compensation required
- Programmable operation using the $I^2C$ serial bus (fast mode and fast mode plus)
- Wide input voltage range: 8–16V
- Preset output voltage: 3.3 or 5V
- Enabled input, programmable under-voltage lock-out (UVLO) circuit
- Open-drain power-good (PG) indicator
- Built-in protection features
- Operating temperature from -40°C to +125°C
- Lead-free and halogen-free
- Compliant with EU Directives REACH and RoHS 6

## Applications

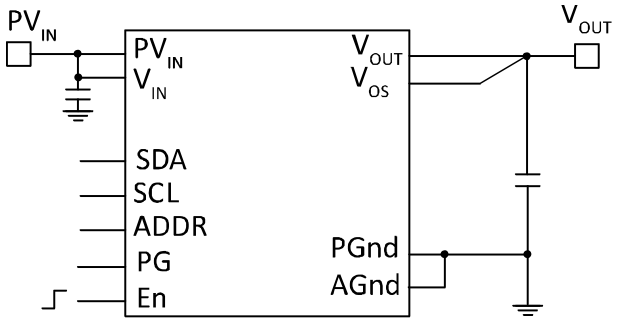
- Storage applications
- Telecom and networking applications
- Industrial applications
- Server applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation
- General DC-DC conversion

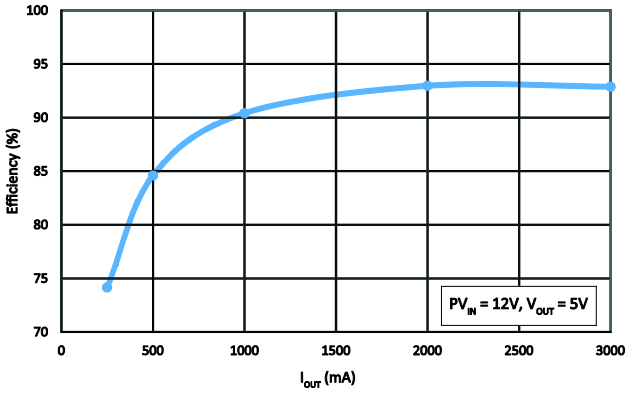
## Description

The FS1403 is an easy-to-use, fully integrated and highly efficient micro-point-of-load (µPOL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1403's operation using the Inter-Integrated Circuit ($I^2C$) protocol is unique in this class of product. Developing and optimizing all of these elements together has yielded the smallest, most efficient and fully featured 3A µPOL™ currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.



# Pin configuration

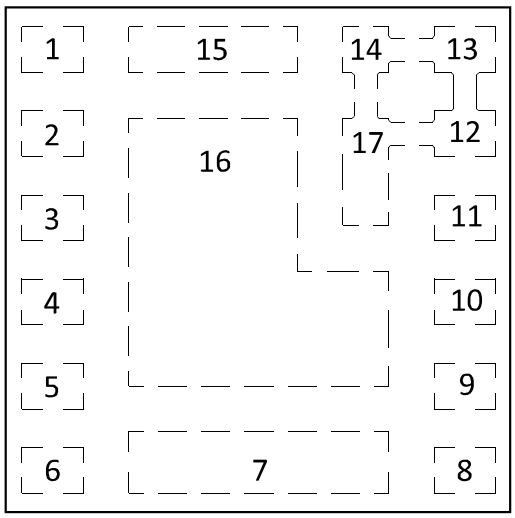



*Figure 1 Pin layout (top view)*

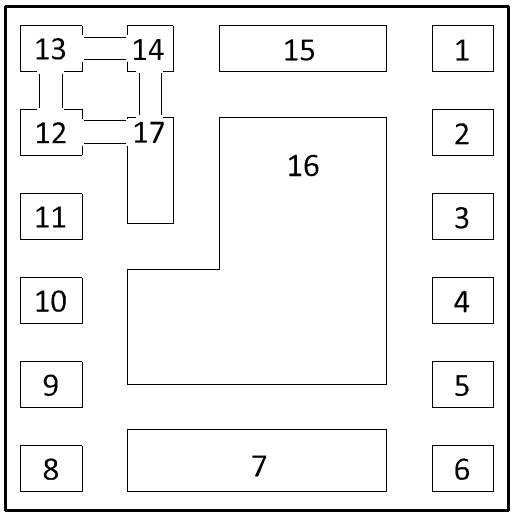



*Figure 2 Pin layout (bottom view)*

# Pin functions

| Pin Number | Name | Description |
|---|---|---|
| 1 | SDA | **$I^2C$ Data Serial Input/Output line.** Pull up to bus voltage with a 4.99kΩ resistor. |
| 2 | PG | **Power Good status.** Open drain of an internal MOSFET. Pull up to $V_{CC}$ – pin 10 or an external bias voltage (Figure 6) – with a 49.9kΩ resistor. |
| 3 | En | **Enable.** Switches the FS1403 on and off. Can be used with two external resistors to set an external UVLO (Figure 5). |
| 4 | SCL | **$I^2C$ Clock line.** Pull up to bus voltage with a 4.99kΩ resistor. |
| 5 | $V_{OS}$ | **$V_{OUT}$ sense pin.** Connect directly to the regulator output ($V_{OUT}$). |
| 6 | ADDR | **Address.** Connect to AGnd through a resistor to program FS1403 address (page 15). |
| 7 | $V_{OUT}$ | **Regulator output voltage.** Place output capacitors between this pin and PGnd (pin 8). |
| 8, 16 | PGnd | **Power ground.** Serves as a separate ground for the MOSFETs. Connect to the power ground plane in the application. |
| 9 | AGnd | **Signal ground.** Serves as the ground for the internal reference and control circuitry. |
| 10 | $V_{CC}$ | **Supply voltage.** May be an input bias for an external $V_{CC}$ voltage or the output of the internal LDO regulator. |
| 11 | $V_{IN}$ | **Input voltage.** Input for the internal LDO regulator. |
| 12,13,14, 17 | $PV_{IN}$ | **Power input voltage.** Input for the MOSFETs. |
| 15 | $V_{SW}$ | **Test point for internal $V_{SW}$.** Connect to an isolated pad on the PCB. |

# Block diagram

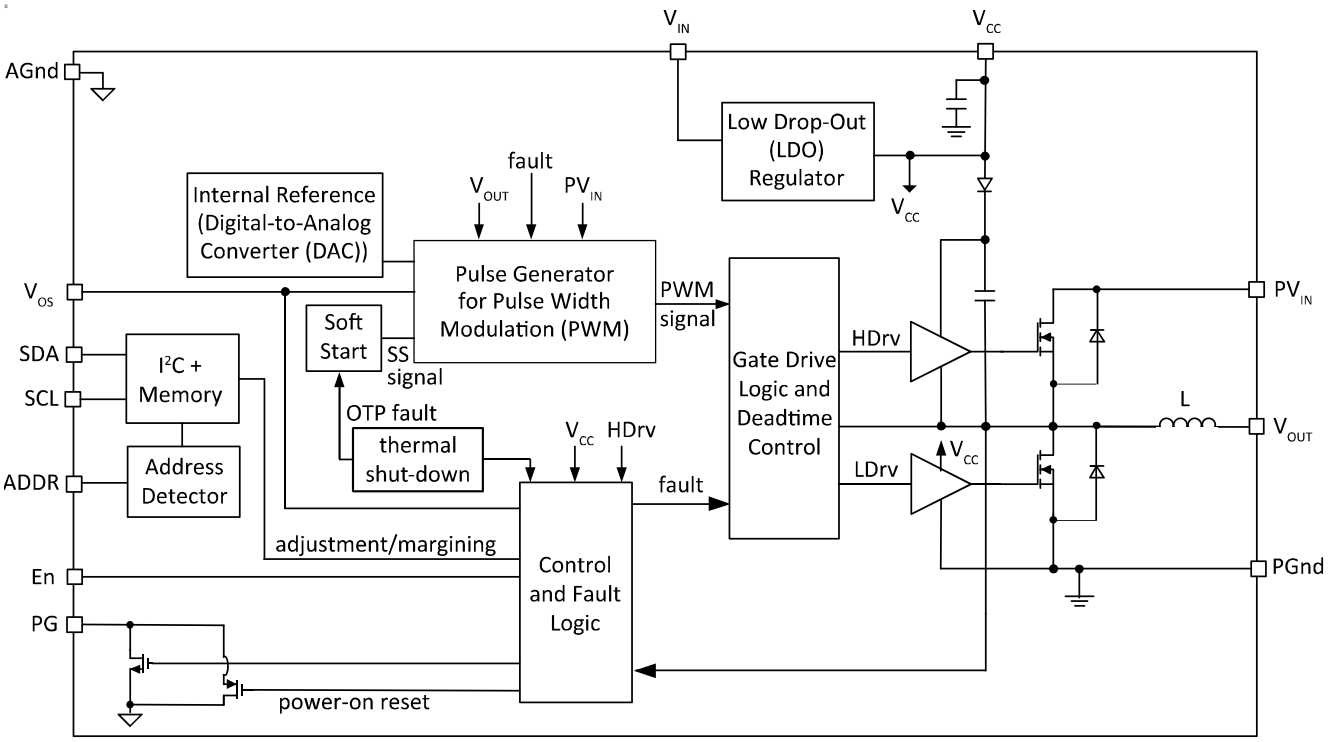



***Figure 3 FS1403 µPOL™***

# Typical applications

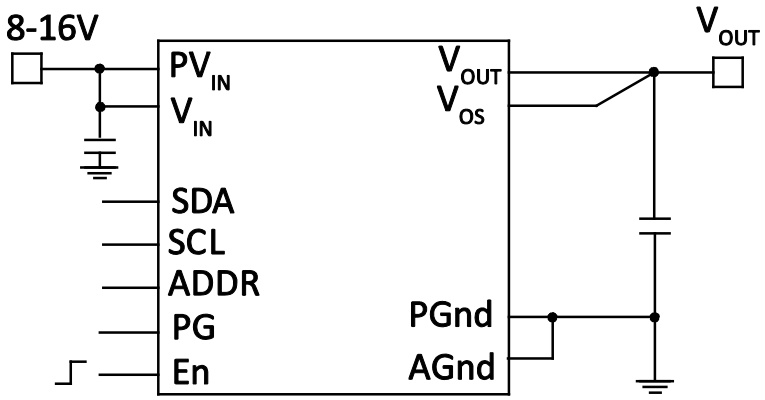



***Figure 4 Typical applications circuit***

# Absolute maximum ratings

**Warning:** Stresses beyond those shown may cause permanent damage to the FS1403.

**Note:** Functional operation of the FS1403 is not implied under these or any other conditions beyond those stated in the FS1403 specification.

| Reference | Range |
|---|---|
| $PV_{IN}$, $V_{IN}$, En to PGnd | -0.3V to 18V (Note 1, page 9) |
| $V_{CC}$ to PGnd | -0.3V to 6V (Note 2, page 9) |
| $V_{OS}$ to AGnd | -0.3V to $V_{CC}$ (Note 2, page 9) |
| PG to AGnd | -0.3V to $V_{CC}$ (Note 2, page 9) |
| PGnd to AGnd | -0.3V to +0.3V |
| ESD Classification | 2kV (HBM JESD22-A114) |
| Moisture Sensitivity Level | MSL 3 (JEDEC J-STD-020D) |

| Thermal Information | Range |
|---|---|
| Junction-to-Ambient Thermal Resistance $\Theta_{JA}$ | 22.6°C/W |
| Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$ | 2.36°C/W |
| Storage Temperature Range | -55°C to 150°C |
| Junction Temperature Range | -40°C to 150°C |
| Note: $\Theta_{JA}$ : FS1403 evaluation board and JEDEC specifications JESD 51-2A<br>$\Theta_{J\text{-}c\ (bottom)}$ : JEDEC specification JESD 51-8 | |

# Order information

## Package details

The FS1403 uses a µPOL™ 3.3 mm x 3.3 mm package delivered in tape-and-reel format (Figure 32), with either 250 or 4000 devices on a reel.

## Standard part numbers

Output voltages of 3.3V and 5V are available.

| | Part numbers | |
|---|---|---|
| $V_{OUT}$ | 250 devices on a reel | 4000 devices on a reel |
| 3.3 | FS1403-3300-AS | FS1403-3300-AL |
| 5.0 | FS1403-5000-AS | FS1403-5000-AL |

# Recommended operating conditions

| Definition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input Voltage Range (Note 3) | $PV_{IN}$, $V_{IN}$ | 8 | 16 | V |
| Output Voltage Range | $V_O$ | 3.3 | 5 | |
| Continuous Output Current Range | $I_O$ | 0 | 3 | A |
| Operating Junction Temperature | $T_J$ | -40 | 125 | °C |

# Electrical characteristics

| ELECTRICAL CHARACTERISTICS | | | | | | |
|---|---|---|---|---|---|---|
| **Unless otherwise stated, these specifications apply over: 5V < $PV_{IN}$ = $V_{IN}$ < 16V, 0°C < T < 125°C**<br>**Typical values are specified at $T_A$ = 25°C** | | | | | | |
| **Parameter** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| **Supply Current** | | | | | | |
| $V_{IN}$ Supply Current (Standby) | $I_{IN\ (STANDBY)}$ | Enable low | | 1 | | mA |
| $V_{IN}$ Supply Current (Static) | $I_{IN\ (STATIC)}$ | No switching, En = 2V | | 2 | | |
| $V_{IN}$ Supply Current (Dynamic) | $I_{IN\ (DYN)}$ | En high, $V_{IN}$ = 12V, $V_{OUT}$ = 5.0V, $F_{SW}$=1.4MHz | | 19 | 25 | |
| **Soft-Start** | | | | | | |
| Soft-Start Rate | $SS_{RATE}$ (default) | (Note 5) | | 1.0 | | V/ms |
| **Output Voltage** | | | | | | |
| Output Voltage Range | $V_{OUT}$ (default) | | | 5 | | V |
| | V (resolution) | | | 10 | | mV |
| Accuracy | | $T_J$ = 25°C, $PV_{IN}$ = 12V, $V_{OUT}$ = 5V (Note 4) | | ±0.5 | | % |
| | | 25°C < $T_J$ < 125°C, $PV_{IN}$ = 12V, $V_{OUT}$ = 3.3V (Note 4) | -1 | | 1 | |
| | | 25°C < $T_J$ < 125°C, $PV_{IN}$ = 12V, $V_{OUT}$ = 5V (Note 4) | -1.2 | | 1.2 | |
| **On-Time Timer Control** | | | | | | |
| On Time | $T_{ON}$ | $PV_{IN}$ = 12V, $V_{OUT}$ = 5V, $F_{SW}$=1.4 MHz | | 305 | | ns |
| Minimum On-Time | $T_{ON(MIN)}$ | (Note 5) | | 50 | | |
| Minimum Off-Time | $T_{OFF(MIN)}$ | | | 220 | 256 | |
| **Internal Low Drop-Out (LDO) Regulator** | | | | | | |
| LDO Regulator Output Voltage | $V_{CC}$ | 5.5V < $V_{IN}$ = 16V, 0 – 20mA | 4.9 | 5.2 | 5.5 | V |
| | | 4.5V <= $V_{IN}$ < 5.5V, 0 – 20mA | 4.3 | | | |
| Line Regulation | $V_{LN}$ | 5.5V < $V_{IN}$ = 16V, 20mA | | | 50 | mV |
| Load Regulation | $V_{LD}$ | 0 – 20mA | | | 100 | |
| Short Circuit Current | $I_{SHORT}$ | (Note 5) | | 90 | | mA |
| **Thermal Shut-Down** | | | | | | |
| Thermal Shut-Down | TSD (default) | | | 145 | | °C |
| Hysteresis | | | | 25 | | |

| ELECTRICAL CHARACTERISTICS | | | | | | |
|---|---|---|---|---|---|---|
| **Unless otherwise stated, these specifications apply over: 5V < $PV_{IN}$ = $V_{IN}$ < 16V, 0°C < T < 125°C<br>Typical values are specified at $T_A$ = 25°C** | | | | | | |
| **Parameter** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| **Under-Voltage Lock-Out** | | | | | | |
| $V_{CC}$ Start Threshold | $V_{CC}$_$UVLO_{(START)}$ | $V_{CC}$ Rising Trip Level | 3.7 | 4.0 | 4.2 | V |
| $V_{CC}$ Stop Threshold | $V_{CC}$_$UVLO_{(STOP)}$ | $V_{CC}$ Falling Trip Level | 3.6 | 3.8 | 3.95 | V |
| Enable Threshold | $En_{(HIGH)}$ | Ramping Up | 1.1 | 1.2 | 1.3 | V |
| | $En_{(LOW)}$ | Ramping Down | 0.9 | 1 | 1.06 | V |
| Input Impedance | $R_{EN}$ | | 500 | 1000 | 1500 | kΩ |
| **Current Limit** | | | | | | |
| Current Limit Threshold | $I_{OC}$ (default) | $T_J$ = 25°C | 3.7 | 4 | 4.4 | A |
| Hiccup Blanking Time | $T_{BLK(HICCUP)}$ | | | 20 | | ms |
| **Over-Voltage Protection** | | | | | | |
| Output Over-Voltage Protection Threshold | $V_{OVP}$ (default) | OVP Detect (Note 5) | 115 | 120 | 125 | $V_{OS}$% |
| Output Over-voltage Protection Delay | $T_{OVPDEL}$ | | | 5 | | µs |
| **Power Good (PG)** | | | | | | |
| Power Good Upper Threshold | $V_{PG(UPPER)}$ (default) | $V_{OUT}$ Rising | 85 | 90 | 95 | $V_{OS}$% |
| Power Good Hysteresis | $V_{PG(LOWER)}$ | $V_{OUT}$ Falling | | 5 | | $V_{OS}$% |
| Power Good Sink Current | $I_{PG}$ | PG = 0.5V, En = 2V | | 9 | | mA |

| ELECTRICAL CHARACTERISTICS | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Unless otherwise stated, these specifications apply over: 5V < $PV_{IN}$ = $V_{IN}$ < 16V, 0°C < T < 125°C<br>Typical values are specified at $T_A$ = 25°C** | | | | | | | |
| **Parameter** | **Symbol** | **Conditions** | **Fast-mode** | | **Fast-mode Plus** | | **Unit** |
| **$I^2C$ parameters** | | **(Note 5 for all parameters)** | **Min** | **Max** | **Min** | **Max** | |
| $I^2C$ bus voltage | $V_{BUS}$ | | 1.8 | 5.5 | 1.8 | 5.5 | V |
| LOW-level input voltage | $V_{IL}$ | | −0.5 | $0.3V_{BUS}$ | −0.5 | $0.3V_{BUS}$ | V |
| HIGH-level input voltage | $V_{IH}$ | | $0.7V_{BUS}$ | | $0.7V_{BUS}$ | | V |
| Hysteresis | $V_{HYS}$ | | $0.05V_{BUS}$ | | $0.05V_{BUS}$ | | V |
| LOW-level output voltage 1 | $V_{OL1}$ | (open-drain or open-collector) at 3mA sink current; $V_{DD}$ > 2 V, | 0 | 0.4 | 0 | 0.4 | V |
| LOW-level output voltage 2 | $V_{OL2}$ | (open-drain or open-collector) at 2mA sink current; $V_{DD}$ ≤ 2 V, | 0 | $0.2V_{BUS}$ | 0 | $0.2V_{BUS}$ | V |
| LOW-level output current | $I_{OL}$ | $V_{OL}$ = 0.4 V, | 3 | - | 3 | - | mA |
| | | $V_{OL}$ = 0.6 V | 6 | - | 6 | - | mA |

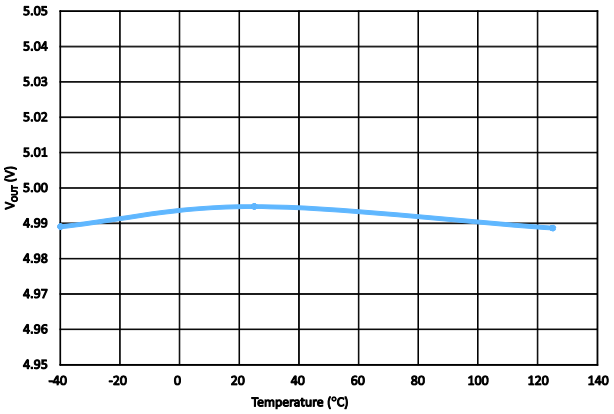
| ELECTRICAL CHARACTERISTICS | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Unless otherwise stated, these specifications apply over: 5V < $PV_{IN}$ = $V_{IN}$ < 16V, 0°C < T < 125°C**<br>**Typical values are specified at $T_A$ = 25°C** | | | | | | | |
| **Parameter** | **Symbol** | **Conditions** | **Fast-mode** | | **Fast-mode Plus** | | **Unit** |
| **$I^2C$ parameters** | | **(Note 5 for all parameters)** | **Min** | **Max** | **Min** | **Max** | |
| Output fall time | $T_{OF}$ | From $V_{IHmin}$ to $V_{ILmax}$ | 20 × ($V_{BUS}$/5.5 V) | 250 | 20 × ($V_{BUS}$/5.5 V) | 125 | ns |
| Pulse width of spikes that must be suppressed by the input filter | $T_{SP}$ | | 0 | 50 | 0 | 50 | |
| Input current each I/O pin | $I_I$ | | −10 | 10 | −10 | 10 | µA |
| Capacitance for each I/O pin | $C_I$ | | - | 10 | - | 10 | pF |
| SCL clock frequency | $F_{SCL}$ | | 0 | 400 | 0 | 1000 | kHz |
| Hold time (repeated) START condition | $T_{HD;STA}$ | After this time, the first clock pulse is generated | 0.6 | - | 0.26 | - | µs |
| LOW period of the SCL clock | $T_{LOW}$ | | 1.3 | - | 0.5 | - | |
| HIGH period of the SCL clock | $T_{HIGH}$ | | 0.6 | - | 0.26 | - | |
| Set-up time for a repeated START condition | $T_{SU;STA}$ | | 0.6 | - | 0.26 | - | |
| Data hold time | $T_{HD;DAT}$ | $I^2C$-bus devices | 0 | - | 0 | - | |
| Data set-up time | $T_{SU;DAT}$ | | 100 | - | 50 | - | ns |
| Rise time of SDA and SCL signals | $T_R$ | | 20 | 300 | - | 120 | |
| Fall time of SDA and SCL signals | $T_F$ | | 20 × ($V_{DD}$/5.5 V) | 300 | 20 × ($V_{DD}$/5.5 V) | 120 | |
| Set-up time for STOP condition | $T_{SU;STO}$ | | 0.6 | - | 0.26 | - | µs |
| Bus free time between a STOP and START condition | $T_{BUF}$ | | 1.3 | - | 0.5 | - | |
| Capacitive load for each bus line | $C_B$ | | - | 400 | - | 550 | pF |
| Data valid time | $T_{VD;DAT}$ | | - | 0.9 | - | 0.45 | µs |
| Data valid acknowledge time | $T_{VD;ACK}$ | | - | 0.9 | - | 0.45 | |
| Noise margin at the LOW level | $V_{NL}$ | For each connected device, including hysteresis | 0.1$V_{DD}$ | - | 0.1$V_{DD}$ | - | V |
| Noise margin at the HIGH level | $V_{NH}$ | | 0.2$V_{DD}$ | - | 0.2$V_{DD}$ | - | |
| SDA timeout | $T_{TO}$ | | 200 | | 200 | | µs |

**Notes**

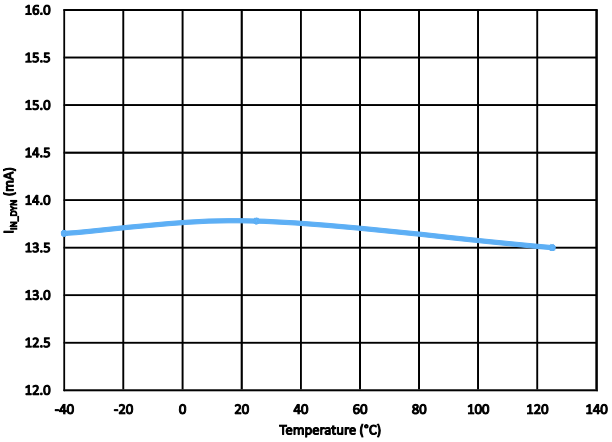
1 PGnd pin and AGnd pin are connected together
2 Must not exceed 6V
3 Maximum switch node voltage should not exceed 22V
4 Hot and cold temperature performance is assured by correlation using statistical quality control but not tested in production; performance at 25°C is tested and guaranteed in production environment
5 Guaranteed by design but not tested in production

# Temperature characteristics

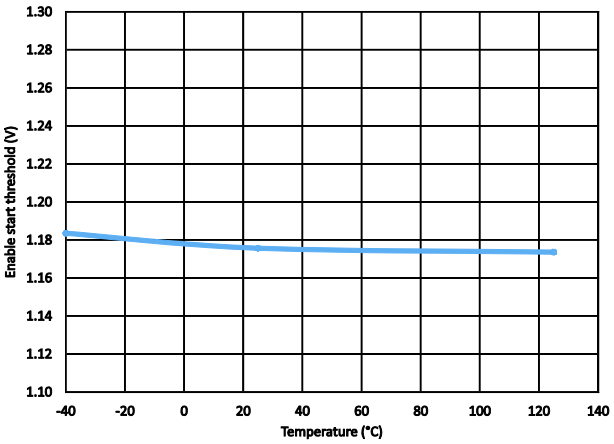
### Output Voltage



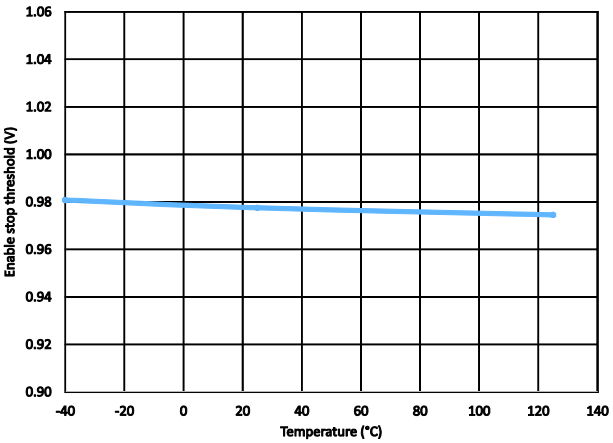

### $V_{IN}$ Supply Current (Dynamic)



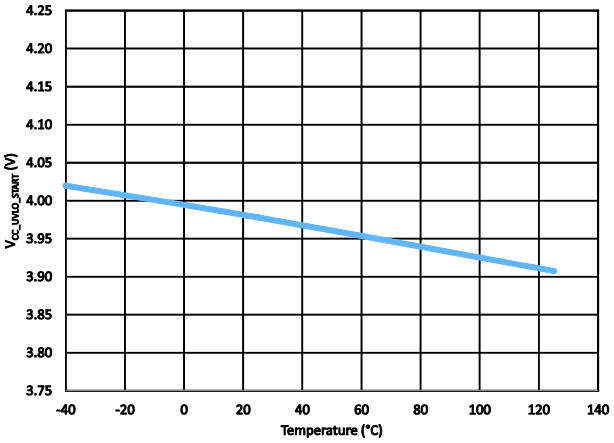

### Enable Start Threshold



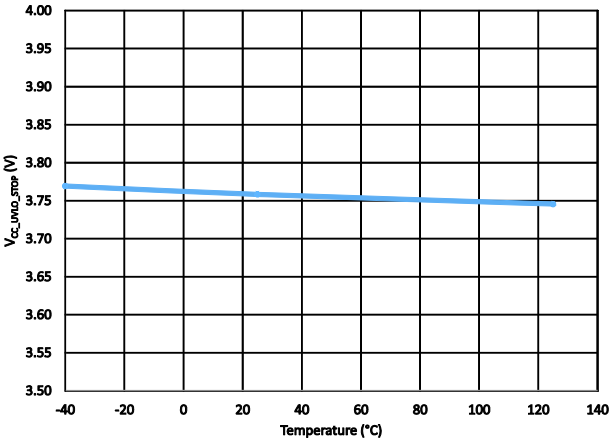

### Enable Stop Threshold



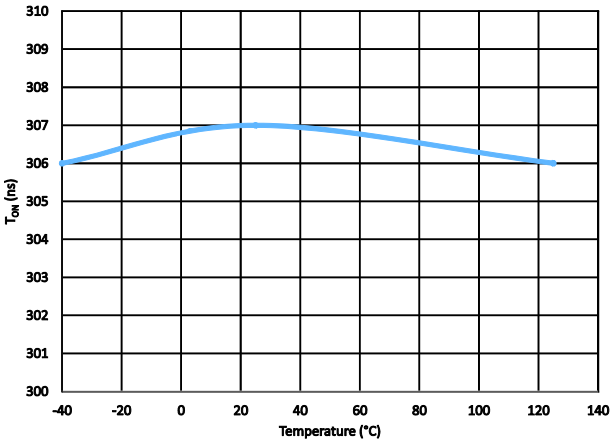

### $V_{CC}$ Start Threshold



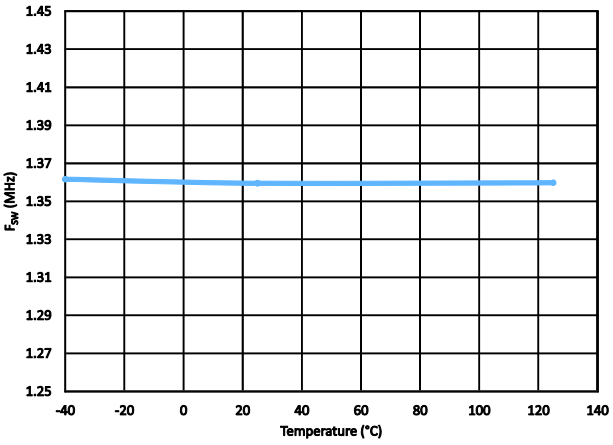

### $V_{CC}$ Stop Threshold



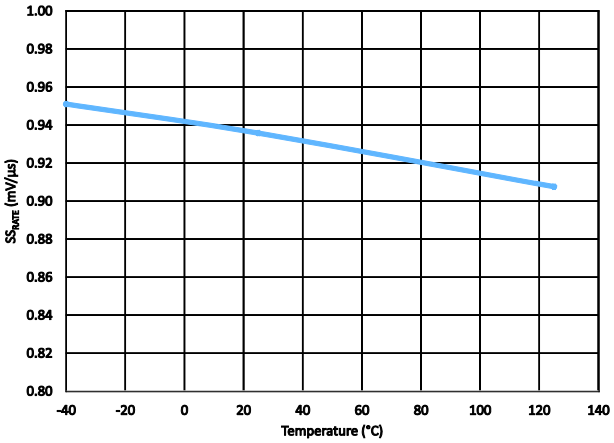
### On Time



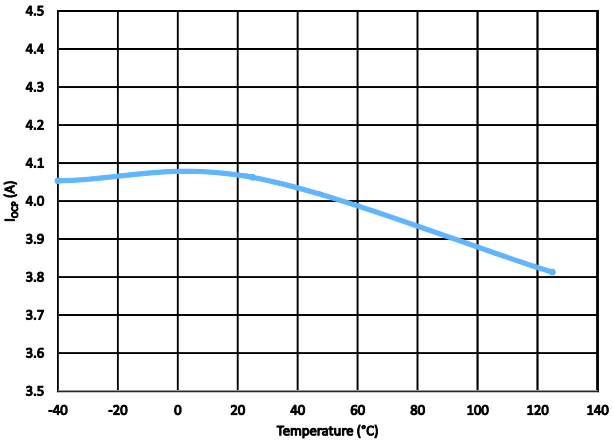

### Switching Frequency




### Soft-Start Rate



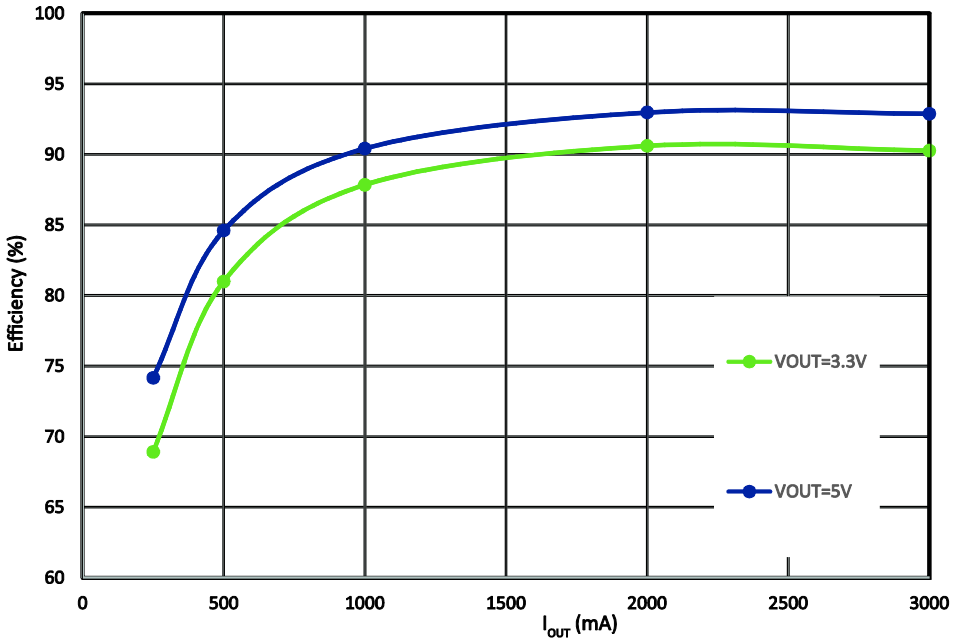

### Current Limit Threshold

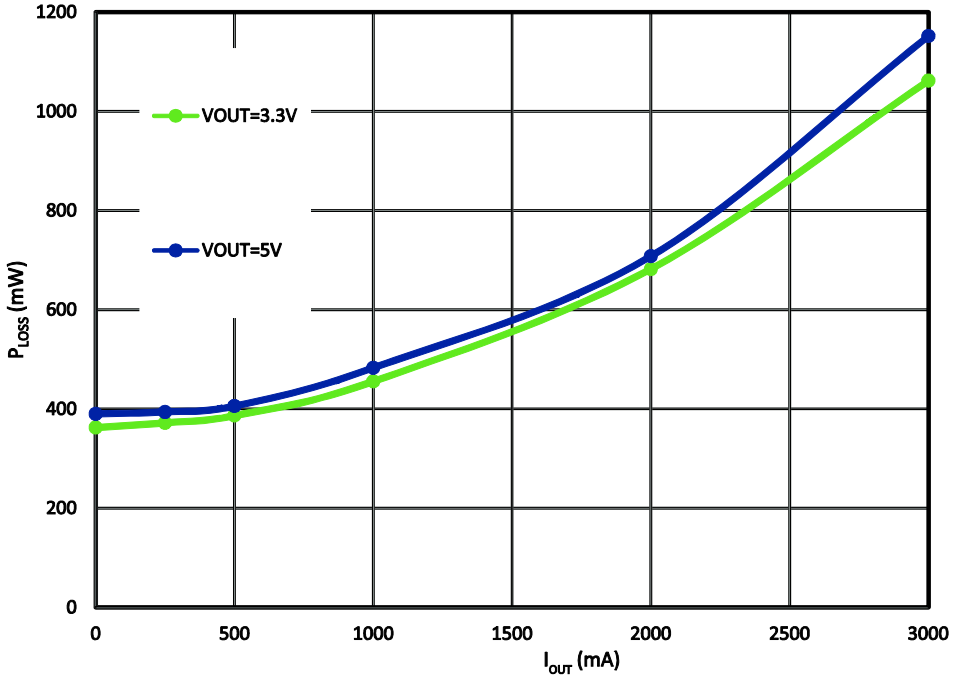


# Efficiency characteristics

**Typical efficiency and power loss at $PV_{IN}$ = 12V**

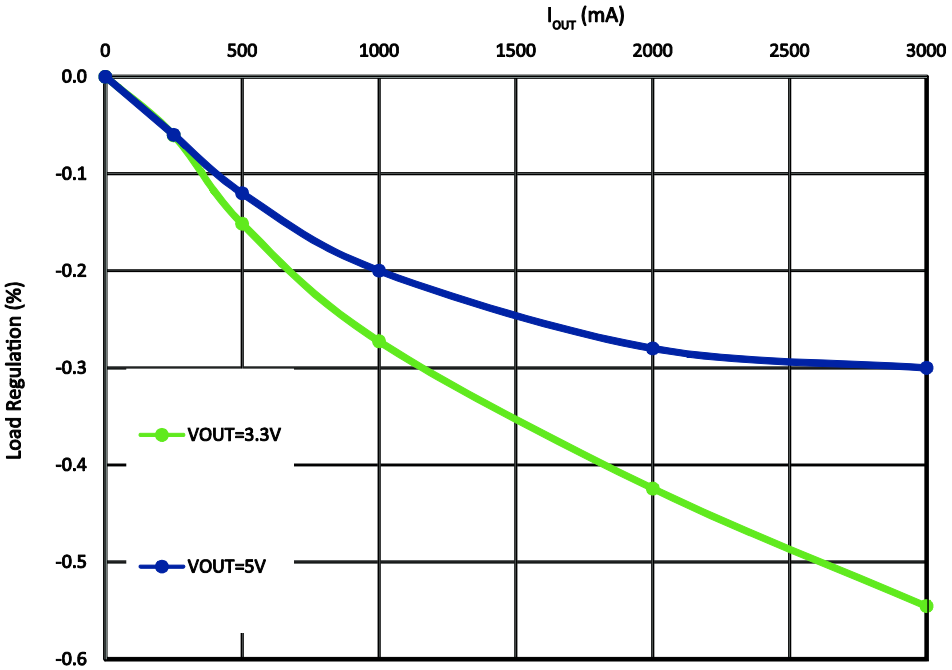
$PV_{IN}$ = 12V, Internal LDO used, $I_O$ = 0A-3A, room temperature, no air flow, all losses included



**Typical load regulation**

$PV_{IN}$ = 12V, internal LDO used, $I_O$ = 0A-3A, room temperature, no air flow



# Applications information

## Overview

The FS1403 is an easy-to-use, fully integrated and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the $I^2C$ protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues.

## Bias voltage

The FS1403 has an integrated Low Drop-Out (LDO) regulator, providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the $V_{IN}$ pin should be connected to the $PV_{IN}$ pin (Figure 5). If an external bias voltage is used, the $V_{IN}$ pin should be connected to the $V_{CC}$ pin to bypass the internal LDO regulator (Figure 6).

The supply voltage (internal or external) rises with $V_{IN}$ and does not need to be enabled using the En pin. Consequently, $I^2C$ communication can begin as soon as:

- $V_{CC}$_UVLO start threshold is exceeded
- Memory contents are loaded
- Initialization is complete
- Address offset is read

**Note:** **Until initialization is complete, a small leakage current (≈3.4µA) will flow from the device into the output. This may significantly pre-bias the output voltage in applications with long $V_{IN}$/$V_{CC}$ rise times. To prevent this, a small load capable of sinking 3.4µA should be connected in such applications.**

The part ID for the FS1403 is 0x80 and may be read in register 0x04. The $I^2C$ bus may be pulled up either to $V_{CC}$ or to a system $I^2C$ bus voltage. The FS1403 offers two ranges for the $I^2C$ bus voltage, defined by the user register bit **Bus_voltage_sel**.

| Register | Bits | Name/Description |
|---|---|---|
| 0x1A | [1] | **Bus_voltage_sel**<br>0:1.8–2.5V, 1: 3.3–5V |

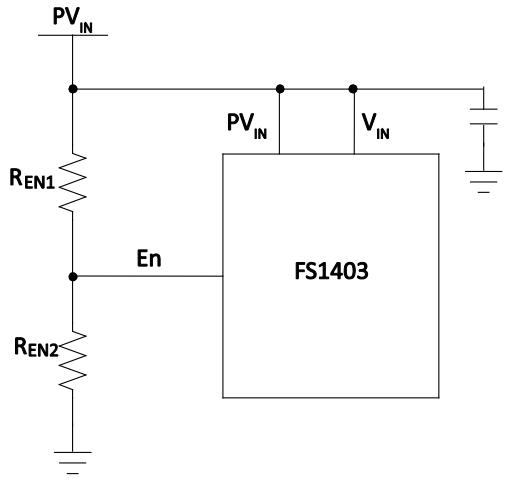



*Figure 5* ***Single supply configuration: internal LDO regulator, adjustable $PV_{IN}$_UVLO***

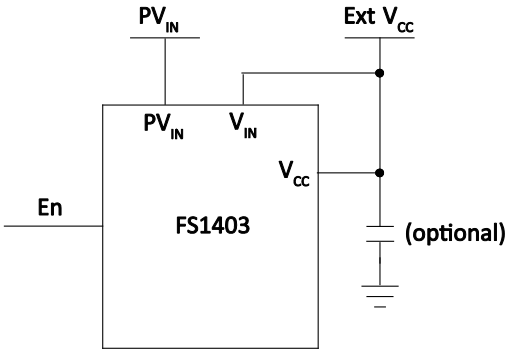



*Figure 6* ***Using an external bias voltage***

## I²C base address and offsets

The FS1403 has a user register called **Base_address**[7:0] stored in memory that sets its base I²C address. The default base address is 0x08. An offset of 0-3 is then defined by connecting the ADDR pin to the AGnd pin either directly or through a resistor. An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I²C address to set the address at which the I²C master device will communicate with the FS1403.

To select offsets of 0 to 3, connect the pins as follows:

- **0** – 0Ω (short ADDR to AGnd)
- **+1** – 10kΩ
- **+2** – 20kΩ
- **+3** – >30.1kΩ

## Soft-start and target output voltage

The FS1403 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When $V_{CC}$ exceeds its start threshold ($V_{CC}$_UVLO$_{(START)}$), the FS1403 exits reset mode; this initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset as described above.

Once initialization is complete and the Enable (En) pin has been asserted (Figure 7), the internal reference soft-starts to the target output voltage at the rate defined by the user register bit **SS_rate**.

| Register | Bits | Name/Description |
|---|---|---|
| 0x14 | [3] | **SS_rate**<br>0: 1mV/µs (default),<br>1: 2 mV/µs |

During initial start-up, the FS1403 operates with a minimum of high-drive (HDrv) pulses until the output voltage increases (see Switching frequency and minimum values for on-time, off-time on page 16). On-time is increased until $V_{OUT}$ reaches the target value defined by the user register bit **Vout_high_byte** and user register **Vout_low_byte**[7:0].

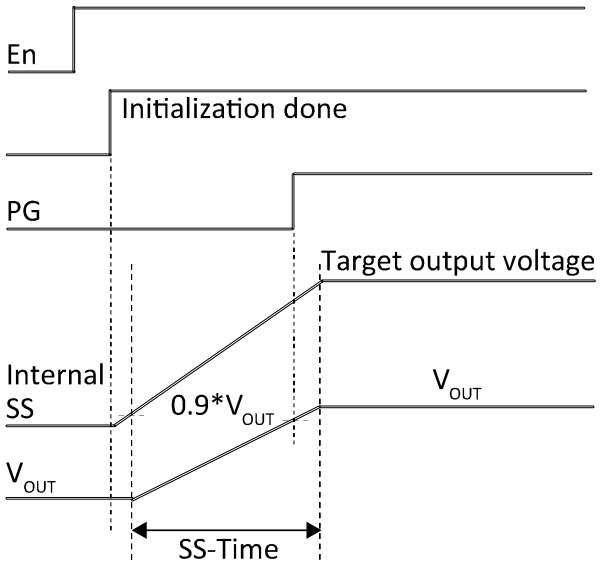



***Figure 7 Theoretical operational waveforms during soft-start***

| Register | Bits | Name/Description |
|---|---|---|
| 0x12 | [0] | **Vout_high_byte** |
| 0x13 | [7:0] | **Vout_low_byte** |

$V_{OUT}$ is set in 10mV increments. Use the following equation to calculate the $V_{OUT}$ code to enter into **Vout_high_byte** and **Vout_low_byte**[7:0]:

$$Vout_{code} = \frac{Vout_{target} - \frac{0.4 \times resolution}{0.005}}{resolution}$$

All voltages and resolutions are in Volts.

*For example:*

To set $V_{OUT}$ =5V (resolution of 10mV):

$$Vout_{code} = \frac{5 - \frac{0.4 \times 0.01}{0.005}}{0.01} = 420$$

420 is 1A4 in hexadecimal, therefore:

Set **Vout_high_byte** to 1

Set **Vout_low_byte** to A4 or $(10100100)_b$

Over-current protection (OCP) and over-voltage protection (OVP) is enabled during soft-start to

protect the FS1403 from short circuits and excess voltages respectively.

For maximum system accuracy, the recommended way to set the output voltage is by programming the user registers with the appropriate code. For optimum performance when using this approach, the change in output voltage should not exceed ±20% of the pre-set default output voltage.

## Pre-biased start-up

The FS1403 can start up into a pre-charged output smoothly, without causing oscillations and disturbances of the output voltage. When it starts up in this way, the Control and Synchronous MOSFETs are forced off until the internal Soft-Start (SS) signal exceeds the sensed output voltage at the $V_{OS}$ pin. Only then is the first gate signal of the Control MOSFET generated, followed by complementary turn on of the Synchronous MOSFET. The Power Good (PG) function is not active until this point.

## Shut-down mechanisms

The FS1403 has two shut-down mechanisms:

- *Hard shut-down or decay according to load*
  Initiated by de-asserting the En pin. Both drivers switch off and the digital-to-analog converter (DAC) and soft-start are pulled down instantaneously.
- *Soft-Stop or controlled ramp down*
  Initiated by setting user register bit **SoftStopEnable** to 1 ***and*** user register bit **SoftDisable** to 1. The SS signal falls to 0 at the same rate as it rises during start-up; the drivers are disabled only when it reaches 0. The output voltage then follows the SS signal down to 0.

  The **SoftDisable** bit must not be toggled while the part is enabled and switching. Instead, for applications requiring soft-stop, this bit must be set to 1 and, with the En pin asserted, the **SoftStopEnable** bit must be toggled to soft-start or soft-stop the device.

  By default, both the **SoftDisable** bit and the **SoftStopEnable** bit are 0, which means that soft-stop operation is disabled by default.

| Register | Bits | Name/Description |
|---|---|---|
| 0x14 | [2] | **SoftStopEnable** |
| 0x1C | [3] | **SoftDisable** |

## Switching frequency and minimum values for on-time, off-time and $PV_{IN}$

The switching frequency of the FS1403 depends on the output voltage. For an output voltage of 3.3V, the switching frequency is nominally 1.1MHz; for an output voltage of 5V, the switching frequency is nominally 1.4MHz. These are set at the factory.

As a result, system designers need not concern themselves with selecting the switching frequency and have one fewer design task to manage.

When input voltage is high relative to target output voltage, the Control MOSFET is switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very small, the FS1403 operates with minimum on-time.

When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ($T_{OFF(MIN)}$). The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. This dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

The minimum input voltage required to support an output voltage of 3.3V over the entire load range is 5V; for an output voltage of 5V, the minimum input voltage required is 8V. However, as these values are affected by both efficiency and dynamic load requirements, system designers should validate them in their own applications.

## Enable (En) pin

The Enable (En) pin has several functions:

- It is used to switch the FS1403 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1MΩ resistor pulls it down to prevent the FS1403 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the $PV_{IN}$ voltage by a set of resistive dividers, $R_{EN1}$ and $R_{EN2}$ (Figure 5). Users can program the UVLO threshold voltage by selecting different ratios. This is a useful feature that stops the FS1403 regulating when $PV_{IN}$ is lower than the desired voltage.
- It can be directly connected to $PV_{IN}$ without external resistive dividers for some space-constrained designs. This is a useful feature for standalone start-up, when no logic signal is available to enable the FS1403.
- It can be used to monitor other rails for a specific power sequencing scheme (Figure 8).

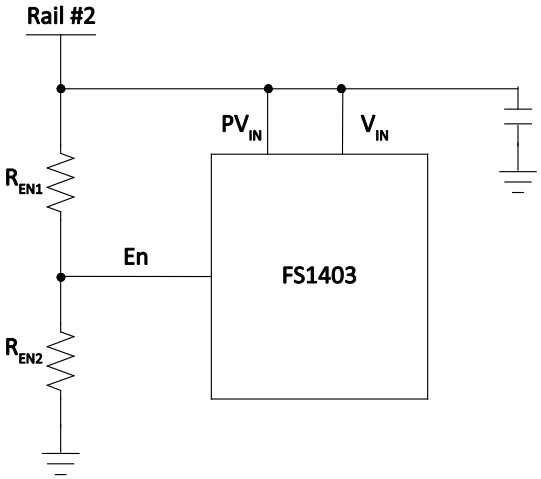



*Figure 8 En pin used to monitor other rails for sequencing purposes*

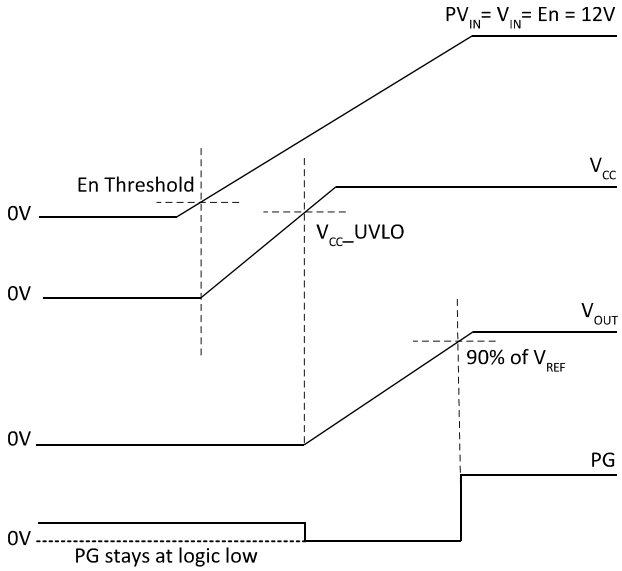



*Figure 9 Start-up: $PV_{IN}$, $V_{IN}$ and En pins tied together, PG pin pulled up to an external supply*

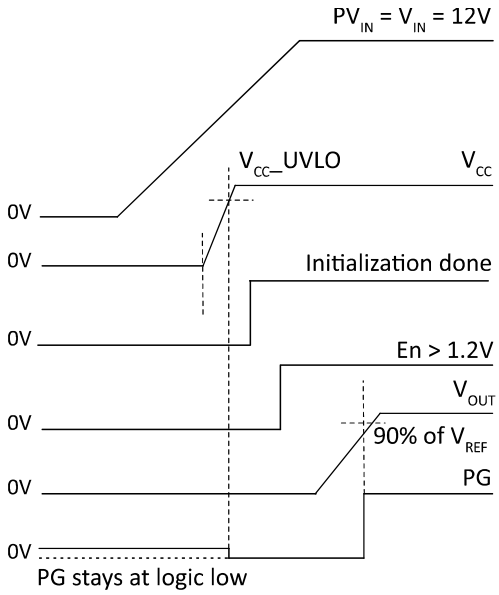



*Figure 10 Start-up: En pin asserted after $PV_{IN}$ and $V_{IN}$, PG pin pulled up to an external supply*

For $V_{OUT}$ to start up as defined by the soft-start rate requires correct sequencing:

- $PV_{IN}$ must start up before $V_{CC}$ and/or Enable.
- $PV_{IN}$ must ramp down only after $V_{CC}$ has ramped down below its UVLO threshold and/or Enable has been de-asserted.

## Over-current protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate overcurrent protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is set to 4A.

The threshold is internally compensated so that it remains almost constant at different ambient temperatures. However, as the inductor current ripple depends on $PV_{IN}$, the load current at which the overcurrent detection circuit trips varies with $PV_{IN}$; the table below shows the typical variation. Consequently, the maximum load applied to the FS1403 should be de-rated with the input voltage.

| $PV_{IN}$ (V) | OCP trigger at DC load (A) |
|---|---|
| 12 | 4.00 |
| 13 | 3.75 |
| 14 | 3.65 |
| 15 | 3.55 |
| 16 | 3.48 |

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1403 enters hiccup mode (Figure 11). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1403 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1403 remains in hiccup mode until the over-current fault is remedied.

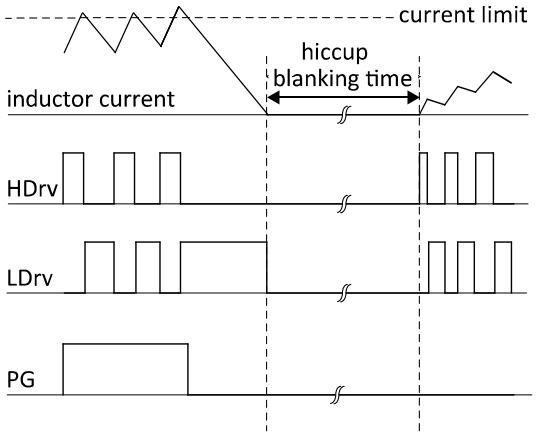



***Figure 11 Illustration of OCP in hiccup mode***

## Over-voltage protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the $V_{OS}$ pin. When $V_{OS}$ exceeds the output OVP threshold for longer than the output OVP delay (typically 5µs), a fault condition is generated.

The OVP threshold is defined by the user register bits **OV_Threshold**.

| Register | Bits | Name/Description |
|---|---|---|
| 0x17 | [1:0] | **OV_Threshold**<br>0:105% of $V_{OUT}$<br>1:110% of $V_{OUT}$<br>2:115% of $V_{OUT}$<br>3:120% of $V_{OUT}$ (default) |

The Control MOSFET is switched off immediately and the PG pin is pulled low. The Synchronous MOSFET is switched on to discharge the output capacitor.

The Control MOSFET remains latched off until reset by cycling either VCC or En. The voltage at the VOS pin falling below the output OVP threshold (with 5% hysteresis) does not switch on the Control MOSFET but it does switch off the Synchronous MOSFET to prevent build-up of negative current.

Figure 12 shows a timing diagram for over-voltage protection.

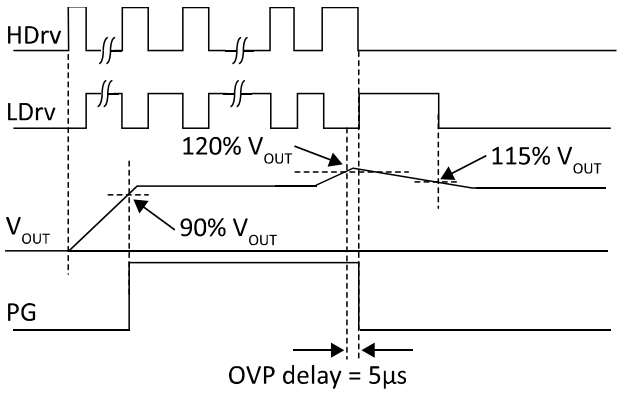



***Figure 12 Illustration of latched OVP***

## Over-temperature protection (OTP)

Temperature sensing is provided inside the FS1403. The OTP threshold is defined by the user register bits **OT_Threshold**.

| Register | Bits | Name/Description |
|---|---|---|
| 0x19 | [1:0] | **OT_Threshold**<br>0:75°C<br>1: 85°C<br>2: 125°C<br>3: 145°C (default) |

When the threshold is exceeded, thermal shut-down switches off both MOSFETs and resets the internal soft-start, but the internal LDO regulator is still in operation.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the OTP threshold.

## Power Good (PG)

Power Good (PG) behavior is defined by the user register bits **PGControl** and **PG_Threshold**.

| Register | Bits | Name/Description |
|---|---|---|
| 0x18 | [1:0] | **PG_Threshold**<br>0:80% of $V_{OUT}$<br>1: 85% of $V_{OUT}$<br>2: 90% of $V_{OUT}$ (default)<br>3: 95% of $V_{OUT}$ |
| 0x14 | [0] | **PG_Control**<br>1:Threshold based (default)<br>0: DAC based |

### PG_Threshold bit

The user register bit **PG_Threshold** defines the PG threshold as a percentage of $V_{OUT}$. Hysteresis of 5% is applied to this, giving a lower threshold.

When $V_{OS}$ rises above the upper threshold, the PG signal is pulled high. When $V_{OS}$ drops below the lower threshold, the PG signal is pulled low.

### PGControl bit set to 1 (default)

Figure 13 shows PG behavior in this situation.

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- En and $V_{CC}$ are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- $V_{OUT}$ is within the target range (determined by continuously monitoring whether $V_{OS}$ is above the PG threshold)

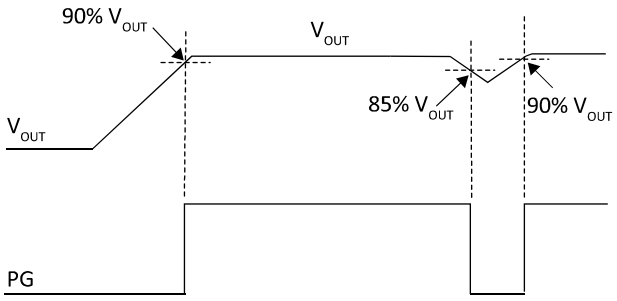



***Figure 13 PG signal when PGControl bit=1***

### PGControl bit set to 0

Figure 14 shows PG behavior in this situation.

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after soft-start is within 2% of target output voltage, not when $V_{OS}$ exceeds the upper PG threshold.

For pre-biased start-up, the PG signal is not active until the first gate signal of the Control MOSFET is generated.

FS1403 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if $V_{CC}$ is low and the PG pin is pulled up to an external voltage not $V_{CC}$ (Figure 9 and Figure 10).

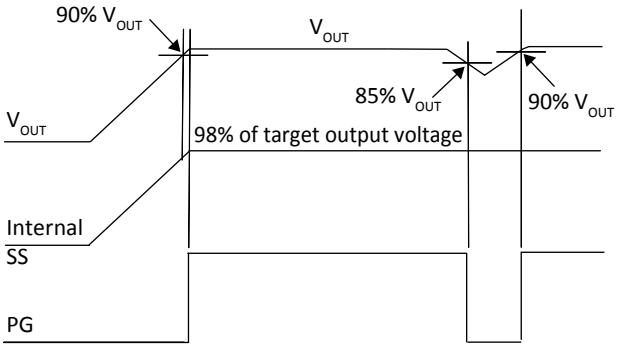



***Figure 14 PG signal when PGControl bit=0***

# Design example

Let us now consider a simple design example, using the FS1403 for the following design parameters:

- $PV_{IN} = V_{IN} = 12V$
- $V_{OUT} = 5V$
- $F_{SW} = 1.4MHz$
- $C_{OUT} = 2 \times 22\mu F$
- $C_{IN} = 2 \times 22\mu F$
- Ripple Voltage = ± 1% * $V_{OUT}$
- $\Delta V_{OUT(MAX)}$ = ±3% * $V_{OUT}$
  (for 100% load transient)

## Input capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1403
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For a buck converter operating at duty cycle D and output current $I_O$, the RMS value of the input current is:

$$I_{RMS} = Io\sqrt{D(1-D)}$$

In this application, $I_O$ = 3A and $D = \frac{V_{OUT}}{PV_{IN}} = 0.416$

Therefore, $I_{RMS}$ = 2.14A and we can select two 22µF 16V ceramic capacitors for the input capacitors (C3216X5R1C226M160AB from TDK).

If the FS1403 is not located close to the 12V power supply, a bulk capacitor (68–330µF) may be used in addition to the ceramic capacitors.

For $V_{IN}$, which is the input to the LDO, it is recommended to use a 1µF capacitor very close to the pin. The $V_{IN}$ pin should be connected to $PV_{IN}$ through a 2.7Ω resistor. Together, the 2.7Ω resistor and 1µF capacitor filter noise on $PV_{IN}$.

## Output voltage and output capacitor

The FS1403 is supplied pre-programmed and factory-trimmed in a closed loop to the target voltage specified for the part number. As a result, no external resistor divider is required and resistor tolerances are eliminated from the error budget.

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions.

For the FS1403, the minimum number of output capacitors required to achieve target peak-to-peak $V_{OUT}$ ripple is:

$$N_{MIN} = 4.54 \times \frac{\frac{(1-D)}{8CF_{SW}} + ESR(1-D) + \frac{ESL \times F_{SW} \times (1-D)^2}{D}}{\Delta V_{OUTripple(p-p)}}$$

where:

- $N_{MIN}$ = minimum number of output capacitors
- $D$ = duty cycle
- $C$ = equivalent capacitance of each output capacitor
- $F_{SW}$ = switching frequency
- $ESR$ = equivalent series resistance of each output capacitor
- $ESL$ = equivalent series inductance of each output capacitor
- $\Delta V_{OUTripple(p-p)}$
  = target peak-to-peak $V_{OUT}$ ripple

This design uses C2012X5R0J226K125AB from TDK; this is a 22µF MLCC, 0805 case size, rated at 6.3V. At 5V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 5µF ($C$). Equivalent series resistance is 3mΩ (ESR) and equivalent series inductance is 0.44nH (ESL).

Putting these parameters into the equation gives:

$N_{MIN}$ = 0.7

To meet the maximum voltage deviation $\Delta Vo_{max}$ under a $\Delta I_o$ load transient, the minimum required number of output capacitors is:

$$\frac{\mathbf{500 \times 10^{-9} \times \Delta I_o^2}}{\Delta V_{OUTmax} \times V_{OUT} \times C}$$

where:

- $\Delta I_o$ = load step
- $\Delta V_{OUTmax}$ = target maximum voltage deviation
- $V_{OUT}$ = output voltage
- $C$ = equivalent capacitance of each output capacitor

Again, using $C$ = 5µF, it can be seen that the minimum number of output capacitors required is 0.3.

In our design intended for space-constrained applications, therefore, we use two C2012X5R0J226K125AB capacitors.

It should be noted here that the calculation for the minimum number of output capacitors under a load transient makes some assumptions:

a) No ESR or ESL

b) Converter can saturate its duty cycle instantly

c) No latency

d) Step load (infinite slew rate)

Assumptions (a), (b) and (c) are liberal, whereas (d) is conservative. Therefore, in a real application, additional capacitance may be required to meet transient requirements and should be carefully considered by the system designer.

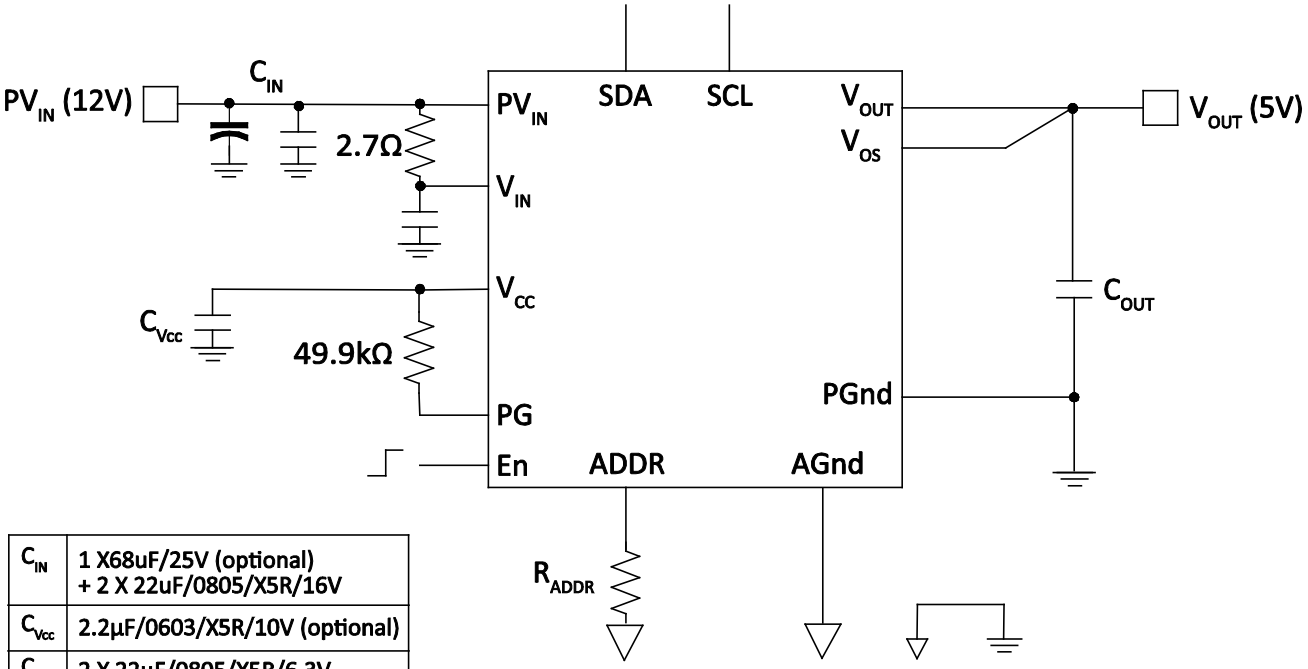
The typical application waveforms in Figure 22 and Figure 23 show the steady state $V_{OUT}$ ripple as well as the voltage deviation in response to a 100% load transient. These waveforms show that the selection of two 22µF capacitors meets the design criteria.

It should be noted that even in the absence of a target $V_{OUT}$ ripple or target maximum voltage deviation under load transient, at least one 22µF capacitor is still required in order to ensure stable operation without excessive jitter.

Up to six 22µF capacitors may be used in the design. If more capacitance is required, it is recommended to use a capacitor with relatively high ESR (>3mΩ) such as POSCAP or specialty polymer capacitors.

## $V_{CC}$ capacitor selection

FS1403 uses an on-package $V_{CC}$ capacitor to ensure effective high-frequency bypassing. However, especially for applications that use an external $V_{CC}$ supply, it is recommended that system designers place a 2.2µF/0603/X7R/10V capacitor on the application board as close as possible to the $V_{CC}$ pin.




| | |
|---|---|
| $C_{IN}$ | 1 X68uF/25V (optional)<br>+ 2 X 22uF/0805/X5R/16V |
| $C_{Vcc}$ | 2.2µF/0603/X5R/10V (optional) |
| $C_{OUT}$ | 2 X 22µF/0805/X5R/6.3V |

*Figure 15 Application circuit for a single supply, $PV_{IN}$=12V, $V_{OUT}$=5V, 3A*

# Typical operating waveforms

$PV_{IN}$=12V, $V_{OUT}$=5V, $I_O$=0-3A, room temperature, no airflow

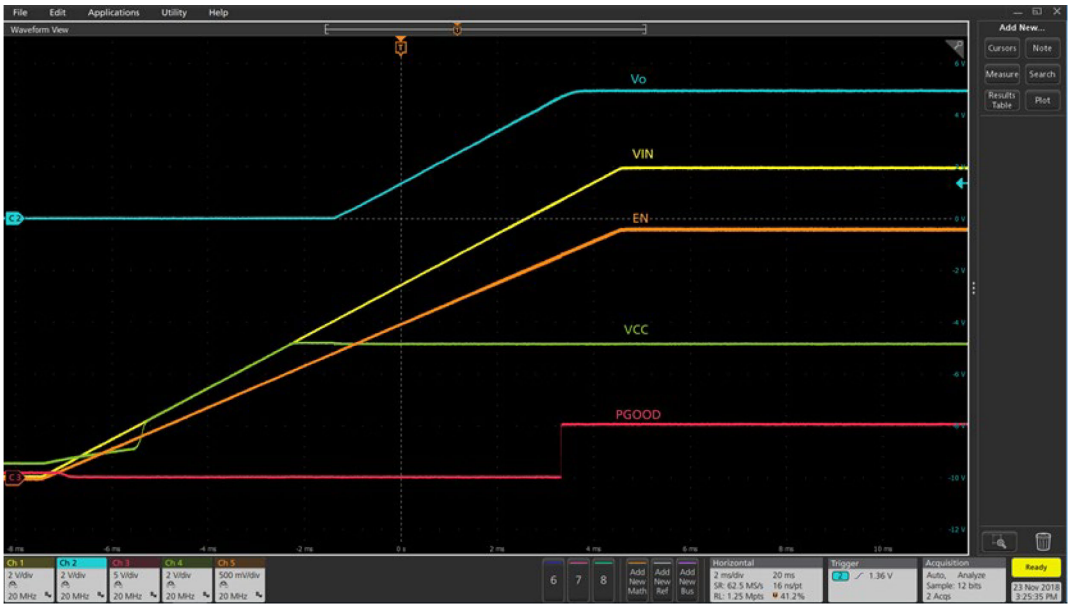



***Figure 16 Startup with no load (Ch1:$PV_{IN}$, Ch2: $V_{OUT}$, Ch3: PGood, Ch4:$V_{CC}$, Ch5: Enable)***

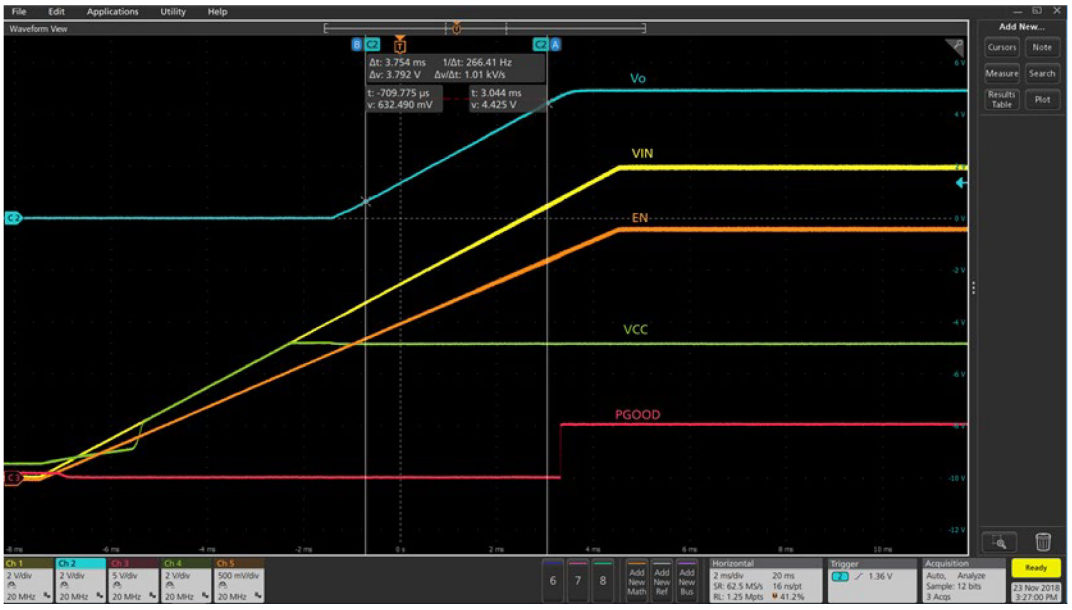



***Figure 17 Startup with 3A load (Ch1:$PV_{IN}$, Ch2: $V_{OUT}$, Ch3: PGood, Ch4:$V_{CC}$, Ch5: Enable)***


*Figure 18 Shutdown with Enable de-assertion at 3A load (Ch1:$PV_{IN}$, Ch2: $V_{OUT}$, Ch3: PGood, Ch4:$V_{CC}$, Ch5: Enable)*

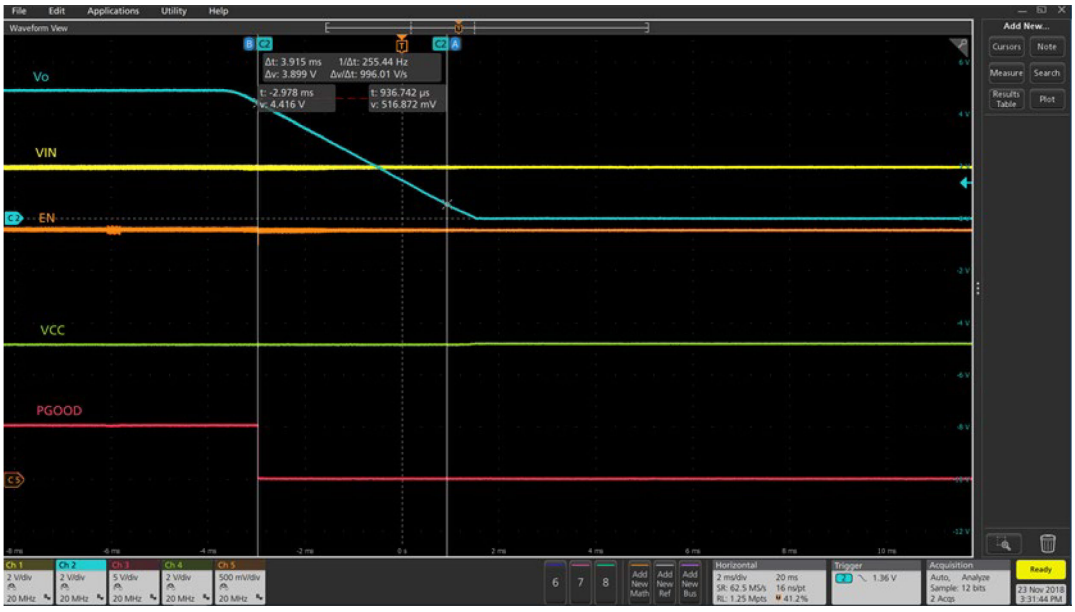



*Figure 19 Soft turn off at 3A load (Ch1:$PV_{IN}$, Ch2: $V_{OUT}$, Ch3: PGood, Ch4:$V_{CC}$, Ch5: Enable)*

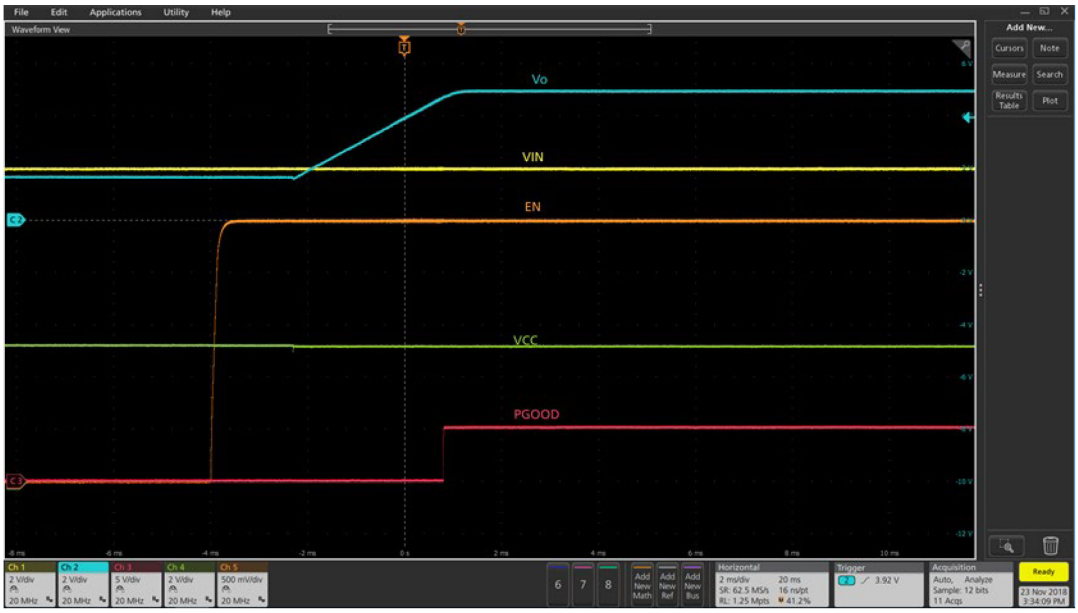



*Figure 20 Startup into pre-bias (Ch1:$PV_{IN}$, Ch2: $V_{OUT}$, Ch3: PGood, Ch4:$V_{CC}$, Ch5: Enable)*

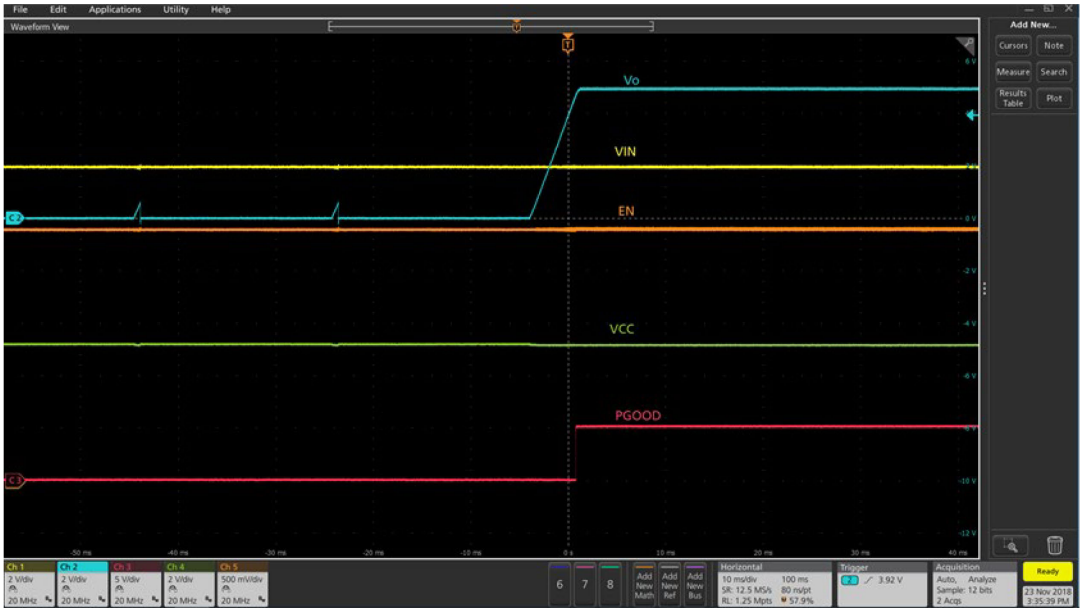



*Figure 21 Over-current protection and auto-recover to 3A (Ch1:$PV_{IN}$, Ch2: $V_{OUT}$, Ch3: PGood, Ch4:$V_{CC}$, Ch5: Enable)*

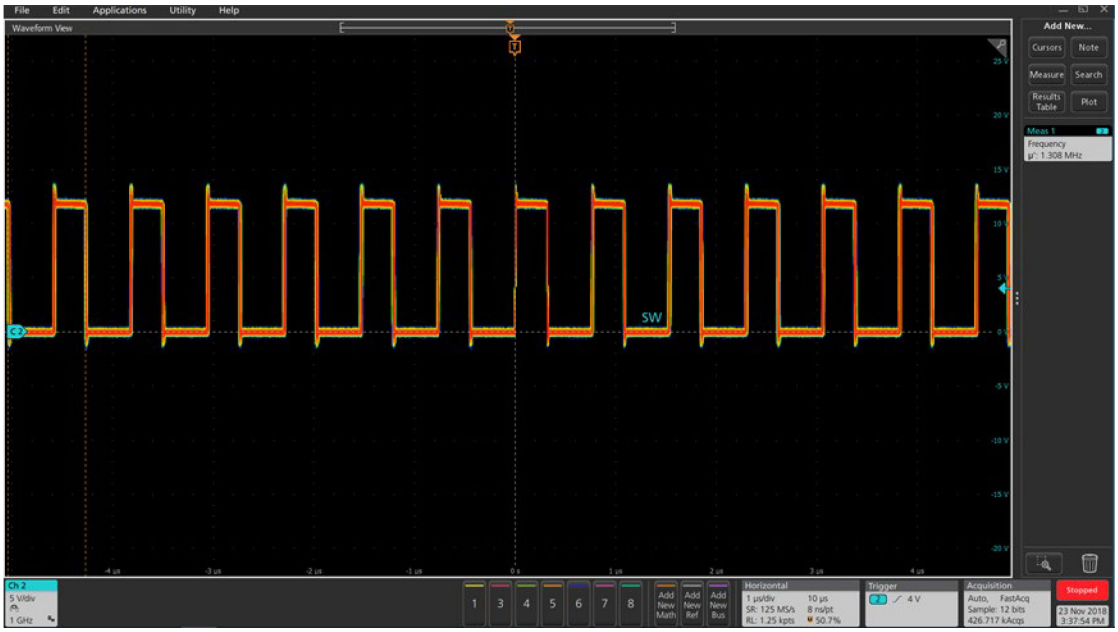



*Figure 22 Sw at 0A (Ch2: Sw)*

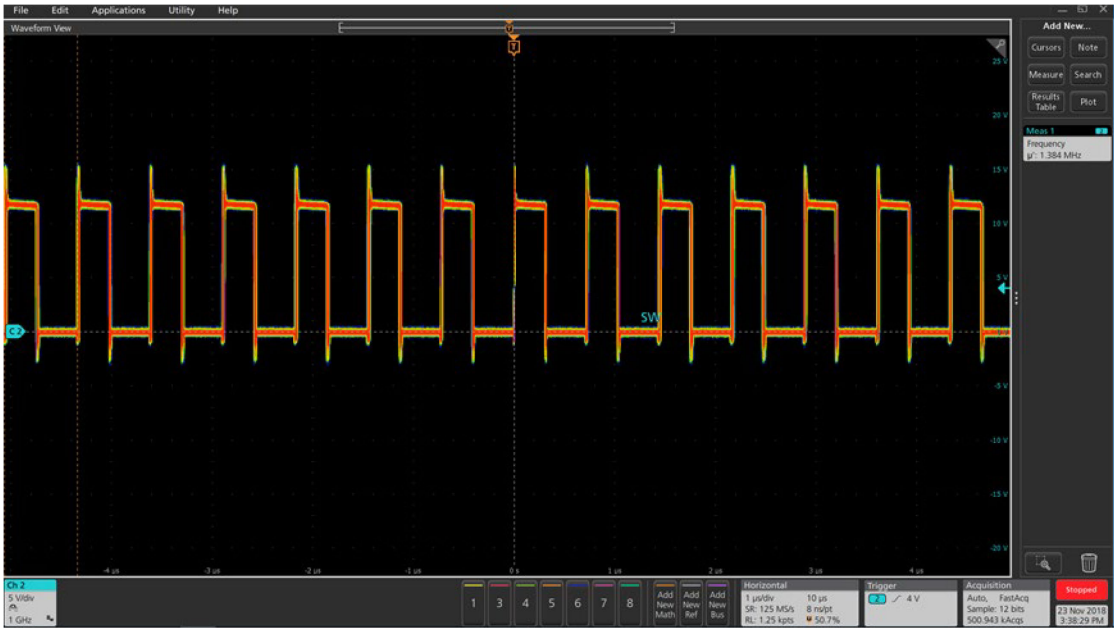



*Figure 23 Sw at 3A (Ch2: Sw)*

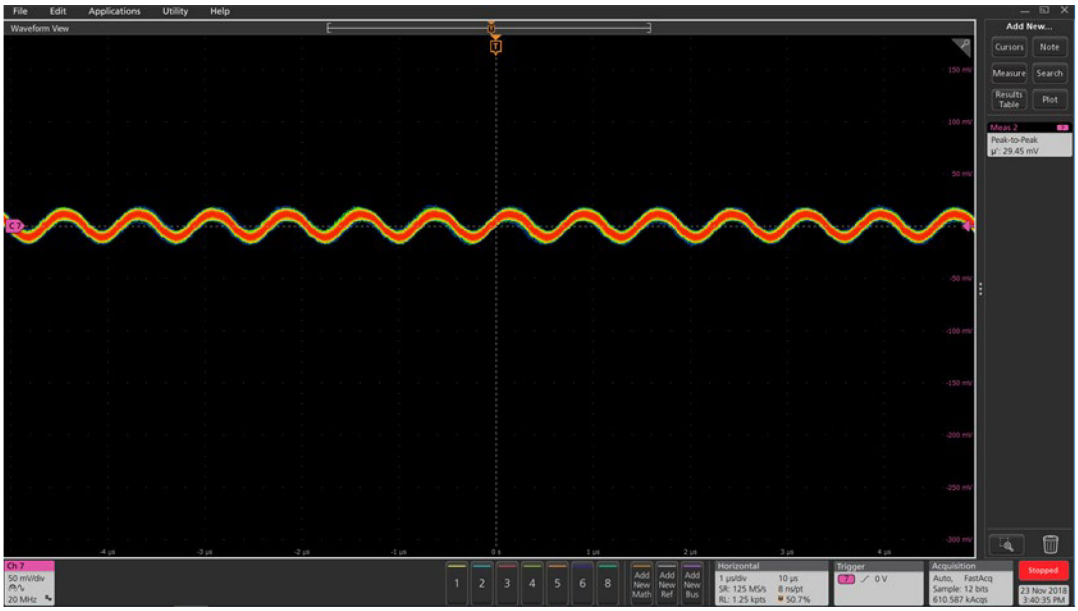



*Figure 24 $V_{OUT}$ ripple at 0A (Ch7: $V_{out}$), Peak-Peak $V_{OUT}$ ripple=30mV*

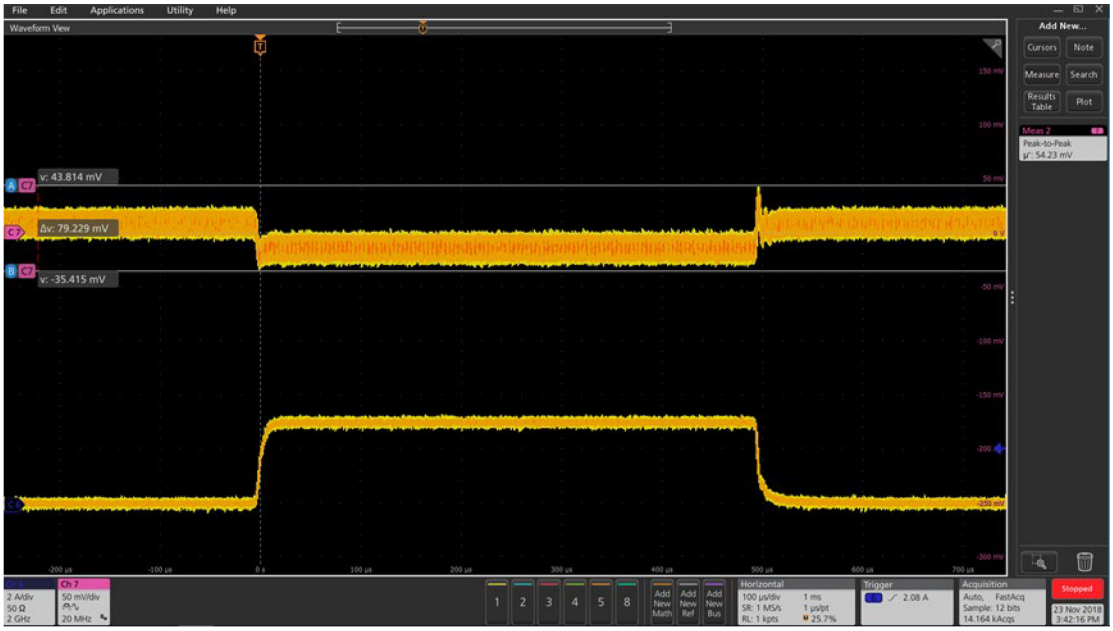



*Figure 25 Transient response 0A to 3A (Ch6:$I_O$, Ch2: $V_{OUT}$), peak-peak deviation=79mV*

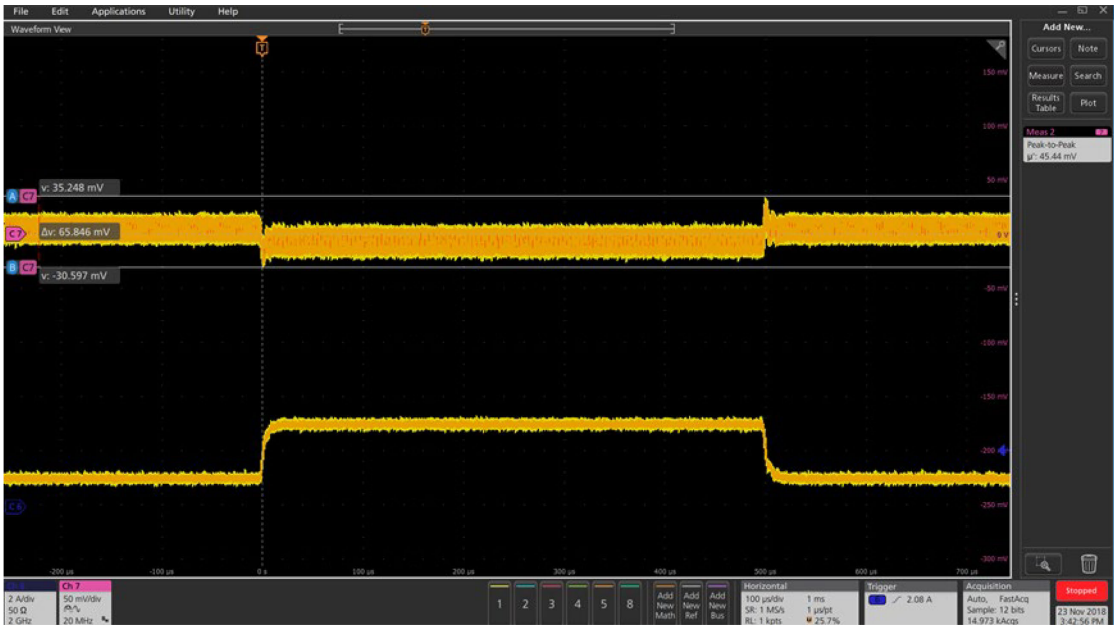



*Figure 26 Transient response 1A to 3A (Ch6:$I_O$, Ch2: $V_{OUT}$), peak-peak deviation=66mV*

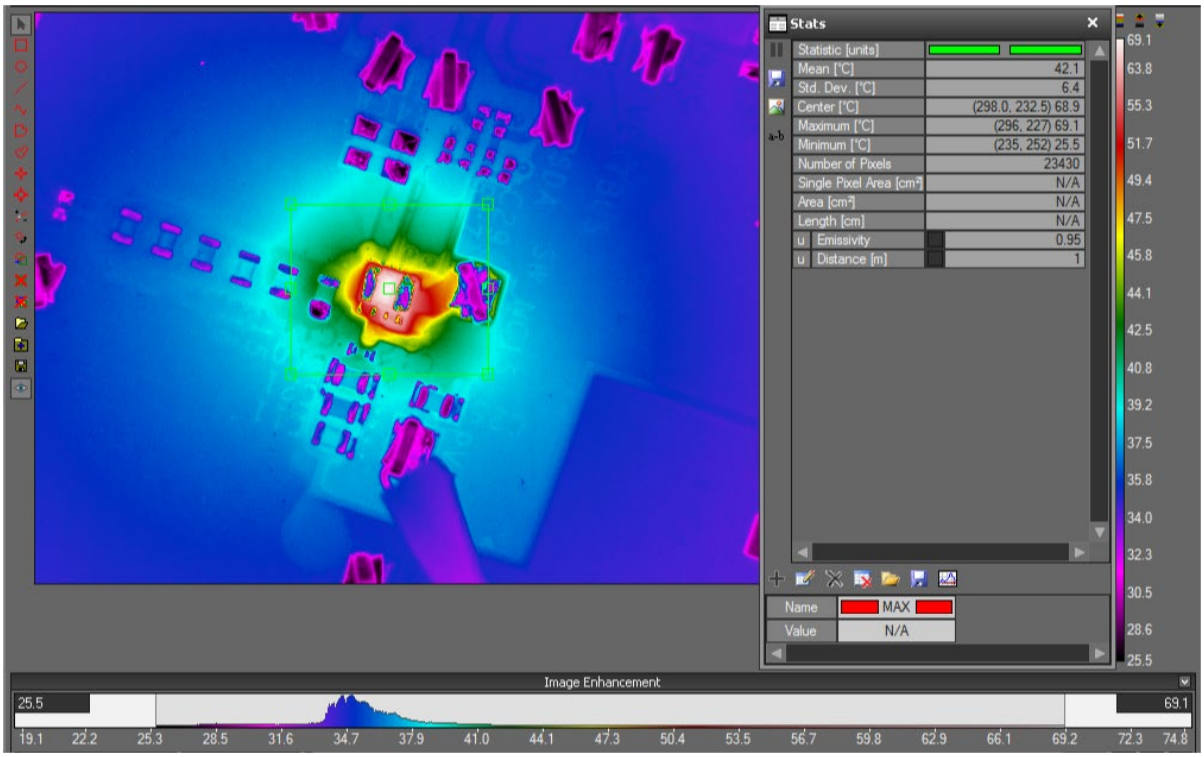



*Figure 27 Thermal image at PVIN = 12V, VOUT = 1.8V, IO = 3A, room temperature, no airflow, FS1403 maximum temperature = 69°C*

## Layout recommendations

FS1403 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Bypass capacitors, including input/output capacitors and the $V_{CC}$ bypass capacitor (if used), should be placed as close as possible to the FS1403 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- Analog ground and power ground are connected through a single-point connection.
- To aid thermal dissipation, the PGnd pad should be connected to the power ground plane using vias. Copper-filled vias are preferred but plated-through-hole vias are acceptable, provided that they are not filled with resin or covered with solder mask.
- Adequate numbers of vias should be used to make connections between layers, especially for the power traces.
- To minimize power losses and thermal dissipation, wide copper polygons should be used for input and output power connections.
- SCL and SDA traces must be at least 10mil wide, with 20–30mil spacing between them.

## Thermal considerations

The FS1403 has been thermally tested and modelled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1403 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.

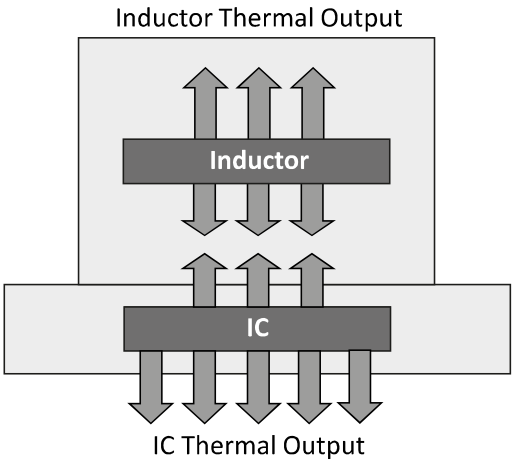



***Figure 28 Heat sources in the FS1403***

Figure 29 shows the thermal resistances in the FS1403, where:

- $\Theta_{JA}$ is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{JCbottom}$ is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- $\Theta_{JCtop}$ is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1403 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.

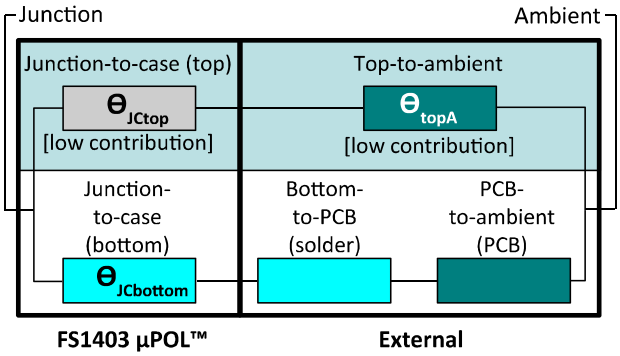



***Figure 29 Thermal resistances of the FS1403***

The values of the thermal resistances are:

- $\Theta_{JA}$ = 22.6°C/W
- $\Theta_{JCbottom}$ = 2.36°C/W

Although these values indicate how the FS1403 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the µPOL™'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

Note: In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

# I²C protocol

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S | = | Start bit | W | = | Write bit (‘1’) | White bits | = | Issued by master |
| P | = | Stop bit | R | = | Read (‘0’) | Grey bits | = | Sent by slave (FS140x) |
| A | = | Ack | Sr | = | Repeated start | | | |
| N | = | Nack | | | | | | |

**Write transaction**

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address | W | A | Register Address | A | Data Byte | A | P |

**Read transaction**

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | W | A | Register Address | A | Sr | Slave Address | R | A | Data Byte | N | P |

## Reflow profiles

TDK does not recommend specific reflow profiles for use with its µPoL products. Many factors influence the selection of an ideal reflow profile. Each PCB should be profiled in accordance with the solder paste manufacturer's recommendations.

Figure 30 shows reflow profiles similar to the one that has been used successfully in mounting µPoL products to PCBs. The linear profile is recommended as a starting point. The soak profile can be useful in two situations:

- For PCBs with uneven loads (areas of high and low component density) – the soak profile allows more time for the PCB to reach an even temperature over its entire area.
- For PCBs with surfaces that are more difficult to solder – the soak profile allows the flux more time to act on the surfaces to be soldered.

To ensure that TDK's µPoL products can be soldered using standard lead-free reflowing parameters, they have been tested using reflow profiles with peak temperatures up to 260°C. Most solder paste manufacturers do not recommend using profiles with peak temperatures over 250°C.

To ensure that TDK's µPoL products solder well within lead-free environments, they are finished with ENiG (Electroless-Nickel-Gold). The nickel can be considered as a barrier layer: it forms a thin but reliable intermetallic with tin. This is in contrast to copper, which dissolves quickly in tin-rich lead-free solders: one reflow operation may dissolve 4µm of copper, potentially causing problems.

When profiling the PCB, remember that many components (not only TDK's µPoL products) may use surface finishes that contain nickel. Profiles that use temperatures above 220°C for very short times, which may have been derived to reduce copper consumption, may not give sufficient time for nickel to form a good intermetallic layer.

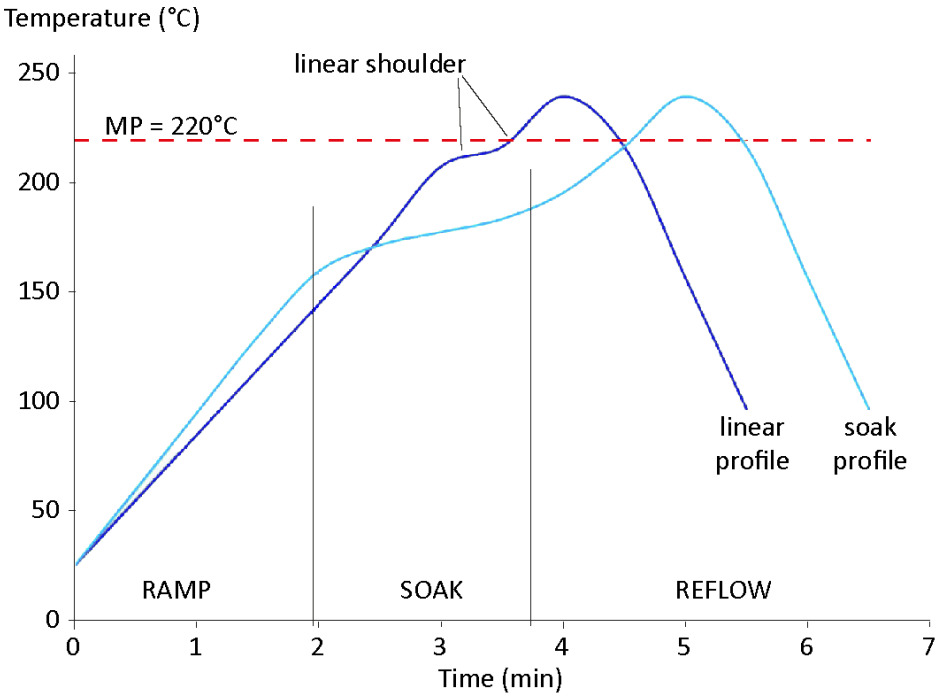



***Figure 30 Reflow profile***

## Package description

The FS1403 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate. The finish on the pads is ENiG.

As a result of these properties, the FS1403 works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Note: Refer to the Design Guidelines for more information about TDK's µPOL™ package series.

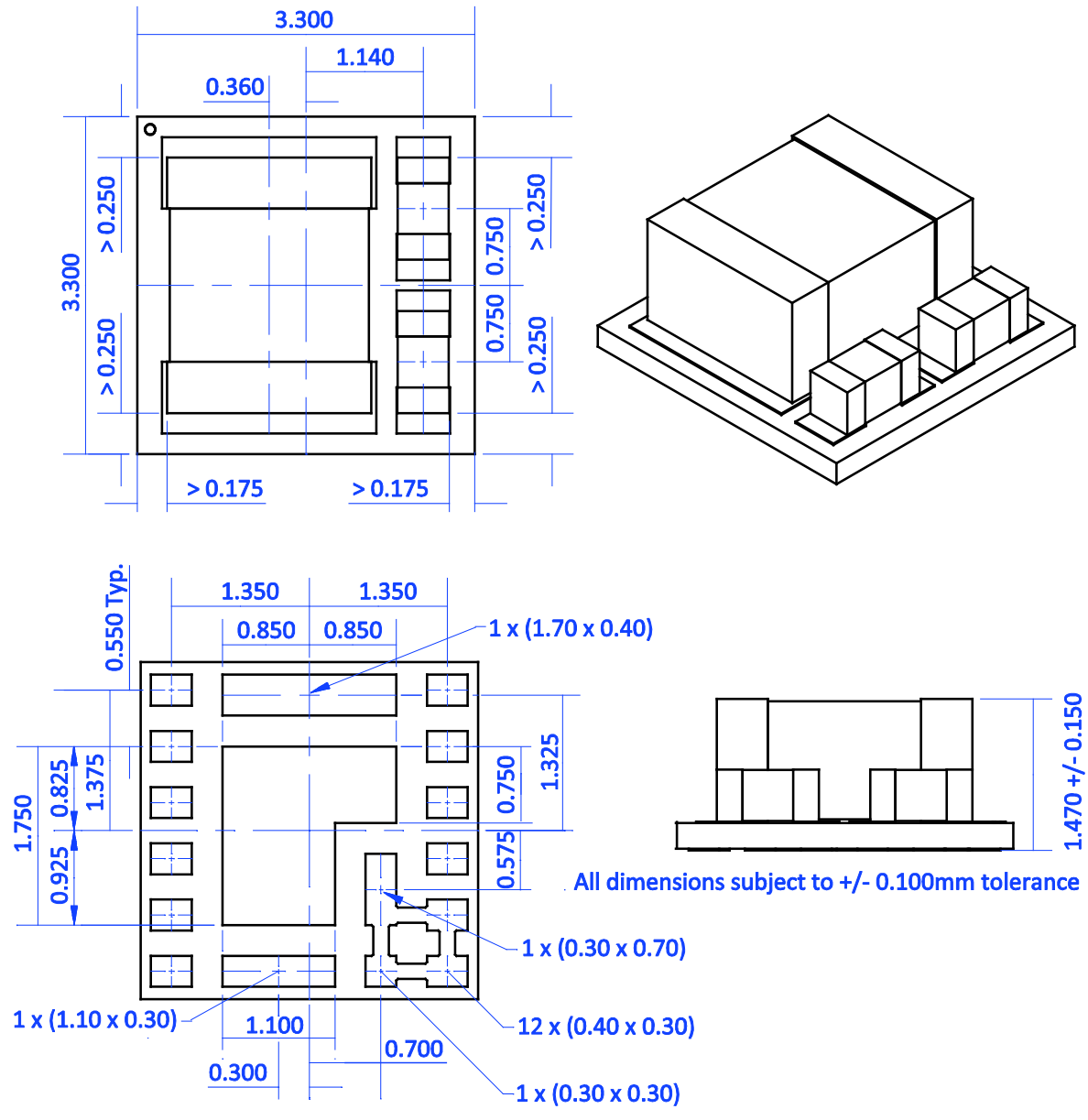
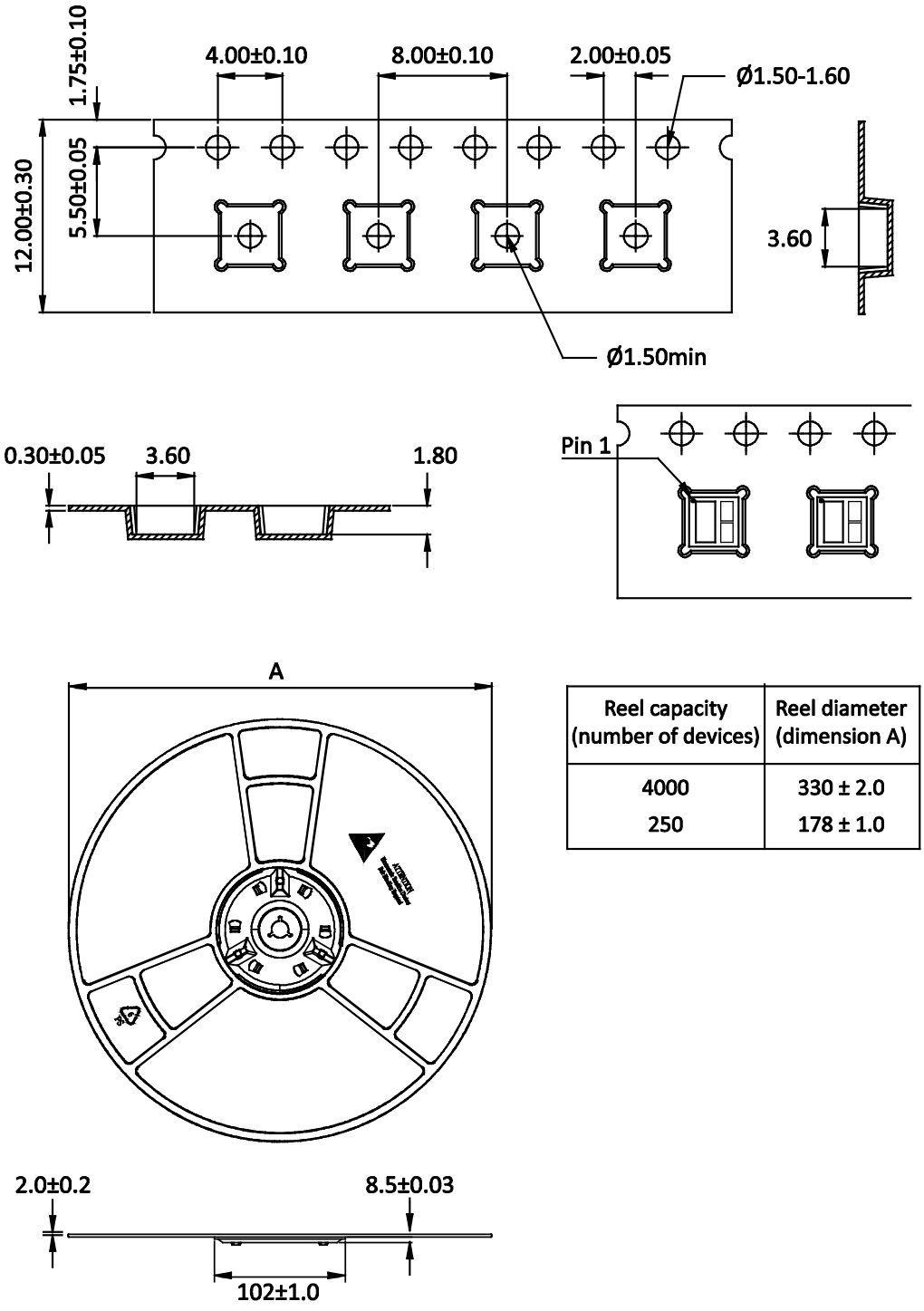



*Figure 31 Dimensioned drawings*




| Reel capacity (number of devices) | Reel diameter (dimension A) |
|---|---|
| 4000 | 330 ± 2.0 |
| 250 | 178 ± 1.0 |

*Figure 32 Tape and reel pack*

## REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

### SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

**REMINDER**

The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety.

**This product is subject to a license from Power One, Inc. related to digital power technology patents owned by Power One, Inc. Power One, Inc. technology is protected by patents including:**

**AU 3287379M 3287437AA 3290643AA 3291357AA**

**CN 10371856C 10452610C 10458656C 10459360C 10465848C 1069332A 11124619A 11346682A 1685299A 1685459A 1685582A 1685583A 1698023A 1802619A**

**EP 1561156A1 1561268A2 1576710A1 1576711A1 1604254A4 1604264A4 1714369A2 1745536A4 1769382A4 1899789A2 1984801A2**

**US 20040246754 2004090219A1 2004093533A1 2004123164A1 2004123167A1 2004178780A1 2004179382A1 20050200344 20050223252 2005209373A1 20060061214 2006015619A1 20060174145 20070226526 20070234095 20070240000 20080052551 20080072080 20080186006 6741099 6788036 6936999 6949916 7000125 7049798 7069021 7080265 7249267 7266709 7315156 7372682 7373527 7394445 7456617 7459892 7493504 7526660**

**WO 04044718A1 04045042A3 04045042C1 04062061A1 04062062A1 04070780A3 04084390A3 04084391A3 05079227A3 05081771A3 06019569A3 2007001584A3 2007094935A3**

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>>TDK Corporation(东电化)