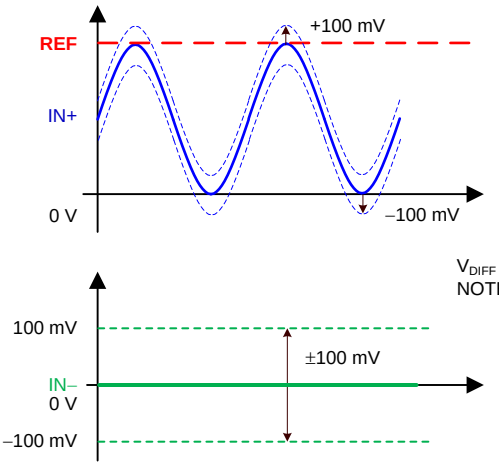
ADS8339 16 位、250kSPS 串行接口微功耗微型 SAR 模数转换器

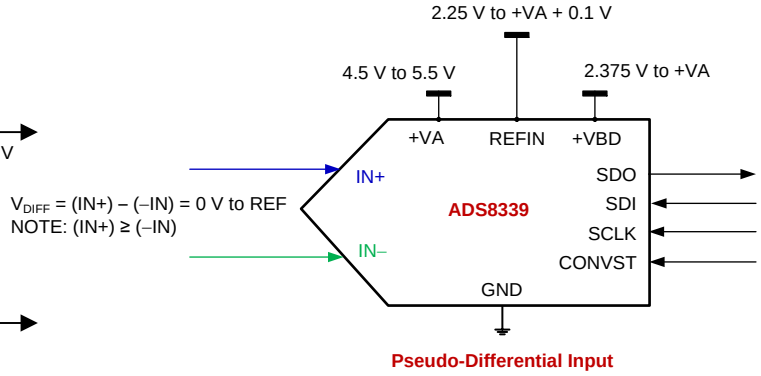
1 特性

- 采样率：250kHz
- 16 位分辨率
- 全速状态下零延迟
- 单极单端输入范围：
  - 0V 至 V_{ref}
- SPI™ 兼容串口，具有菊花链选项
- 使用内部时钟进行转换
- 出色的性能：
  - 输入为 10kHz 时，信噪比 (SNR) 典型值为 93.6dB
  - 输入为 10kHz 时，总谐波失真 (THD) 典型值为 –106dB
  - ±2.0 最低有效位 (LSB) 最大积分非线性 (INL)
  - ±1.0 LSB 最大微分非线性 (DNL)
- 低功耗：
  - 250kSPS 时为 17.5mW（典型值）
- 功率可根据速度进行线性缩放：
  - 25kSPS 时为 1.75mW
- 断电状态下的功耗：
  - 0.25μW（典型值）
- 封装：超薄小外形尺寸封装 (VSSOP)-10

2 应用

- 电池供电类设备
- 数据采集系统
- 仪表和过程控制
- 医用电子产品
- 光纤网络





3 说明

ADS8339 是一款 16 位、250kSPS 模数转换器 (ADC)。 该器件的外部工作基准电压为 2.25V 至 5.5V。 此器件包括一个基于电容器且具有内置采样保持电路的逐次逼近寄存器 (SAR) ADC。

此器件还包括一个 25MHz 串行外设接口 (SPI) 兼容串口。 该接口设计用于支持菊花链或级联多个器件。 此外，忙闲指示器可轻松实现与数字主机的同步。 该器件的单极单端输入范围支持的输入电压摆幅为 0V 至 V_{ref}。

该器件已经过优化，可实现低功耗运行以及根据速度直接调节功耗。 这一特性使得该器件对低速应用尤为实用。 ADS8339 采用 VSSOP-10 封装。

器件信息(1)

部件号	封装	封装尺寸（标称值）
ADS8339	VSSOP (10)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

目录

4 修订历史记录

Changes from Original (June 2014) to Revision A **Page**

- 已更改产品预览数据表 1

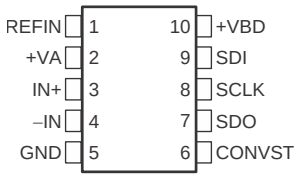
5 Device Family(1)

SAMPLING RATE	16-BIT, SINGLE-ENDED	16-BIT, DIFFERENTIAL	18-BIT, DIFFERENTIAL
100 kSPS	ADS8866	ADS8867	ADS8887
250 kSPS	ADS8339	—	—
400 kSPS	ADS8864	ADS8865	ADS8885
500 kSPS	ADS8319	ADS8318	—
680 kSPS	ADS8862	ADS8863	ADS8883
1 MSPS	ADS8860	ADS8861	ADS8881

(1) All devices are pin-to-pin compatible. The ADS8339, ADS8319, and ADS8318 require a 4.5-V to 5.5-V analog supply. The remaining devices use a 2.7-V to 3.6-V analog supply.

6 Pin Configuration and Functions

DGS Package
VSSOP-10
(Top View)



Pin Functions

PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	REFIN	Input	Reference (positive) input. Decouple to GND with a 0.1-µF bypass capacitor and a 10-µF storage capacitor.
2	+VA	Supply	Analog power supply. Decouple with the GND pin.
3	+IN	Input	Noninverting analog signal input
4	–IN	Input	Inverting analog signal input. Note that this input has a limited range of ±0.1 V and is typically grounded at the input decoupling capacitor.
5	GND	Supply	Device ground. Note that this pin is a common ground pin for both the analog power supply (+VA) and digital I/O supply (+VBD).
6	CONVST	Input	Convert input. CONVST also functions as the $\overline{CS}$ input in 3-wire interface mode. Refer to the *Description* and *Timing Diagrams* sections for more details.
7	SDO	Output	Serial data output
8	SCLK	Input	Serial I/O clock input. Data (on the SDO output) are synchronized with this clock.
9	SDI	Input	Serial data input. The SDI level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). SDI also serves as the $\overline{CS}$ input in 4-wire interface mode. Refer to the *Description* and *Timing Diagrams* sections for more details.
10	+VBD	Supply	Digital I/O power supply. Decouple with the GND pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
+IN, –IN input	Voltage	–0.3	+VA + 0.3	V
	Momentary current(2)		130	mA
	Continuous current		±10	mA
+VA to GND		–0.3	7	V
+VBD to GND		–0.3	7	V
Digital input voltage to GND		–0.3	+VBD + 0.3	V
Digital output voltage to GND		–0.3	+VBD + 0.3	V
Temperature	Operating free-air range, T_A	–40	85	°C
	Junction, T_J max		150	°C
VSSOP package	Power dissipation		$(T_J max – T_A) / \theta_{JA}$	°C
	θ_{JA} thermal impedance		121.1	°C/W
Maximum VSSOP reflow temperature(3)			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Limit the duration for this current to less than 10 ms.
(3) The device is rated at MSL2, 260°C, as per the JSTD-020 specification.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1000	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–250	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{+VA}	Analog power-supply voltage	4.5	5.0	5.5	V
V_{+VBD}	Digital I/O-supply voltage	2.375	3.3	5.5	V
V_{ref}	Reference voltage	2.25	4.096	V_{+VA} + 0.1	V
$f_{(SCLK)}$	SCLK frequency			25	MHz
T_A	Operating temperature range	–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		ADS8339 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	32.0	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	31.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

All minimum and maximum specifications are at T_A = –40°C to 85°C, +VA = 5 V, +VBD = 5 V to 2.375 V, V_{ref} = 4 V, and f_{sample} = 250 kHz, unless otherwise noted. Typical specifications are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)	+IN – (–IN)	0		V_{ref}	V
	Operating input range	+IN	–0.1		V_{ref} + 0.1	V
		–IN	–0.1		0.1	V
C_i	Input capacitance			59		pF
	Input leakage current	During acquisition		1000		pA
SYSTEM PERFORMANCE						
	Resolution			16		Bits
NMC	No missing codes		16			Bits
INL	Integral linearity(2)		–2.0	±1.2	2.0	LSB(3)
DNL	Differential linearity	At 16-bit level	–0.99	±0.65	1.0	LSB
E_O	Offset error(4)		–1.5	±0.3	1.5	mV
E_G	Gain error		–0.03	±0.0045	0.03	%FSR
CMRR	Common-mode rejection ratio	With common-mode input signal = 200 mV_{PP} at 250 kHz		78		dB
PSRR	Power-supply rejection ratio	At FFF0h output code		80		dB
	Transition noise			0.5		LSB
SAMPLING DYNAMICS						
t_{cnv}	Conversion time		500(5)		3300	ns
t_{acq}	Acquisition time		700			ns
	Maximum throughput rate with or without latency				0.25	MHz
	Aperture delay			2.5		ns
	Aperture jitter, RMS			6		ps
	Step response	Settling to 16-bit accuracy		600		ns
	Overvoltage recovery	Settling to 16-bit accuracy		600		ns

(1) Ideal input span, does not include gain or offset error.
(2) This parameter is the endpoint INL, not best-fit INL.
(3) LSB = least significant bit.
(4) Measured relative to actual measured reference.
(5) Refer to the *$\overline{CS}$ Mode for a 3-Wire Interface* section in the *Device Functional Modes*.

Electrical Characteristics (continued)

All minimum and maximum specifications are at T_A = –40°C to 85°C, +VA = 5 V, +VBD = 5 V to 2.375 V, V_{ref} = 4 V, and f_{sample} = 250 kHz, unless otherwise noted. Typical specifications are at T_A = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion(6)		V_{IN} = 0.4 dB below f_S at 1 kHz, V_{ref} = 5 V		–111		dB
			V_{IN} = 0.4 dB below f_S at 10 kHz, V_{ref} = 5 V		–106		dB
SNR	Signal-to-noise ratio		V_{IN} = 0.4 dB below f_S at 1 kHz, V_{ref} = 5 V		93.9		dB
			V_{IN} = 0.4 dB below f_S at 10 kHz, V_{ref} = 5 V		93.6		dB
SINAD	Signal-to-noise + distortion		V_{IN} = 0.4 dB below f_S at 1 kHz, V_{ref} = 5 V		93.8		dB
			V_{IN} = 0.4 dB below f_S at 10 kHz, V_{ref} = 5 V		93.4		dB
SFDR	Spurious-free dynamic range		V_{IN} = 0.4 dB below f_S at 1 kHz, V_{ref} = 5 V		113		dB
			V_{IN} = 0.4 dB below f_S at 10 kHz, V_{ref} = 5 V		107		dB
	–3-dB small-signal bandwidth				15		MHz
EXTERNAL REFERENCE INPUT							
V_{ref}	Input range			2.25	4.096	VA + 0.1	V
	Reference input current(7)		During conversion		75		µA
POWER-SUPPLY REQUIREMENTS							
	Power-supply voltage	+VBD		2.375	3.3	5.5	V
		+VA		4.5	5	5.5	V
I_{CC}	Supply current	+VA	250-kHz sample rate		3.5	4.0	mA
P_{VA}	Power dissipation		+VA = 5 V, 250-kHz sample rate		17.5	20.0	mW
IVA_{pd}	Device power-down current(8)		+VA = 5 V		50	300	nA
LOGIC FAMILY CMOS							
V_{IH}	High-level input voltage		I_{IH} = 5 µA	0.7 × VBD		VBD + 0.3	V
V_{IL}	Low-level input voltage		I_{IL} = 5 µA	–0.3		0.3 × VBD	V
V_{OH}	High-level output voltage		I_{OH} = 2 TTL loads	VBD – 0.3		V_{BD}	V
V_{OL}	Low-level output voltage		I_{OL} = 2 TTL loads	0		0.4	V
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		85	°C

(6) Calculated on the first nine harmonics of the input frequency.
(7) Can vary by ±20%.
(8) The device automatically enters a power-down state at the end of every conversion and remains in a power-down state as long as the device is in an acquisition phase.

7.6 Timing Requirements

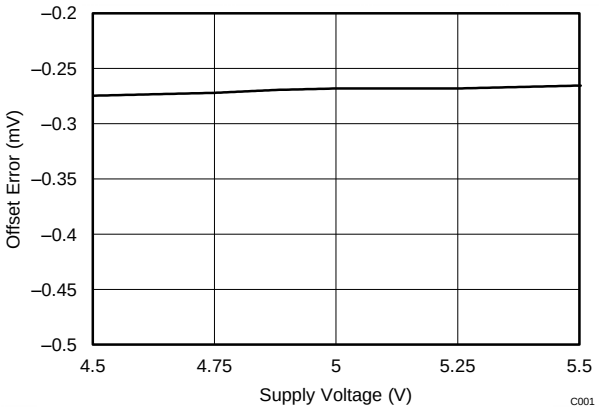
All specifications are at T_A = –40°C to 85°C, +VA = 5 V, and 5.5 V > +VBD ≥ 2.375 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING AND CONVERSION						
t_{acq}	Acquisition time (see Figure 47, Figure 49, Figure 50, Figure 53)		700			ns
t_{cnv}	Conversion time (see Figure 47, Figure 49, Figure 50, Figure 53)		500(1)		3300	ns
t_{cyc}	Time between conversions (see Figure 47, Figure 49, Figure 50, Figure 53)		4000			ns
t_1	Pulse duration, CONVST high (see Figure 47, Figure 49)		10			ns
t_6	Pulse duration, CONVST low (see Figure 50, Figure 53, Figure 55)		20			ns
INPUTS AND OUTPUTS (I/O)						
t_{clk}	SCLK period (see Figure 47, Figure 49, Figure 50, Figure 53, Figure 55, Figure 57)		40.0			ns
t_{clkl}	SCLK low time (see Figure 47, Figure 49, Figure 50, Figure 53, Figure 55, Figure 57)		0.45		0.55	t_{clk}
t_{clkh}	SCLK high time (see Figure 47, Figure 49, Figure 50, Figure 53, Figure 55, Figure 57)		0.45		0.55	t_{clk}
t_2	SCLK falling edge to data remains valid (see Figure 47, Figure 49, Figure 50, Figure 53, Figure 55, Figure 57)		5			ns
t_3	SCLK falling edge to next data valid delay (see Figure 47, Figure 49, Figure 50, Figure 53, Figure 55, Figure 57)	5.5 V ≥ +VBD ≥ 4.5 V			16	ns
		4.5 V > +VBD ≥ 2.375 V			24	ns
t_{en}	CONVST or SDI low to MSB valid (see Figure 47, Figure 50)	5.5 V ≥ +VBD ≥ 4.5 V			15	ns
		4.5 V > +VBD ≥ 2.375 V			22	ns
t_{dis}	CONVST or SDI high or last SCLK falling edge to SDO 3-state ($\overline{CS}$ mode) (see Figure 47, Figure 49, Figure 50, Figure 53)	5.5 V ≥ +VBD ≥ 4.5 V			12	ns
		4.5 V > +VBD ≥ 2.375 V			15	ns
t_4	SDI valid setup time to CONVST rising edge (see Figure 50, Figure 53)		5			ns
t_5	SDI valid hold time from CONVST rising edge (see Figure 50, Figure 53)		5			ns
t_7	SCLK valid setup time to CONVST rising edge (see Figure 55)		5			ns
t_8	SCLK valid hold time from CONVST rising edge (see Figure 55)		5			ns

(1) Refer to the *$\overline{CS}$ Mode for a 3-Wire Interface* subsection in the *Device Functional Modes* section.

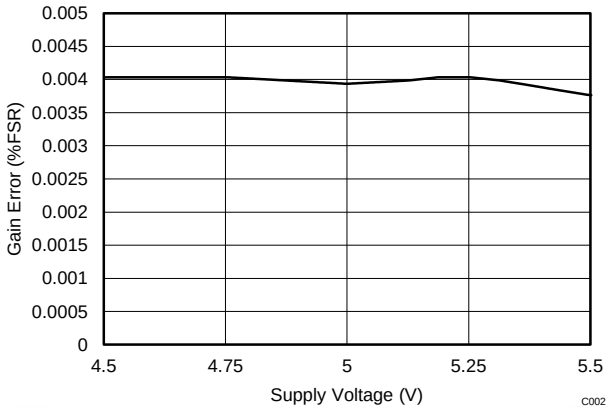
7.7 Typical Characteristics

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



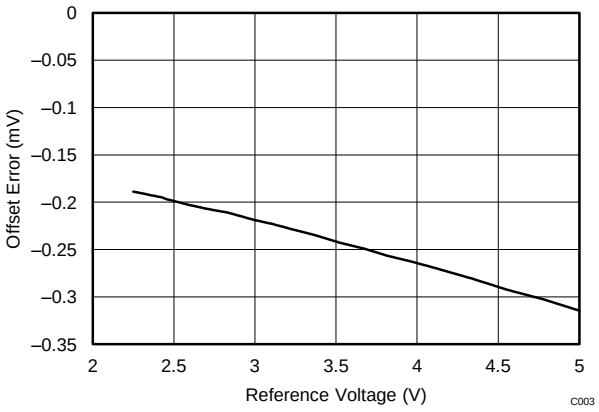
+VBD = 2.7 V, V_{ref} = 4.096 V, f_S = 250 kSPS, T_A = 30°C

Figure 1. Offset Error vs Supply Voltage



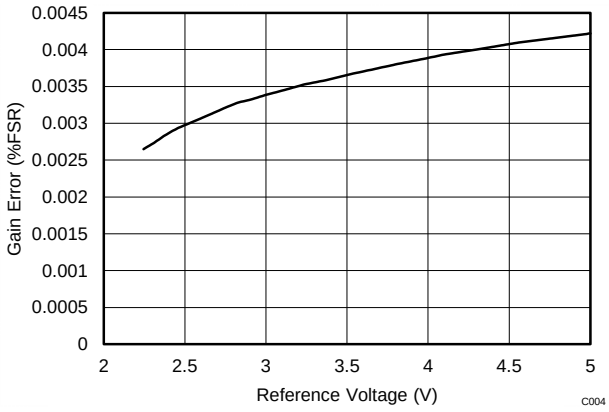
+VBD = 2.7 V, V_{ref} = 4.096 V, f_S = 250 kSPS, T_A = 30°C

Figure 2. Gain Error vs Supply Voltage



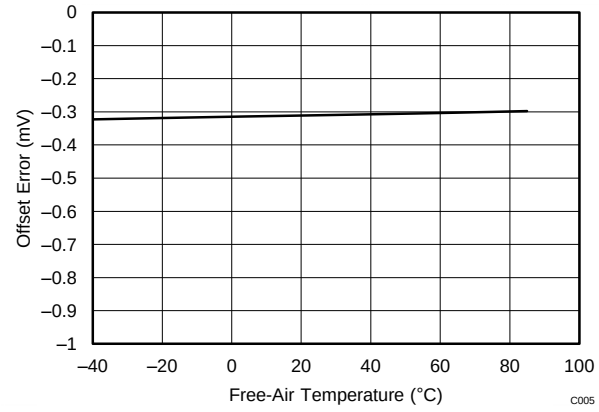
+VBD = 2.7 V, +VA = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 3. Offset Error vs Reference Voltage



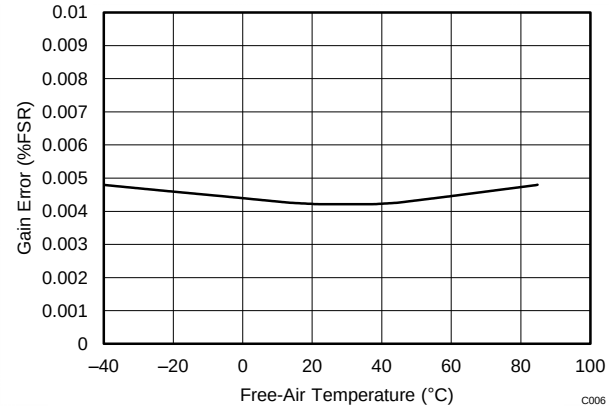
+VBD = 2.7 V, +VA = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 4. Gain Error vs Reference Voltage



+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS

Figure 5. Offset Error vs Free-Air Temperature

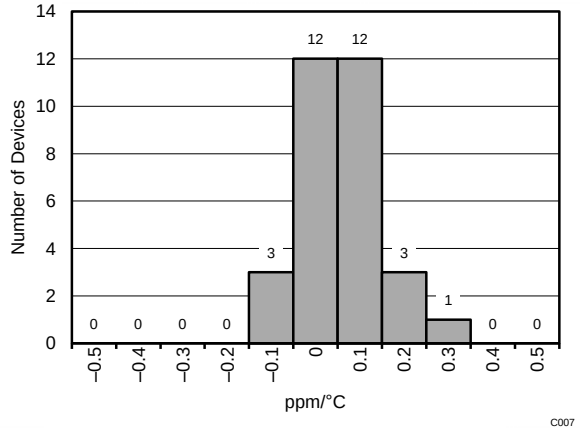


+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS

Figure 6. Gain Error vs Free-Air Temperature

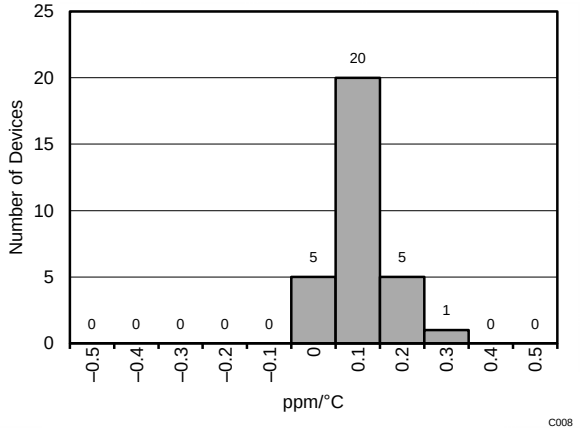
Typical Characteristics (continued)

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



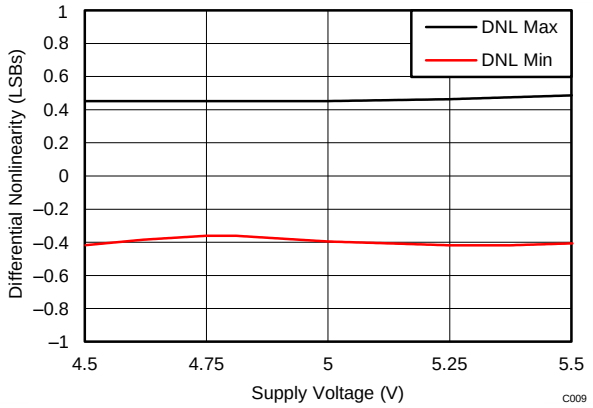
+VBD = 2.7 V, +VA = 5 V, f_S = 250 kSPS

Figure 7. Gain Error Drift Histogram



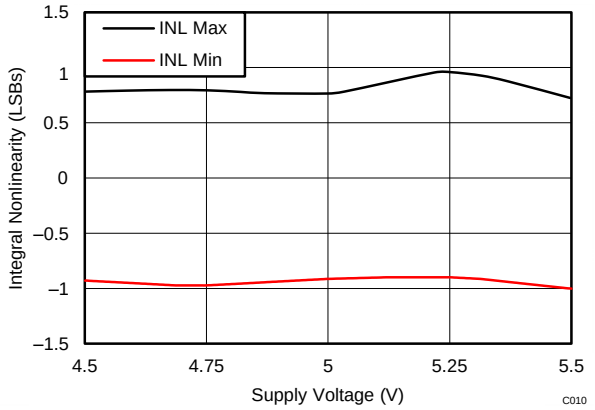
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS

Figure 8. Offset Error Drift Histogram



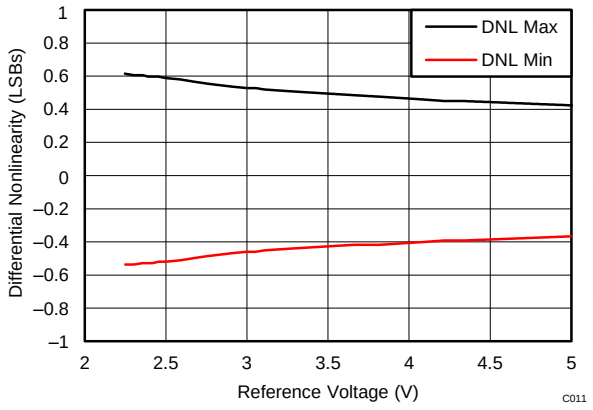
+VBD = 2.7 V, V_{ref} = 4.096 V, f_S = 250 kSPS, T_A = 30°C

Figure 9. DNL vs Supply Voltage



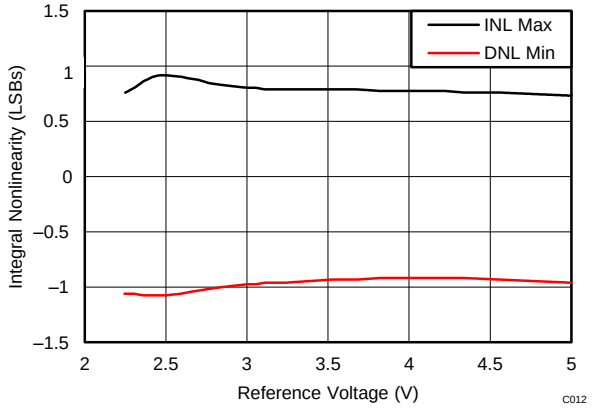
+VBD = 2.7 V, V_{ref} = 4.096 V, f_S = 250 kSPS, T_A = 30°C

Figure 10. INL vs Supply Voltage



+VBD = 2.7 V, +VA = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 11. DNL vs Reference Voltage

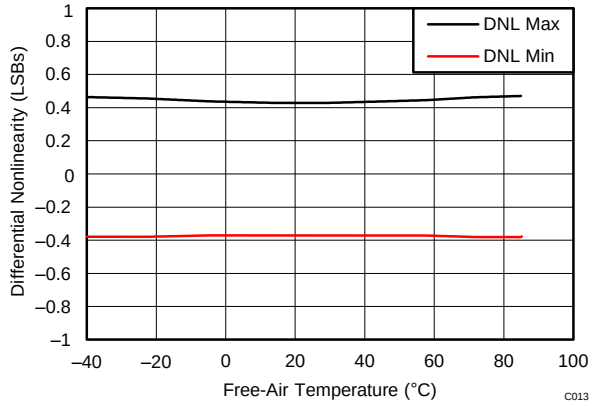


+VBD = 2.7 V, +VA = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 12. INL vs Reference Voltage

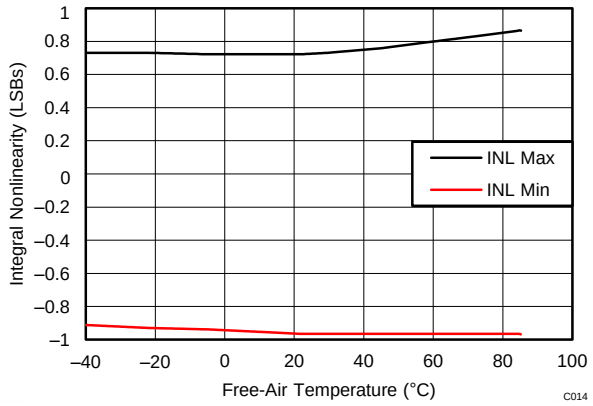
Typical Characteristics (continued)

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



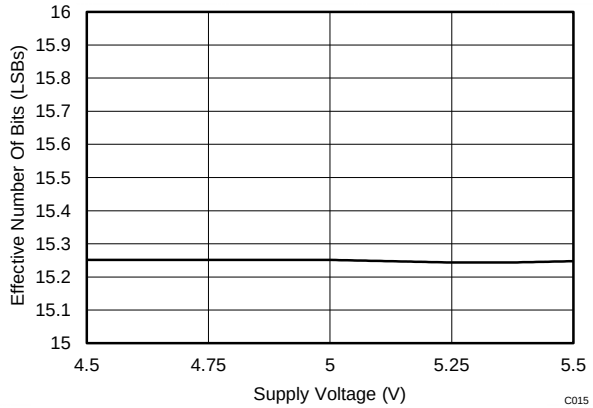
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS

Figure 13. DNL vs Free-Air Temperature



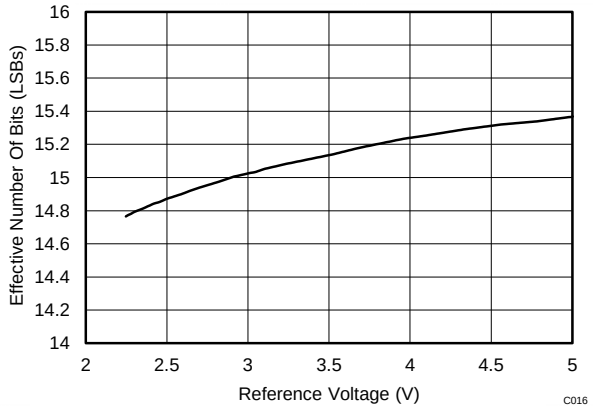
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS

Figure 14. INL vs Free-Air Temperature



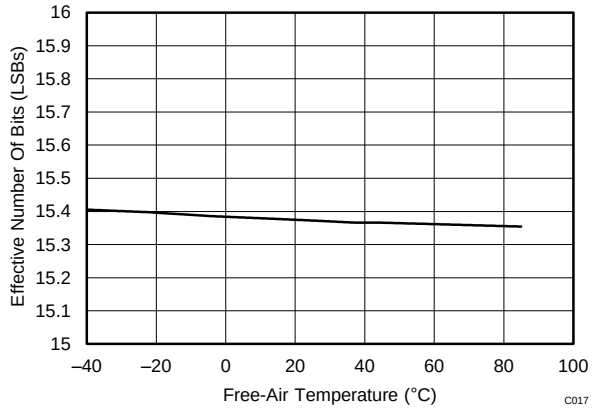
+VBD = 2.7 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 15. ENOB vs Supply Voltage



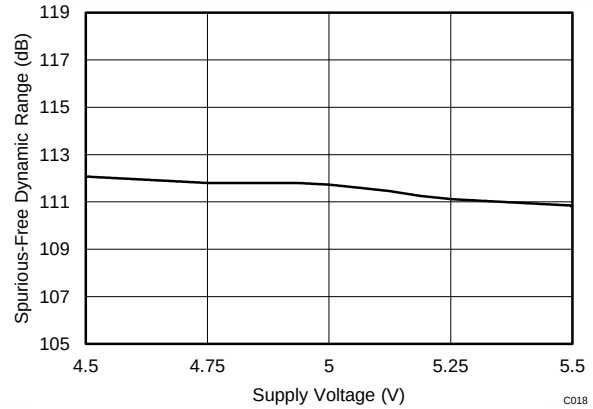
+VBD = 2.7 V, +VA = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 16. ENOB vs Reference Voltage



+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS

Figure 17. ENOB vs Free-Air Temperature

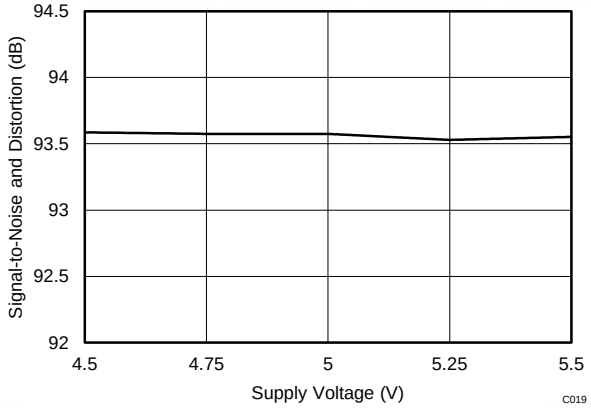


+VBD = 2.7 V, V_{ref} = 4.096 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 18. SFDR vs Supply Voltage

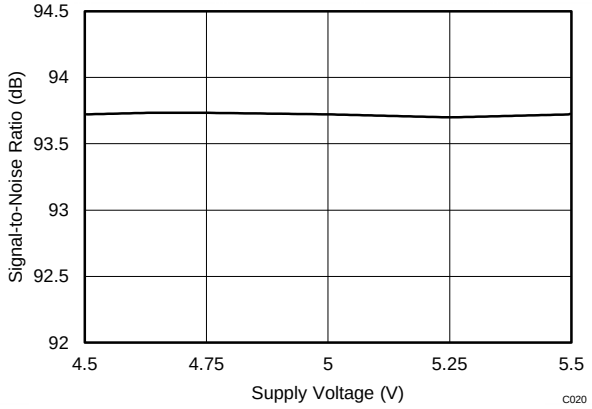
Typical Characteristics (continued)

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



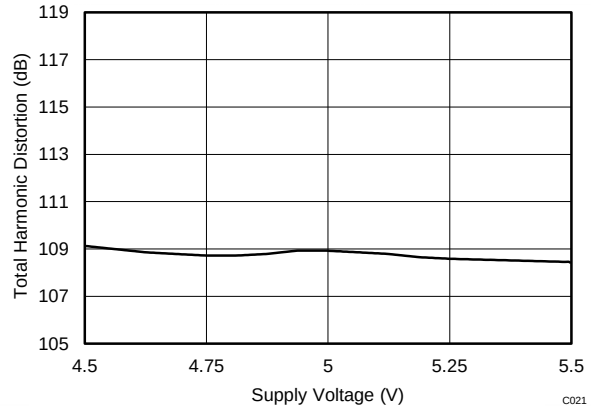
+VBD = 2.7 V, V_{ref} = 4.096 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 19. SINAD vs Supply Voltage



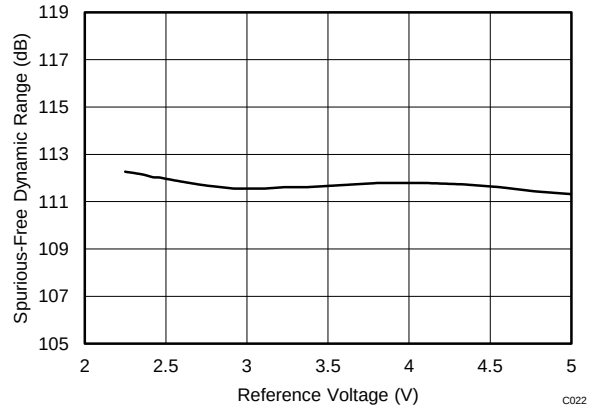
+VBD = 2.7 V, V_{ref} = 4.096 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 20. SNR vs Supply Voltage



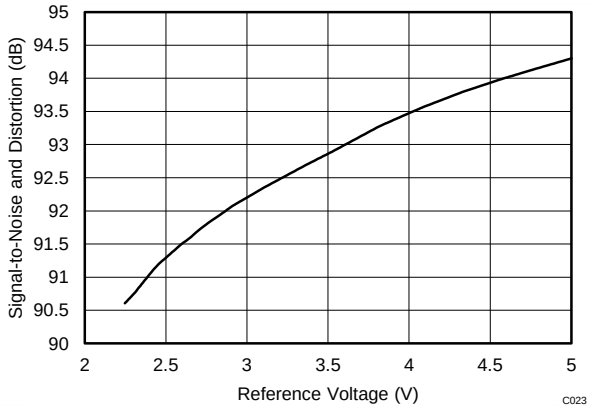
+VBD = 2.7 V, V_{ref} = 4.096 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 21. THD vs Supply Voltage



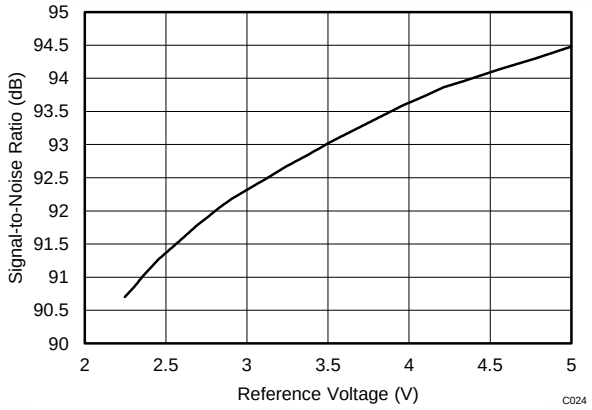
+VBD = 2.7 V, +VA = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 22. SFDR vs Reference Voltage



+VBD = 2.7 V, +VA = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 23. SINAD vs Reference Voltage

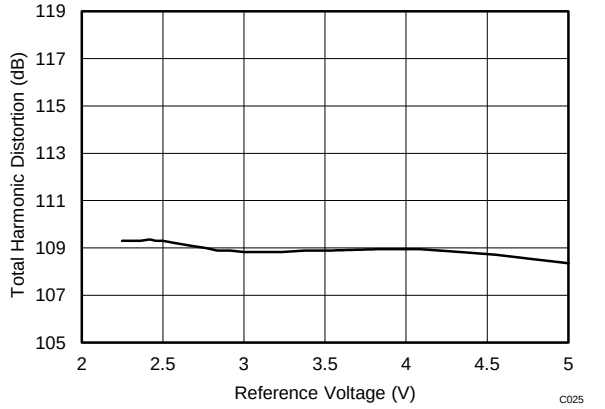


+VBD = 2.7 V, +VA = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 24. SNR vs Reference Voltage

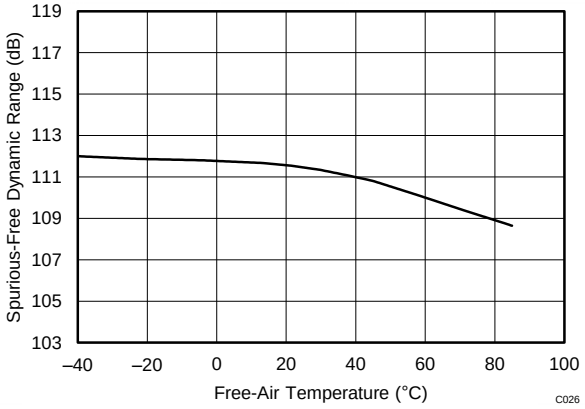
Typical Characteristics (continued)

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



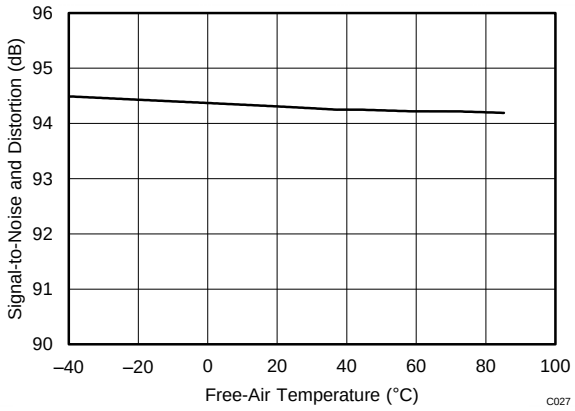
+VBD = 2.7 V, +VA = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 25. THD vs Reference Voltage



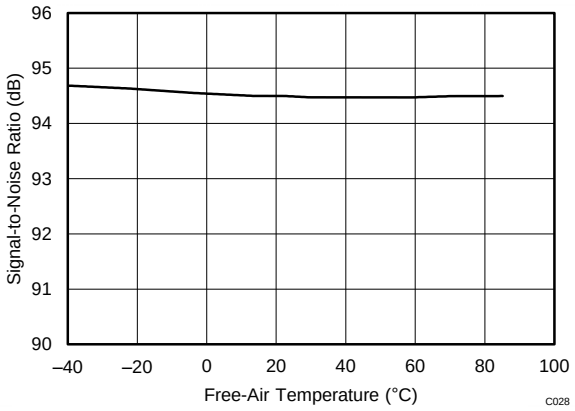
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS

Figure 26. SFDR vs Free-Air Temperature



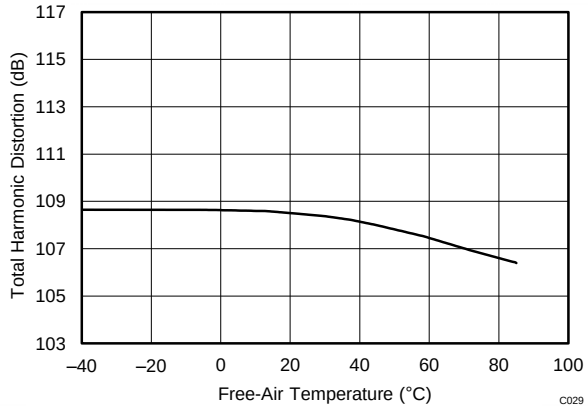
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS

Figure 27. SINAD vs Free-Air Temperature



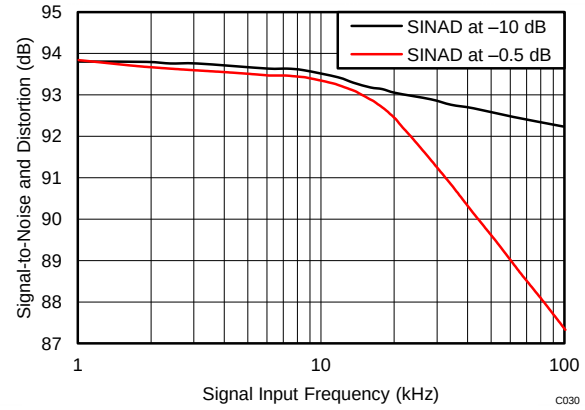
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS

Figure 28. SNR vs Free-Air Temperature



+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS

Figure 29. THD vs Free-Air Temperature

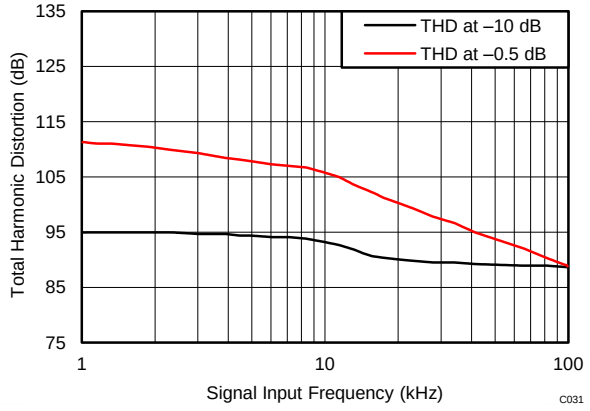


+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 30. SINAD vs Signal Input Frequency

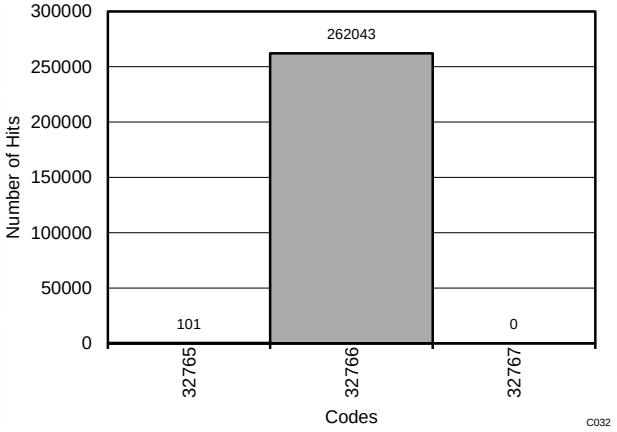
Typical Characteristics (continued)

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



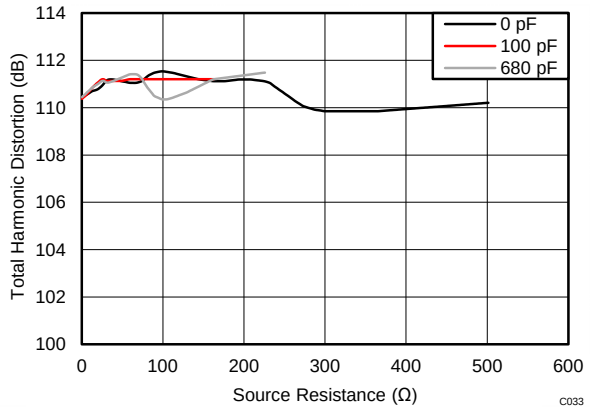
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 31. THD vs Signal Input Frequency



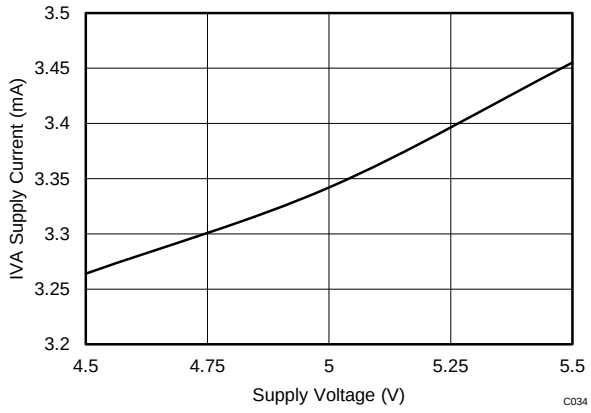
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 32. DC Histogram of ADC Close-to-Center Code



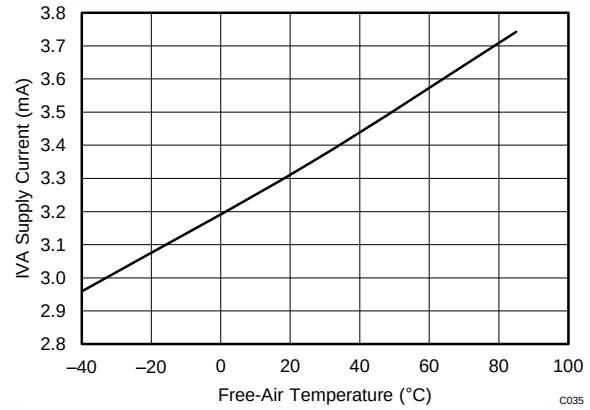
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz, f_S = 250 kSPS, T_A = 30°C

Figure 33. THD vs Source Resistance



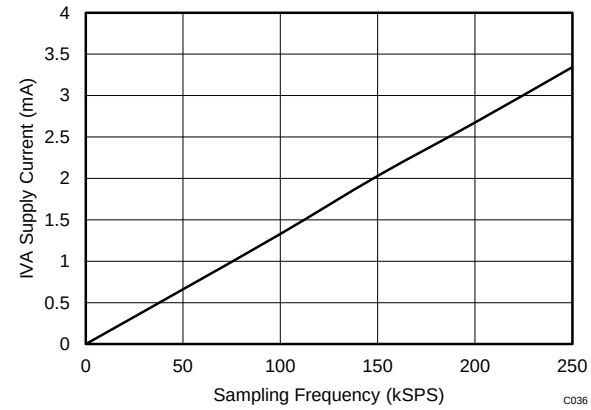
+VBD = 2.7 V, V_{ref} = 4.096 V, f_S = 250 kSPS, T_A = 30°C

Figure 34. Supply Current vs Supply Voltage



+VBD = 2.7 V, +VA = 5 V, f_S = 250 kSPS

Figure 35. Supply Current vs Free-Air Temperature

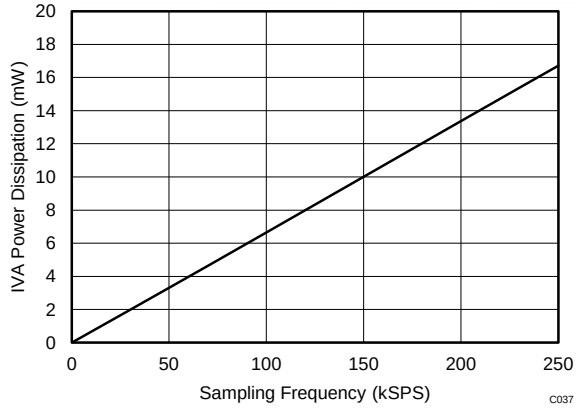


+VBD = 2.7 V, +VA = 5 V, T_A = 30°C

Figure 36. Supply Current vs Sampling Frequency

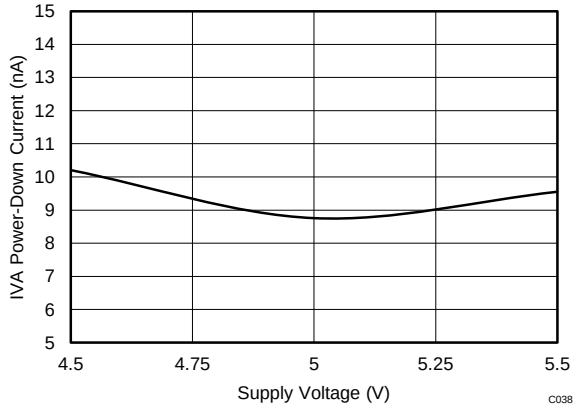
Typical Characteristics (continued)

At T_A = 30°C, +VA = 5 V, +VBD = 2.7 V, V_{ref} = 4.096 V, and f_{sample} = 250 kHz, unless otherwise noted.



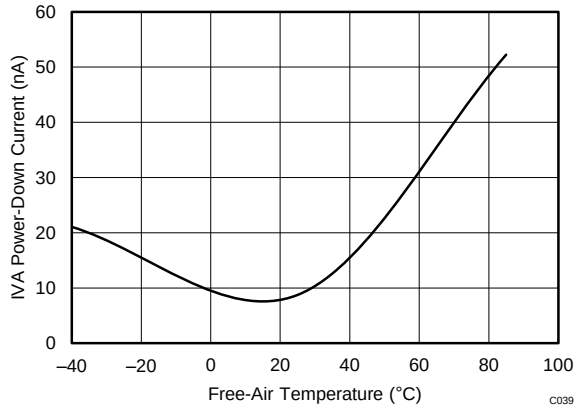
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, T_A = 30°C

Figure 37. Power Dissipation vs Sampling Frequency



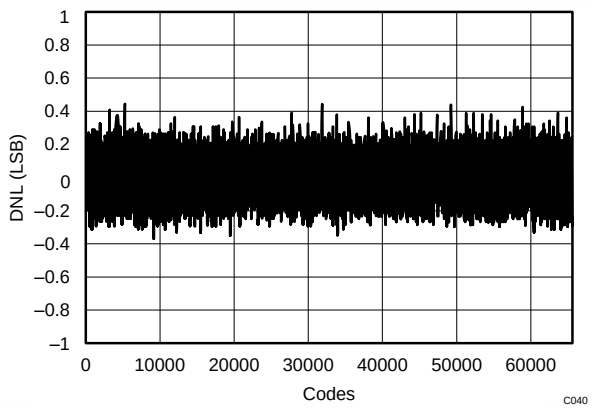
+VBD = 2.7 V, V_{ref} = 4.096 V, f_S = 250 kSPS, T_A = 30°C

Figure 38. Power-Down Current vs Supply Voltage



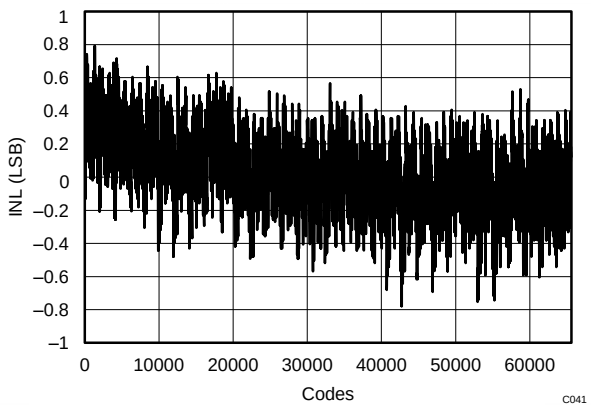
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 4.096 V, f_S = 250 kSPS

Figure 39. Power-Down Current vs Free-Air Temperature



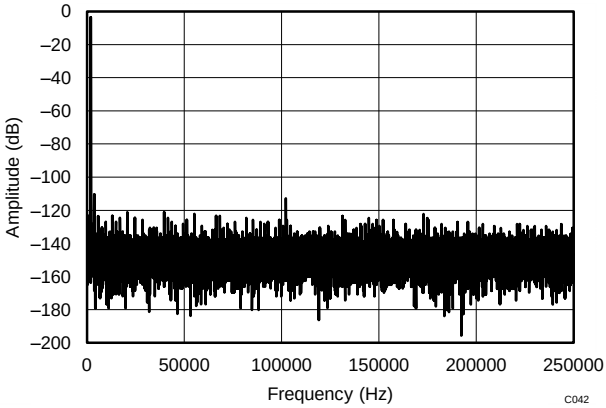
+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 40. DNL Error vs Output Code



+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_S = 250 kSPS, T_A = 30°C

Figure 41. INL Error vs Output Code



+VBD = 2.7 V, +VA = 5 V, V_{ref} = 5 V, f_{IN} = 1.9 kHz,
f_S = 250 kSPS, T_A = 30°C

Figure 42. Signal Strength vs Frequency

8 Parametric Measurement Information

8.1 Timing Diagrams

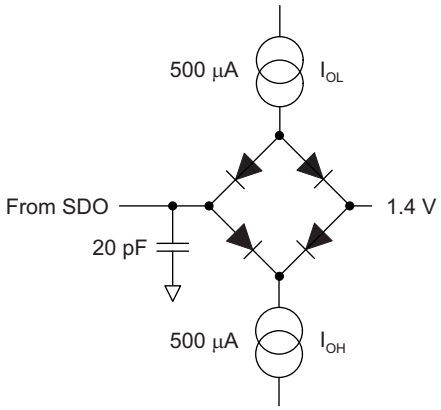


Figure 43. Digital Interface Timing Load Circuit

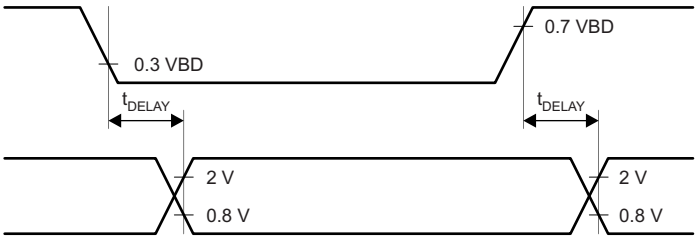


Figure 44. Timing Voltage Levels

9 Detailed Description

9.1 Overview

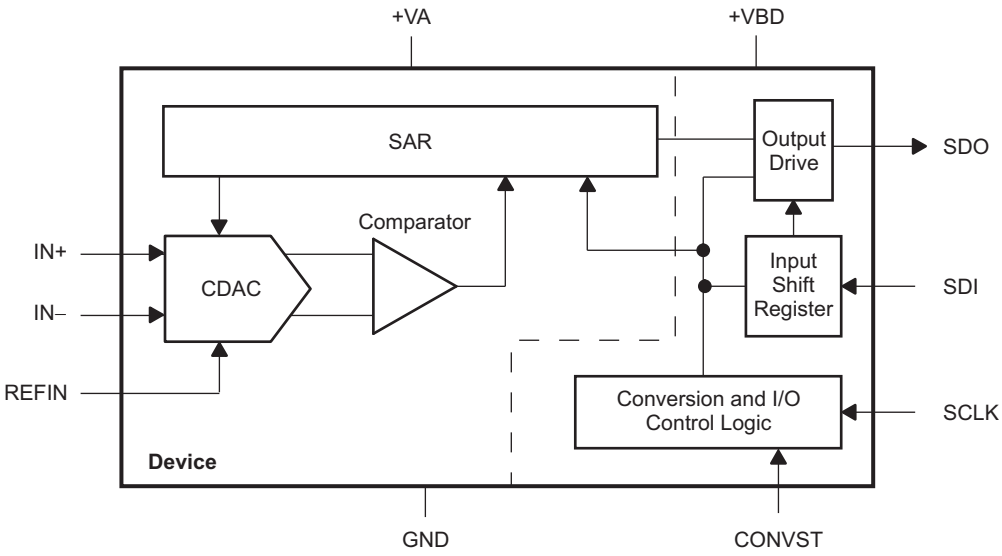
The ADS8339 is a 250-kSPS, low-power, successive-approximation register (SAR), analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample-and-hold function.

The ADS8339 is a single-channel device. The analog input is provided to two input pins: +IN and –IN, where –IN is a pseudo-differential input and has a limited range of ±0.1 V. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both the +IN and –IN inputs are disconnected from any internal functions.

The device has an internal clock that is used to run the conversion. Therefore, the conversion requires a fixed amount of time. After a conversion is completed, the device reconnects the sampling capacitors to the +IN and –IN pins and the device is in the acquisition phase. During this phase, the device is powered down and conversion data can be read.

The device digital output is available in SPI-compatible format. The device easily interfaces with microprocessors, digital signal processors (DSPs), or field-programmable gate arrays (FPGAs).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Analog Input

When the converter samples the input, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The differential signal range is [(+IN) – (–IN)]. The voltage on +IN is limited between GND – 0.1 V and V_{ref} + 0.1 V and the voltage on –IN is limited between GND – 0.1 V to GND + 0.1 V. The input rejects any small signal that is common to both the +IN and –IN input.

The (peak) input current through the analog input depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the device charges the internal capacitor array (as shown in Figure 45) during the sample period. When this capacitance is fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (59 pF) to a 18-bit settling level within the minimum acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the +IN input, –IN input, and span [+IN – (–IN)] must be within the limits specified. Outside of these ranges, the converter linearity may not meet specifications.

Care must also be taken to ensure that the output impedance of the sources driving the +IN input and the –IN input is matched. If this output impedance is not well matched, the two inputs can have different settling times. This mismatch may result in an offset error, gain error, and linearity error that changes with temperature and input voltage. Typically, the –IN input is grounded at the input decoupling capacitor.

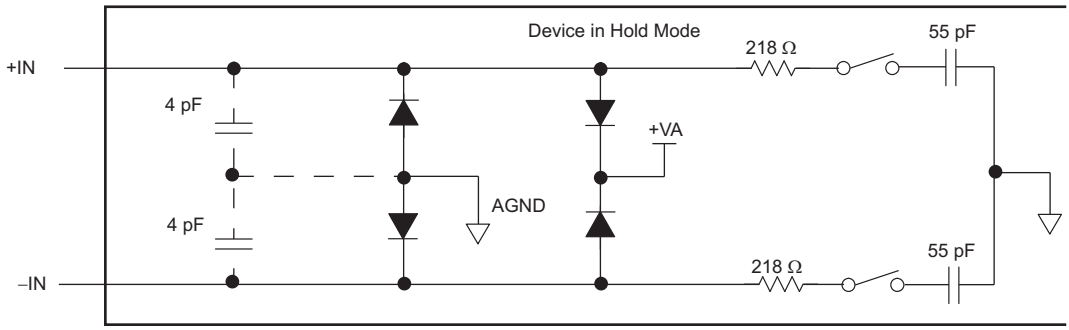


Figure 45. Input Equivalent Circuit

9.3.2 Power Saving

The device has an auto power-down feature. The device powers down at the end of every conversion. The input signal is acquired on sampling capacitors when the device is in power-down state. At the same time, the conversion results are available for reading. The device powers up automatically at the start of the conversion. The conversion runs on an internal clock and requires a fixed time. As a result, device power consumption is directly proportional to the speed of operation.

Feature Description (continued)

9.3.3 Digital Output

As discussed in the *Description* and *Timing Diagrams* sections, the device digital output is SPI-compatible. Table 1 lists the output codes corresponding to various analog input voltages.

Table 1. Output Codes

DESCRIPTION	ANALOG VALUE (V)	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full-scale range	V_{ref}	—	—
Least significant bit (LSB)	V_{ref} / 65536	—	—
Positive full-scale	$+V_{ref}$ – 1 LSB	1111 1111 1111 1111	FFFF
Mid-scale	V_{ref} / 2	1000 0000 0000 0000	8000
Mid-scale – 1 LSB	V_{ref} / 2 – 1 LSB	0111 1111 1111 1111	7FFF
Zero	0	0000 0000 0000 0000	0000

9.3.4 SCLK Input

The device uses SCLK for the serial data output. Data are read after the conversion is complete and the device is in acquisition phase. A free-running SCLK can be used, but TI recommends stopping the clock during conversion time because the clock edges can couple with the internal analog circuit that, in turn, can affect the conversion results.

9.4 Device Functional Modes

The ADS8339 supports three interface options. Under each option, the device can be used with or without a busy indicator.

1. $\overline{CS}$ *mode* for a 3-wire interface (with or without a busy indicator): This mode is useful for applications where a single ADS8339 device is connected to the digital host.
2. $\overline{CS}$ *mode* for a 4-wire interface (with or without a busy indicator): This mode can be used when more than one ADS8339 device is connected to the digital host on a common data bus.
3. Daisy-chain mode (with or without a busy indicator): This mode is provided to connect multiple ADS8339 devices in a chain (such as a shift register) and is useful when reducing the number of signal traces on the board or the component count.

The busy indicator is generated as the bit preceding the 16-bit serial data.

Device Functional Modes (continued)

9.4.1 $\overline{CS}$ Mode for a 3-Wire Interface

$\overline{CS}$ mode is selected if SDI is high at the CONVST rising edge. As previously indicated, the device can be used without or with a busy indicator. This section discusses this interface and the two options in detail.

9.4.1.1 3-Wire $\overline{CS}$ Mode Without a Busy Indicator

In a 3-wire $\overline{CS}$ mode, SDI is permanently tied to +VBD, as shown in Figure 46. CONVST functions like $\overline{CS}$. As shown in Figure 47, the device samples the input signal and enters the conversion phase on the CONVST rising edge. SDO goes to 3-state at the same time. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be brought low after the start of the conversion to select other devices on the board.

CONVST must return to high before the minimum conversion time (t_{cnv_min} in the *Timing Requirements* table) elapses. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

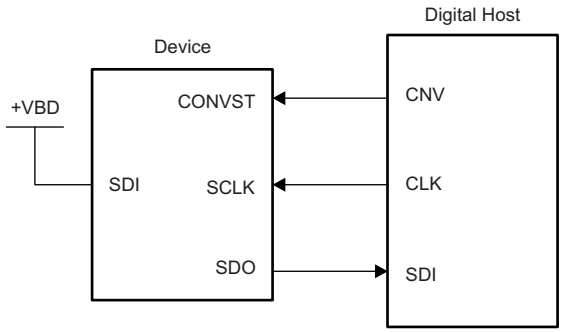


Figure 46. Connection Diagram: 3-Wire $\overline{CS}$ Mode without a Busy Indicator (SDI = 1)

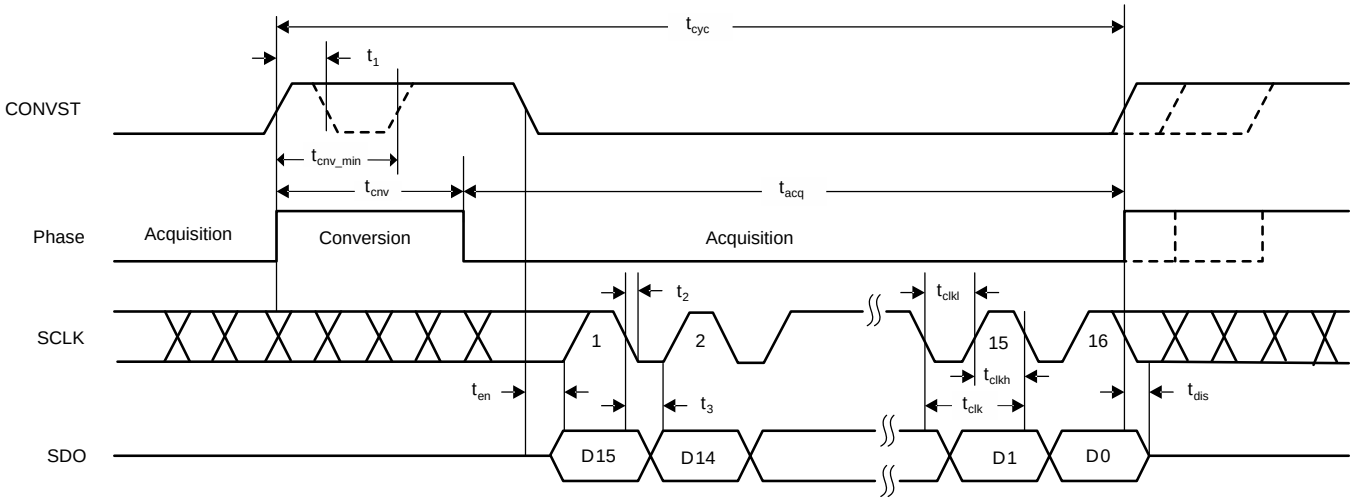


Figure 47. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode Without a Busy Indicator (SDI = 1)

When the conversion is complete, the device enters acquisition phase and powers down. On the CONVST falling edge, SDO comes out of 3-state and the device outputs the MSB of the data. Afterwards, the device outputs the next lower data bits on every subsequent SCLK falling edge. A minimum of 15 SCLK falling edges must occur during the low period of CONVST. SDO goes to 3-state after the 16th SCLK falling edge or when CONVST is high, whichever occurs first.

Device Functional Modes (continued)

9.4.1.2 3-Wire $\overline{CS}$ Mode With a Busy Indicator

As stated in the *3-Wire $\overline{CS}$ Mode Without a Busy Indicator* section, SDI is permanently tied to +VBD, as shown in Figure 48. CONVST functions like $\overline{CS}$. As shown in Figure 49, the device samples the input signal and enters the conversion phase on the CONVST rising edge. SDO goes to 3-state at the same time. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be toggled after the start of the conversion to select other devices on the board.

CONVST must return to low before the minimum conversion time (t_{cnv_min} in the *Timing Requirements* table) elapses and remains low until the end of the maximum conversion time. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator (low level on SDO). For fast settling, a 10-kΩ pull-up resistor tied to +VBD is recommended to provide the necessary current to drive SDO low.

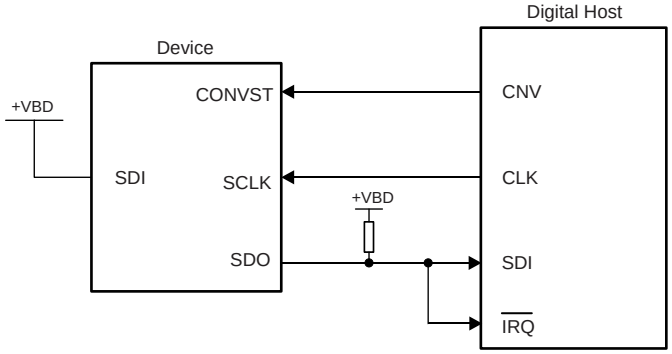


Figure 48. Connection Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator

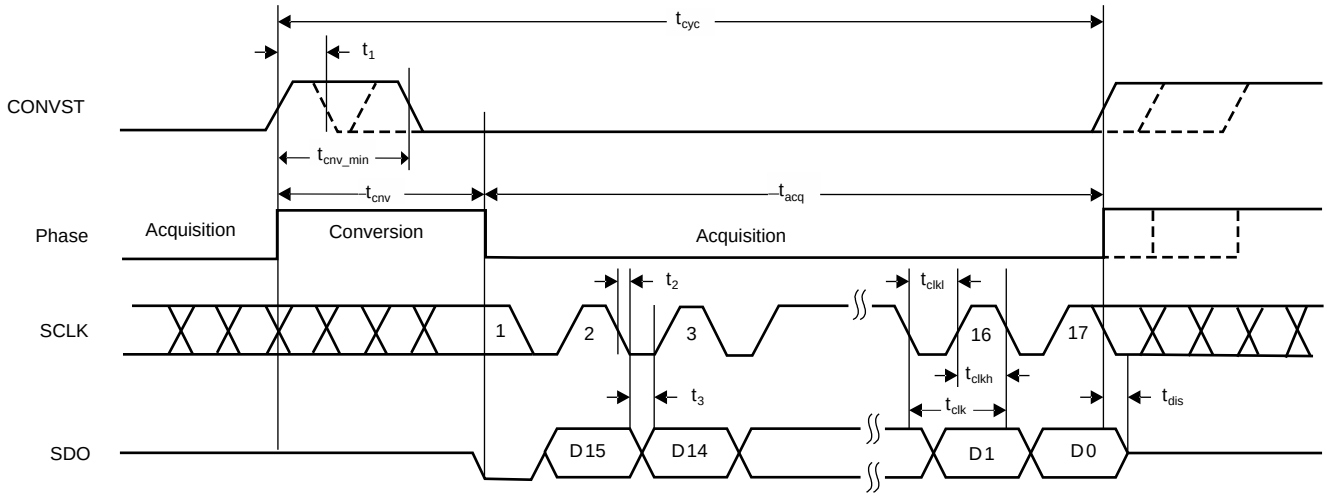


Figure 49. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator (SDI = 1)

When the conversion is complete, the device enters acquisition phase, powers down, forces SDO out of 3-state, and outputs a busy indicator bit (low level). The device outputs the MSB of data on the first SCLK falling edge after the conversion is complete and continues to output the next lower data bits on every subsequent SCLK falling edge. A minimum of 16 SCLK falling edges must occur during the low period of CONVST. SDO goes to 3-state after the 17th SCLK falling edge or when CONVST is high, whichever occurs first.

Device Functional Modes (continued)

9.4.2 $\overline{CS}$ Mode for a 4-Wire Interface

This interface is similar to the $\overline{CS}$ mode for 3-wire interface except that SDI is controlled by the digital host. This section discusses in detail the interface option with and without a busy indicator.

9.4.2.1 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

As mentioned previously, in order to select $\overline{CS}$ mode, SDI must be high at the time of the CONVST rising edge. Unlike in the 3-wire interface option, SDI is controlled by the digital host and functions like $\overline{CS}$. As shown in Figure 50, SDI goes to a high level before the CONVST rising edge. When SDI is high, the CONVST rising edge selects $\overline{CS}$ mode, forces SDO to 3-state, samples the input signal, and the device enters the conversion phase.

In the 4-wire interface option, CONVST must be at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of SDI. As a result, SDI (functioning as $\overline{CS}$) can be brought low to select other devices on the board.

SDI must return to high before the minimum conversion time (t_{cnv_min} in the *Timing Requirements* table) elapses.

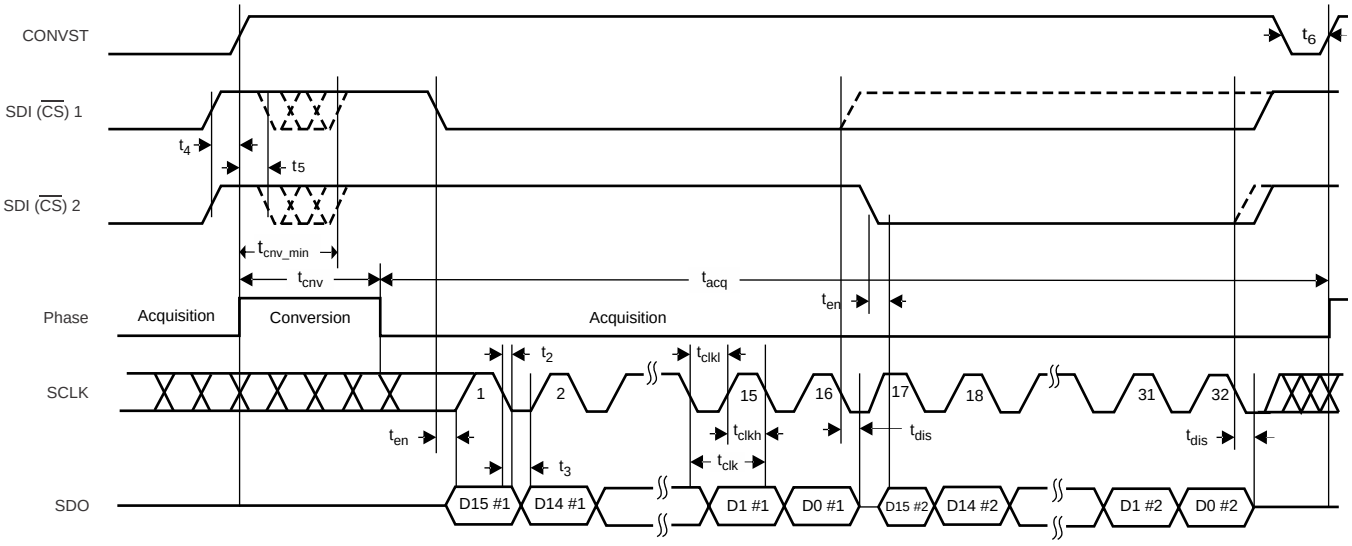


Figure 50. Interface Timing Diagram: 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

Device Functional Modes (continued)

When the conversion is complete, the device enters the acquisition phase and powers down. An SDI falling edge can occur after the maximum conversion time (t_{cnv} in the *Timing Requirements* table). Note that SDI must be high at the end of the conversion so that the device does not generate a busy indicator. The SDI falling edge brings SDO out of 3-state and the device outputs the MSB of the data. Subsequently, the device outputs the next lower data bits on every subsequent SCLK falling edge. SDO goes to 3-state after the 16th SCLK falling edge or when SDI ($\overline{CS}$) is high, whichever occurs first. As shown in Figure 51, multiple devices can be chained on the same data bus. In this case, the second device SDI (functioning as $\overline{CS}$) can go low after the first device data are read and the device 1 SDO is in 3-state.

Care must be taken so that CONVST and SDI are not both low at any time during the cycle.

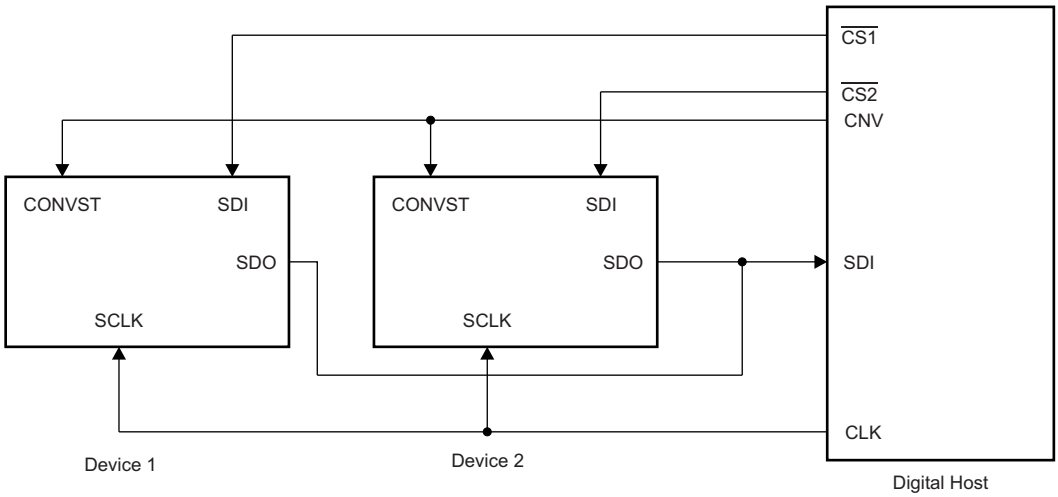


Figure 51. Connection Diagram: 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

9.4.2.2 4-Wire $\overline{CS}$ Mode With a Busy Indicator

As mentioned previously, in order to select $\overline{CS}$ mode, SDI must be high at the time of the CONVST rising edge. In this mode of operation, the connection is made as shown in Figure 52.

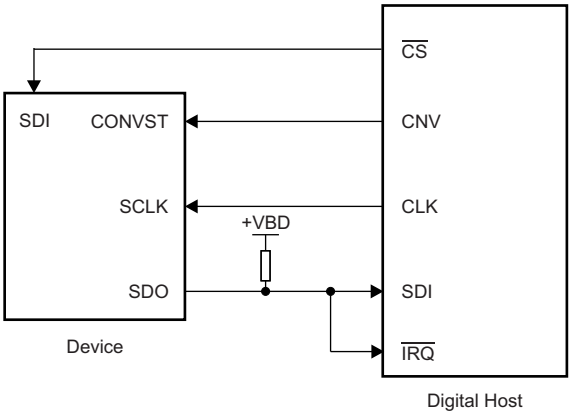


Figure 52. Connection Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

Device Functional Modes (continued)

Unlike in the 3-wire interface option, SDI is controlled by the digital host and functions like $\overline{CS}$. As shown in Figure 53, SDI goes to a high level before the CONVST rising edge. When SDI is high, the CONVST rising edge selects the $\overline{CS}$ mode, forces SDO to 3-state, samples the input signal, and the device enters the conversion phase.

In the 4-wire interface option, CONVST must be at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of SDI. As a result, SDI (functioning as $\overline{CS}$) can be toggled to select other devices on the board.

SDI must return low before the minimum conversion time (t_{cnv_min} in the *Timing Requirements* table) elapses and must remain low until the end of the maximum conversion time. A low level on the SDI input at the end of a conversion ensures the device generates a busy indicator (low on SDO). For fast settling, a 10-kΩ pull-up resistor tied to +VBD is recommended to provide the necessary current to drive SDO low.

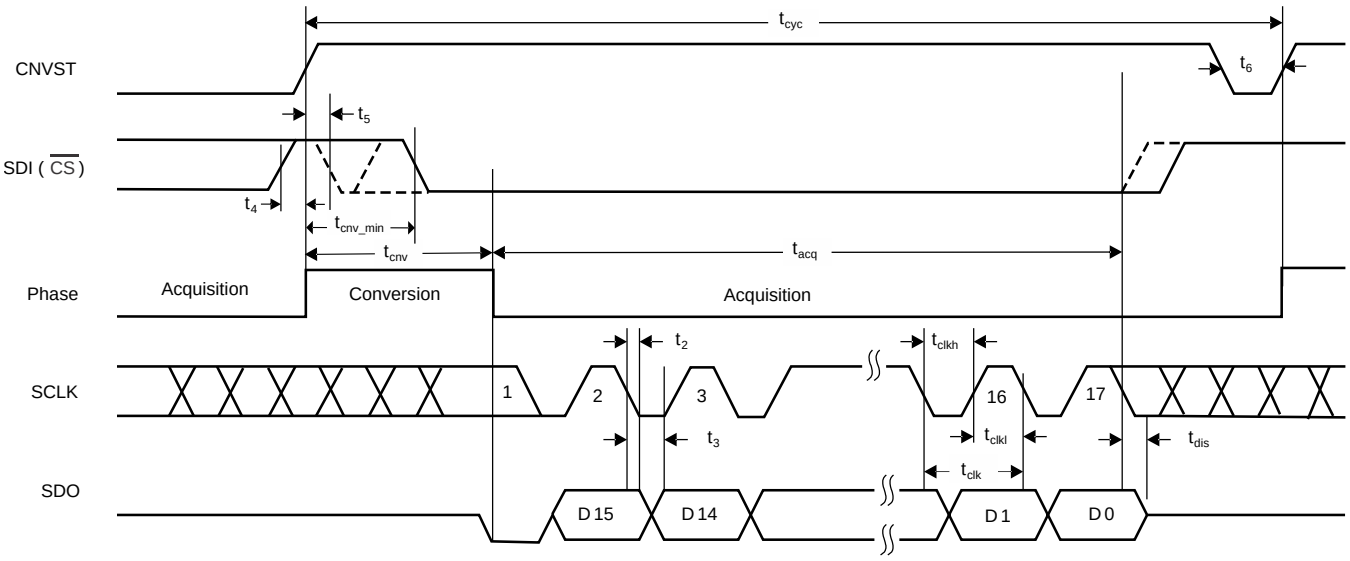


Figure 53. Interface Timing Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

When the conversion is complete, the device enters acquisition phase, powers down, forces SDO out of 3-state, and outputs a busy indicator bit (low level). The device outputs the MSB of the data on the first SCLK falling edge after the conversion is complete and continues to output the next lower data bits on every subsequent SCLK falling edge. SDO goes to 3-state after the 17th SCLK falling edge or when SDI ($\overline{CS}$) is high, whichever occurs first.

Care must be taken so that CONVST and SDI are not both low at any time during the cycle.

9.4.3 Daisy-Chain Mode

Daisy-chain mode is selected if SDI is low at the time of the CONVST rising edge. This mode is useful to reduce wiring and hardware requirements (such as digital isolators in applications where multiple ADC devices are used). In this mode, all devices are connected in a chain (the SDO of one device is connected to the SDI of the next device) and data transfer is analogous to a shift register.

As in $\overline{CS}$ mode, this mode offers operation with or without a busy indicator. This section discusses these interface options in detail.

Device Functional Modes (continued)

9.4.3.1 Daisy-Chain Mode Without a Busy Indicator

A connection diagram for this mode is shown in Figure 54. The SDI for device 1 is tied to ground and the SDO of device 1 goes to the SDI of device 2, and so on. The SDO of the last device in the chain goes to the digital host. CONVST for all devices in the chain are tied together. There is no $\overline{CS}$ signal in this mode.

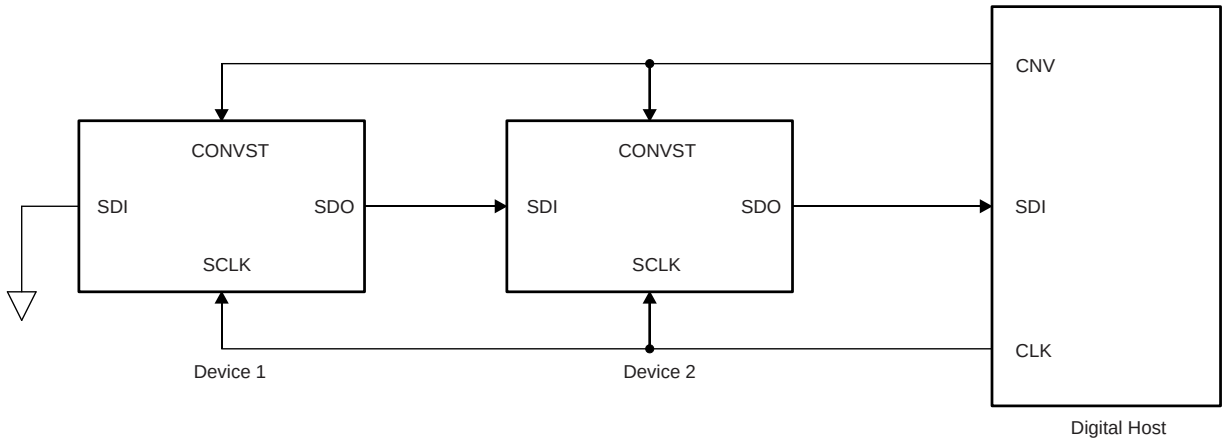


Figure 54. Connection Diagram: Daisy-Chain Mode Without a Busy Indicator (SDI = 0)

The device SDO is driven low when SDI low selects daisy-chain mode and the device samples the analog input and enters the conversion phase. SCLK must be low at the CONVST rising edge (as shown in Figure 55) so that the device does not generate a busy indicator at the end of the conversion. In this mode, CONVST remains high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK.

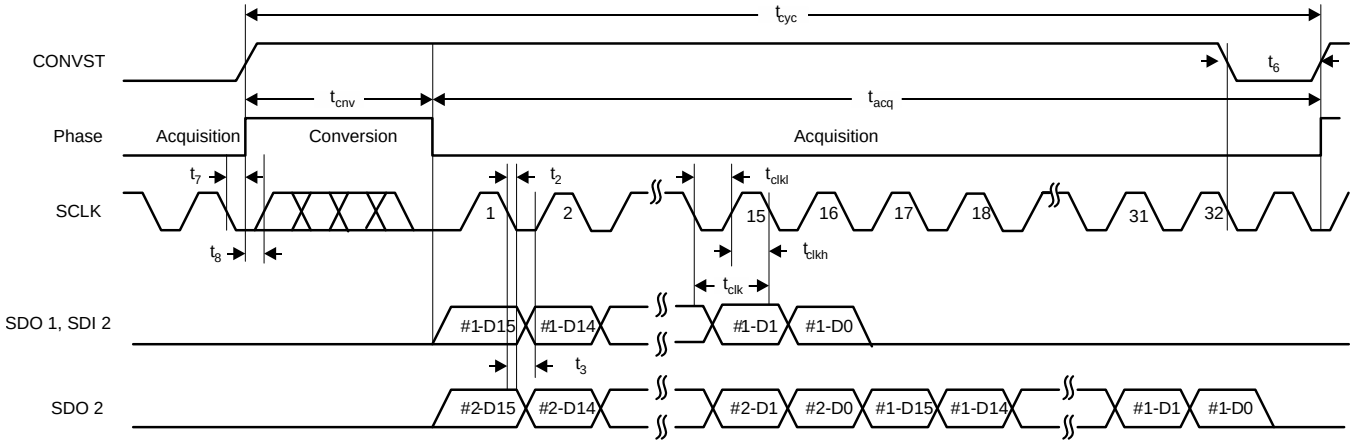


Figure 55. Interface Timing Diagram: Daisy-Chain Mode Without a Busy Indicator

At the end of the conversion, every device in the chain initiates an output of its conversion data starting with the MSB bit. Furthermore, the next lower data bit is output on every subsequent SCLK falling edge. While every device outputs its data on the SDO pin, each device also receives the previous device data on the SDI pin (other than device 1) and stores the data in the shift register. The device latches incoming data on every SCLK falling edge. The SDO of the first device in the chain goes low after the 16th SCLK falling edge. All subsequent devices in the chain output the stored data from the previous device in MSB-first format immediately following their own data word. 16 × N clocks must read data for N devices in the chain.

Device Functional Modes (continued)

9.4.3.2 Daisy-Chain Mode With a Busy Indicator

A connection diagram for this mode is shown in Figure 56. The SDI for device 1 is wired to its CONVST and the CONVST for all devices in the chain are wired together. The SDO of device 1 goes to the SDI of device 2, and so on. The SDO of the last device in the chain goes to the digital host. There is no $\overline{CS}$ signal in this mode.

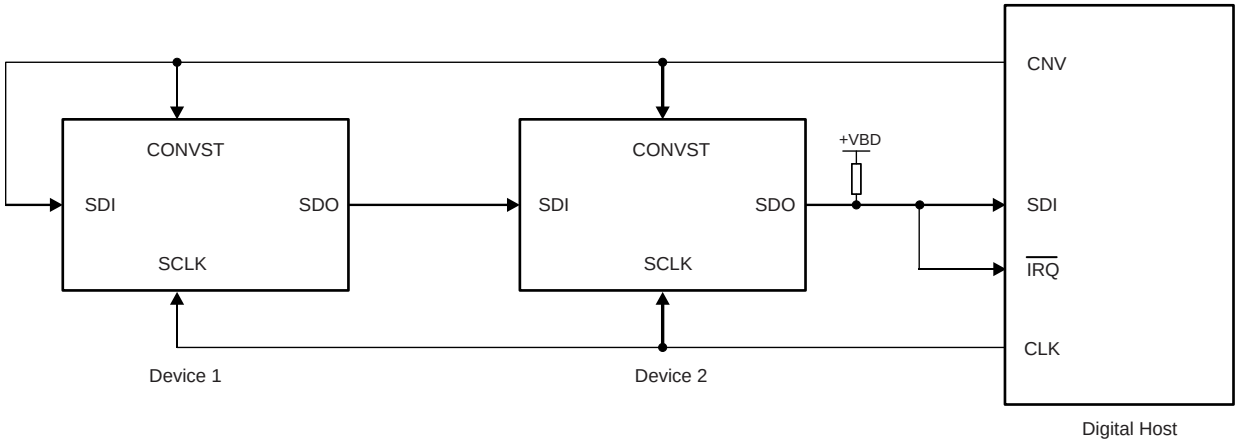


Figure 56. Connection Diagram: Daisy Chain Mode With a Busy Indicator (SDI = 0)

On the CONVST rising edge, all devices in the chain sample the analog input and enter the conversion phase. For the first device, SDI and CONVST are wired together and the setup time of SDI to the CONVST rising edge is adjusted so that the device still enters daisy-chain mode even though SDI and CONVST rise together. SCLK must be high at the CONVST rising edge (as shown in Figure 57) so that the device generates a busy indicator at the end of the conversion. In this mode, CONVST remains high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK.

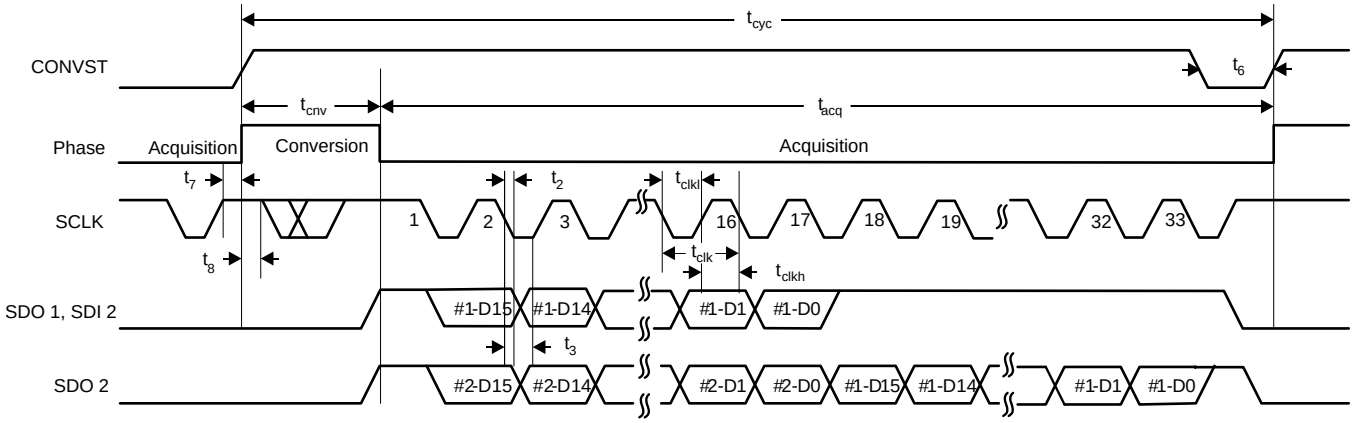


Figure 57. Interface Timing Diagram: Daisy Chain Mode With a Busy Indicator

At the end of the conversion, all devices in the chain generate busy indicators. On the first SCLK falling edge following the busy indicator bit, all devices in the chain output their conversion data starting with the MSB bit. Afterwards, the next lower data bit is output on every SCLK falling edge. While every device outputs its data on the SDO pin, each device also receives the previous device data on the SDI pin (except for device 1) and stores the data in the shift register. Each device latches incoming data on every SCLK falling edge. The SDO of the first device in the chain goes high after the 17th SCLK falling edge. All subsequent devices in the chain output the stored data from the pervious device in MSB-first format immediately following their own data word. 16 × N + 1 clock pulses are required to read data for N devices in the chain.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

To obtain the best performance from a high-precision successive approximation register (SAR) analog-to-digital converter (ADC), the reference driver and the input driver circuit must be optimized. This section details general principles for designing such drivers, followed by typical application circuits designed using the ADS8339.

10.1.1 ADC Reference Driver

A simplified circuit diagram for such a reference driver is shown in Figure 58.The external voltage reference must provide a low-noise, low-drift, highly-accurate voltage for the ADC reference input pin. The output broadband noise of most voltage references can be in the order of a few hundred μV_{RMS}, which degrades the conversion result. To prevent any noticeable degradation in the noise performance of the ADC, the noise from the voltage reference must be filtered. This filtering can be done by using a low-pass filter with a cutoff frequency of a few hundred hertz.

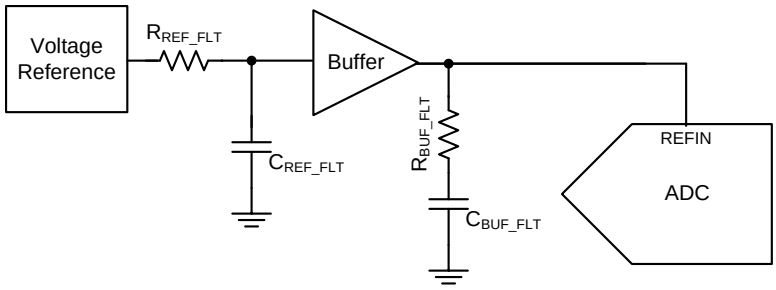


Figure 58. Reference Driver Schematic

During the conversion process, the ADS8339 switches binary-weighted capacitors onto the reference pin (REFIN). The switching frequency is proportional to the internal conversion clock frequency. The dynamic charge required by the capacitors is a function of the ADC input voltage and the reference voltage. Design the reference driver circuit such that the dynamic loading of the capacitors can be handled without degrading the noise and linearity performance of the ADC.

When the noise of the voltage reference is band-limited the next step is to design a reference buffer that can drive the dynamic load posed during the conversion cycle. The buffer must regulate the voltage at the REFIN pin of the device such that the reference voltage to the ADC stays within 1 LSB of an error at the start of each conversion. This condition necessitates the use of a large capacitor, C_{BUF_FLT} (as shown in Figure 58). The amplifier selected as the buffer must have very low offset, temperature drift, and output impedance to drive the internal binary-weighted capacitors at the REFIN pin of the ADC without any stability issues.

Application Information (continued)

10.1.1.1 Reference Driver Circuit

A more detailed circuit shows the schematic (as shown in Figure 59) of a complete reference driver circuit that generates 4.5 V dc using a single 5-V supply. This circuit can drive the reference pin of the ADS8339 at sampling rates of up to 250 kSPS. The 4.5-V reference voltage is generated using a high-precision, low-noise REF5045. The output broadband noise of the reference is further filtered using a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

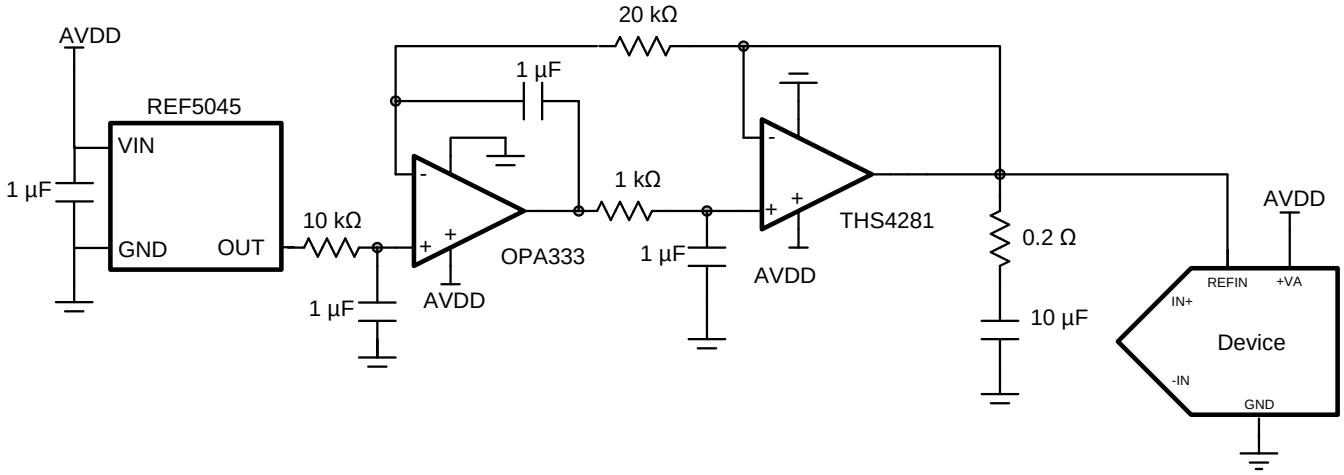


Figure 59. Reference Driver Circuit Schematic

The driver also includes a THS4281 and an OPA333. This composite architecture provides superior ac and dc performance at reduced power levels compared to a single high-performance amplifier.

The THS4281 is a high-bandwidth amplifier with very low output impedance of 1 Ω at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving large capacitive loads. The high offset and drift specifications of the THS4281 are corrected using a dc-correcting amplifier (OPA333) inside the feedback loop. Thus, the composite scheme also inherits the extremely low offset and temperature drift specifications of the OPA333.

10.1.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and an RC filter. An amplifier is used for signal conditioning the input voltage. The low output impedance of the amplifier functions as a buffer between the signal source and the sampling capacitor input of the ADC. The RC filter functions as an antialiasing filter that band-limits the wideband noise contributed by the front-end circuit. The RC filter also helps attenuate the sampling capacitor charge injection from the switched-capacitor input stage of the ADC. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision, 16-bit ADC such as the ADS8339.

Application Information (continued)

10.1.2.1 Input Amplifier Selection

Selection criteria for the input amplifier is dependent on the input signal type as well as performance goals of the data acquisition system. Some key specifications to consider when selecting an amplifier to drive the inputs of the ADS8339 are:

- *Small-signal bandwidth.* The small-signal bandwidth of the input amplifier must be as high as possible for a given power budget. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the RC filter (with low cutoff frequency) at the inputs of the ADC. Higher bandwidth also minimizes harmonic distortion at higher input frequencies. In order to maintain overall stability, the amplifier bandwidth must satisfy Equation 1:

$$Unity-Gain\ Bandwidth \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (1)$$

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in the overall SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. Noise from the input driver circuit gets band-limited by the RC filter, as given in Equation 2.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \quad \leq \quad \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (2)$$

where:

- $V_{1\ /\ f\_AMP\_PP}$ is the peak-to-peak flicker noise in µV,
- e_{n_RMS} is the amplifier broadband noise density in nV/√Hz,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration.

- *Distortion.* The ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as given in Equation 3.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \quad (3)$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to a 16-bit accuracy level at the device inputs during the acquisition time. This condition is critical in maintaining the overall linearity of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 16-bit accuracy. Therefore, the settling behavior of the input driver must always be verified by TINA™-SPICE simulations before selecting the amplifier.

10.1.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling the input signal at a constant rate. Any frequency content in the input signal that is beyond half the sampling frequency is folded back into the low-frequency spectrum, which is undesirable. This process is called *aliasing*. An analog antialiasing filter must be used to remove the high-frequency component (beyond half the sampling frequency) from the input signal before being sampled by the ADC.

An antialiasing filter is designed as a low-pass, RC filter for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow for accurate settling of the signal at the input of the ADC. For ac signals, keep the filter bandwidth as low as possible to band-limit the noise fed into the ADC, which improves the signal-to-noise ratio (SNR) performance of the system.

Application Information (continued)

The RC filter also helps absorb the sampling charge injection from the switched-capacitor input of the ADC. A filter capacitor, C_{FLT}, is connected across the inputs of the ADC (as shown in Figure 60). This capacitor helps absorb the sampling capacitor charge injection in addition to functioning as a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition phase.

When selecting this capacitor, as a rule of thumb, the capacitor value must be at least 10 times the ADC sampling capacitor specified on the data sheet. The input sampling capacitance is approximately 59 pF for the ADS8339. The value of C_{FLT} must be greater than 590 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

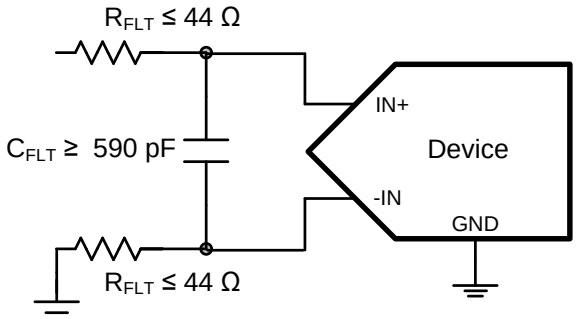


Figure 60. Antialiasing Filter

NOTE

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective. Distortion increases with source impedance, input signal frequency, and input signal amplitude. The selection of R_{FLT} thus requires a balance between stability and distortion of the design.

TI recommends limiting the value of R_{FLT} to a maximum of 44 Ω in order to avoid any significant degradation in linearity performance for the ADS8339. The tolerance of resistors can be 1% because the differential capacitor at the input balances the effects resulting from resistor mismatch.

The input amplifier bandwidth must be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends running a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the filter that is designed. Simulation is critical because some amplifiers may require more bandwidth than others to drive similar filters. If an amplifier has less than 40° phase margin with 44-Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

10.2 Typical Application

This section describes a typical application circuit using the ADS8339. The circuit is optimized to derive the best ac performance. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams.

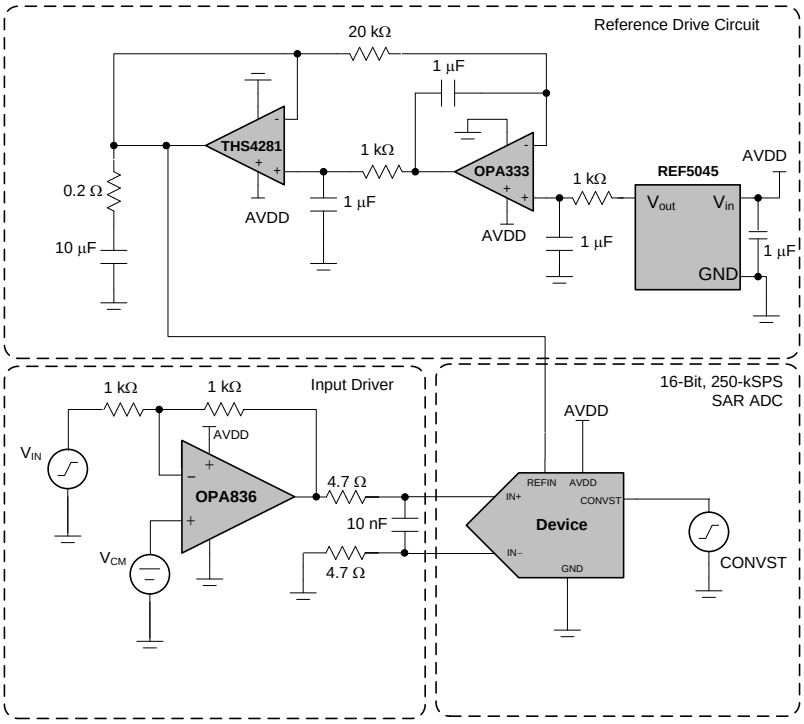


Figure 61. Single-Ended Input DAQ Circuit for Lowest Distortion and Noise at 250 kSPS

10.2.1 Design Requirements

The application circuit for the ADS8339 (as shown in Figure 61) is optimized for lowest distortion and noise for a 10-kHz input signal to achieve:

- –106-dB THD and 93-dB SNR at a maximum specified throughput of 250 kSPS.

10.2.2 Detailed Design Procedure

In the application circuit, the input signal is processed through a high-bandwidth, low-distortion, inverting amplifier and a low-pass RC filter before being fed to the ADC.

The reference driver circuit illustrated in Figure 59 generates 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference at sampling rates of up to 250 kSPS. To keep the noise low, a high-precision REF5045 is used. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

The reference buffer is designed in a composite architecture to achieve superior dc and ac performance at reduced power consumption. The low output impedance makes the THS4281 a good choice for driving large capacitive loads that regulate the voltage at the reference input pin of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (such as the OPA333) inside the feedback loop.

For the input driver, as a rule of thumb, the distortion of the amplifier must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the driver in an inverting gain configuration. This configuration also eliminates the need for an amplifier that supports rail-to-rail input. The OPA836 is a good choice for an input driver because of its low-power consumption and exceptional ac performance (such as low distortion and high bandwidth).

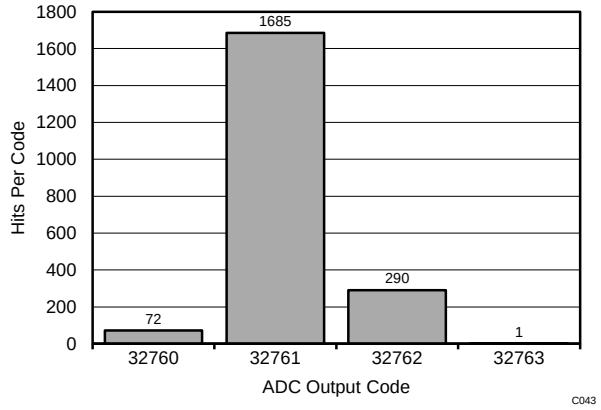
Finally, the components of the antialiasing filter are chosen such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

Typical Application (continued)

10.2.3 Application Curve

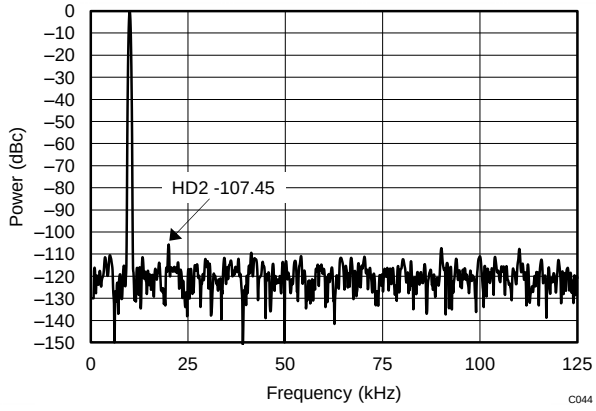
To ensure that the circuit meets the design requirements, the dc noise performance and the frequency content of the digitized output is verified. The input is set to a fixed dc value at half the reference. The histogram of the output code shows a peak-to-peak noise distribution of four codes which translates to 14 bits of noise-free bits.

An ac signal at 10 kHz is then fed to the input. The FFT of the output shows a THD of –106 dB and an SNR of 92 dB, which is close to the design requirements.



$V_{DIFF} = V_{ref} / 2$, 2048 data points, standard deviation = 0.41 bits

Figure 62. DC Input Histogram at Mid-Code



SNR = 92 dB, THD = – 106 dB, number of samples = 1024

Figure 63. 0.4-dBFS, 10-kHz Sine Input FFT

10.3 Do's and Don'ts

- Use multiple capacitors to decouple the dynamic current transients at various input pins including the reference, supply, and input signal.
- Parasitic inductance can induce ringing on the clock signal. Include a resistor on the SCLK pin to clean up the clock edges.

11 Power-Supply Recommendations

The ADS8339 is designed to operate from an analog supply voltage range between 4.5 V and 5.5 V and a digital supply voltage range between 2.375 V and 5.5 V. Both supplies must be well regulated. The analog supply must always be greater than or equal to the digital supply. A 1-µF ceramic decoupling capacitor is required at each supply pin and must be placed as close as possible to the device.

12 Layout

12.1 Layout Guidelines

Figure 64 shows one of the board layouts as an example when using ADS8339 in a circuit.

- A printed circuit board (PCB) board with at least four layers is recommended to keep all critical components on the top layer.
- Analog input signals and the reference input signals must be kept away from noise sources. Crossing digital lines with the analog signal path should be avoided. The analog input and the reference signals are routed on to the left side of the board and the digital connections are routed on the right side of the device.
- Due to the dynamic currents that occur during conversion and data transfer, each supply pin (AVDD and DVDD) must have a decoupling capacitor that keeps the supply voltage stable. TI recommends using one 1-µF ceramic capacitor at each supply pin.
- A layout that interconnects the converter and accompanying capacitors with the low inductance path is critical for achieving optimal performance. Using 15-mil vias to interconnect components to a solid analog ground plane at the subsequent inner layer minimizes stray inductance. Avoid placing vias between the supply pin and the decoupling capacitor. Any inductance between the supply capacitor and the supply pin of the converter must be kept to less than 5 nH by placing the capacitor within 0.2 inches from the supply or input pins of the ADS8339 and by using 20-mil traces, as shown in Figure 64.
- Dynamic currents are also present at the REFIN pin during the conversion phase. Therefore, good decoupling is critical to achieve optimal performance. The inductance between the reference capacitor and the REFIN pin must be kept to less than 2 nH by placing the capacitor within 0.1 inches from the REFIN pin and by using 20-mil traces.
- A single 10-µF, X7R-grade, 0805-size ceramic capacitor with at least a 10-V rating is recommended for good performance over temperature range.
- A small, 0.1-Ω to 0.47-Ω, 0603-size resistor placed in series with the reference capacitor keeps the overall impedance low and constant, especially at very high frequencies.
- Avoid using additional lower value capacitors because the interactions between multiple capacitors can affect the ADC performance at higher sampling rates.
- Place the RC filters immediately next to the input pins. Among surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

12.2 Layout Example

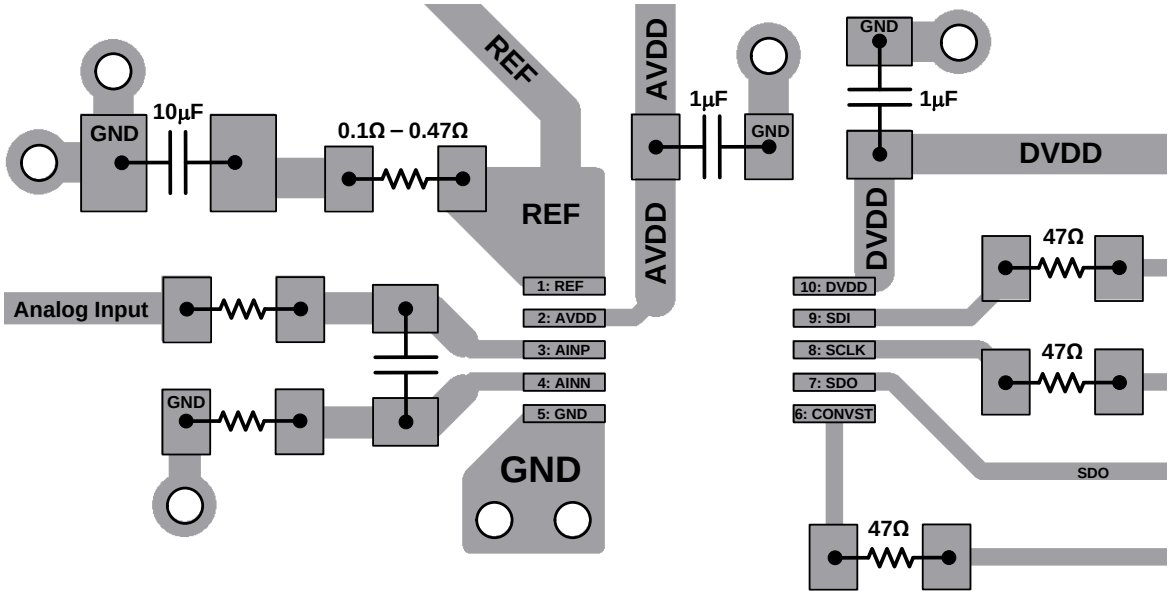


Figure 64. Board Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

《REF5045 数据表》（文献编号 SBOS410）

《THS4281 数据表》（文献编号 SLOS432）

《OPA333 数据表》（文献编号 SBOS351）

《OPA836 数据表》（文献编号 SLOS713）

《ADS886xEVM-PDK 和 ADS83x9EVM-PDK 用户指南》（文献编号 SBAU233）

13.2 商标

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13.3 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8339IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	8339	Samples
ADS8339IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	8339	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

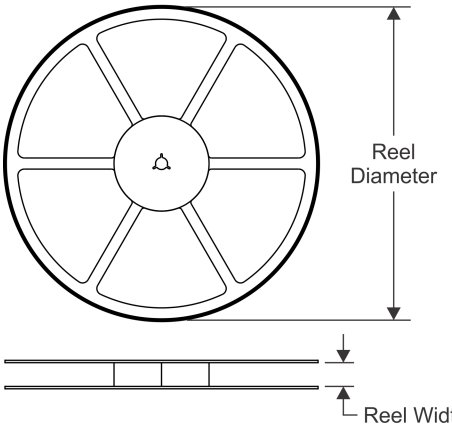
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

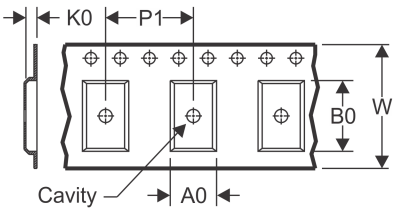
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

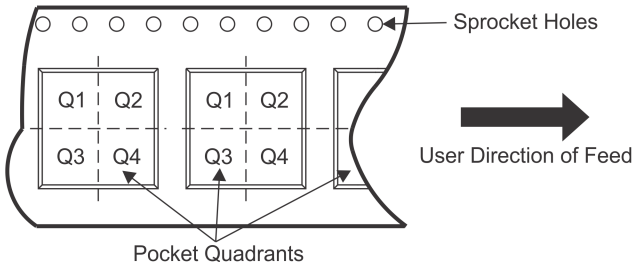


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

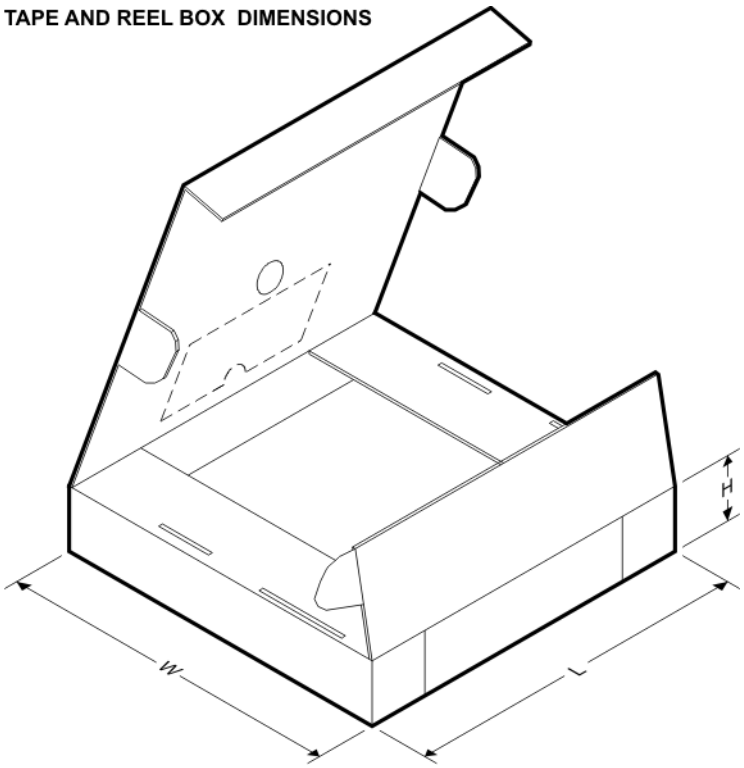
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8339IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8339IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

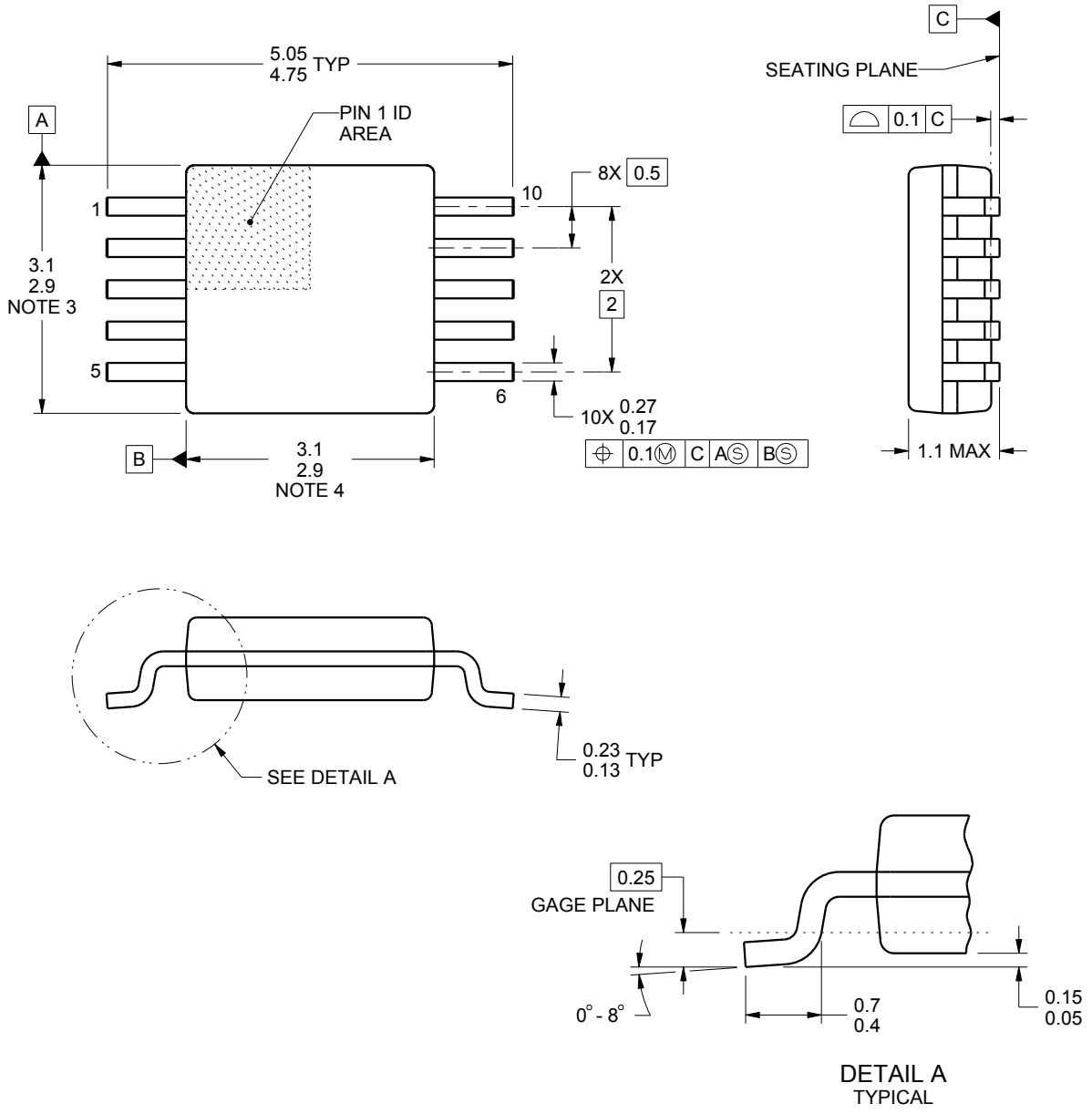
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8339IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8339IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

VSSOP - 1.1 mm max height

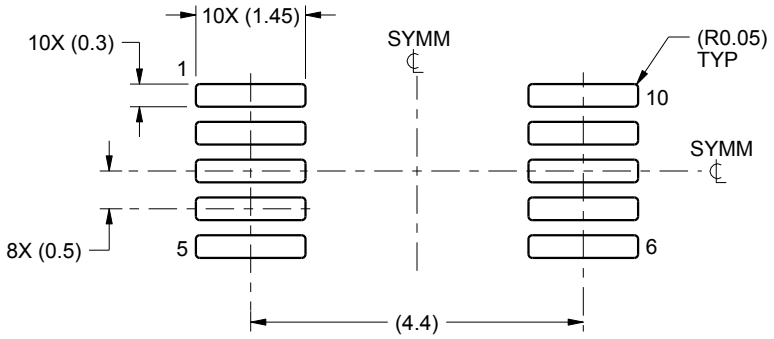
SMALL OUTLINE PACKAGE



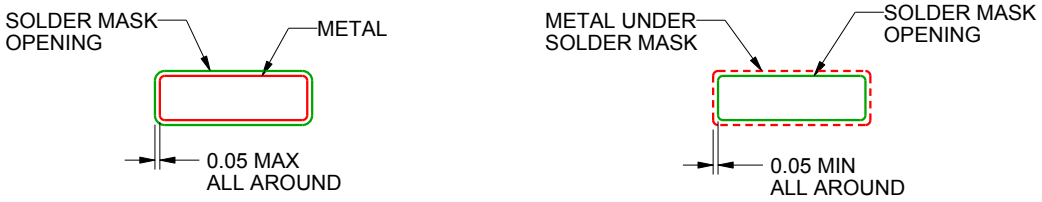
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

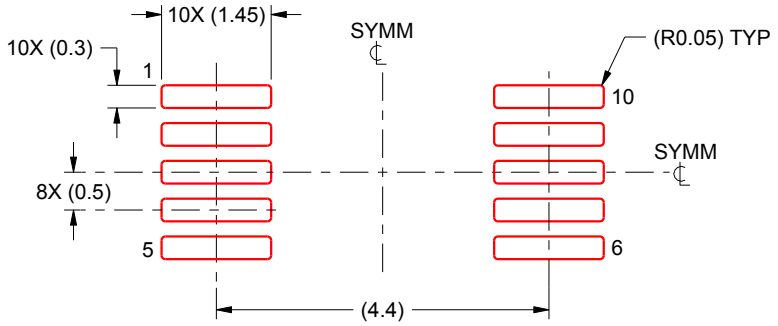


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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