UCC28600 8-Pin Quasi-Resonant Flyback Green-Mode Controller

1 Features

- Green-Mode Controller With Advanced Energy Saving Features
- Quasi-Resonant Mode Operation for Reduced EMI and Low Switching Losses (Low-Voltage Valley Switching)
- Low Standby Current for Minimum System No-Load Power Consumption
- Low Start-up Current: 25-µA Maximum
- Programmable Line and Load Over-Voltage Protection
- Internal Over-Temperature Protection
- Current Limit Protection
  - Cycle-by-Cycle Power Limit
  - Primary-Side Over-Current Hiccup Restart Mode
- 1-A Sink, –0.75-A Source TrueDrive™ Gate Drive Output
- Programmable Soft-Start
- Green-Mode Status Pin (PFC Disable Function)

2 Applications

- Bias Supplies for LCD-Monitors, LCD-TV, PDP-TV, and Set Top Boxes
- AC-to-DC Adapters and Off-Line Battery Chargers
- Energy Efficient Power Supplies up to 200 W

3 Description

The UCC28600 is a PWM controller with advanced energy features to meet stringent world-wide energy efficiency requirements.

UCC28600 integrates built-in advanced energy saving features with high-level protection features to provide cost-effective solutions for energy-efficient power supplies. UCC28600 incorporates frequency fold-back and green-mode operation to reduce the switching losses at light-load and no-load conditions.

UCC28600 is available in the 8-pin SOIC package. Operating junction temperature range is –40°C to +105°C.

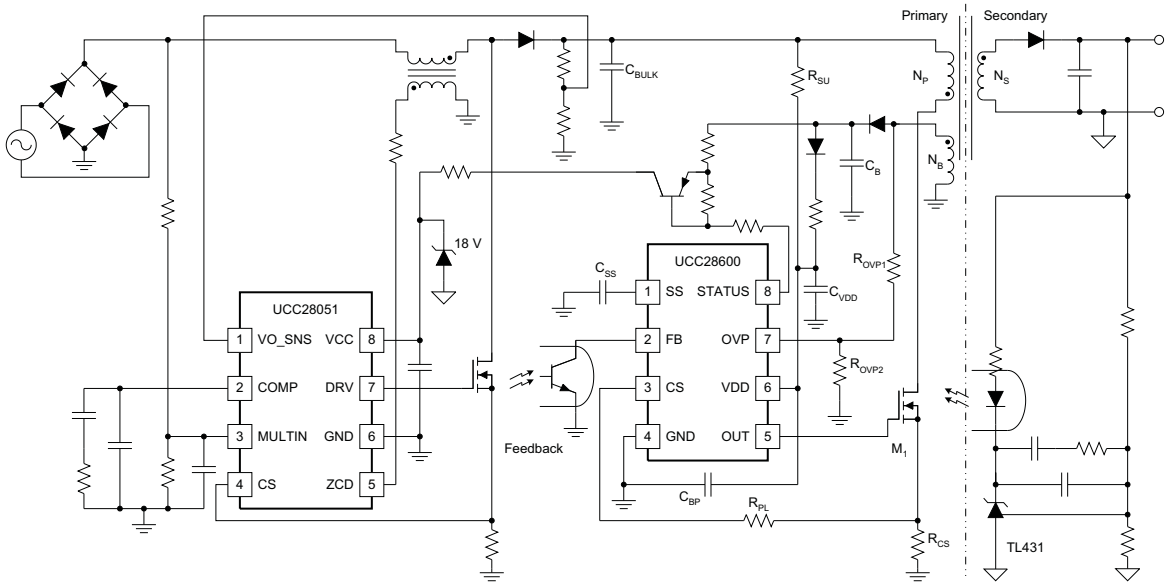
The UCC28600 Design Calculator, (SLVC104), located in the Tools and Software section of the UCC28600 product folder, provides a user-interactive iterative process for selecting recommended component values for an optimal design.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28600	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (July 2011) to Revision K **Page**

- Added Pin Configuration and Functions section, ESD table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Changed Functional Block diagram ... 8
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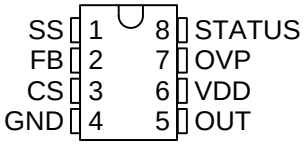
- Changed Equation 35 ... 29

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	3	I	Current sense input. Also programs power limit, and used to control modulation and activate overcurrent protection. The CS voltage input originates across a current sense resistor and ground. Power limit is programmed with an effective series resistance between this pin and the current sense resistor.
FB	2	I	Feedback input or control input from the optocoupler to the PWM comparator used to control the peak current in the power MOSFET. An internal 20-kΩ resistor is between this pin and the internal 5-V regulated voltage. Connect the collector of the photo-transistor of the feedback optocoupler directly to this pin; connect the emitter of the photo-transistor to GND. The voltage of this pin controls the mode of operation in one of the three modes: quasi resonant (QR), frequency foldback mode (FFM) and green mode (GM).
GND	4	–	Ground for internal circuitry. Connect a ceramic 0.1-µF bypass capacitor between VDD and GND, with the capacitor as close to these two pins as possible.
OUT	5	O	1-A sink (TrueDrive™) and 0.75-A source gate drive output. This output drives the power MOSFET and switches between GND and the lower of VDD or the 13-V internal output clamp.
OVP	7	I	Over voltage protection (OVP) input senses line-OVP, load-OVP and the resonant trough for QR turn-on. Detect line, load and resonant conditions using the primary bias winding of the transformer, adjust sensitivity with resistors connected to this pin.
SS	1	I	Soft-start programming pin. Program the soft-start rate with a capacitor to ground; the rate is determined by the capacitance and the internal soft-start charge current. The soft-start capacitor should be placed as close as possible to the SS pin and GND, keeping trace length to a minimum. All faults discharge the SS pin to GND through an internal MOSFET with an $R_{DS(on)}$ of approximately 100 Ω. The internal modulator comparator reacts to the lowest of the SS voltage, the internal FB voltage and the peak current limit.
STATUS	8	O	ACTIVE HIGH open drain signal that indicates the device has entered standby mode. This pin can be used to disable the PFC control circuit (high impedance = green mode). STATUS pin is high during UVLO, (VDD < start-up threshold), and softstart, (SS < FB).
VDD	6	I	Provides power to the device. Use a ceramic 0.1-µF by-pass capacitor for high-frequency filtering of the VDD pin, as described in the GND pin description. Operating energy is usually delivered from auxiliary winding. To prevent hiccup operation during start-up, a larger energy storage cap is also needed between VDD and GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VDD	Supply voltage range, I_{DD} < 20 mA		32	V
I_{DD}	Supply current		20	mA
$I_{OUT(sink)}$	Output sink current (peak)		1.2	A
$I_{OUT(source)}$	Output source current (peak)		–0.8	A
	Analog inputs: FB, CS, SS	–0.3	6.0	V
V_{OVP}		–1.0	6.0	V
$I_{OVP(source)}$			–1.0	mA
V_{STATUS}	VDD = 0 V to 30 V		30	V
	Power dissipation, SOIC-8 package, T_A = 25°C		650	mW
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C
T_J	Operating junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Input voltage			21	V
C_{VDD}	VDD bypass capacitor	0.1	1.0		µF
C_{FB}	FB filter capacitor			390	pF
T_J	Operating junction temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC (1)		UCC28600 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VDD = 15 V, 0.1-µF capacitor from VDD to GND, 3.3-nF capacitor from SS to GND charged over 3.5 V, 500-Ω resistor from OVP to –0.1 V, FB = 4.8 V, STATUS = not connected, 1-nF capacitor from OUT to GND, CS = GND, T_A = –40°C to +105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{STARTUP}$	Start-up current	VDD = V_{UVLO} –0.3 V		12	25	µA
$I_{STANDBY}$	Standby current	V_{FB} = 0 V		350	550	µA
I_{DD}	Operating current	Not switching		2.5	3.5	mA
		130 kHz, QR mode		5.0	7.0	mA
	VDD clamp	FB = GND, I_{DD} = 10 mA	21	26	32	V
UNDERVOLTAGE LOCKOUT						
$VDD_{(uvlo)}$	Start-up threshold	VDD increasing	10.3	13.0	15.3	V
$VDD_{(uvlo)}$	Stop threshold	VDD decreasing	6.3	8	9.3	V
$\Delta VDD_{(uvlo)}$	Hysteresis		4.0	5.0	6.0	V
PWM (RAMP) (1)						
D_{MIN}	Minimum duty cycle	V_{SS} = GND, V_{FB} = 2 V			0%	
D_{MAX}	Maximum duty cycle	QR mode, f_S = max, (open loop)		99%		
OSCILLATOR (OSC)						
$f_{QR(max)}$	Maximum QR and DCM frequency		117	130	143	kHz
$f_{QR(min)}$	Minimum QR and FFM frequency	V_{FB} = 1.3 V	32	40	48	kHz
f_{SS}	Soft start frequency	V_{SS} = 2.0 V	32	40	48	kHz
dT_S/dFB	VCO gain	T_S for 1.6 V < V_{FB} < 1.8 V	–38	–30	–22	µs/V
FEEDBACK (FB)						
R_{FB}	Feedback pullup resistor		12	20	28	kΩ
V_{FB}	FB, no load	QR mode	3.30	4.87	6.00	V
	Green-mode ON threshold	V_{FB} threshold	0.3	0.5	0.7	V
	Green-mode OFF threshold	V_{FB} threshold	1.2	1.4	1.6	V
	Green-mode hysteresis	V_{FB} threshold	0.7	0.9	1.1	V
	FB threshold burst-ON	V_{FB} during green mode	0.3	0.5	0.7	V
	FB threshold burst-OFF	V_{FB} during green mode	0.5	0.7	0.9	V
	Burst Hysteresis	V_{FB} during green mode	0.13	0.25	0.42	V
STATUS						
$R_{DS(on)}$	STATUS on resistance	V_{STATUS} = 1 V	1.0	2.4	3.8	kΩ
$I_{STATUS(leakage)}$	STATUS leakage/off current	V_{FB} = 0.44 V, V_{STATUS} = 15 V	–0.1		2.0	µA

(1) R_{CST} and C_{CST} are not connected in the circuit for maximum and minimum duty cycle tests, current sense tests, and power limit tests.

Electrical Characteristics (continued)

VDD = 15 V, 0.1-µF capacitor from VDD to GND, 3.3-nF capacitor from SS to GND charged over 3.5 V, 500-Ω resistor from OVP to –0.1 V, FB = 4.8 V, STATUS = not connected, 1-nF capacitor from OUT to GND, CS = GND, T_A = –40°C to +105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE (CS) (1)						
$A_{CS(FB)}$	Gain = ΔV_{FB} / ΔV_{CS}	QR mode		2.5		V/V
	Shutdown threshold	V_{FB} = 2.4 V, V_{SS} = 0 V	1.13	1.25	1.38	V
	CS discharge impedance	CS = 0.1 V, V_{SS} = 0 V	25	115	250	Ω
$V_{CS(os)}$	CS offset	SS mode, V_{SS} ≤ 2.0 V	0.35	0.40	0.45	V
POWER LIMIT (PL) (1)						
$I_{PL(cs)}$	CS current	OVP = –300 µA	–165	–150	–135	µA
	Peak CS voltage	QR mode	0.70	0.81	0.92	V
V_{PL}	PL threshold	Peak CS voltage + CS offset	1.05	1.20	1.37	V
SOFT START (SS)						
$I_{SS(chg)}$	Softstart charge current	V_{SS} = GND	–8.3	–6.0	–4.5	µA
$I_{SS(dis)}$	Softstart discharge current	V_{SS} = 0.5 V	2.0	5.0	10	mA
V_{SS}	Switching ON threshold	Output switching start	0.8	1.0	1.2	V
OVERVOLTAGE PROTECTION (OVP)						
$I_{OVP(line)}$	Line overvoltage protection	I_{OVP} threshold, OUT = HI	–512	–450	–370	µA
$V_{OVP(on)}$	OVP voltage at OUT = HIGH	V_{FB} = 4.8 V, V_{SS} = 5.0 V, $I_{OVP(on)}$, = –300 µA	–125		–25	mV
$V_{OVP(load)}$	Load overvoltage protection	V_{OVP} threshold, OUT = LO	3.37	3.75	4.13	V
THERMAL PROTECTION (TSP)						
	Thermal shutdown (TSP) temperature (2)		130	140	150	°C
	Thermal shutdown hysteresis			15		°C

(2) Ensured by design. Not production tested.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
CURRENT SENSE (CS) (1)					
	CS to output delay time (power limit), CS = 1.0 V_{PULSE}	100	175	300	ns
	CS to output delay time (over current fault), CS = 1.45 V_{PULSE}	50	100	150	ns
OUT					
t_{RISE}	Rise time, 10% to 90% of 13-V typical OUT clamp		50	75	ns
t_{FALL}	Fall time		10	20	ns

(1) R_{CST} and C_{CST} are not connected in the circuit for maximum and minimum duty cycle tests, current sense tests, and power limit tests.

6.7 Typical Characteristics

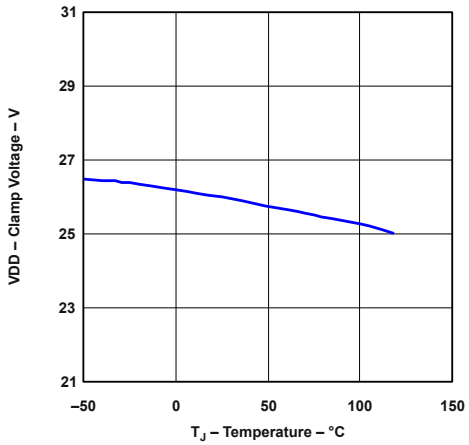


Figure 1. Clamp Voltage vs. Temperature

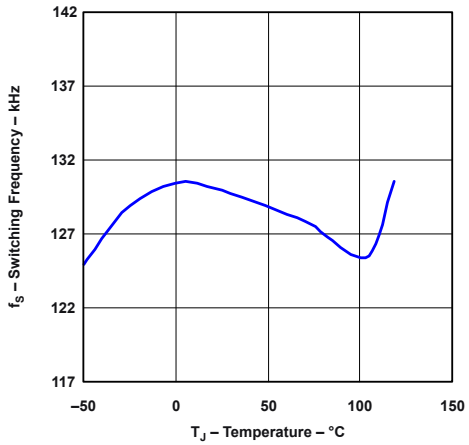


Figure 2. Switching Frequency vs. Temperature

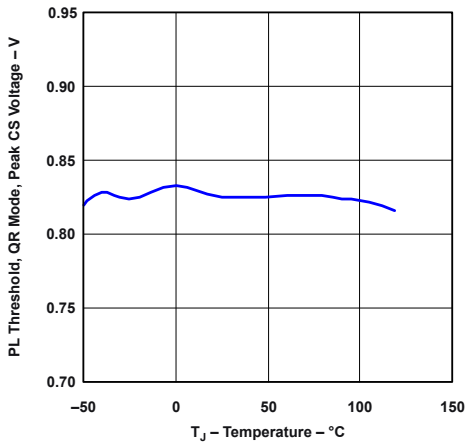


Figure 3. PL Threshold vs. Temperature

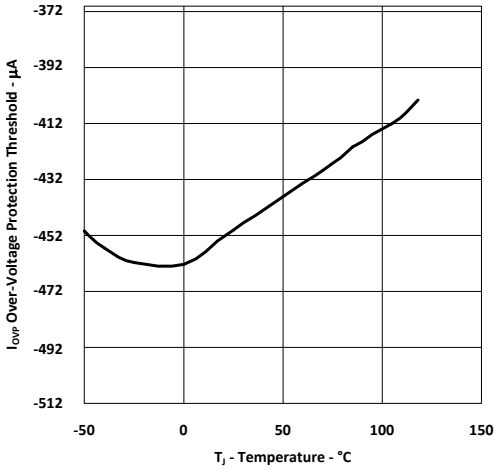


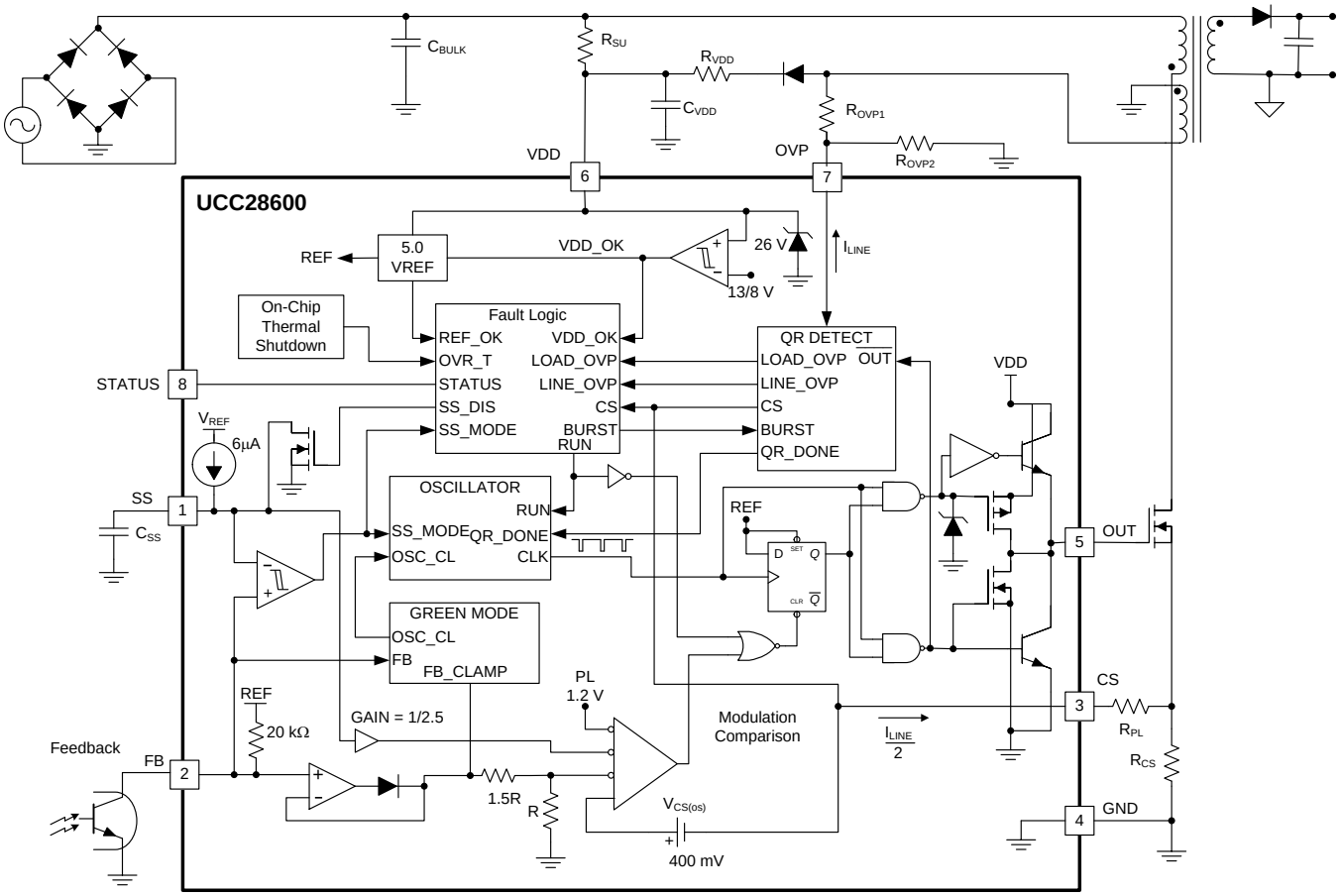
Figure 4. Over-Voltage Protection Threshold vs. Temperature

7 Detailed Description

7.1 Overview

The UCC28600 is a flyback power supply controller that operates in different operating modes, modulating the peak primary current and/or the switching frequency, depending upon the line and load conditions. The controller will operate in burst mode operation, or green mode (GM) driving the primary side MOSFET with packets of 40-kHz pulses, at fixed peak primary current for light-load conditions. As the load increases, the 40-kHz switching will become consistent and the controller will transition to frequency fold-back mode (FFM), where the peak primary current is held constant and the switching frequency is modulated from 40 kHz up to 130 kHz, in order to maintain regulation. At higher loads, the UCC28600 will operate in either DCM, where the peak primary current is modulated but the switching frequency is maintained at its maximum value, or quasi-resonant mode (QRM), where the switching frequency and the peak primary current are both modulated in order to maintain regulation.

7.2 Functional Block Diagram



Functional Block Diagram (continued)

7.2.1 Terminal Components

Table 1. Terminal Components

PIN		I/O	DESCRIPTION (1) (2)
NAME	NO.		
CS	3	I	$R_{CS} = \frac{\left(V_{PL} - V_{CS(os)}\left(I_{CS(2)} - I_{CS(1)}\right)\right)}{I_{CS(2)} - I_{P(1)} - I_{CS(1)} - I_{P(2)}}$ (1) $R_{PL} = \frac{\left(V_{PL} - V_{CS(os)}\left(I_{P(2)} - I_{P(1)}\right)\right)}{I_{CS(1)} - I_{P(2)} - I_{CS(2)} - I_{P(1)}}$ (2) where: • $I_{P(1)}$ is the peak primary current at low line, full load (2) • $I_{P(2)}$ is the peak primary current at high line, full load (2) • $I_{CS(1)}$ is the power limit current that is sourced at the CS pin at low-line voltage (2) • $I_{CS(2)}$ is the power limit current that is sourced at the CS pin at high-line voltage (2) • V_{PL} is the Power Limit (PL) threshold (1) • $V_{CS(os)}$ is the CS offset voltage (1)
FB	2	I	Opto-isolator collector
GND	4	–	Bypass capacitor to VDD, C_{BP} = 0.1 µF
OUT	5	O	Power MOSFET gate
OVP	7	I	$R_{OVP1} = \frac{1}{I_{OVP(line)}}\left(\frac{N_B}{N_P} V_{BULK(ov)}\right)$ (3) $R_{OVP2} = R_{OVP1}\left(\frac{V_{OVP(line)}}{\frac{N_B}{N_P}\left(V_{OUT(shutdown)} + V_F\right) - V_{OVP(load)}}\right)$ (4) where: • $I_{OVP(line)}$ is OVP_{line} current threshold (1) • $V_{BULK(ov)}$ is the allowed input over- voltage level (2) • $V_{OVP(load)}$ is OVP_{load} (1) • $V_{OUT(shutdown)}$ is the allowed output over-voltage level (2) • V_F is the forward voltage of the secondary rectifier • N_B is the number of turns on the bias winding (2) • N_S is the number of turns on the secondary windings (2) • N_P is the number of turns on the primary windings (2)
SS	1	I	$C_{SS} > I_{SS} \times \frac{t_{SS(min)}\left(\text{due power limit}\right)}{A_{CS(FB)} \times \left(V_{PL} - V_{CS(os)}\right)}$ (5) where $t_{SS(min)}$ is the greater of: $t_{SS(min)} = \left[\frac{-R_{LOAD(ss)} C_{OUT}}{2} ln \frac{V_{OUT} - \Delta V_{OUT(step)}}{R_{LOAD(ss)} P_{OUT(max)limit}}\right]$ (6) or $t_{SS(min)} = \left[\frac{C_{OUT} V_{OUT}^2}{2 P_{LIM}}\right]$ (7) • $R_{LOAD(ss)}$ is the effective load impedance during soft-start (2) • $\Delta V_{OUT(step)}$ is the allowed change in V_{OUT} due to a load step (2) • $P_{OUT(max\ limit)}$ Programmed power limit level, in W (2) • $A_{CS(FB)}$ is the current sense gain (1) • $V_{CS(os)}$ is the CS offset voltage (1) • I_{SS} is the soft-start charging current (1) • V_{PL} is the power limit threshold (1)

(1) Refer to the *Electrical Characteristics* for constant parameters.
(2) Refer to the UCC28600 Design Calculator (SLVC104) or laboratory measurements for currents, voltages and times in the operational circuit.

Functional Block Diagram (continued)

Table 1. Terminal Components (continued)

PIN		I/O	DESCRIPTION (1) (2)
NAME	NO.		
STATUS	8	O	$R_{ST2} = \frac{V_{BE(off)}}{I_{STATUS(leakage)}}$ (8) $R_{ST1} = \frac{R_{ST2} \times \left[VDD_{(uvlo-on)} - V_{BE(sat)} - R_{DS(on)} \times \left(\frac{I_{CC}}{\beta_{sat}} \right) \right] - R_{DS(on)} V_{BE(sat)}}{\left(\left(\frac{I_{CC}}{\beta_{sat}} \right) \times R_{ST2} \right) + V_{BE(sat)}}$ (9) where: • β_{SAT} is the gain of transistor Q_{ST} in saturation • $V_{BE(sat)}$ is the base-emitter voltage of transistor Q_{ST} in saturation • $VDD_{(uvlo-on)}$ is the start-up threshold (1) • I_{CC} is the collector current of Q_{ST} • $I_{STATUS(leakage)}$ is the maximum leakage/off current of the STATUS pin (1) • $V_{BE(off)}$ is the maximum allowable voltage across the base emitter junction that will not turn Q_{ST} on • $R_{DS(on)}$ is the $R_{DS(on)}$ of STATUS (1)
VDD	6	I	C_{VDD} is the greater of: $C_{VDD} = \left[\left(I_{DD} + C_{ISS} V_{OUT(hi)} f_{QR(max)} \right) \frac{T_{BURST}}{\Delta V_{DD(burst)}} \right]$ (10) or $C_{VDD} = \left[\left(I_{DD} + C_{ISS} V_{OUT(hi)} f_{QR(max)} \right) \frac{T_{SS}}{\Delta V_{DD(uvlo)}} \right]$ (11) $R_{VDD} = \left(\frac{\pi}{4} \right) \left(\frac{N_B}{N_P} \right) \left(\frac{V_{DS1(os)} f_{QR(max)} \sqrt{L_{LEAKAGE} (C_D + C_{SNUB})}}{IDD + C_{ISS} V_{OUT(hi)} f_{QR(max)}} \right)$ (12) $R_{SU} = \frac{V_{BULK(min)}}{I_{STARTUP}}$ (13) where: • I_{DD} is the operating current of the UCC28600 (1) • C_{ISS} is the input capacitance of MOSFET M_1 • $V_{OUT(hi)}$ is VOH of the OUT pin, either 13 V (typ) V_{OUT} clamp or less as measured • $f_{QR(max)}$ is f_S at high line, maximum load (1) • T_{BURST} is the measured burst mode period • $\Delta VDD_{(burst)}$ is the allowed V_{DD} ripple during burst mode • $\Delta VDD_{(uvlo)}$ is the UVLO hysteresis (1) • $V_{DS1(os)}$ is the amount of drain-source overshoot voltage • $L_{LEAKAGE}$ is the leakage inductance of the primary winding • C_D is the total drain node capacitance of MOSFET M_1 • $I_{STARTUP}$ is I_{DD} start-up current of the UCC28600 (1) • C_{SNUB} is the snubber capacitor value • t_{SS} is the soft start charge time (2)

7.3 Feature Description

The UCC28600 is a multi-mode controller, as illustrated in Figure 5 and Figure 12. The mode of operation depends upon line and load conditions. Under all modes of operation, the UCC28600 terminates the OUT = HI signal based on the switch current. Thus, the UCC28600 always operates in current mode control so that the power MOSFET current is always limited.

Under normal operating conditions, the FB pin commands the operating mode of the UCC28600 at the voltage thresholds shown in the control flow chart, Figure 11. Soft-start and fault responses are the exception. During soft start, the converter switching frequency is fixed at 40 kHz and FB is set to 5V. The soft-start mode is latched-OFF when V_{SS} becomes greater than V_{FB} for the first time after $UVLO_{ON}$. The soft-start state cannot be recovered until after passing $UVLO_{OFF}$, and then, $UVLO_{ON}$.

From 100% to approximately 30% full rated power the UCC28600 controls the converter in quasi-resonant mode (QRM) or discontinuous conduction mode (DCM), where DCM operation is at the clamped maximum switching frequency (130 kHz). For loads that are between approximately 30% and 10% full rated power, the converter operates in frequency foldback mode (FFM), where the peak switch current is constant and the output voltage is regulated by modulating the switching frequency for a given and fixed V_{IN}. Effectively, operation in FFM results in the application of constant volt-seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 130 kHz to 40 kHz. For extremely light loads (below approximately 10% full rated power), the converter is controlled using bursts of 40-kHz pulses.

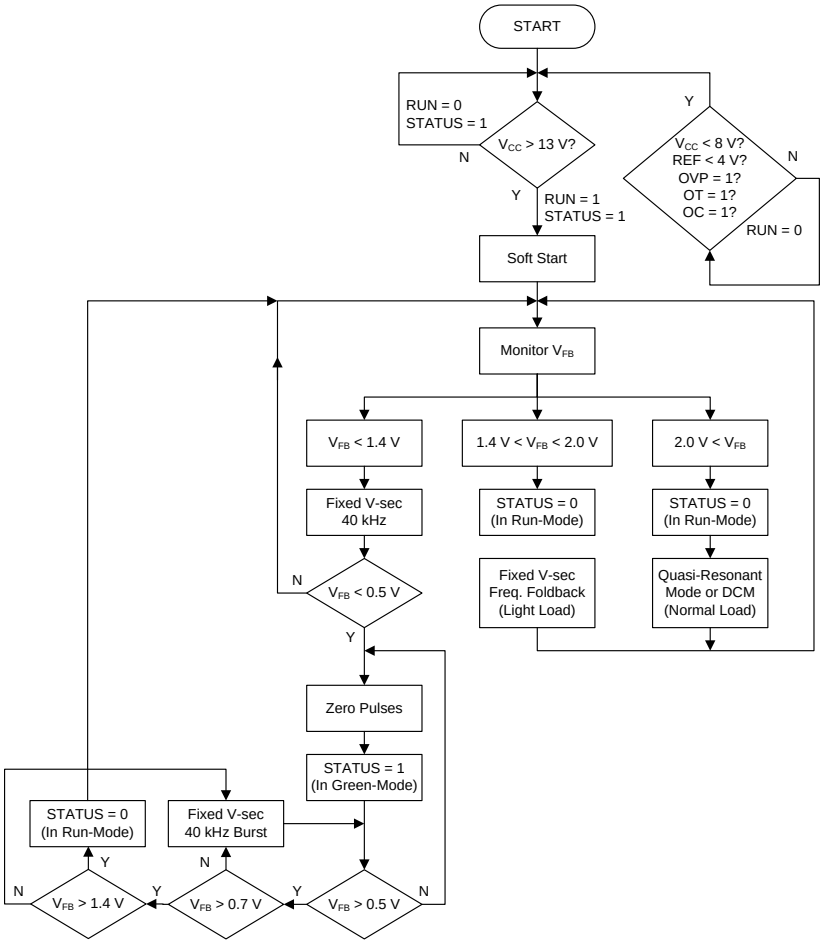


Figure 5. Control Flow Chart

Feature Description (continued)

Details of the functional boxes in the Block Diagram/Typical Application drawing are shown in Figure 8, Figure 6, Figure 7 and Figure 10. These figures conceptualize how the UCC28600 executes the command of the FB voltage to have the responses that are shown in Figure 11, Figure 5 and Figure 12. The details of the functional boxes also conceptualize the various fault detections and responses that are included in the UCC28600. During all modes of operation, this controller operates in current mode control. This allows the UCC28600 to monitor the FB voltage to determine and respond to the varying load levels such as heavy, light or ultra-light.

Quasi-resonant mode and DCM occurs for feedback voltages V_{FB} between 2.0 V and 4.0 V, respectively. In turn, the CS voltage is commanded to be between 0.4 V and 0.8 V. A cycle-by-cycle power limit imposes a fixed 0.8-V limit on the CS voltage. An overcurrent shutdown threshold in the fault logic gives added protection against high-current, slew-rate shorted winding faults, shown in Figure 10. The power limit feature in the QR DETECT circuit of Figure 7 adds an offset to the CS signal that is proportional to the line voltage. The power limit feature is programmed with R_{PL}, as shown in the *Typical Application Diagram*.

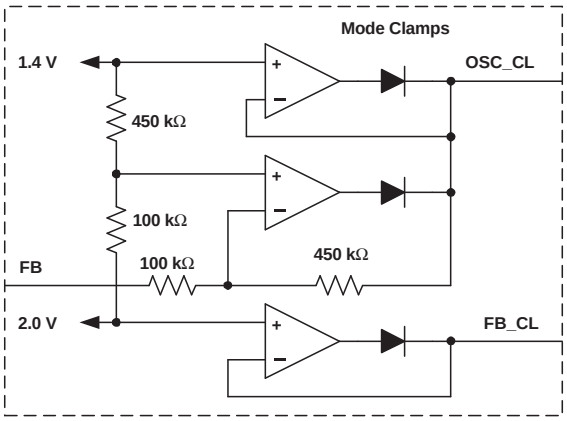


Figure 6. Mode Clamp Details

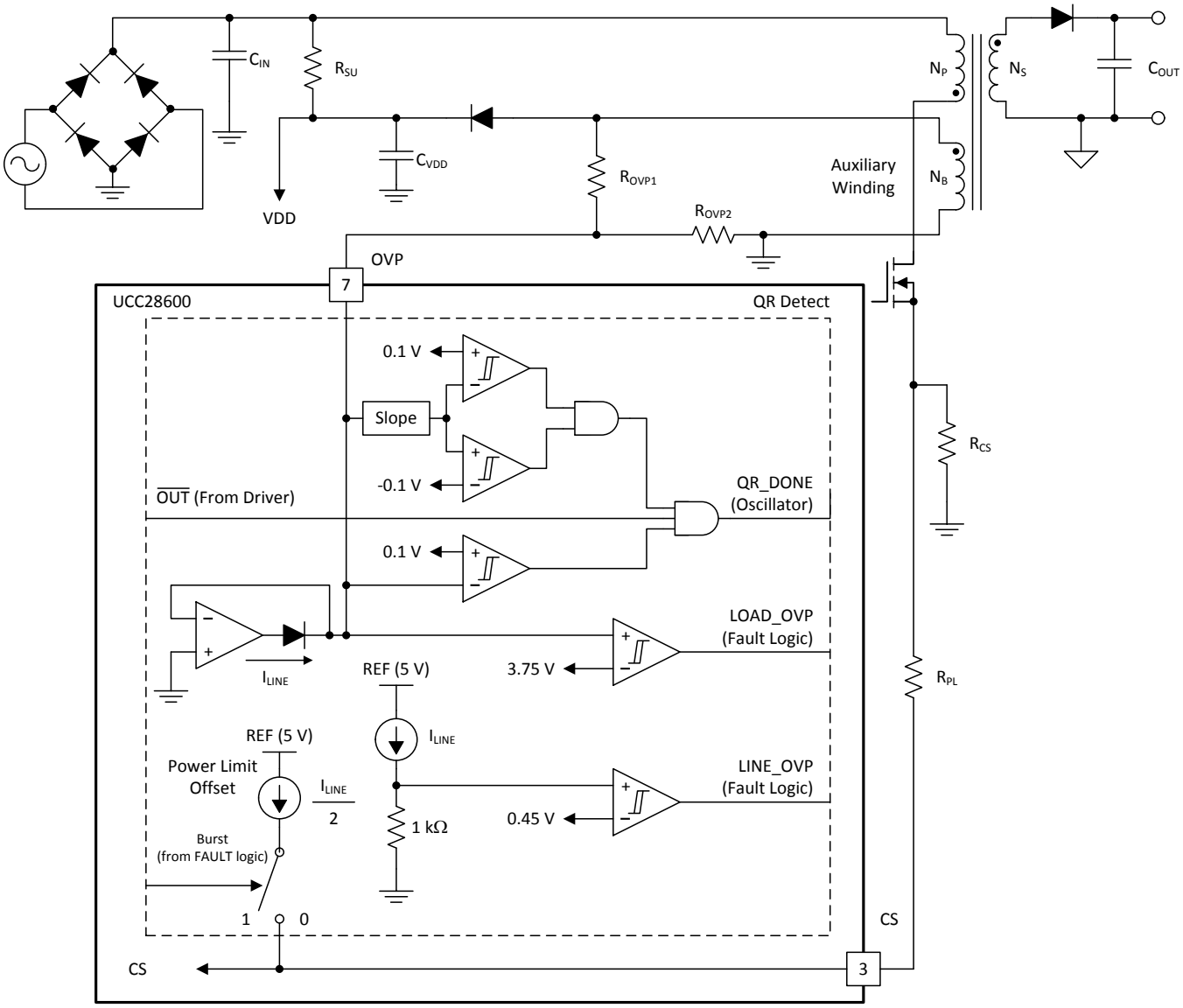


Figure 7. QR Detect Details

7.3.1 Oscillator

The oscillator, shown in Figure 8, is internally set and trimmed so it is clamped by the circuit in Figure 8 to a nominal 130-kHz maximum operating frequency. It also has a minimum frequency clamp of 40 kHz. If the FB voltage tries to drive operation to less than 40 kHz, the converter operates in green mode.

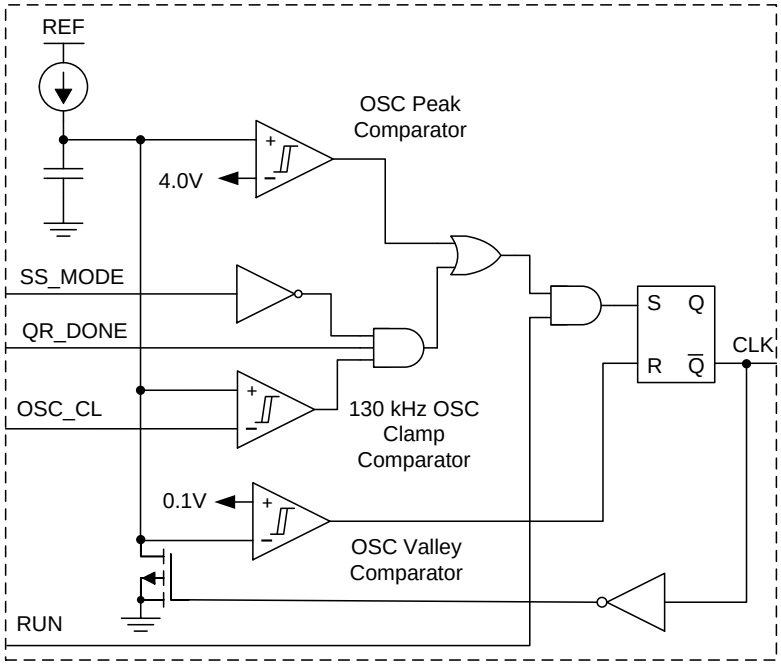


Figure 8. Oscillator Details

7.3.2 Status

The STATUS pin is an open drain output, as shown in Figure 10. The status output goes into the OFF-state when FB falls below 0.5 V and it returns to the ON-state (low impedance to GND) when FB rises above 1.4 V. This pin is used to control bias power for a PFC stage, as shown in Figure 9. Key elements for implementing this function include Q1, R_{ST1} and R_{ST2}, as shown in Figure 9. Resistors R_{ST1} and R_{ST2} are selected to saturate Q1 when it is desirable for the PFC to be operational. During green mode, the STATUS pin becomes a high impedance and R_{ST2} causes Q1 to turn-OFF, thus saving bias power. If necessary, use a Zener diode and a resistor (D_{Z1} and R_{VCC}) to maintain VCC in the safe operating range of the PFC controller.

NOTE

The D_{VDD} – C_{VDD} combination is in addition to the standard D_{BIAS} – C_{BIAS} components.

This added stage is required to isolate the STATUS circuitry from the start-up resistor, R_{SU}, to ensure there is no conduction through STATUS when VDD is below the UVLO turn-on threshold.

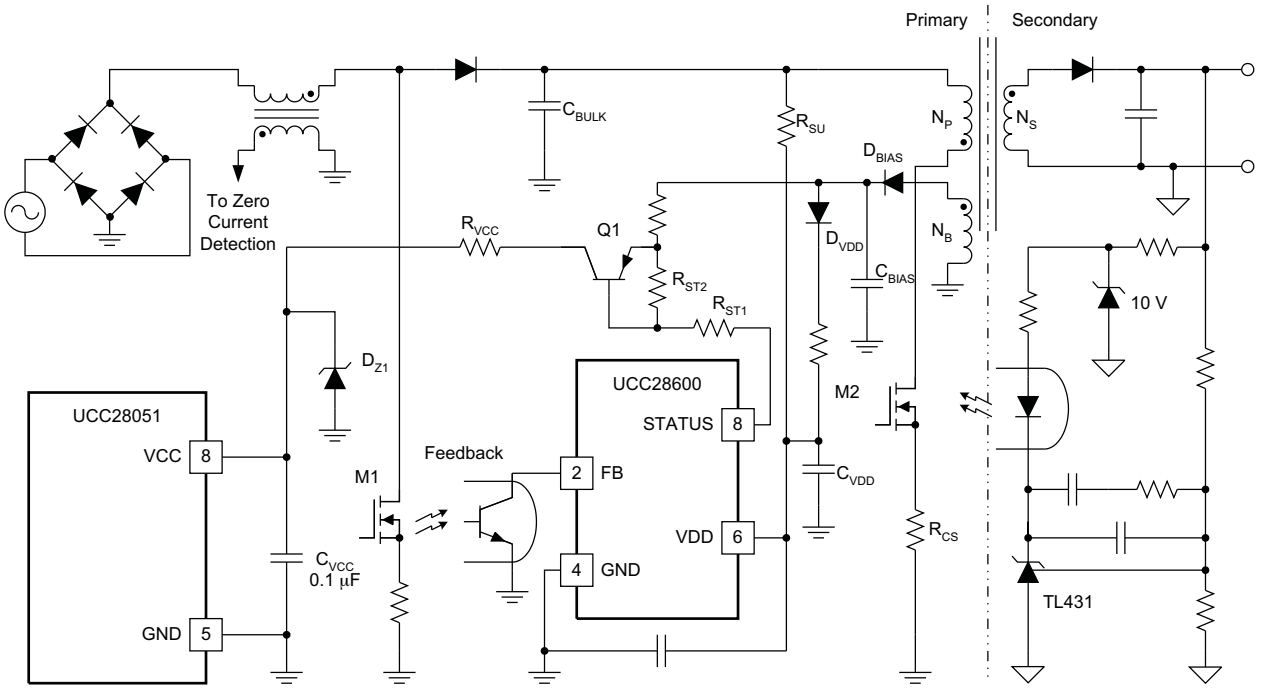


Figure 9. Using STATUS for PFC Shut-Down During Green Mode

7.3.3 Fault Logic

Advanced logic control coordinates the fault detections to provide proper power supply recovery. This provides the conditioning for the thermal protection. Line overvoltage protection (line OVP) and load OVP are implemented in this block. It prevents operation when the internal reference is below 4.5 V. If a fault is detected in the thermal shutdown, line OVP, load OVP, or REF, the UCC28600 undergoes a shutdown/retry cycle.

Refer to the fault logic diagram in Figure 10 and the QR detect diagram in Figure 7 to program line OVP and load OVP. To program the load OVP, select the R_{OVP1} – R_{OVP2} divider ratio to be 3.75 V at the desired output shut-down voltage. To program line OVP, select the impedance of the R_{OVP1} – R_{OVP2} combination to draw 450 µA when the V_{OVP} is 0.45 V during the ON-time of the power MOSFET at the highest allowable input voltage.

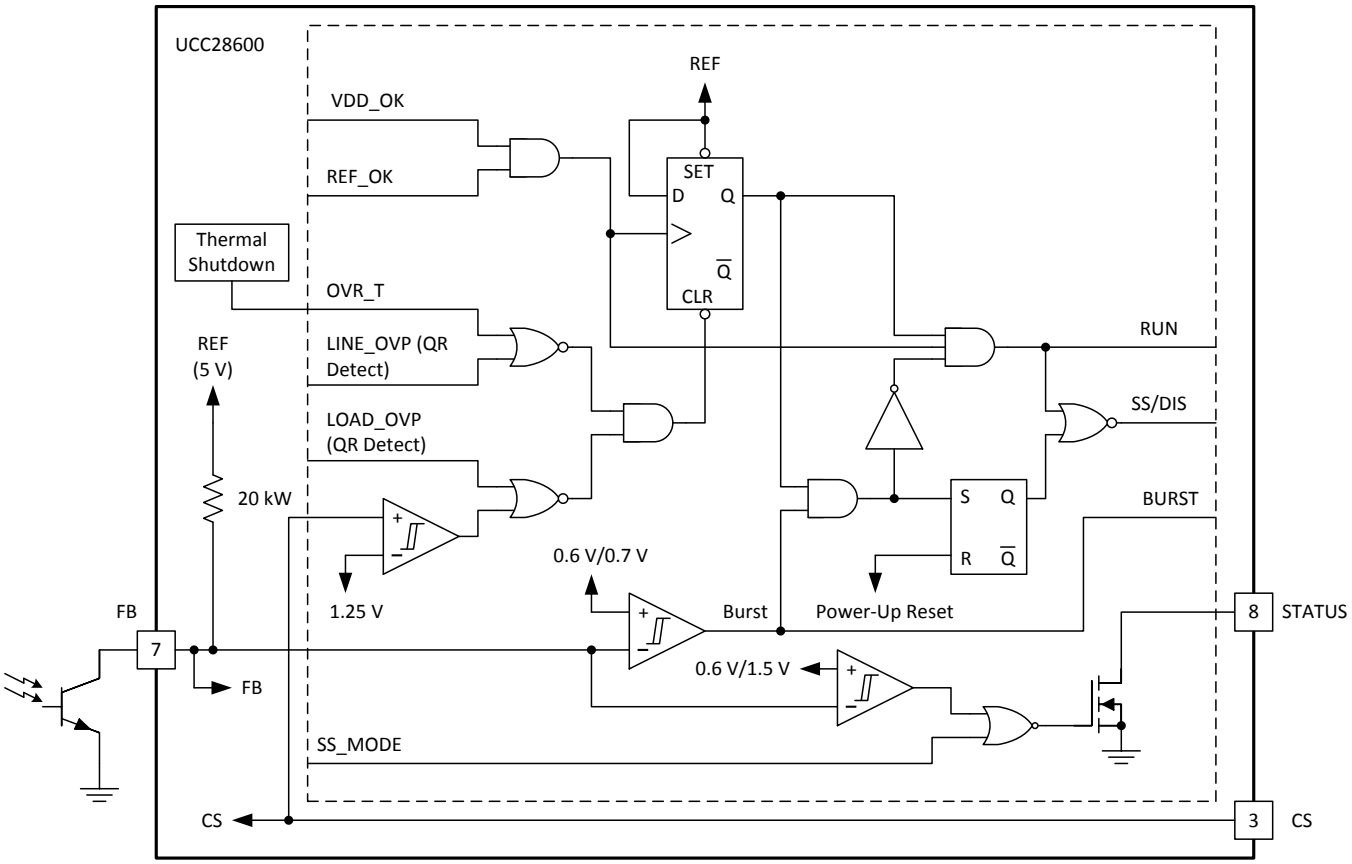


Figure 10. Fault Logic Details

7.3.4 Protection Features

The UCC28600 has many protection features that are found only on larger, full featured controllers. Refer to the *Functional Block Diagram*, *Typical Application Diagram*, Figure 6, Figure 7, Figure 8, Figure 10, Figure 11, and Figure 12 for detailed block descriptions that show how the features are integrated into the normal control functions.

7.3.5 Overtemperature

Overtemperature lockout typically occurs when the substrate temperature reaches 140°C. Retry is allowed if the substrate temperature reduces by the hysteresis value. Upon an overtemperature fault, C_{SS} on softstart is discharged and STATUS is forced to a high impedance.

7.3.6 Cycle-by-Cycle Power Limit

The cycle terminates when the CS voltage plus the power limit offset exceeds 1.2 V.

In order to have power limited over the full line voltage range of the QR Flyback converter, the CS pin voltage must have a component that is proportional to the primary current plus a component that is proportional to the line voltage due to predictable switching frequency variations due to line voltage. At power limit, the CS pin voltage plus the internal CS offset is compared against a constant 1.2-V reference in the PWM comparator. Thus during cycle-by-cycle power limit, the peak CS voltage is typically 0.8 V.

The current that is sourced from the OVP pin (I_{LINE}) is reflected to a dependent current source of ½ I_{LINE}, that is connected to the CS pin. The power limit function can be programmed by a resistor, R_{PL}, that is between the CS pin and the current sense resistor. The current, I_{LINE}, is proportional to line voltage by the transformer turns ratio N_B/N_P and resistor R_{OVP1}. Current I_{LINE} is programmed to set the line over voltage protection. Resistor R_{PL} results in the addition of a voltage to the current sense signal that is proportional to the line voltage. The proper amount of additional voltage has the effect of limiting the power on a cycle-by-cycle basis. Note that R_{CS}, R_{PL}, R_{OVP1} and R_{OVP2} must be adjusted as a set due to the functional interactions.

7.3.7 Primary Current Protection

When the primary current exceeds maximum current level which is indicated by a voltage of 1.25 V at the CS pin, the device initiates a shutdown. Retry occurs after a $UVLO_{OFF}$ or $UVLO_{ON}$ cycle. Because the device will initiate cycle-by-cycle power limit first, primary side current protection is not intended to protect against output short circuit conditions. However, this feature does protect the MOSFET against extreme conditions such as transformer saturation.

7.3.8 Over-Voltage Protection

Line and load over voltage protection is programmed with the transformer turn ratios, R_{OVP1} and R_{OVP2}. The OVP pin has a 0-V voltage source that can only source current; OVP cannot sink current.

Line over voltage protection occurs when the OVP pin is clamped at 0 V. When the bias winding is negative, during OUT = HI or portions of the resonant ring, the 0-V voltage source clamps OVP to 0 V and the current that is sourced from the OVP pin is mirrored to the Line_OVP comparator and the QR detection circuit. The Line_OVP comparator initiates a shutdown-retry sequence if OVP sources any more than 450 µA.

Load-over voltage protection occurs when the OVP pin voltage is positive. When the bias winding is positive, during demagnetization or portions of the resonant ring, the OVP pin voltage is positive. If the OVP voltage is greater than 3.75 V, the device initiates a shutdown. Retry occurs after a $UVLO_{OFF}$ or $UVLO_{ON}$ cycle.

7.3.9 Undervoltage Lockout

Protection is provided to guard against operation during unfavorable bias conditions. Undervoltage lockout (UVLO) always monitors VDD to prevent operation below the UVLO threshold.

7.4 Device Functional Modes

Depending upon the line and load conditions, the UCC28600 controls the converter using different modes of operation, which are defined as quasi-resonant (QR mode), discontinuous conduction mode (DCM), frequency foldback mode (FFM) and green mode (GM), determined by the voltage on the FB pin, as shown in Figure 11.

For extremely light loads (below approximately 10% full rated power), the converter is controlled using bursts of 40-kHz pulses. As the load increases, the number of pulses in these burst packets increases until the converter is switching consistently at 40 kHz, at which point it transitions into the next operating mode, called frequency foldback. Frequency foldback mode (FFM) typically begins at loads that are between approximately 10% and up to 30% full rated power, the peak primary side switch current is constant and the output voltage is regulated by modulating the switching frequency from 40 kHz up to 130 kHz. From approximately 30% to 100% full rated power, the UCC28600 controls the converter in either quasi-resonant mode (QRM) or discontinuous conduction mode (DCM). In QRM, the switching frequency will decrease as the load increases; DCM operation is at the clamped maximum switching frequency (130 kHz). The valley detection circuitry is active during FFM, DCM, and QRM operation.

Keep in mind that the aforementioned boundaries of steady-state operation are approximate because they are subject to converter design parameters.

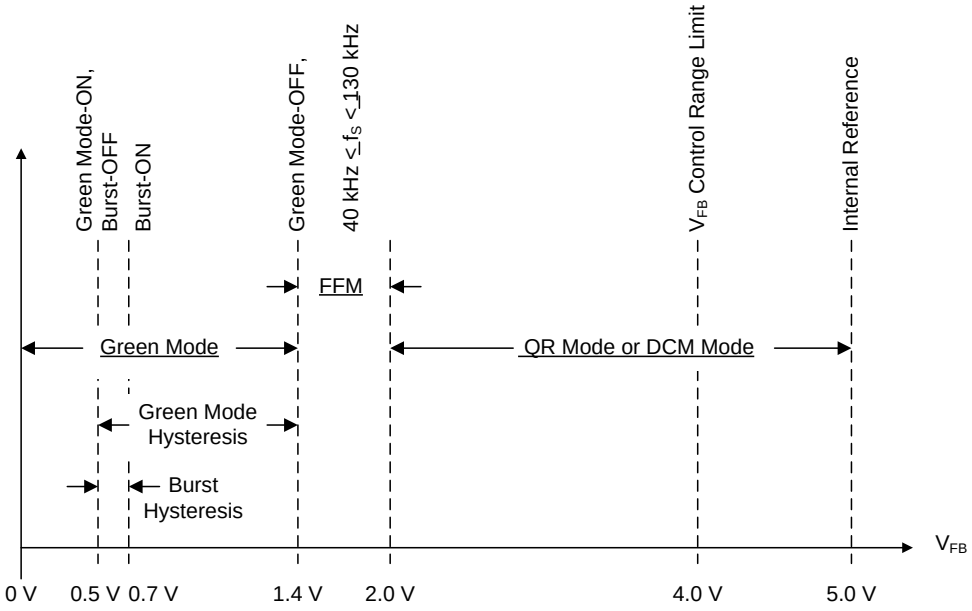


Figure 11. Mode Control with FB Pin Voltage

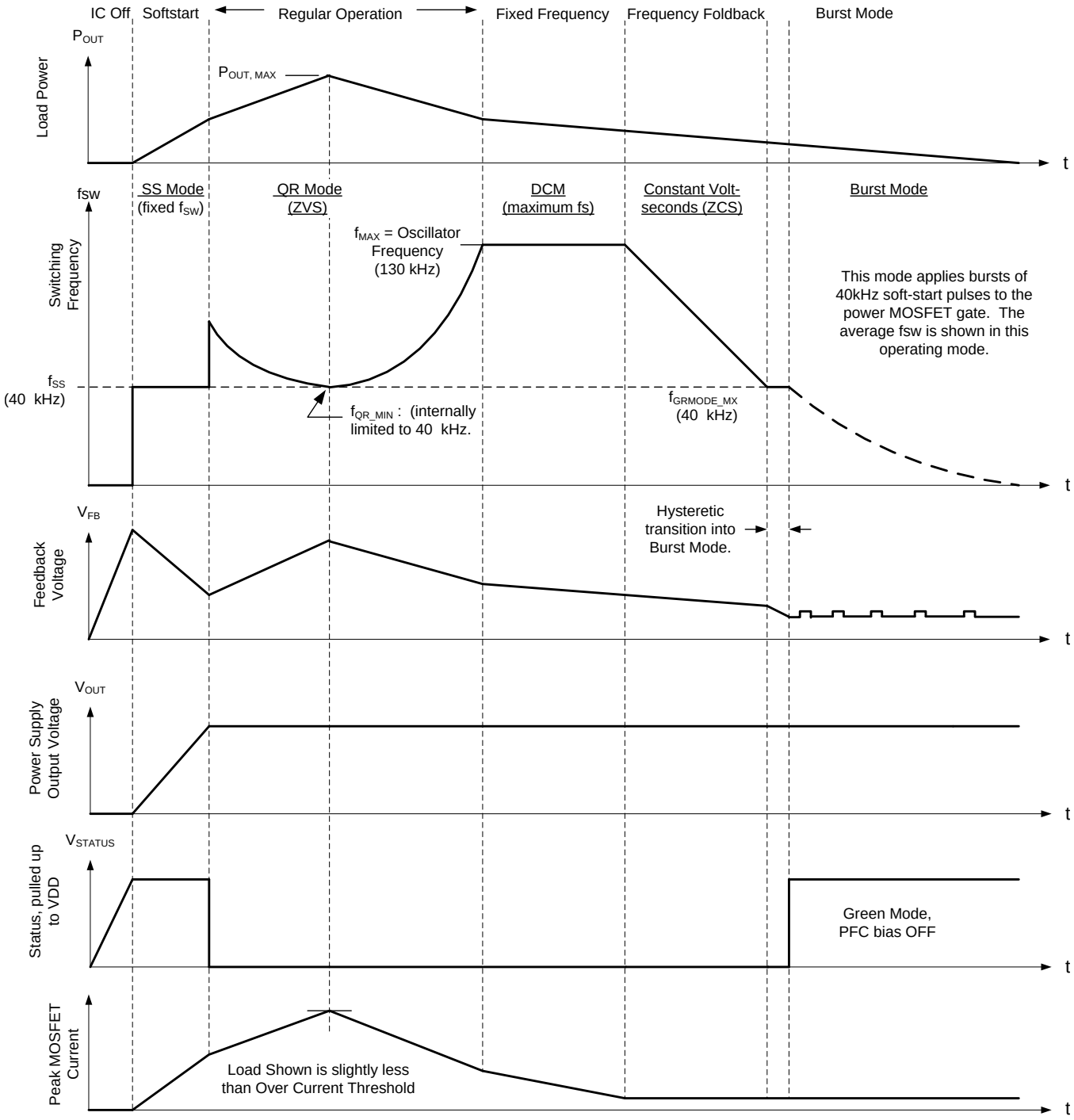


Figure 12. Operation Mode Switching Frequencies

7.4.1 Quasi-Resonant and DCM Control

During this control mode, the rising edge of OUT will occur just after the valley of the resonant ring when the transformer is fully demagnetized. Resonant valley switching is an integral part of QR operation. In this mode, the flyback converter operates at the boundary of discontinuous conduction mode and continuous conduction mode. By adjusting both the peak current and the switching frequency, the output power is adjusted to match the load requirement. When the load increases, the peak current increases and the switching frequency decreases. The minimum switching frequency of the converter is limited to 40 kHz. The transformer magnetizing inductor value has to be designed accordingly so that the converter can deliver the maximum required power while maintaining a switching frequency that is greater than the $f_{QR(min)}$ over the entire input operating range.

As the load decreases from its designed maximum output power, the UCC28600 will demand a higher switching frequency and decreased peak current. The converter's maximum switching frequency will be limited to 130 kHz. At this maximum switching frequency, the converter enters DCM control. At DCM control, the peak current is adjusted to control the output power. Slight frequency dithering between resonant valleys will occur as the valley detection is active in DCM control.

Quasi-resonant (QR) and DCM operation occur for feedback voltages, V_{FB}, between 2.0 V and 3.0 V. In turn, the peak CS voltage is commanded to be between 0.4 V and 0.8 V. The CS pin has an internal dependent current source, 1/2 I_{LINE}. This current source adds a proportional step offset (power limit offset) to the CS signal and is part of the cycle-by-cycle power limit function that is discussed in the *Protection Features* section.

7.4.2 Frequency Foldback Mode Control

Operation in FFM results in the application of constant volt-seconds to the flyback transformer during each switching cycle. During frequency foldback mode, as the load decreases, the MOSFET peak current is kept constant and the switching frequency is reduced (foldback) to reduce the output power. In this mode, the flyback converter will always operate in discontinuous conduction mode. When the FB voltage is between 1.4 V and 2.0 V, the voltage controlled oscillator restricts the operating frequency between 40 kHz and 130 kHz and the CS is clamped to 0.4 V, including the power limit offset. Valley detection is active during FFM.

7.4.3 Green-Mode Control

During green mode, the converter operates at a fixed switching frequency of 40 kHz and fixed peak current. The output power is adjusted by the converter ON/OFF durations, which is also known as burst mode. When the FB voltage is between 1.4 V and 0.5 V, the controller is commanding an excess of energy to be transferred to the load which in turn, drives the error higher and FB lower. When FB reaches 0.5 V, the OUT pulses are terminated and do not resume until FB reaches 0.7 V. In this mode, the converter operates in hysteretic control with the OUT pulse terminated at a fixed CS voltage level of 0.4 V. The power limit offset is turned OFF during Green mode and it returns to ON when FB is above 1.4 V. Green mode reduces the average switching frequency in order to minimize switching losses and increase the efficiency at light-load conditions.

7.4.4 Operating Mode Programming

Boundaries of the operating modes are programmed by the flyback transformer and the four components R_{PL}, R_{CS}, R_{OVP1} and R_{OVP2}; shown in the *Functional Block Diagram* and *Typical Application Diagram* drawing.

The transformer characteristics that predominantly affect the modes are the magnetizing inductance of the primary and the magnitude of the output voltage, reflected to the primary. To a lesser degree (yet significant), the boundaries are affected by the MOSFET output capacitance and transformer leakage inductance. The design procedure here is to select a magnetizing inductance and a reflected output voltage that operates at the DCM/CCM boundary at maximum load and maximum line. The actual inductance should be noticeably smaller to account for the ring between the magnetizing inductance and the total stray capacitance measured at the drain of the power MOSFET. This programs the QR/DCM boundary of operation. All other mode boundaries are preset with the thresholds in the oscillator and green-mode blocks.

The four components R_{PL}, R_{CS}, R_{OVP1} and R_{OVP2} must be programmed as a set due to the interactions of the functions. The use of the UCC28600 design calculator, SLVC104, is highly recommended in order to achieve the desired results with a careful balance between the transformer parameters and the programming resistors.

8 Application and Implementation

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28600 device is a flyback controller that operates in a mode that is determined by the FB voltage. Line and load conditions set the FB voltage and the controller will operate in Green Mode (GM) under light-load conditions, Frequency Foldback Mode (FFM) when operating at loads approximately between 10% and 30% full rated load, and Quasi-Resonant (QR) or Discontinuous Mode (DCM) at higher loads. Valley switching under all modes, except green mode, reduces switching losses and improves efficiency. Valley skipping also helps reduce EMI. A dedicated STATUS pin is used in higher power applications that use a power factor corrected (PFC) front end. Under light-load conditions, the STATUS signal can be used to disconnect the bias power to the PFC controller, reducing light-load power consumption.

8.2 Typical Application

A typical application for the UCC28600 is an off-line flyback controller from 65 W to 120 W, using a PFC output voltage as its input, as shown in Figure 13. The PFC stage is assumed to operate from a universal AC input and can be controlled by a device such as the UCC28051. The auxiliary winding provides the bias to the controllers and provides over voltage protection and valley switching information, as well as bias to the UCC28600 and UCC28051. The UCC28600 will disable the PFC controller during green mode operation, improving light-load system efficiency. The series resistor connected between the current sense pin and the current sense resistor programs the power limit of the converter. Low valley voltage switching and multi-mode operation will keep the efficiency curve high over the entire operation range. Typical applications include bias supplies for LCD monitors, LCD and PDP televisions, set top boxes, AC-DC adaptors, and energy efficient power supplies up to 200 W.

Typical Application (continued)

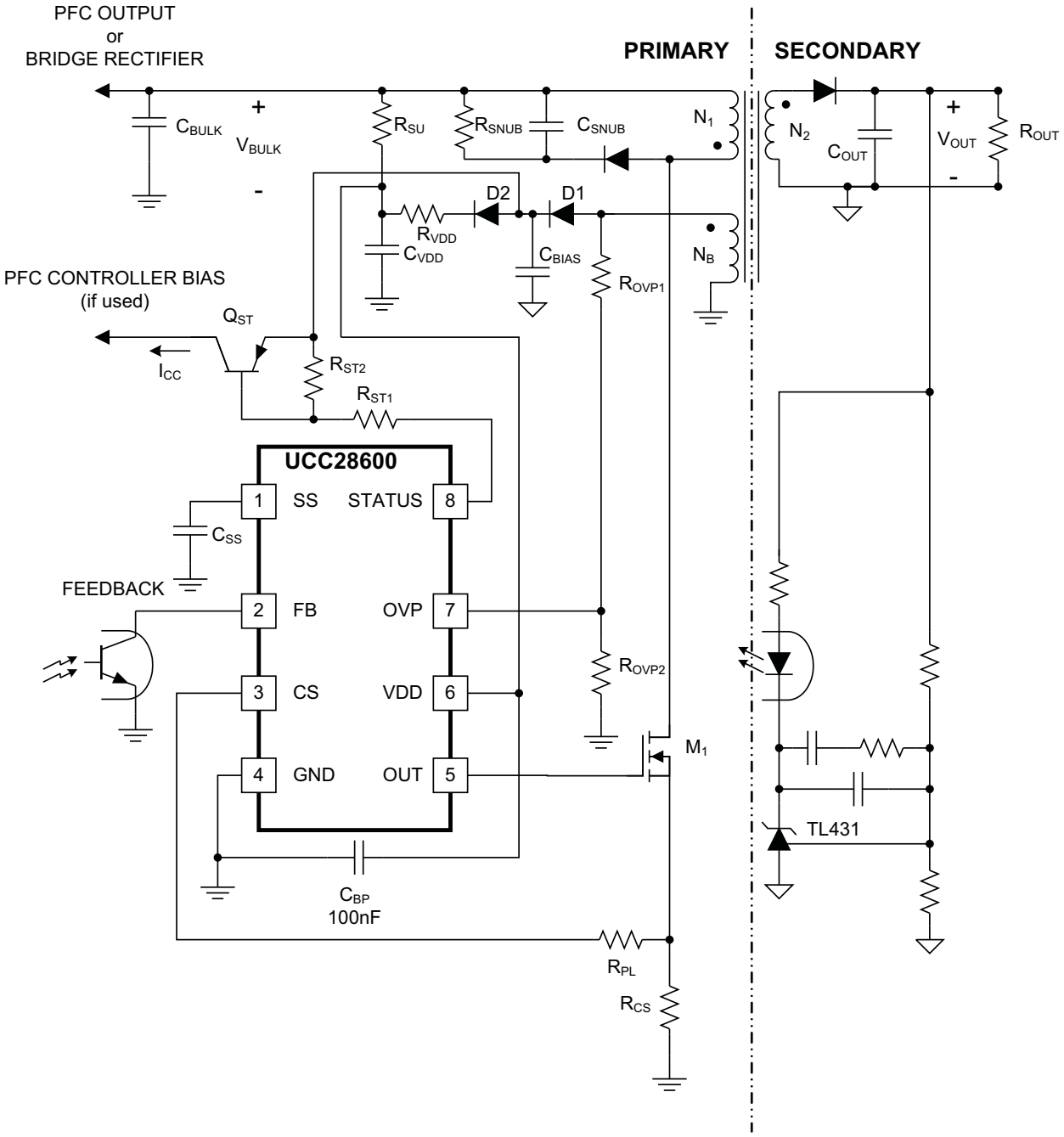


Figure 13. Simplified Application

Typical Application (continued)

8.2.1 Design Requirements

The following table illustrates a typical set of performance requirements for an off-line flyback converter.

Table 2. Design Example Performance Requirements

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{IN}	AC line input voltage	Input to PFC stage	85	115/230	265	V_{RMS}
f_{LINE}	Line frequency		47	50/60	63	Hz
PFC_{OUTPUT}	PFC output voltage		350	390	400	V
PFC	Input power factor	V_{IN} = 115 V_{RMS}, I_{OUT} = 6.2 A			0.998	
		V_{IN} = 230 V_{RMS}, I_{OUT} = 6.2 A			0.97	
V_{OUT}	Output voltage	85 V_{RMS} ≤ V_{IN} ≤ 265 V_{RMS}, 0 A ≤ I_{OUT} ≤ 6.2 A	19.0	19.4	19.8	V
I_{OUT}	Output load current	85 V_{RMS} ≤ V_{IN} ≤ 265 V_{RMS}	0		6.2	A
V_{RIPPLE}	Output voltage ripple	85 V_{RMS} ≤ V_{IN} ≤ 265 V_{RMS}, I_{OUT} = 6.2 A		250		mV
V_{OVP}	Output over voltage limit	V_{IN} = 115 V_{RMS}, I_{OUT} = 6.2 A		23.4		V
		V_{IN} = 230 V_{RMS}, I_{OUT} = 6.2 A		23.6		V
f_{CO}	Control loop bandwidth	V_{IN} = 115 V_{RMS}, I_{OUT} = 3 A		2.6		kHz
	Phase margin	V_{IN} = 115 V_{RMS}, I_{OUT} = 3 A		70		degrees
η_{PEAK}	Peak efficiency	V_{IN} = 265 V_{RMS}, I_{OUT} = 6 A		87.4%		
η	Full load efficiency	V_{IN} = 115 V_{RMS}, I_{OUT} = 6.2 A		82.7%		
		V_{IN} = 230 V_{RMS}, I_{OUT} = 6.2 A		86.4%		
	No load power consumption	V_{IN} = 115 V_{RMS}, I_{OUT} = 0 A		230		mW
		V_{IN} = 230 V_{RMS}, I_{OUT} = 0 A		420		mW

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design an off-line universal input quasi-resonant flyback converter using the UCC28600. Refer to Figure 13 for component names and network locations. For additional design help, the design calculator, SLVC104, provides a user-interactive iterative process for selecting recommended component values for an optimum design when used without a PFC input.

8.2.2.1 Input Bulk Capacitor and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel, often with some inductance between them to suppress differential-mode conducted noise. EMI filter design is beyond the scope of this design procedure.

The minimum bulk valley voltage, $V_{BULK(min)}$ is dependent upon the input C_{BULK} capacitor value; this minimum valley voltage is used in the power stage design. The input capacitor is chosen to maintain an acceptable input voltage ripple. For a design that uses a regulated PFC output voltage for the input rail the required input capacitor to the flyback stage is calculated using the minimum PFC output voltage, $V_{PFCoutput(min)}$. Assuming a 15% ripple, the desired minimum bulk valley voltage is:

$$V_{BULK(min)} = 0.85 \times V_{PFCoutput(min)} \tag{14}$$

Designs that do not have a PFC input stage will require a much larger input capacitor. The $V_{BULK(min)}$ when designing without a PFC input stage will be based upon the allowable voltage at the valley of the ripple on the input rail, which can be 25% to 40% of the minimum rectified AC line voltage. Under those conditions, substitute the value of the minimum rectified line voltage for $V_{PFCoutput(min)}$ and the value of the maximum rectified line voltage wherever $V_{PFCoutput(max)}$ is used.

The maximum input power, P_{IN}, is estimated by the output power, P_{OUT}, and full-load efficiency target, η, as shown:

$$P_{IN(max)} = \frac{P_{OUT}}{\eta} = \frac{V_{OUT} \times I_{OUT(max)}}{\eta} \tag{15}$$

The following equation provides an accurate solution for determining the input capacitance needed to achieve the minimum bulk valley voltage target, $V_{BULK(min)}$:

$$C_{BULK} \geq \frac{2P_{IN} \times \left[0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{V_{PFCoutput(min)}}\right)\right]}{\left(V^2_{PFCoutput(min)} - V^2_{BULK(min)}\right) \times f_{LINE(min)}} \tag{16}$$

If an input capacitance other than the calculated value is used, iterate the $V_{BULK(min)}$ value until the desired capacitance is obtained so that the actual $V_{BULK(min)}$ is determined.

8.2.2.2 Transformer Turns Ratio and Primary Inductance

The allowable flyback voltage, $V_{FLYBACK}$, seen by the MOSFET, determines the minimum primary to secondary turns-ratio, N_{PS}. The flyback voltage is calculated based upon the acceptable Drain to Source voltage rating of the MOSFET and the maximum PFC output voltage rail, $V_{PFCoutput(max)}$ (or rectified maximum line voltage if not using a PFC input stage), and derating to account for voltage spikes due to leakage inductance:

$$V_{FLYBACK} = \frac{\left(V_{DS(max)} - V_{PFCoutput(max)}\right)}{1.5} \tag{17}$$

Typically, in an off-line design or a design with a PFC output voltage of 390 VDC to 400 VDC, a MOSFET rated for $V_{DS(max)}$ of 600 V_{DS} or greater is used. The primary to secondary turns-ratio takes the output diode voltage drop, V_F, into account:

$$N_{PS} = \frac{V_{FLYBACK}}{V_{OUT} + V_F} \tag{18}$$

The primary to bias winding turns ratio is calculated, based upon the desired bias voltage, V_{BIAS}, for the UCC28600 controller and the PFC controller bias voltage, making sure to avoid the absolute maximum rating for VDD of each controller:

$$N_{PB} = N_{PS} \times \frac{V_{OUT}}{V_{BIAS}} \tag{19}$$

The switching frequency at the minimum bulk valley voltage is used as a limiting factor for the maximum primary inductance. The UCC28600 will operate in quasi-resonant mode during operation at maximum load, minimum input voltage and its peak primary current and its switching frequency will be modulated during each switching cycle. Using a switching frequency of 80 kHz, for f_{SW}, at this operating point will give adequate margin for manufacturing tolerances in the transformer, the parasitic switch node capacitance, which influences the resonant frequency to each valley, and keep the controller from trying to go continuous during transient conditions. The switching period, t_{SW}, is equal to $1/f_{SW}$. Using volt-second balance, the maximum primary inductance can be calculated:

$$L_{P(max)} = \left[\frac{V_{BULK(min)} \times \left(V_{OUT} + V_F\right) \times N_{PS} \times \left(0.925 \times t_{SW}\right)}{V_{BULK(min)} + \left(N_{PS} \times \left(V_{OUT} + V_F\right)\right)}\right]^2 \times \frac{f_{SW}}{2 \times P_{IN(max)}} \tag{20}$$

The resistor divider on OVP senses the line voltage during the switch on-time when the auxiliary winding voltage is proportional to the line voltage. During this portion of the switching cycle, the OVP pin is internally clamped to approximately 0 V and sources current proportional to the line voltage. The R_{OVP1} resistor is chosen using the nominal line over-voltage protection current threshold, $I_{OVP(line)}$, which is equal to 450 µA.

$$R_{OVP1} = \frac{V_{BULK(OVP)}}{N_{PB} \times I_{OVP(line)}} \tag{21}$$

The OVP pin is also used to sense the output voltage when the OUT signal is low. To set the output over-voltage level, $V_{OUT(shutdown)}$, which is the desired voltage level on the output that would cause the controller to shutdown, use the load overvoltage protection threshold, $V_{OVP(load)}$, equal to 3.75 V, to determine the required R_{OVP2} resistor.

$$R_{OVP2} = \frac{R_{OVP1} \times V_{OVP(load)}}{\frac{N_{PS}}{N_{PB}} \times \left(V_{OUT(shutdown)} + V_F\right) - V_{OVP(load)}} \tag{22}$$

The peak primary current at low input voltage, full load, $I_{P(1)}$, can be estimated with the following equation:

$$I_{P(1)} = \frac{V_{BULK(min)} \times \left(V_{OUT} + V_F\right) \times N_{PS} \times \left(0.925 \times t_{SW}\right)}{L_P \times \left(V_{BULKmin} + N_{PS} \times \left(V_{OUT} + V_F\right)\right)} \tag{23}$$

The switching frequency at maximum input voltage can be estimated:

$$f_{SWvin(max)} = \frac{N_{PS}^2 \times V_{PFCoutput(max)}^2 \times 0.925^2 \times (V_{OUT} + V_F)^2}{2 \times L_P \times P_{INmax} \times \left[V_{PFCoutput(max)} + N_{PS} \times (V_{OUT} + V_F)\right]^2} \quad (24)$$

Now that the switching frequency at the maximum input voltage has been determined, the peak primary current at maximum load, $I_{P(2)}$, at the maximum input voltage can be calculated:

$$I_{P(2)} = \frac{V_{PFCoutput(max)} \times \left[N_{PS} \times (V_{OUT} + V_F) \times \frac{0.925}{f_{SWvin(max)}}\right]}{L_P \times \left[N_{PS} \times (V_{OUT} + V_F) + V_{PFCoutput(max)}\right]} \quad (25)$$

The power limit current that is sourced at the CS pin adds a voltage step to the CS waveform that is proportional to the line voltage. At minimum input voltage, maximum load, this current is referred to as $I_{CS(1)}$ and can be estimated from the following equation:

$$I_{CS(1)} = 0.5 \times \left[550mV \times \left(\frac{1}{R_{OVP1}} + \frac{1}{R_{OVP2}}\right) + \frac{V_{BULK(min)}}{N_{PB} \times R_{OVP1}}\right] \quad (26)$$

At maximum input voltage and maximum load, the power limit current sourced from CS is referred to as $I_{CS(2)}$ and is estimated using the same formula:

$$I_{CS(2)} = 0.5 \times \left[550mV \times \left(\frac{1}{R_{OVP1}} + \frac{1}{R_{OVP2}}\right) + \frac{V_{PFCoutput(max)}}{N_{PB} \times R_{OVP1}}\right] \quad (27)$$

The appropriate values of the current sense resistor, R_{CS}, and the power limit resistor, R_{PL}, are both dependent upon the internal power limit threshold, V_{PL} = 1.20 V, the CS offset voltage, $V_{CS(os)}$ = 0.40 V, peak primary currents, and the power limit currents, calculated above, and can be calculated as shown:

$$R_{CS} = \frac{\left(V_{PL} - V_{CS(os)}\right) \times \left(I_{CS(2)} - I_{CS(1)}\right)}{\left(I_{CS(2)} \times I_{P(1)}\right) - \left(I_{CS(1)} \times I_{P(2)}\right)} \quad (28)$$

$$R_{PL} = \frac{\left(V_{PL} - V_{CS(os)}\right) \times \left(I_{P(2)} - I_{P(1)}\right)}{\left(I_{CS(1)} \times I_{P(2)}\right) - \left(I_{CS(2)} \times I_{P(1)}\right)} \quad (29)$$

8.2.2.3 Non-Ideal Current Sense Value

Resistors R_{CS}, R_{PL}, R_{OVP1} and R_{OVP2} must be programmed as a set due to functional interactions in the converter. Often, the ideal value for R_{CS} is not available because the selection range of current sense resistors is too coarse to meet the required power limit tolerances. This issue can be solved by using the next larger available value of R_{CS} and use a resistive divider with a Thevenin resistance that is equal to the ideal R_{PL} value in order to attenuate the CS signal to its ideal value, as shown in Figure 14. The equations for modifying the circuit are:

$$R_{PL1} = R_{PL} \times \frac{(R_{CS})}{(R_{DCS})}$$

where

- R_{DCS} = ideal, but non-standard, value of current sense resistor.
- R_{PL} = previously calculated value of the power limit resistor. (30)

$$R_{PL2} = \frac{R_{PL1}}{\left(\frac{R_{CS}}{R_{DCS}}\right) - 1}$$

where

- R_{CS} = available, standard value current sense resistor. (31)

The board should be laid out to include R_{PL2} in order to fascillitate final optimization of the design based upon readily available components.

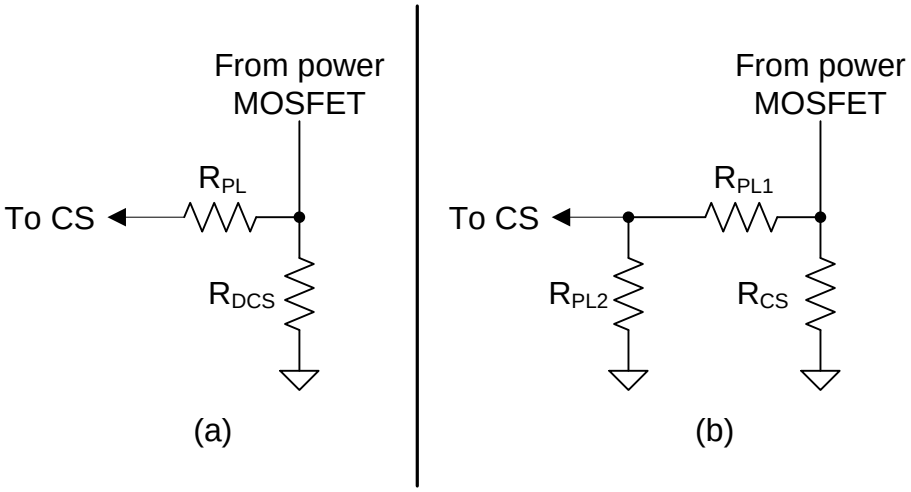


Figure 14. Modifications to Fit a Standard Current Sense Resistor Value

8.2.2.4 Snubber Damping

Resonance between the leakage inductance and the MOSFET drain capacitance can cause false load-OVP faults, in spite of the typical 2-µs delay in load-OVP detection. The bias winding is sensitive to the overshoot and ringing because it is well coupled to the primary winding. A technique to eliminate the problem is to use an R^2CD snubber instead of an RCD snubber, shown in Figure 15. A damping resistor added to the RCD snubber reduces ringing between the drain capacitor and the inductance when the snubber diode commutates OFF.

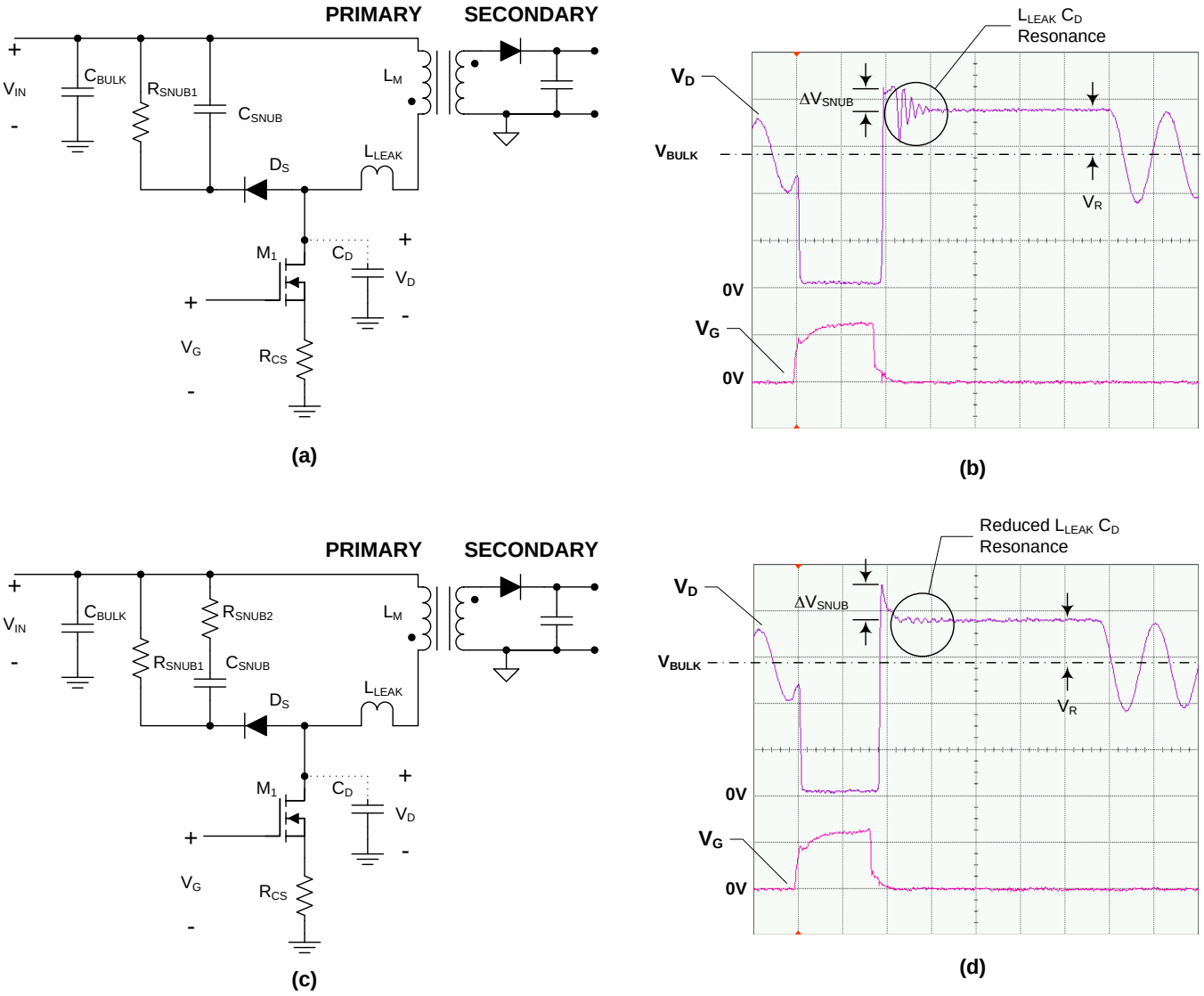


Figure 15. (a) RCD Snubber, (b) RCD Snubber Waveform, (c) R^2CD Snubber, (d) R^2CD Snubber Waveform

Begin the design of the R^2CD using the same procedure as designing an RCD snubber. Then, add the damping resistor, R_{SNUB2}. The procedure is as follows:

$$\text{Pick}\ \frac{\Delta V_{SNUB}}{V_R} = \text{between}\ 0.5\ \text{and}\ 1 \tag{32}$$

Select a capacitor for ΔV_{SNUB}:

$$C_{SNUB} = \frac{I_{CS(peak)}{}^2 L_{LEAK}}{\left(V_R + \Delta V_{SNUB}\right)2 - V_R{}^2} \tag{33}$$

Pick R_{SNUB} to discharge C_{SNUB}:

$$R_{SNUB} = \left(\frac{1}{2} + \frac{V_R}{\Delta V_{SNUB}}\right)\frac{1}{C_{SNUB}}\left(\frac{L_{LEAK} I_{CS(peak)}}{\Delta V_{SNUB}}\right) \tag{34}$$

$$P\left(R_{SNUB1}\right) = \frac{\left(V_R + \frac{\Delta V_{SNUB}}{2}\right)^2 \times \left[1 + \left(\frac{1}{3}\right) \times \left[\frac{1}{\frac{V_R}{V_{SNUB}} + \frac{1}{2}}\right]\right]^2}{R_{SNUB1}} \tag{35}$$

Pick R_{SNUB2} to dampen the L_{LEAK}-C_{SNUB} resonance with a Q that is between 1.7 and 2.2:

$$R_{SNUB2} = \left(\frac{\Delta V_{SNUB}}{I_{CS(peak)}}\right) \tag{36}$$

$$P\left(R_{SNUB}\right) = I_{CS(peak)}{}^2 R_{SNUB2}\left[\frac{1}{3}\frac{L_{LEAK} f_{S(max)}}{\left(V_R + \frac{\Delta V_{SNUB}}{2}\right)}\right] \tag{37}$$

For the original selection of ΔV_{SNUB},

$$Q = \sqrt{\frac{2V_R}{\Delta V_{SNUB}} + 1} \tag{38}$$

8.2.2.5 Open Loop Test Circuit

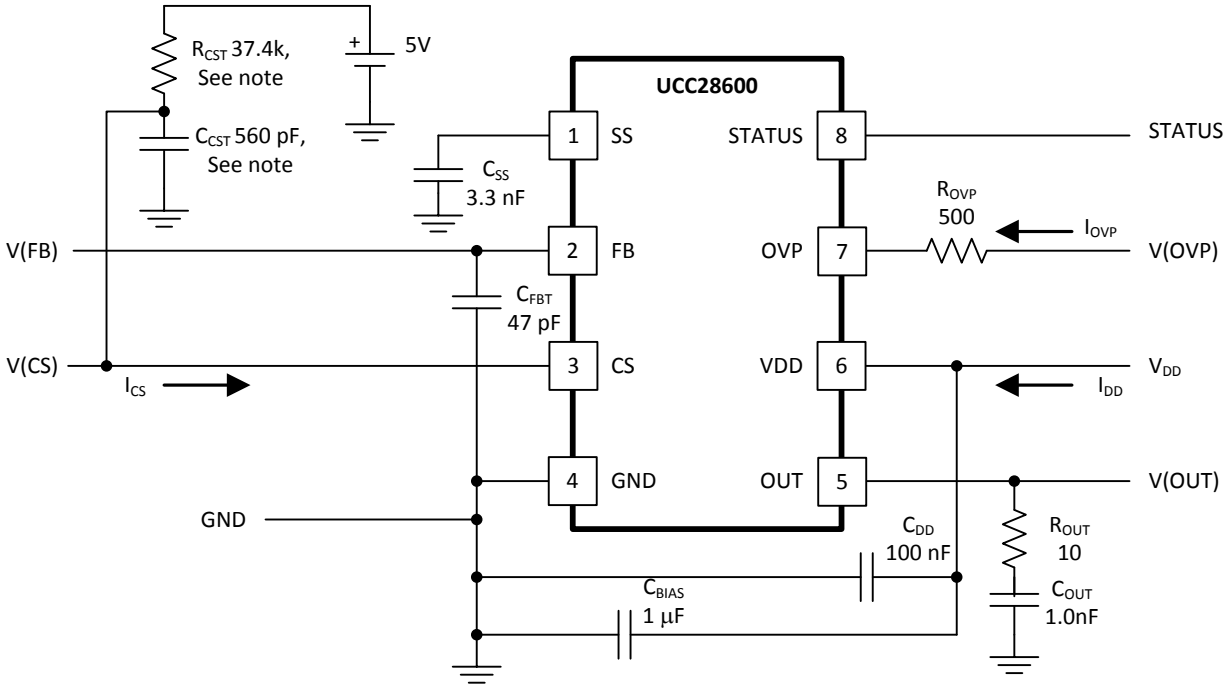


Figure 16. Open Loop Test Circuit

NOTE

R_{CST} and C_{CST} are not connected for maximum and minimum duty cycle tests, current sense tests and power limit tests.

8.2.3 Application Curves

The following figures show the UCC28600 in various operating modes in a 120-W converter, output voltage equal to 19.4 V.

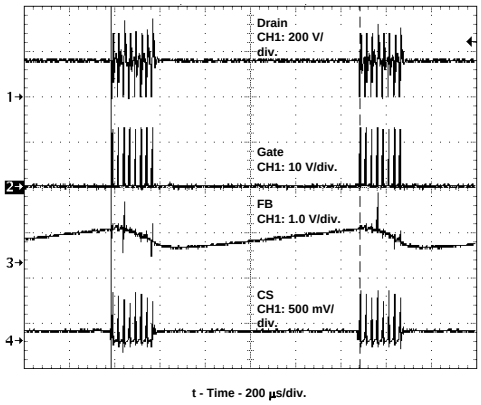


Figure 17. Green Mode Showing Frequency of Burst Packets, 900 Hz Apart, 3% Full-Rated Load

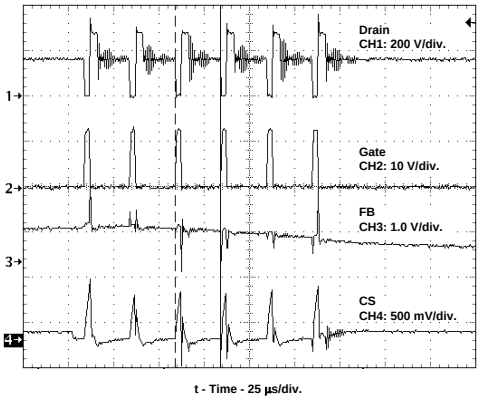


Figure 18. Green Mode Showing 40-kHz Switching Within Burst Packets, 3% Full-Rated Load

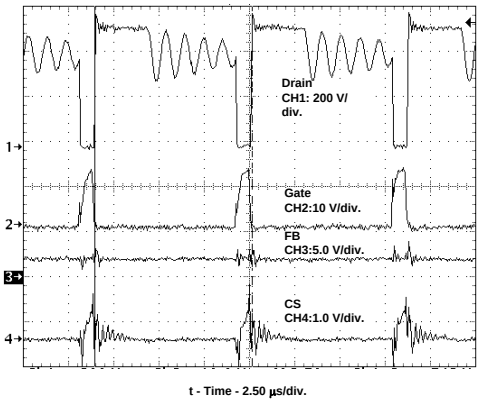


Figure 19. Frequency Foldback Mode, 115-kHz Switching, 24% Full-Rated Load

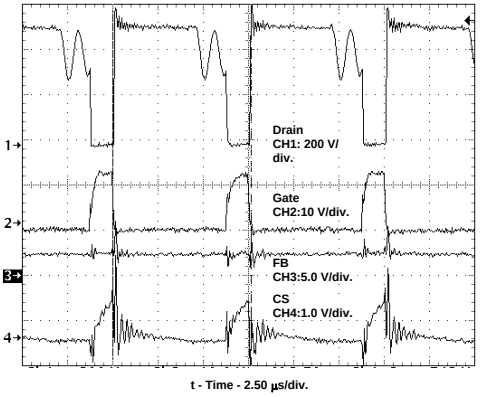


Figure 20. DCM Operation, 130-kHz Switching, 74% Full-Rated Load

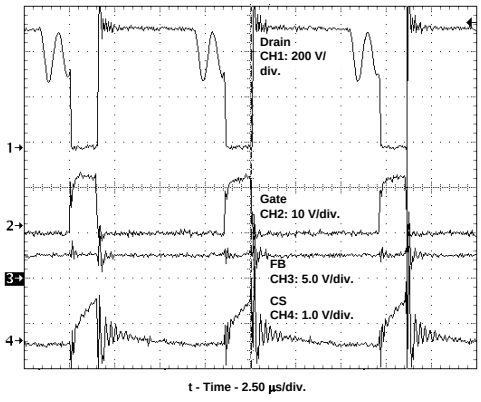


Figure 21. QR Operation, 116-kHz Switching, 90% Full-Rated Load

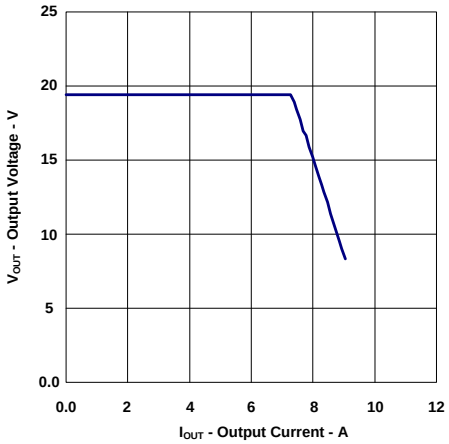


Figure 22. Output Voltage vs. Output Current

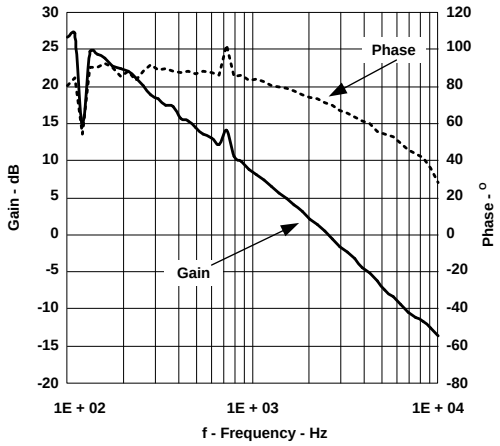


Figure 23. Phase/Gain vs. Frequency

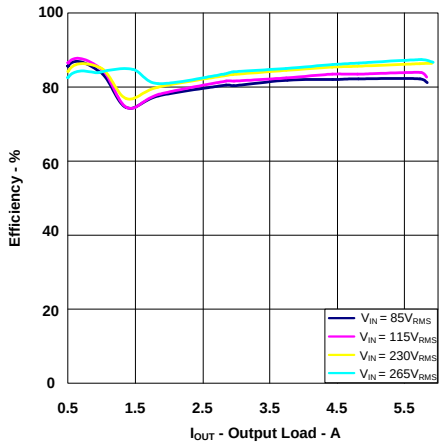


Figure 24. Efficiency vs. Output Load

8.3 Do's and Don'ts

Always be sure to do the following:

- Isolate the STATUS pin from the start up resistor with a diode to prevent the bias current from the bulk input rail from being diverter away from VDD and into STATUS circuit.
- Use a bypass capacitor on VDD, minimum value of 0.1 µF, to filter high frequency noise.
- Use a large bulk capacitor on VDD to hold the bias above the UVLO turn off threshold between the long periods of time between burst packets at light load.
- Use a large enough capacitor on SS to prevent triggering power limit when charging the output capacitor bank at turn on.
- Place the SS capacitor as close as possible to the SS pin with short traces and return to the quiet signal ground.
- Design the loop crossover frequency to be between 2 kHz to 3 kHz at nominal input voltage and 50% load with a phase margin of 70 degrees to satisfactorily stabilize the loop for the entire range of operation.
- Add a small filter capacitor to CS to effectively create an RC low pass filter in conjunction with the power limit resistor, R_{PL}, which will improve noise immunity at the current sense pin.
- Place a 10-kΩ resistor between the gate of the MOSFET and ground to discharge the gate capacitance and protect against inadvertent dv/dt triggered turn-on.
- Use a small value gate drive resistor in series with the gate drive to control the turn on transition time and reduce the dv/dt ringing in this node.
- Select the R_{OVP1}, R_{OVP2}, R_{PL}, and R_{CS} together as the OVP resistors set up an internal dependent current source that impact the R_{CS} and R_{PL} component values.
- Design the transformer so the bias winding is well coupled to both the primary winding and the secondary winding. The bias winding is used not only for VDD bias but also for valley detection, line over-voltage, load over-voltage, and power limit off-set current.

CAUTION

Do not use a filter capacitor larger than 390 pF on the FB pin, this capacitor will provide a delay time to over-load response; capacitors larger than 390 pF will adversely affect performance.

9 Power Supply Recommendations

The UCC28600 is intended for AC-to-DC adaptors with input voltage range of 85 $V_{AC(rms)}$ to 265 $V_{AC(rms)}$ using the flyback topology. This controller can be used in supplies from a few Watts of power up to 200 Watts limited only by the practical use of a DCM flyback in regards to peak currents and output capacitor component size. The UCC28600 can be used in bias supplies for LCD monitors, TVs, and set-top boxes, as well as AC-to-DC adapters for energy-efficient supplies.

10 Layout

10.1 Layout Guidelines

To increase the reliability and feasibility of the design it is recommended to adhere to the following guidelines for PCB layout.

1. Minimize the high current loops to reduce parasitic capacitances and inductances. At the same time, do not inadvertently make traces with a high dv/dt too wide as this will create a very good E-field antenna.
2. Separate the device signal ground from the high current power ground in order to isolate the noise away from the device substrate. The separate grounds should, ideally, be tied together at the input capacitor on the primary side.
3. Return the sense resistor to the ground side of the input capacitor, instead of to the ground plane under the device.
4. The bypass capacitor on VDD must be placed as close as possible to the VDD and GND pins of the device.
5. The filter capacitor on CS must be placed as close as possible to the CS pin and GND pin of the device.
6. The filter capacitor on FB must be placed as close as possible to the FB and GND pins of the device.

10.2 Layout Example

The partial layout example shown in Figure 25 demonstrates an effective component and track arrangement for the printed circuit board. Actual board layout must conform to the constraints on a specific design, so many variations are possible.

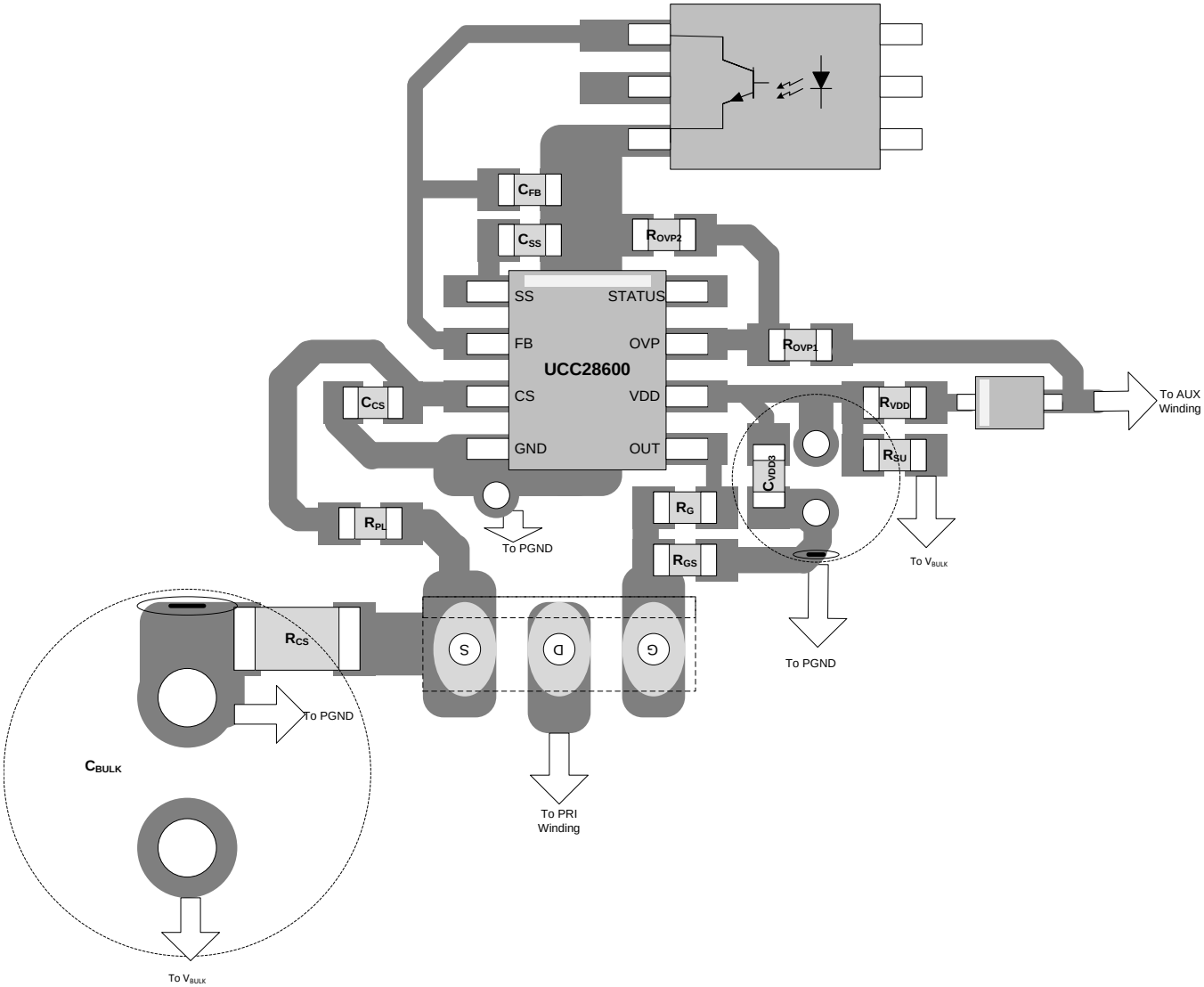


Figure 25. Partial Layout Example Showing Component Placement

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

UCC28600 Design Calculator, *A QR Flyback Designer.xls*, spreadsheet for Microsoft Excel 2003, (SLVC104)

11.2 Documentation Support

11.2.1 Related Documentation

- Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, (SLUP169)
- Datasheet, *UCC3581 Micro Power PWM Controller*, (SLUS295)
- Datasheet, *UCC28051 Transition Mode PFC Controller*, (SLUS515)
- *Design Considerations for the UCC28600*, (SLUA399)

11.2.2 Related Products

- *UCC28051 Transition Mode PFC Controller* (SLUS515)
- *UCC3581 Micro Power PWM Controller* (SLUS295)

11.3 Trademarks

TrueDrive is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28600D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28600D	Samples
UCC28600DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28600D	Samples
UCC28600DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28600D	Samples
UCC28600DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28600D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UCC28600 :

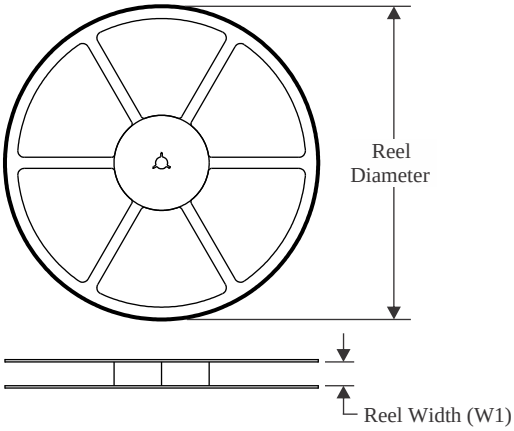
- Automotive : UCC28600-Q1

NOTE: Qualified Version Definitions:

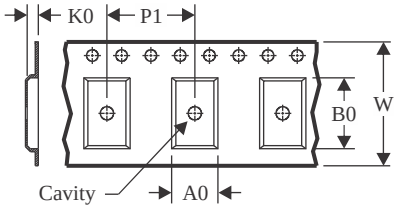
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

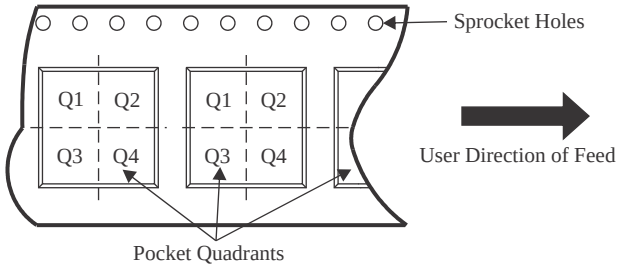


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

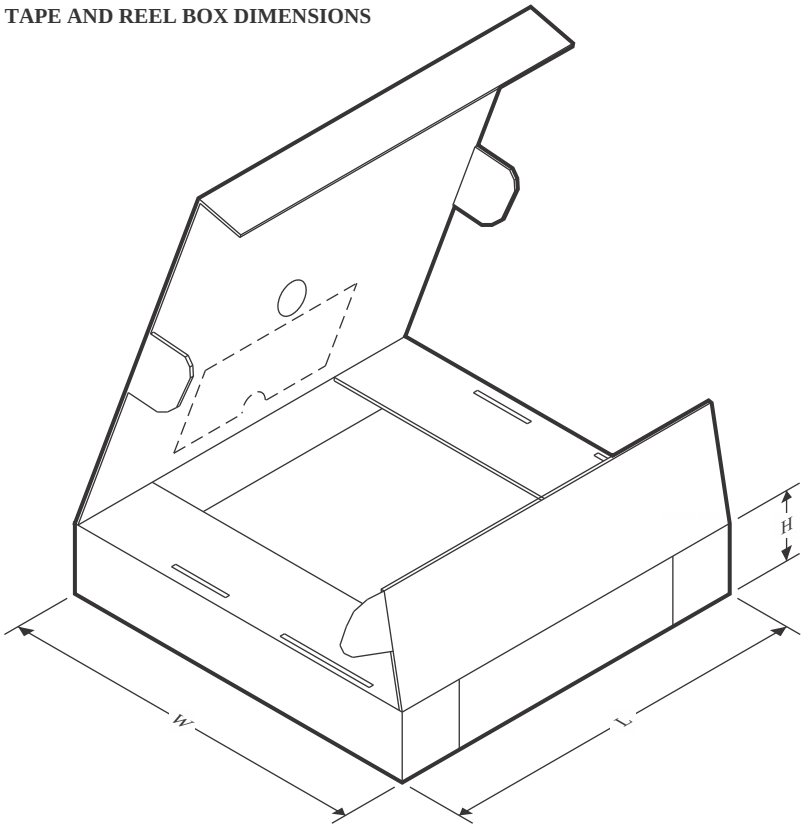
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28600DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

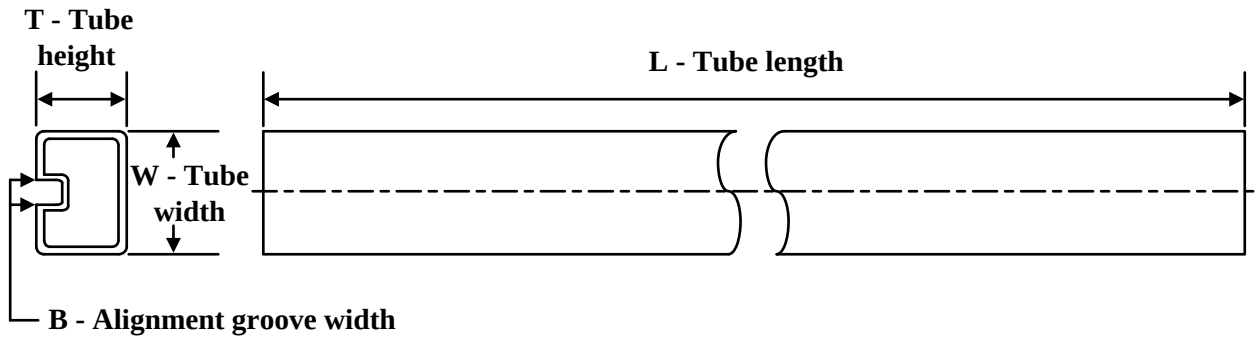
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28600DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

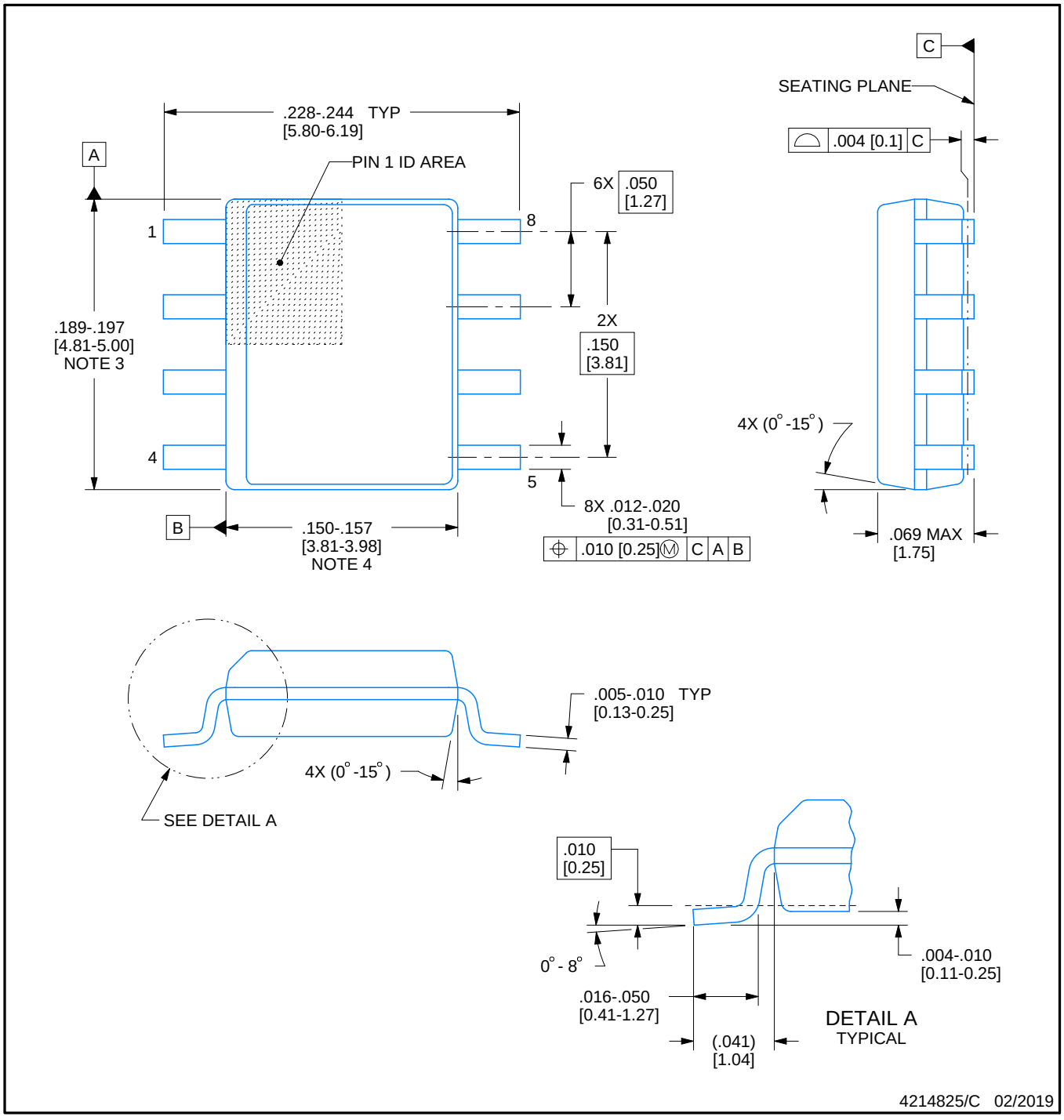
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28600D	D	SOIC	8	75	507	8	3940	4.32
UCC28600DG4	D	SOIC	8	75	507	8	3940	4.32

PACKAGE OUTLINE

D0008A

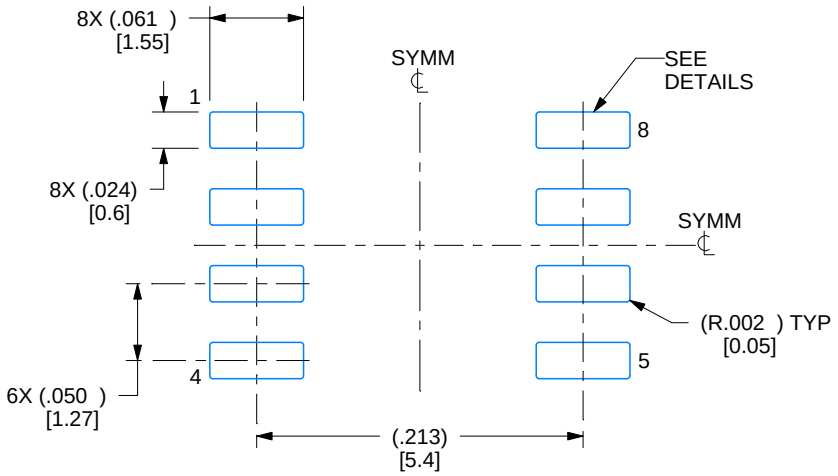
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

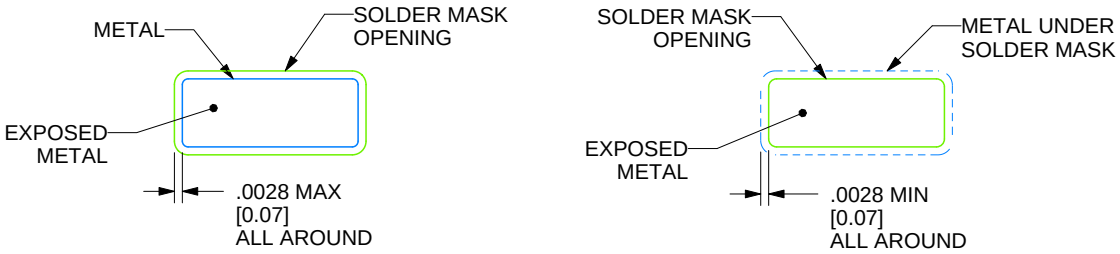


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

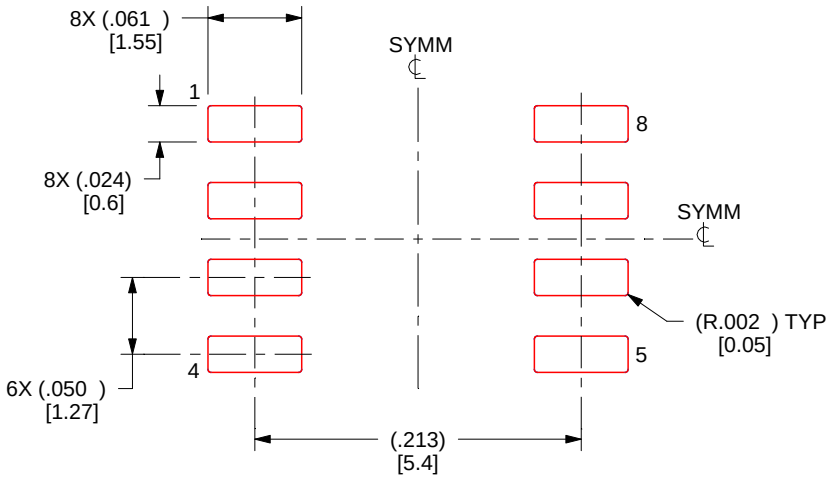
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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