LMx39-N, LM2901-N, LM3302-N Low-Power Low-Offset Voltage Quad Comparators

1 Features

- Wide Supply Voltage Range
- LM139/139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM2901-N: 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM3302-N: 2 to 28 V_{DC} or ±1 to ±14 V_{DC}
- Very Low Supply Current Drain (0.8 mA) — Independent of Supply Voltage
- Low Input Biasing Current: 25 nA
- Low Input Offset Current: ±5 nA
- Offset Voltage: ±3 mV
- Input Common-Mode Voltage Range Includes GND
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 250 mV at 4 mA
- Output Voltage Compatible With TTL, DTL, ECL, MOS, and CMOS Logic Systems
- Advantages:
  - High-Precision Comparators
  - Reduced V_{OS} Drift Overtemperature
  - Eliminates Need for Dual Supplies
  - Allows Sensing Near GND
  - Compatible With All Forms of Logic
  - Power Drain Suitable for Battery Operation

2 Applications

- Limit Comparators
- Simple Analog-to-Digital Converters (ADCs)
- Pulse, Squarewave, and Time Delay Generators
- Wide Range VCO; MOS Clock Timers
- Multivibrators and High-Voltage Digital Logic Gates

3 Description

The LMx39-N series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV maximum for all four comparators. These comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

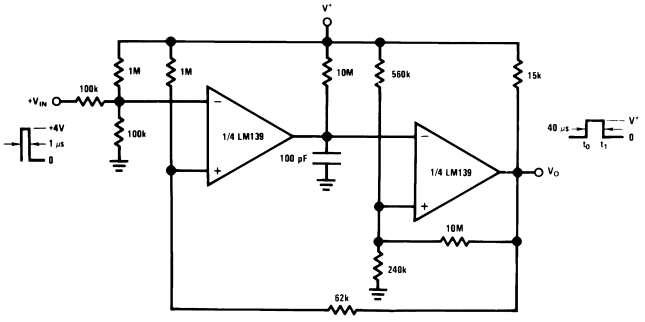
The LMx39-N series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the devices directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM139-N	CDIP (14)	19.56 mm × 6.67 mm
LM239-N		
LM2901-N	SOIC (14)	8.65 mm × 3.91 mm
	PDIP (14)	19.177 mm × 6.35 mm
LM339-N	CDIP (14)	19.56 mm × 6.67 mm
	SOIC (14)	8.65 mm × 3.91 mm
	PDIP (14)	19.177 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

One-Shot Multivibrator With Input Lock Out



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Changes from Revision D (March 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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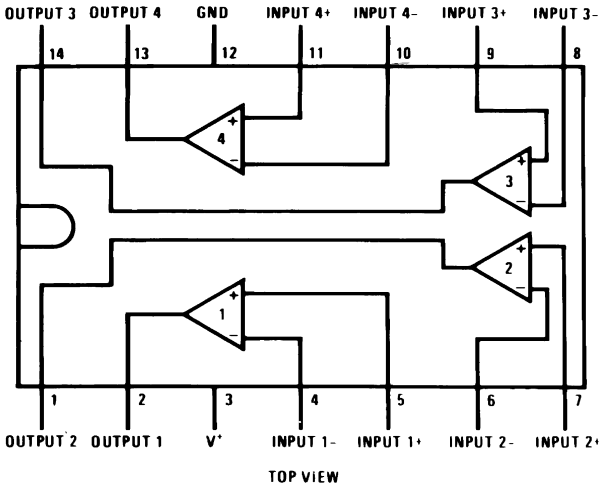
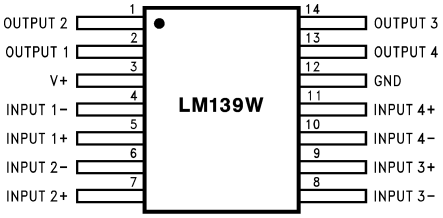
- Changed layout of National Data Sheet to TI format ... 10

5 Pin Configuration and Functions

J, D and NFF Package
14-Pin CDIP, SOIC, PDIP
Top View



14-Pin CLGA Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUTPUT2	O	Output, Channel 2
2	OUTPUT1	O	Output, Channel 1
3	V+	P	Positive Supply
4	INPUT1-	I	Inverting Input, Channel 1
5	INPUT1+	I	Noninverting Input, Channel 1
6	INPUT2-	I	Inverting Input, Channel 2
7	INPUT2+	I	Noninverting Input, Channel 2
8	INPUT3-	I	Inverting Input, Channel 3
9	INPUT3+	I	Noninverting Input, Channel 3
10	INPUT4-	I	Inverting Input, Channel 4
11	INPUT4+	I	Noninverting Input, Channel 4
12	GND	P	Ground
13	OUTPUT4	O	Output, Channel 4
14	OUTPUT3	O	Output, Channel 3

6 Specifications

6.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
Supply Voltage, V^+	LM139N, LM239N, LM339N, LM2901N			36	V_{DC}
	LM3302N			28	
Differential Input Voltage	LM139N, LM239N, LM339N, LM2901N (2)			36	
	LM3302N(2)			28	
Input Voltage	LM139N, LM239N, LM339N, LM2901N		−0.3	36	
	LM3302		–0.3	28	
Input Current (V_{IN}<−0.3 V_{DC})(3)				50	mA
Power Dissipation(4)	PDIP			1050	mW
	Cavity DIP			1190	
	SOIC Package			760	
Output Short-Circuit to GND(5)				Continuous	
Lead Temperature (Soldering, 10 seconds)				260	°C
Soldering Information	PDIP Package (10 seconds)			260	
	SOIC Package	Vapor Phase (60 seconds)		215	
		Infrared (15 seconds)		220	
Storage temperature, T_{stg}			−65	150	

(1) Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.
(2) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) (at 25°C).
(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).
(4) For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239-N and LM139-N must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the “ON-OFF” characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided the output transistors are allowed to saturate.
(5) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±600	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply Voltage	Single Supply	LM139N, LM239N, LM339N, LM2901N	2	36	V
		LM3302N	2	28	
	Dual Supply	LM139N, LM239N, LM339N, LM2901N	±1	±18	
		LM3302N	±1	±14	
Operating Temperature	LM139/LM139A		−55	125	°C
	LM2901/LM3302		−40	85	
	LM239/LM239A		−25	85	
	LM339/LM339A		0	70	

6.4 Thermal Information

THERMAL METRIC(1)		LM139-N, LM239-N, LM339-N	LM2901-N, LM339-N	LM2901-N, LM339-N	UNIT
		J	D	NFF	
		14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95	95	95	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: LM139A, LM239A, LM339A, LM139

(V^+=5 V_{DC}, T_A = 25°C[1] unless otherwise stated)

PARAMETER	TEST CONDITIONS	LM139A			LM239A, LM339A			LM139			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	See[2]		1.0	2.0		1.0	2.0		2.0	5.0	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range[3], V_{CM}=0 V		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM}= 0 V		3.0	25		5.0	50		3.0	25	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+ = 28 V_{DC})[4]	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	(LM3302, V^+ = 28 V_{DC}), R_L = ∞ on all Comparators		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	(LM3302, V^+ = 28 V_{DC}), R_L = ∞, V^+ = 36 V					1.0	2.5		1.0	2.5	mA_{DC}
Voltage Gain	R_L≥15 kΩ, V^+ = 15 V_{DC} V_O = 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ		300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ[5]		1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0, V_O ≤ 1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(-)}$ = 0, V_O = 5 V_{DC}		0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	See[2]			4.0			4.0			9.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0 V			100			150			100	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in			300			400			300	nA_{DC}
	Linear Range, V_{CM} = 0 V[3]										
Input Common-Mode	V^+=30 V_{DC} (LM3302),	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
Voltage Range	V^+ = 28 V_{DC})[4]										
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA			700			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(-)}$ = 0, V_O = 30 V_{DC}, (LM3302, V_O = 28 V_{DC})			1.0			1.0			1.0	$µA_{DC}$
Differential Input Voltage	Keep all V_{IN}'s ≥ 0 V_{DC} (or V^-, if used)[6]			36			36			36	V_{DC}

(1) These specifications are limited to −55°C ≤ T_A ≤ 125°C, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to −25°C ≤ T_A ≤ 85°C, the LM339/LM339A temperature specifications are limited to 0°C ≤ T_A ≤ 70°C, and the LM2901, LM3302 temperature range is −40°C ≤ T_A ≤ 85°C.

(2) At output switch point, V_O≅1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ −1.5 V_{DC}), at 25°C. For LM3302, V^+ from 5 V_{DC} to 28 V_{DC}.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V^+ −1.5V at 25°C, but either or both inputs can go to 30 V_{DC} without damage (25V for LM3302), independent of the magnitude of V^+.

(5) The response time specified is a 100-mV input step with 5-mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

(6) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

6.6 Electrical Characteristics: LM239, LM339, LM2901, LM3302

(V^+ = 5 V_{DC}, T_A = 25°C(1) unless otherwise stated)

PARAMETER	TEST CONDITIONS	LM239, LM339			LM2901			LM3302			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	See(2)		2.0	5.0		2.0	7.0		3	20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range(3), V_{CM}=0 V		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM} = 0 V		5.0	50		5	50		3	100	nA_{DC}
Input Common-Mode Voltage Range	V^+ = 30 V_{DC} (LM3302, V^+ = 28 V_{DC})(4)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	(LM3302, V^+ = 28 V_{DC}) R_L = ∞ on all Comparators		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	(LM3302, V^+ = 28 V_{DC}) R_L = ∞, V^+ = 36 V		1.0	2.5		1.0	2.5		1.0	2.5	mA_{DC}
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC} V_O = 1 V_{DC} to 11 V_{DC}	50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ,		300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ(5)		1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)}$= 1 V_{DC}, $V_{IN(+)}$ = 0, V_O ≤ 1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ = 1 V_{DC},$V_{IN(-)}$ = 0, V_O = 5 V_{DC}		0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	See(2)			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)}$− $I_{IN(-)}$, V_{CM} = 0 V			150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in			400		200	500			1000	nA_{DC}
	Linear Range, V_{CM} = 0V(3)										
Input Common-Mode	V^+ = 30 V_{DC} (LM3302, V^+ = 28 V_{DC})			V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
Voltage Range	See(4)										
Saturation Voltage	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(-)}$ = 0, V_O = 30 V_{DC}, (LM3302, V_O = 28 V_{DC})			1.0			1.0			1.0	$µA_{DC}$
Differential Input Voltage	Keep all V_{IN}'s ≥ 0 V_{DC} (or V^-, if used)(6)			36			36			28	V_{DC}

(1) These specifications are limited to −55°C ≤ T_A ≤ 125°C, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to −25°C ≤ T_A ≤ 85°C, the LM339/LM339A temperature specifications are limited to 0°C ≤ T_A ≤ 70°C, and the LM2901, LM3302 temperature range is −40°C ≤ T_A ≤ 85°C.

(2) At output switch point, V_O≈1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ −1.5 V_{DC}), at 25°C. For LM3302, V^+ from 5 V_{DC} to 28 V_{DC}.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V^+ −1.5V at 25°C, but either or both inputs can go to 30 V_{DC} without damage (25V for LM3302), independent of the magnitude of V^+.

(5) The response time specified is a 100-mV input step with 5-mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

(6) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

6.7 Typical Characteristics

6.7.1 LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

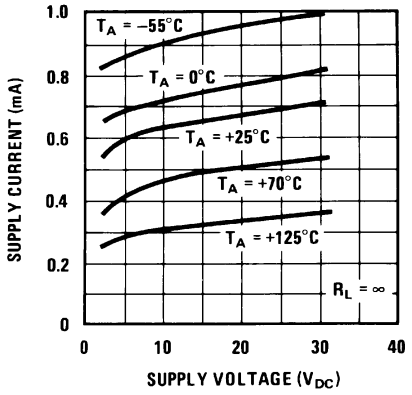


Figure 1. Supply Current

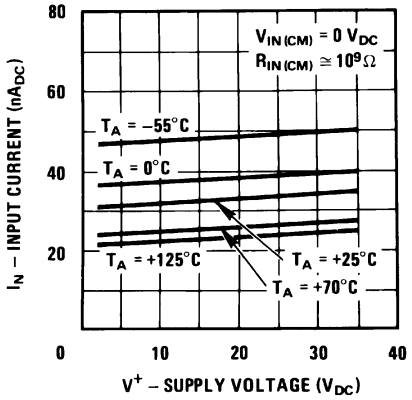


Figure 2. Input Current

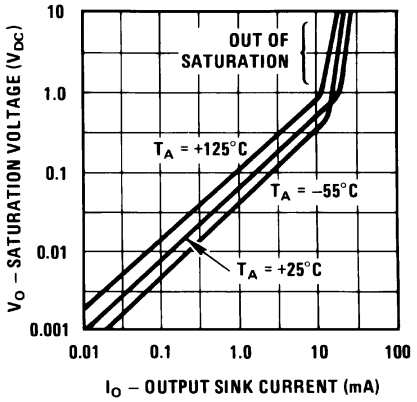


Figure 3. Output Saturation Voltage

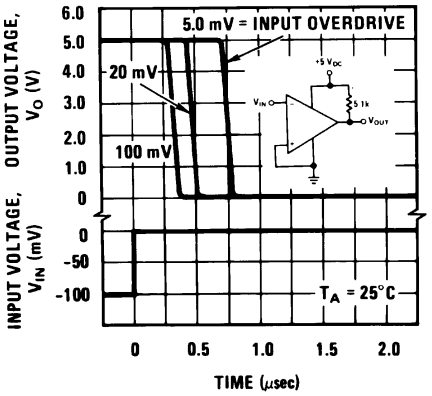


Figure 4. Response Time for Various Input Overdrives – Negative Transition

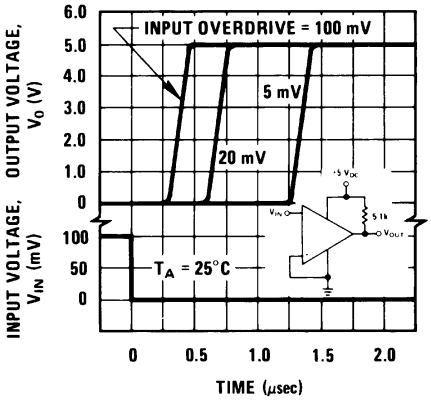


Figure 5. Response Time for Various Input Overdrives – Positive Transition

6.7.2 LM2901

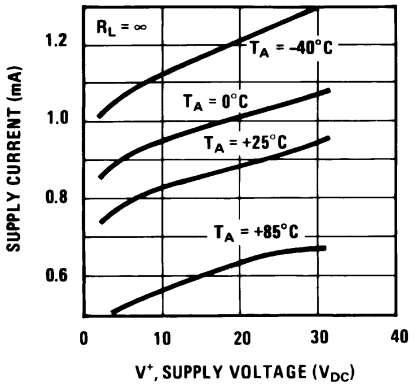


Figure 6. Supply Current

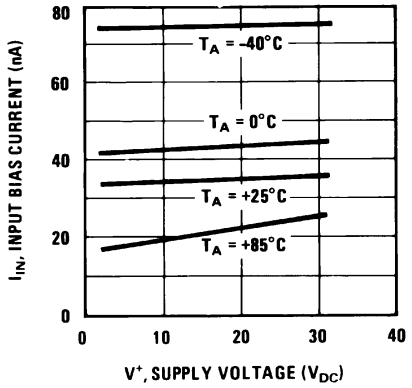


Figure 7. Input Current

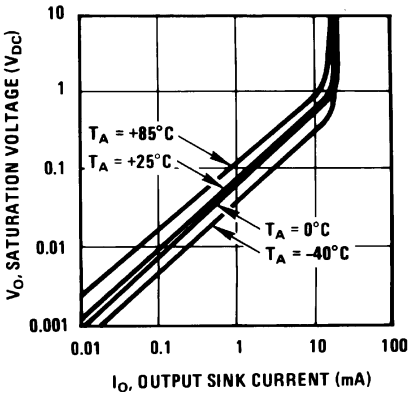


Figure 8. Output Saturation Voltage

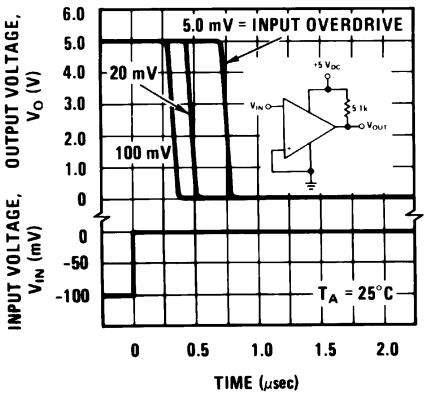


Figure 9. Response Time for Various Input Overdrives – Negative Transition

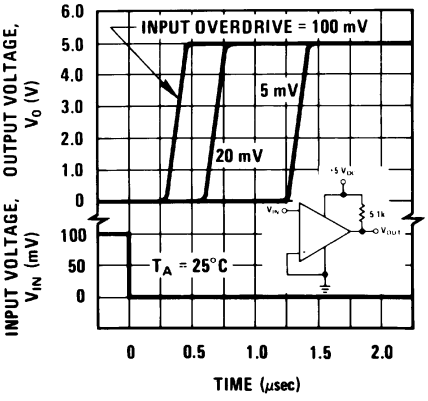


Figure 10. Response Time for Various Input Overdrives – Positive Transition

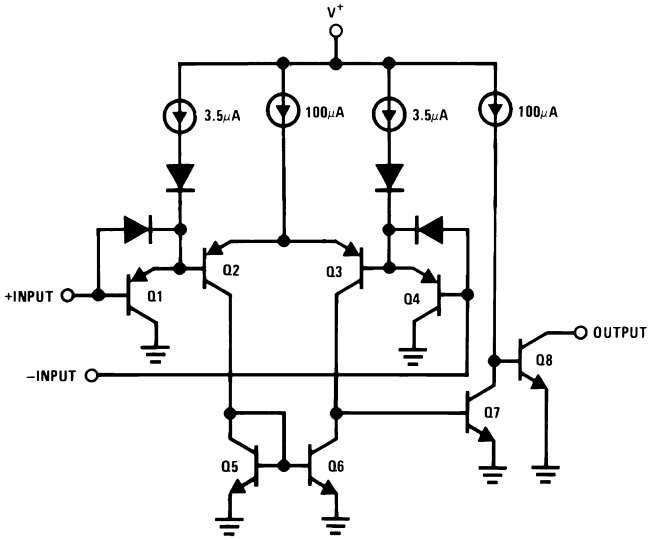
7 Detailed Description

7.1 Overview

The LM139/LM239/LM339 family of devices is a monolithic quad of independently functioning comparators designed to meet the needs for a medium-speed, TTL compatible comparator for industrial applications. Since no antisaturation clamps are used on the output such as a Baker clamp or other active circuitry, the output leakage current in the OFF state is typically 0.1 nA. This makes the device ideal for system applications where it is desired to switch a node to ground while leaving it totally unaffected in the OFF state. Other features include single supply, low voltage operation with an input common mode range from ground up to approximately one volt below V_{CC} . The output is an uncommitted collector so it may be used with a pullup resistor and a separate output supply to give switching levels from any voltage up to 36V down to a V CE SAT above ground (approximately 100 mV), sinking currents up to 16 mA. The open collector output configuration allows the device to be used in wired-OR configurations, such as a window comparators.

In addition it may be used as a single pole switch to ground, leaving the switched node unaffected while in the OFF state. Power dissipation with all four comparators in the OFF state is typically 4 mW from a single 5-V supply (1 mW/comparator).

7.2 Functional Block Diagram



7.3 Feature Description

The LMx39-N series are high-gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs through stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LMx39-N series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pullup resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pullup resistor is not used).

Feature Description (continued)

The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60-Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (4 mV) allows the output to clamp essentially to ground level for small load currents.

7.4 Device Functional Modes

A basic comparator circuit is used for converting analog signals to a digital output. The output is HIGH when the voltage on the non-inverting (+IN) input is greater than the inverting (-IN) input. The output is LOW when the voltage on the noninverting (+IN) input is less than the inverting (-IN) input. The inverting input (-IN) is also commonly referred to as the "reference" or "VREF" input.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LMx39-N series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM139-N is specified for operation from 2.0 V to 36 V (±1V to ±18V) over the temperature range of –55°C to 125°C. While it may seem like a comparator has a well-defined and somewhat limited functionality as a '1-bit ADC', a comparator is a versatile component which can be used for many functions.

Refer to *AN-74 LM139/LM239/LM339 A Quad of Independently Functioning Comparators* (SNOA654) for additional application information on use of the LM139-N.

8.2 Typical Applications

8.2.1 Basic Comparator

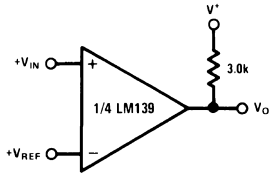


Figure 11. Basic Comparator Schematic

8.2.1.1 Design Requirements

The basic usage of a comparator is to indicate when a specific analog signal has exceeded some predefined threshold. In this application, the negative input is tied to a reference voltage, and the positive input is connected to the input signal. The output is pulled up with a resistor to the logic supply voltage, V+.

For an example application, the supply voltage is 5 V. The input signal varies between 1 V and 3 V, and we want to know when the input exceeds 2.5 V. For this example, we would set the V_{REF} to 2.5 V.

8.2.1.2 Application Curve

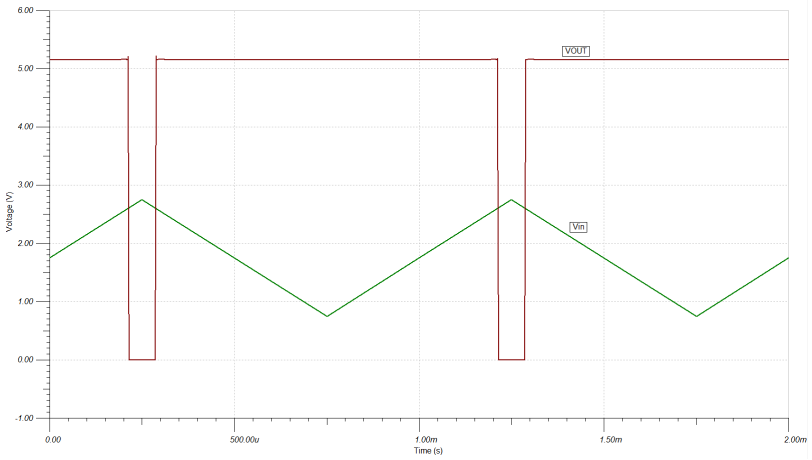


Figure 12. Basic Comparator Response

Typical Applications (continued)

8.2.2 System Examples

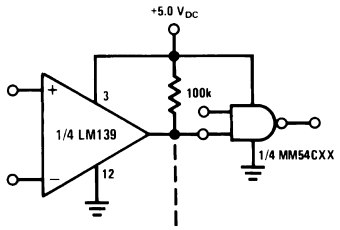


Figure 13. Driving CMOS
(V^+ = 5.0 V_{DC})

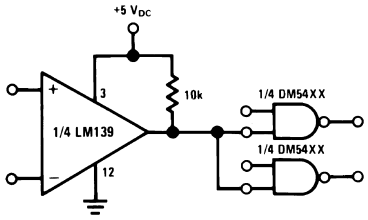


Figure 14. Driving TTL
(V^+ = 5.0 V_{DC})

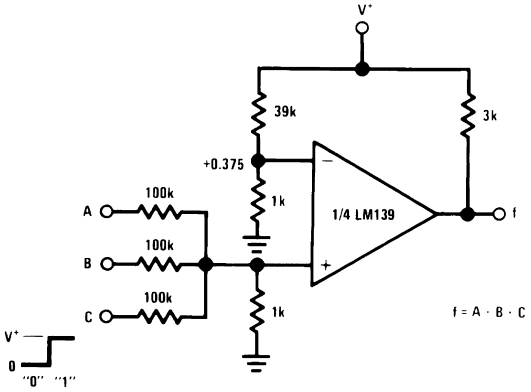


Figure 15. AND Gate
(V^+ = 5.0 V_{DC})

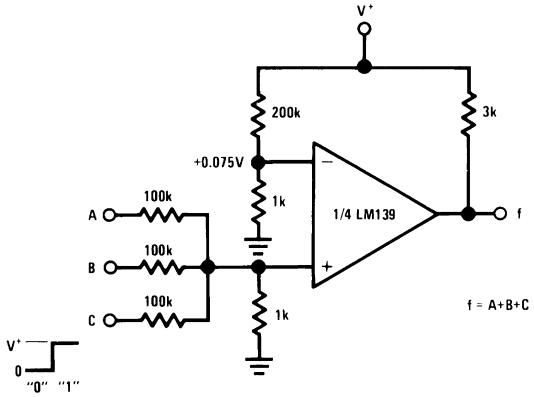


Figure 16. OR Gate
(V^+ = 5.0 V_{DC})

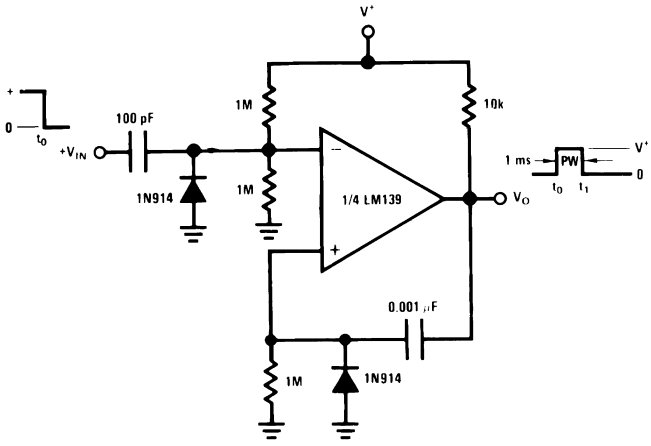


Figure 17. One-Shot Multivibrator
(V^+= 15 V_{DC})

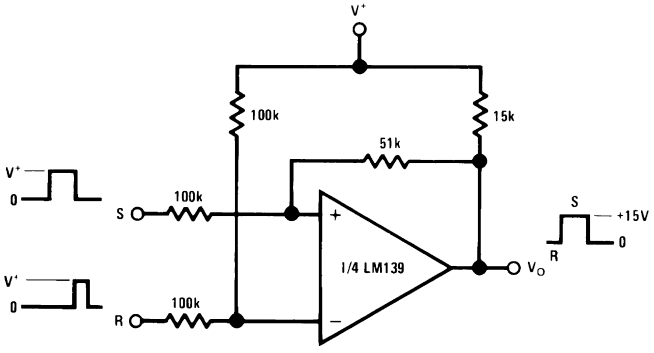


Figure 18. Bi-Stable Multivibrator
(V^+= 15 V_{DC})

Typical Applications (continued)

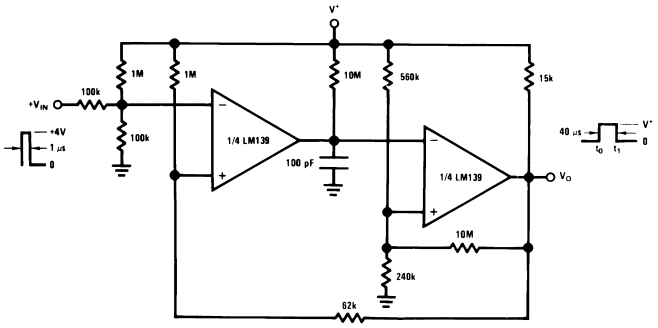


Figure 19. One-Shot Multivibrator with Input Lock Out
(V^+= 15 V_{DC})

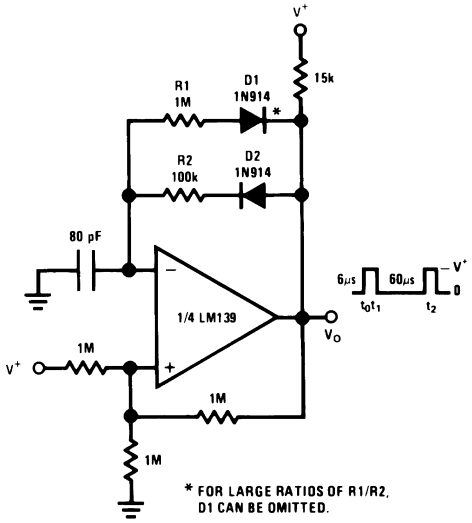


Figure 20. Pulse Generator
(V^+= 15 V_{DC})

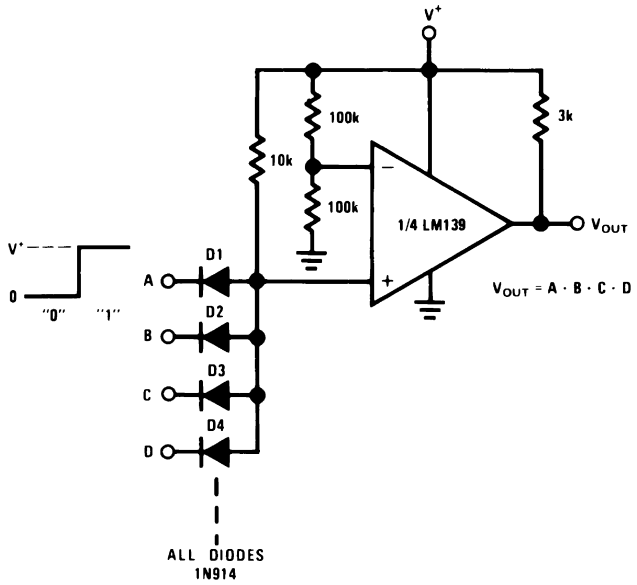


Figure 21. Large Fan-In AND Gate
(V^+= 15 V_{DC})

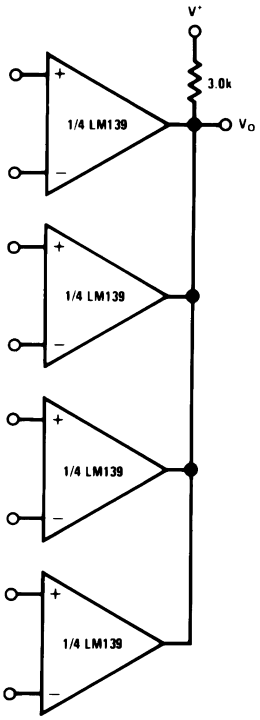


Figure 22. ORing the Outputs
(V^+= 15 V_{DC})

Typical Applications (continued)

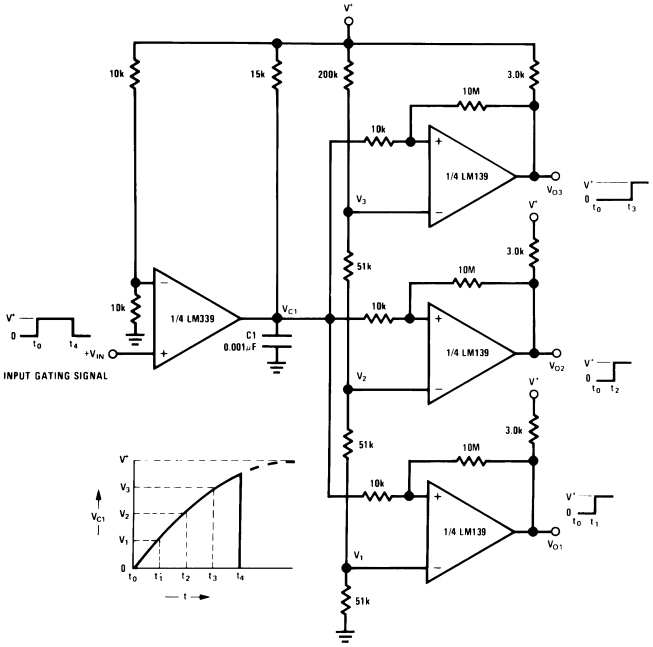


Figure 23. Time Delay Generator
(V^+= 15 V_{DC})

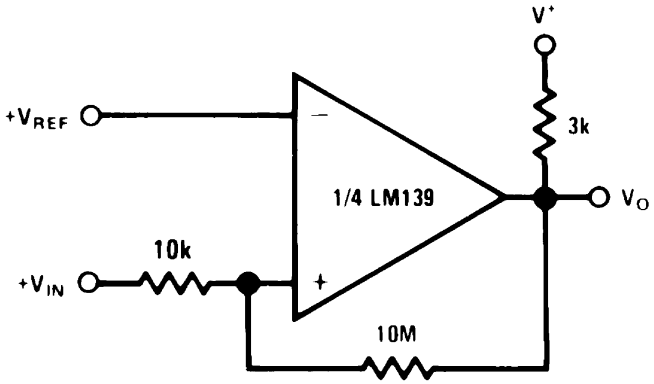


Figure 24. Non-Inverting Comparator with Hysteresis
(V^+= 15 V_{DC})

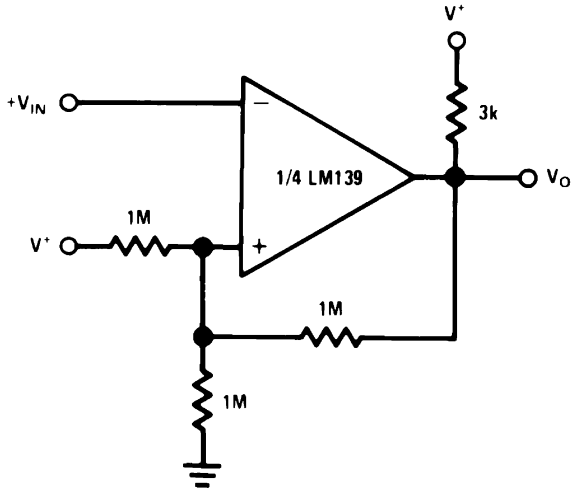


Figure 25. Inverting Comparator With Hysteresis
(V^+= 15 V_{DC})

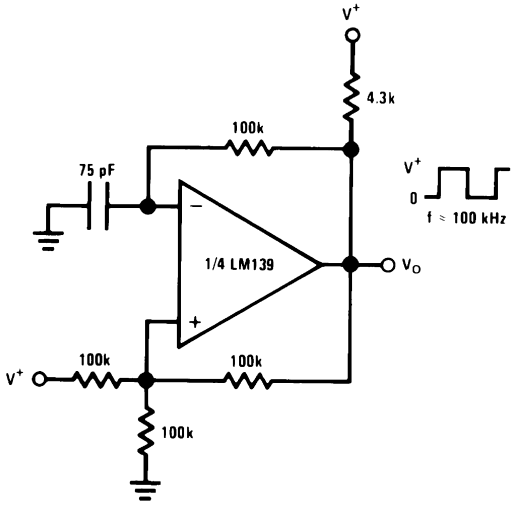


Figure 26. Squarewave Oscillator
(V^+= 15 V_{DC})

Typical Applications (continued)

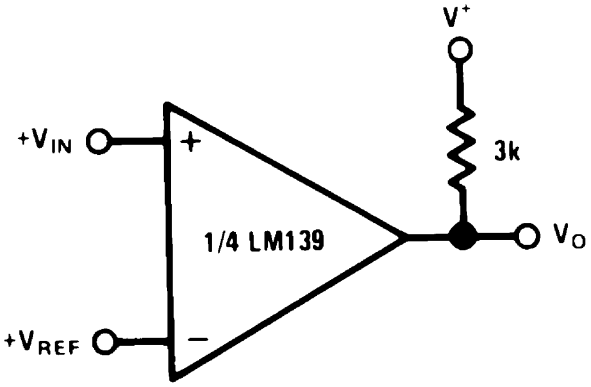


Figure 27. Basic Comparator
(V^+= 15 V_{DC})

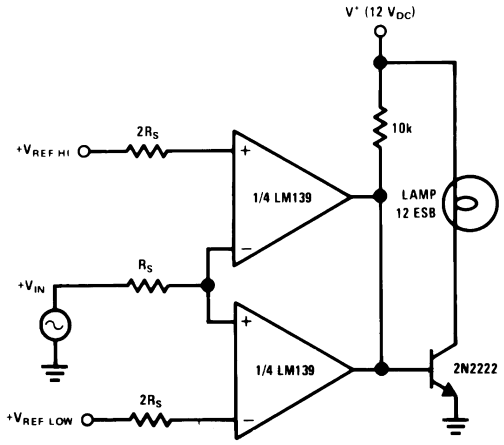


Figure 28. Limit Comparator
(V^+= 15 V_{DC})

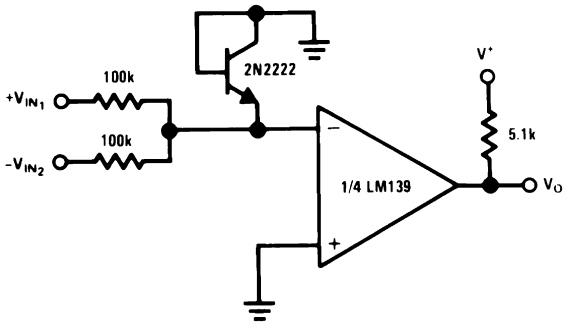
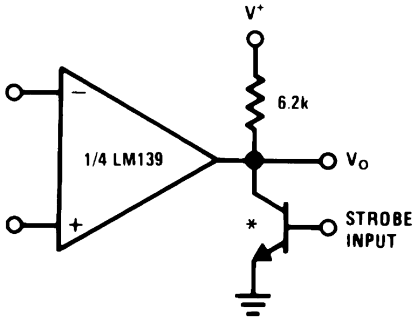


Figure 29. Comparing Input Voltages of Opposite Polarity
(V^+= 15 V_{DC})



* Or open-collector logic gate without pullup resistor

Figure 30. Output Strobing
(V^+= 15 V_{DC})

Typical Applications (continued)

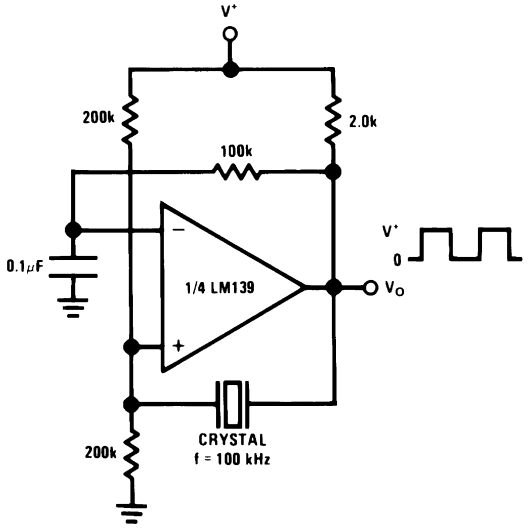
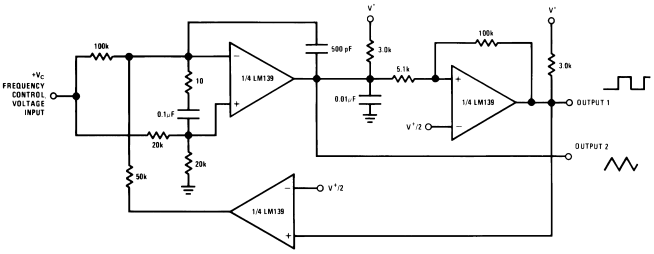


Figure 31. Crystal Controlled Oscillator (V^+= 15 V_{DC})



250 mV_{DC} ≤ V_C ≤ +50 V_{DC}

700 Hz ≤ f_O ≤ 100 kHz

Figure 32. Two-Decade High-Frequency VCO V^+ = +30 V_{DC}

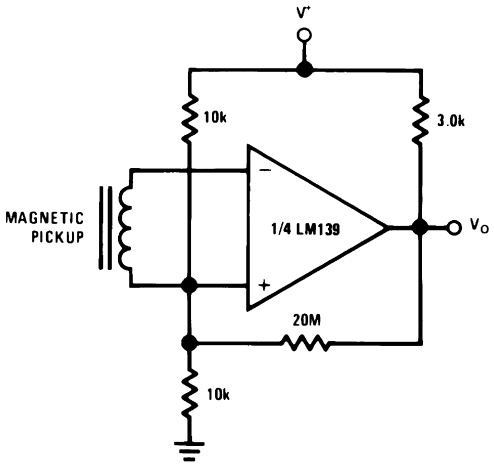


Figure 33. Transducer Amplifier (V^+= 15 V_{DC})

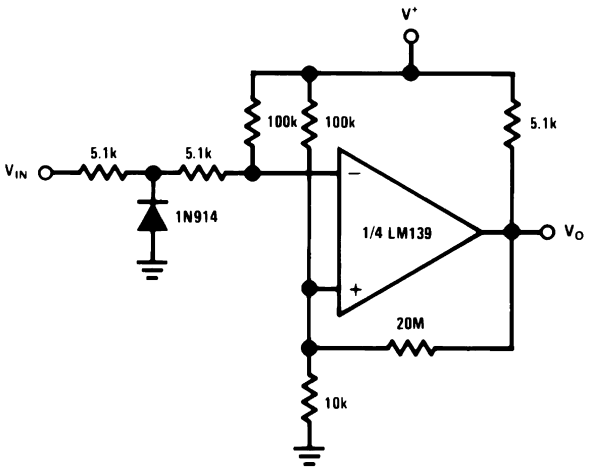


Figure 34. Zero Crossing Detector (Single Power Supply) (V^+= 15 V_{DC})

Typical Applications (continued)

8.2.2.1 Split-Supply Applications

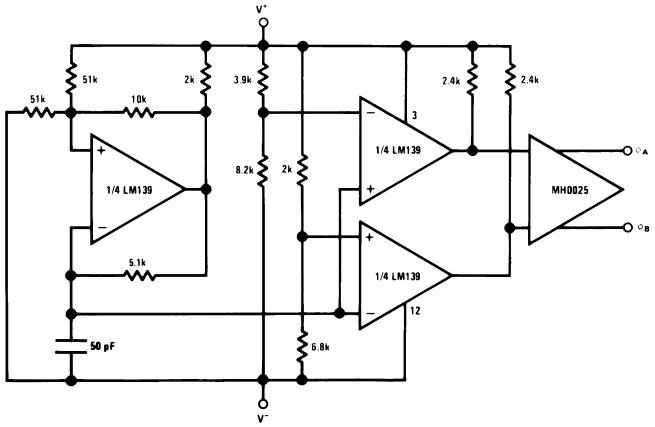


Figure 35. MOS Clock Driver
(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

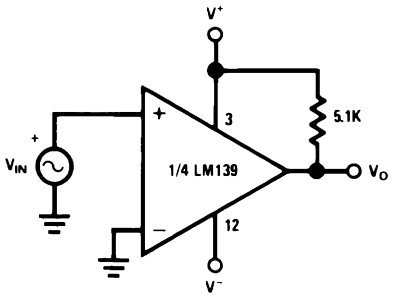


Figure 36. Zero Crossing Detector
(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

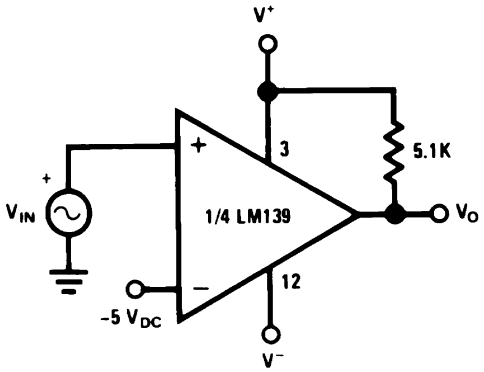


Figure 37. Comparator With a Negative Reference
(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

9 Power Supply Recommendations

Even in low-frequency applications, the LM139-N can have internal transients which are extremely quick. For this reason, bypassing the power supply with 1.0 µF to ground will provide improved performance; the supply bypass capacitor should be placed as close as possible to the supply pin and have a solid connection to ground. The bypass capacitors should have a low ESR.

10 Layout

10.1 Layout Guidelines

Try to minimize parasitic impedances on the inputs to avoid oscillation. Any positive feedback used as hysteresis should place the feedback components as close as possible to the input pins. Take care to ensure that the output pins do not couple to the inputs. This can occur through capacitive coupling if the traces are too close and lead to oscillations on the output.

The optimum bypass capacitor placement is closest to the V+ and ground pins. Take care to minimize the loop area formed by the bypass capacitor connection between V+ and ground. The ground pin should be connected to the PCB ground plane at the pin of the device. The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

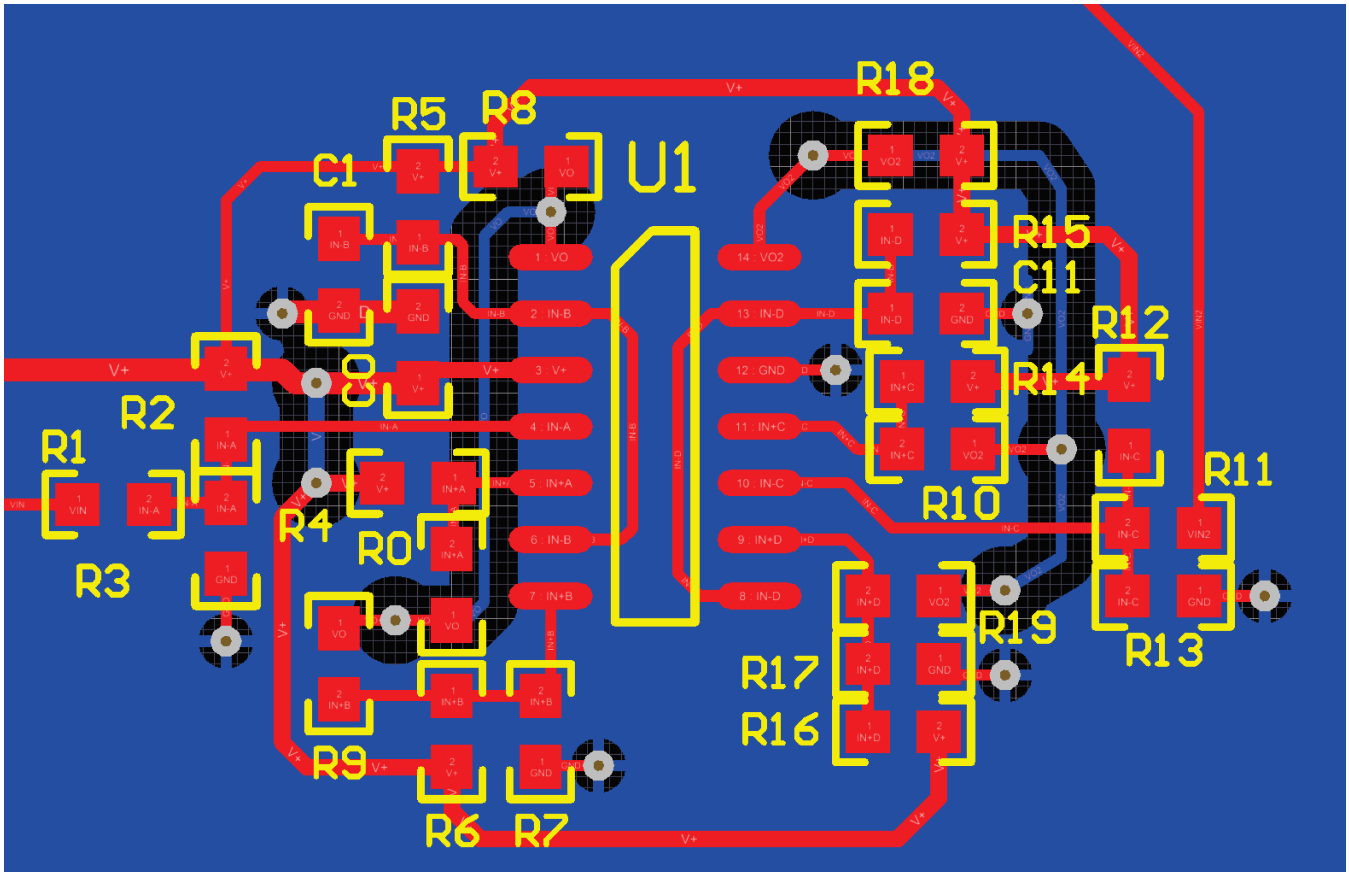


Figure 38. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM139-N	Click here	Click here	Click here	Click here	Click here
LM239-N	Click here	Click here	Click here	Click here	Click here
LM2901-N	Click here	Click here	Click here	Click here	Click here
LM3302-N	Click here	Click here	Click here	Click here	Click here
LM339-N	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM139AJ/PB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM139AJ	Samples
LM139J/PB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM139J	Samples
LM239J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-25 to 85	LM239J	Samples
LM2901M	ACTIVE	SOIC	D	14	55	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM2901M	Samples
LM2901M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LM2901M	Samples
LM2901MX	ACTIVE	SOIC	D	14	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM2901M	Samples
LM2901MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LM2901M	Samples
LM2901N/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM2901N	Samples
LM339AM	ACTIVE	SOIC	D	14	55	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	0 to 70	LM339AM	Samples
LM339AM/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM339AM	Samples
LM339AMX	ACTIVE	SOIC	D	14	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	0 to 70	LM339AM	Samples
LM339AMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM339AM	Samples
LM339AN/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM339AN	Samples
LM339M	ACTIVE	SOIC	D	14	55	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	0 to 70	LM339M	Samples
LM339M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM339M	Samples
LM339MX	ACTIVE	SOIC	D	14	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	0 to 70	LM339M	Samples
LM339MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM339M	Samples
LM339N/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM339N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM139-N, LM2901-N :

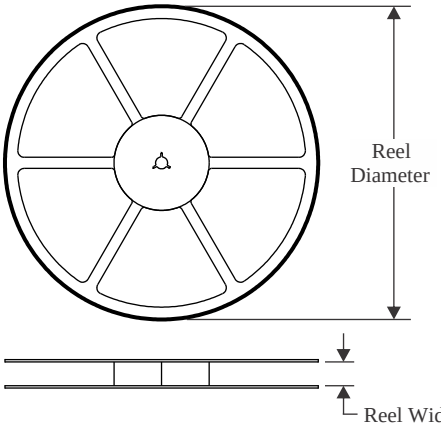
- Automotive : LM2901-Q1
- Space : LM139-SP

NOTE: Qualified Version Definitions:

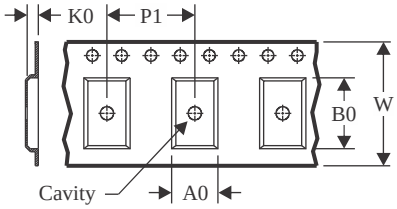
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

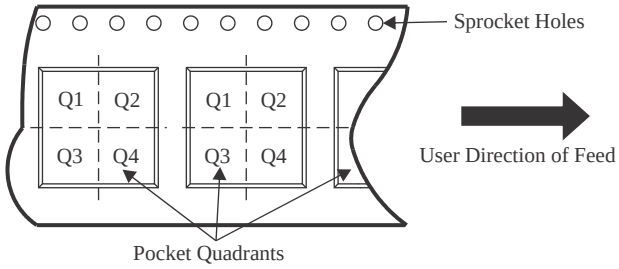


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

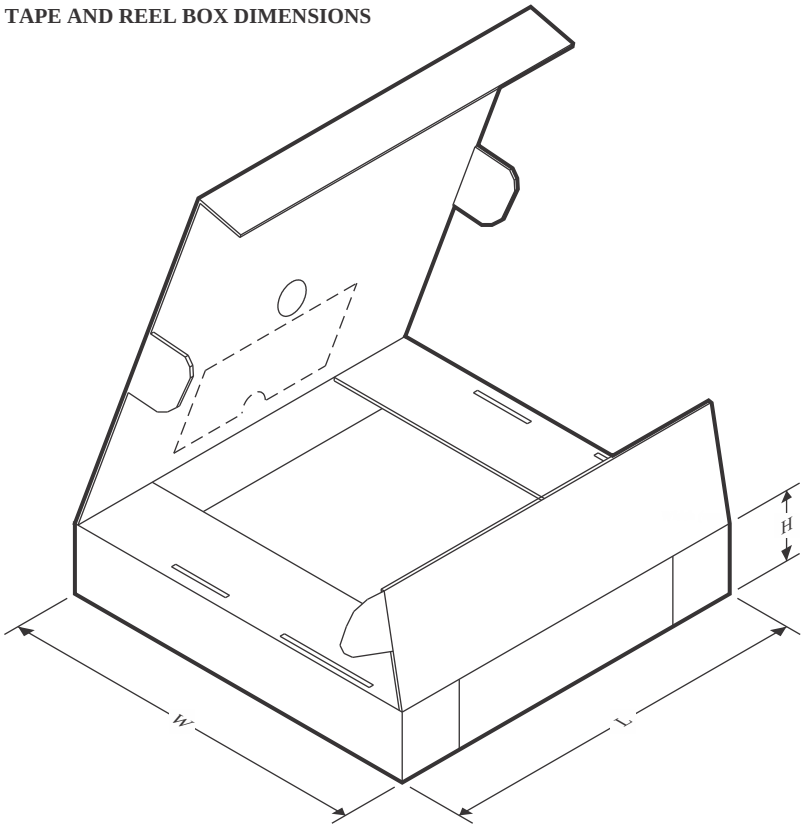
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2901MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM2901MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM339AMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM339AMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM339MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM339MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

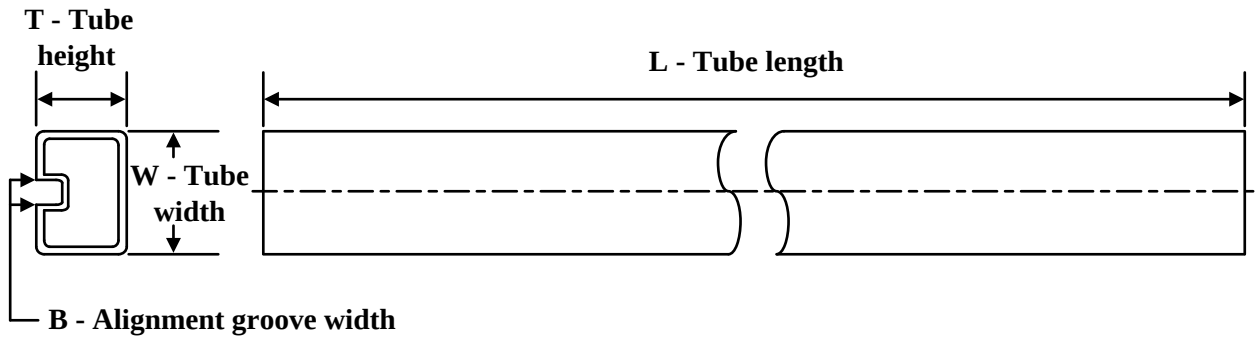
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2901MX	SOIC	D	14	2500	356.0	356.0	35.0
LM2901MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM339AMX	SOIC	D	14	2500	367.0	367.0	35.0
LM339AMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM339MX	SOIC	D	14	2500	367.0	367.0	35.0
LM339MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE



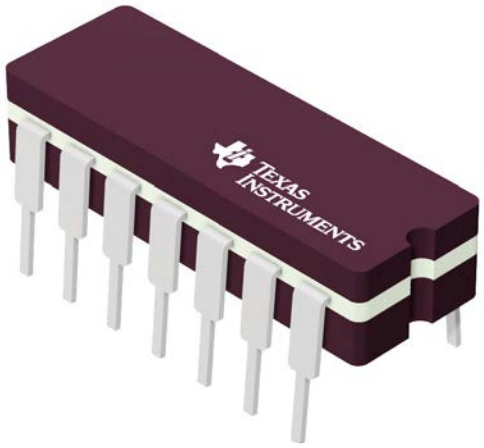
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM139AJ/PB	J	CDIP	14	25	502	14	11938	4.32
LM139J/PB	J	CDIP	14	25	502	14	11938	4.32
LM239J	J	CDIP	14	25	502	14	11938	4.32
LM2901M	D	SOIC	14	55	495	8	4064	3.05
LM2901M	D	SOIC	14	55	495	8	4064	3.05
LM2901M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM2901N/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM339AM	D	SOIC	14	55	495	8	4064	3.05
LM339AM	D	SOIC	14	55	495	8	4064	3.05
LM339AM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM339AN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM339M	D	SOIC	14	55	495	8	4064	3.05
LM339M	D	SOIC	14	55	495	8	4064	3.05
LM339M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM339N/NOPB	N	PDIP	14	25	502	14	11938	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

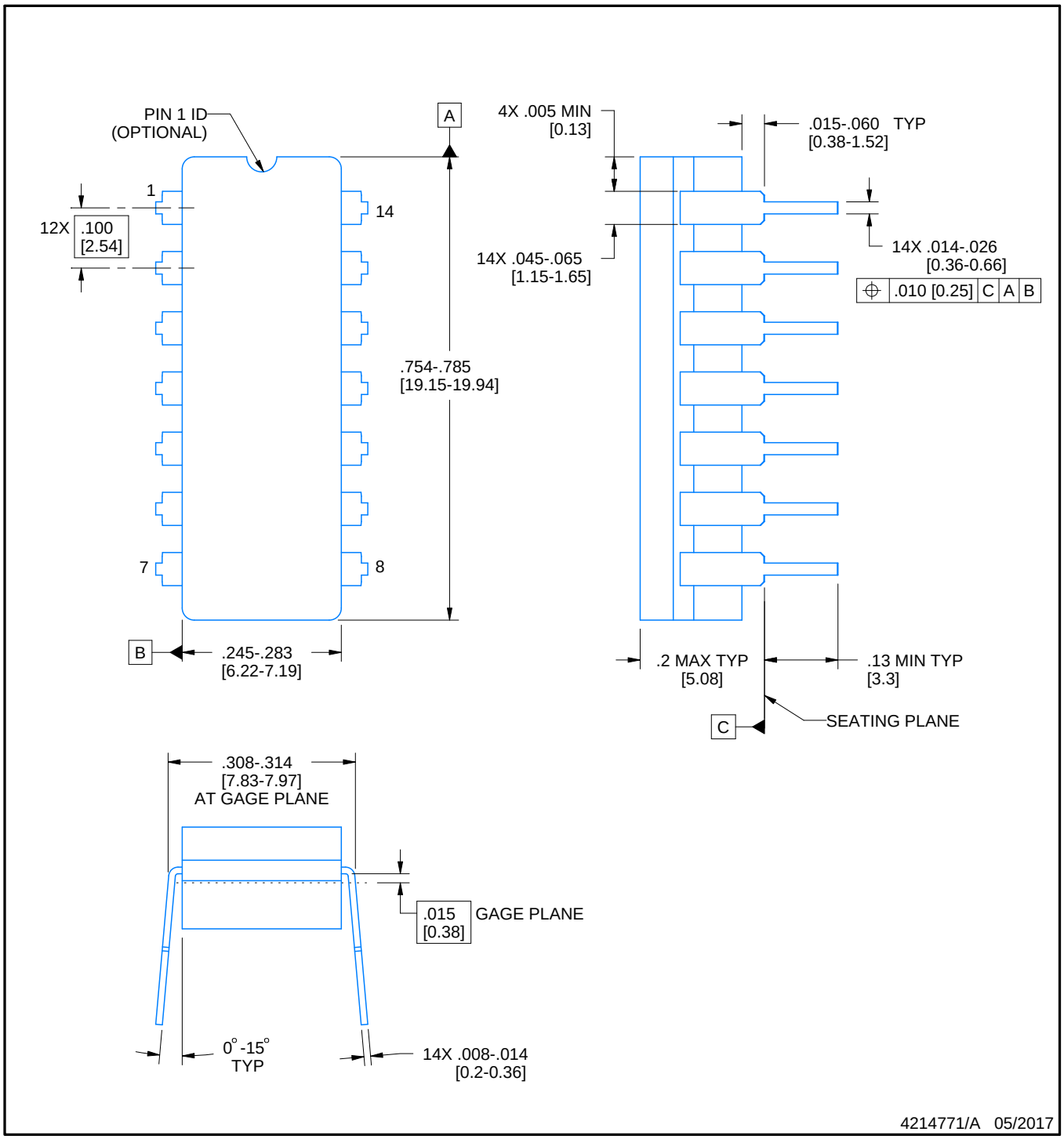
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

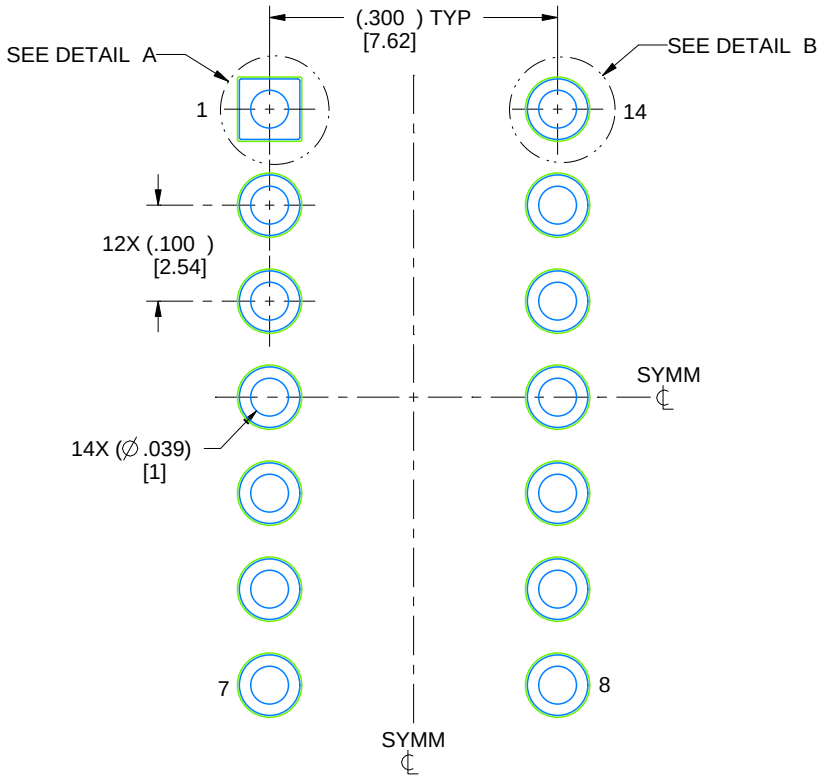
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

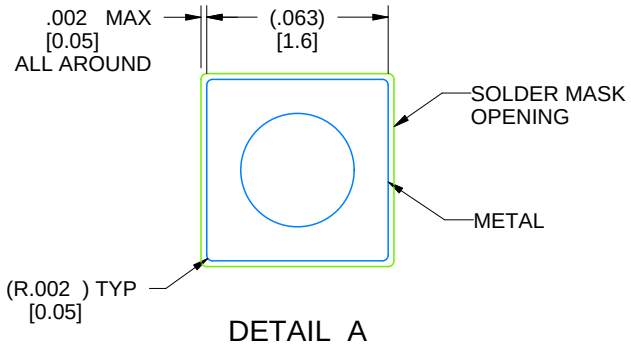
J0014A

CDIP - 5.08 mm max height

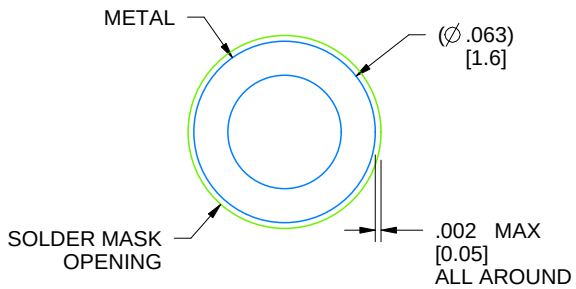
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



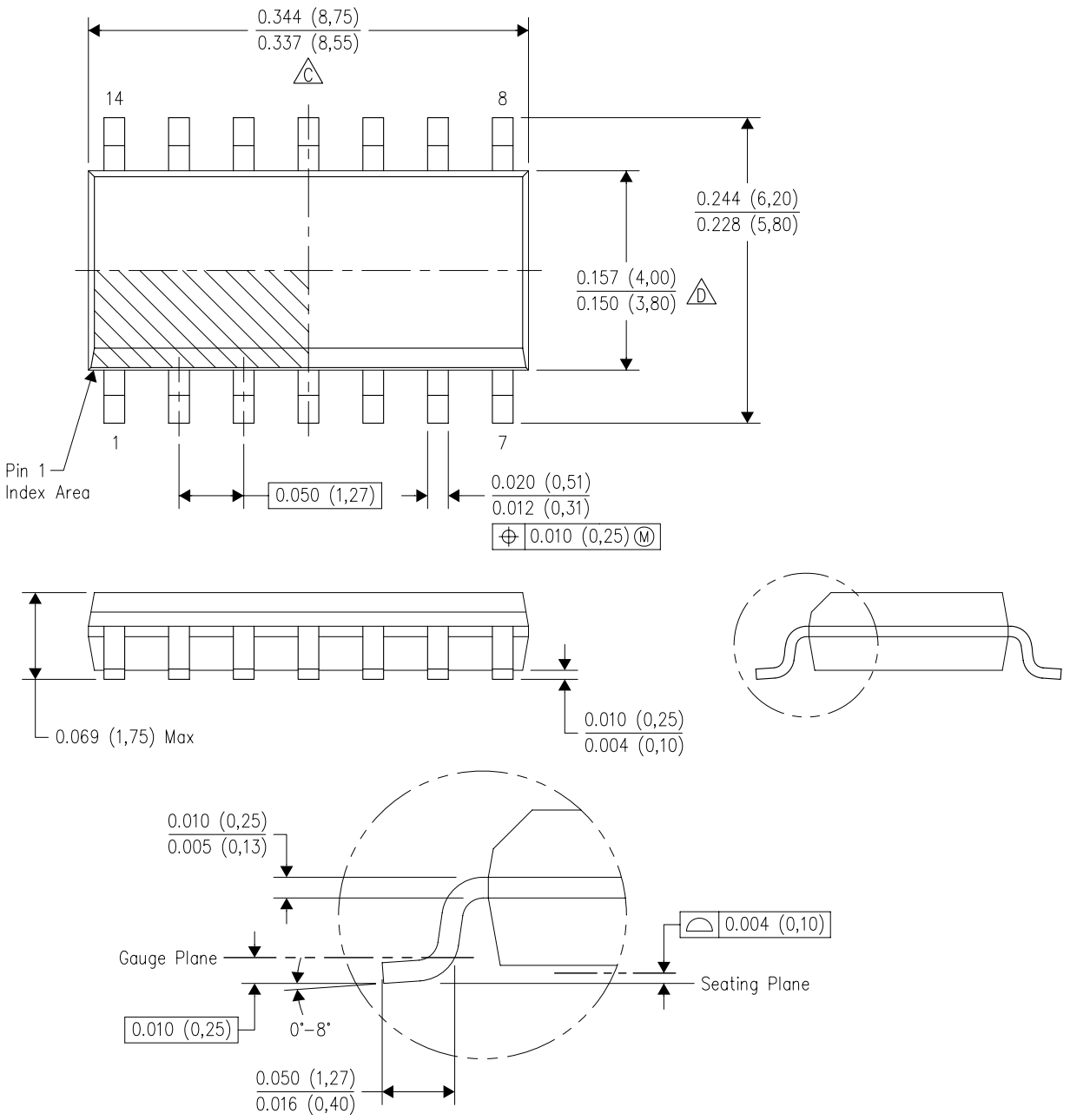
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

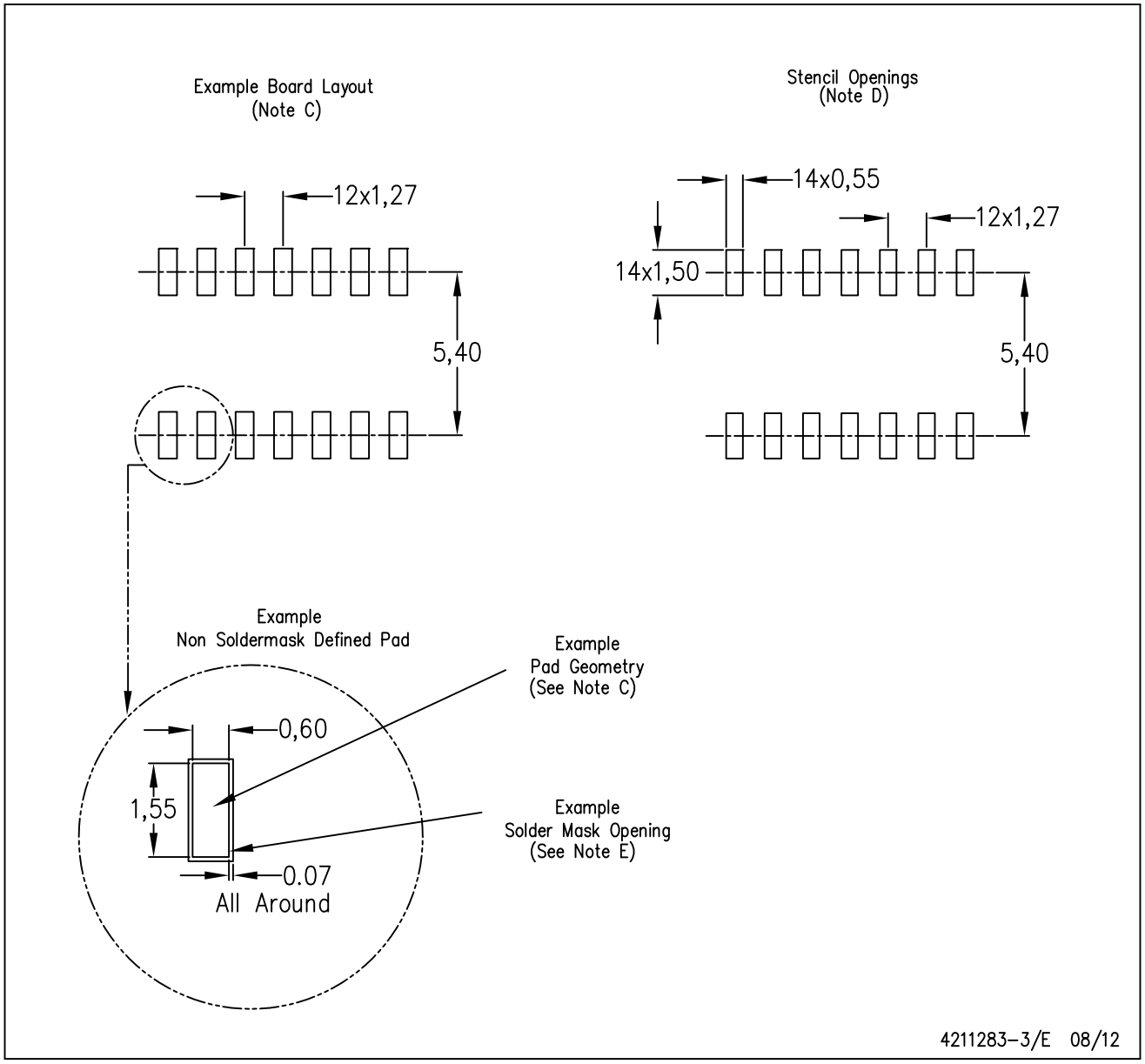
4214771/A 05/2017

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

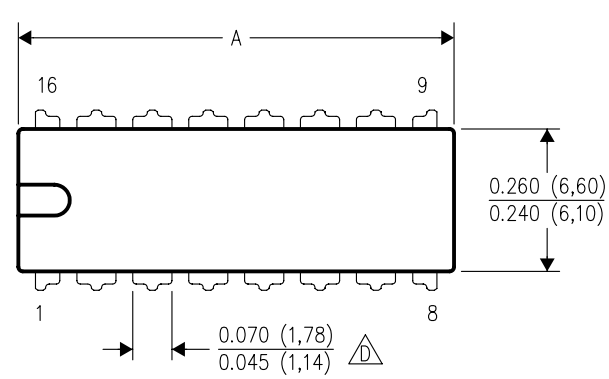


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

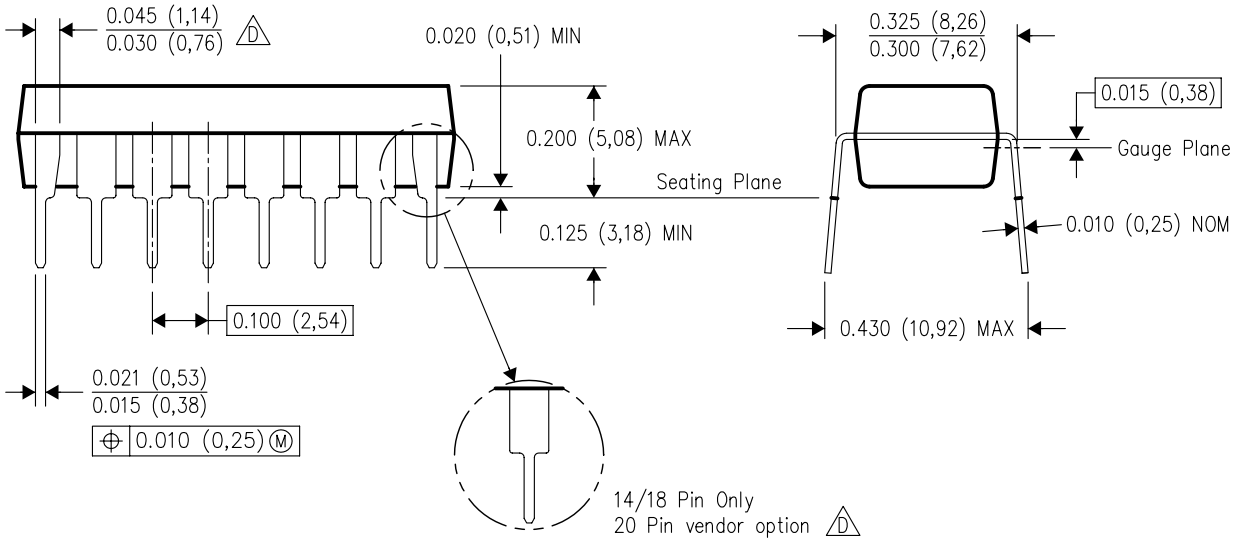
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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