TPS9264x Synchronous Buck Controllers for Precision Dimming LED Drivers

1 Features

- V_{IN} Range from 7 V to 85 V
- Wide Dimming Range
  - 500:1 Analog Dimming
  - 2500:1 Standard PWM Dimming
  - 20000:1 Shunt FET PWM Dimming
- Adjustable LED Current Sense Voltage
- 2-Ω, 1-A_{peak} MOSFET Gate Drivers
- Shunt Dimming MOSFET Gate Driver (TPS92641)
- Programmable Switching Frequency
- Precision Voltage Reference 3 V ±2%
- Input UVLO and Output OVP
- Low Power Shutdown Mode and Thermal Shutdown

2 Applications

- LED Driver / Constant Current Regulator
- Architectural LED Lighting Drivers
- Automotive LED Drivers
- General LED Illumination

3 Description

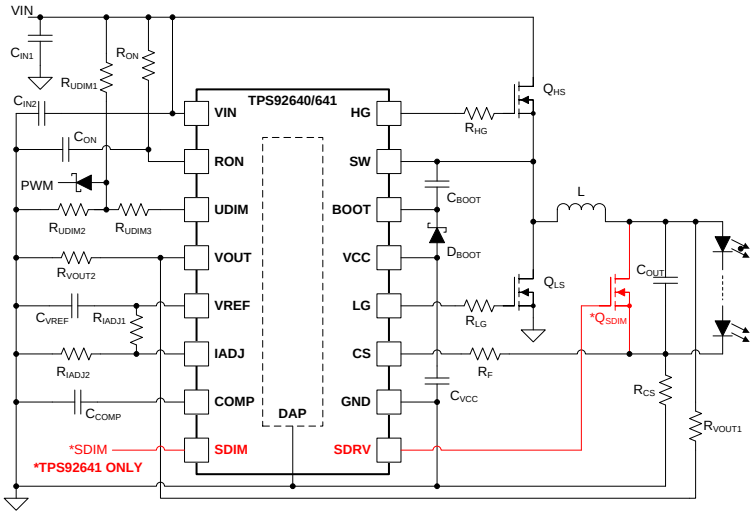
The TPS92640 and TPS92641 devices are high-voltage, synchronous NFET controllers for buck-current regulators. Output current regulation is based on valley current-mode operation using a controlled on-time architecture. This control method eases the design of loop compensation while maintaining nearly constant switching frequency. The TPS92640 and TPS92641 devices include a high-voltage start-up regulator that operates over a wide input range of 7 V to 85 V. The PWM controller is designed for high speed capability, including an oscillator frequency range up to 1 MHz. The deadtime between high side and low side gate driver is optimized to provide very high efficiency over a wide input operating voltage and output power range. The TPS92640 and TPS92641 devices accept both analog and PWM input signals, resulting in exceptional dimming control range. Linear response characteristics between input command and LED current is achieved with true zero LED current using low off-set error amplifier and proprietary PWM dimming logic. Both devices also include precision reference capable of supplying current to low power microcontroller. Protection features include cycle-by-cycle current protection, overvoltage protection, and thermal shutdown. The TPS92641 device includes a shunt FET dimming input and MOSFET driver for high resolution PWM dimming.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92640	HTSSOP (14)	4.40 mm × 5.00 mm
TPS92641	HTSSOP (16)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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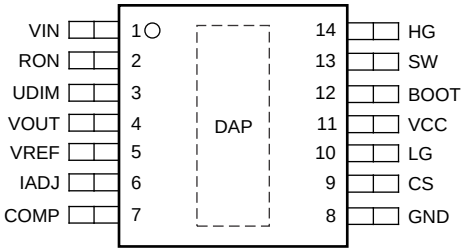
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

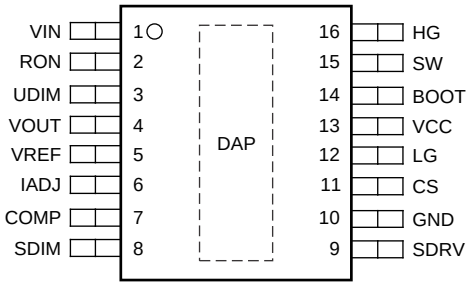
Changes from Original (October 2012) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

TPS92640 PWP Package
14-Pin HTSSOP
Top View



TPS92641 PWP Package
16-Pin HTSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. (TPS92640)	NO. (TPS92641)		
BOOT	12	14	O	Connect 100-nF ceramic capacitor to switch node and diode to VCC to provide boosted voltage for high-side gate drive.
COMP	7	7	O	Connect ceramic capacitor to GND to set loop compensation.
CS	9	11	I	Connect to positive terminal of sense resistor at the bottom of the LED stack.
GND	8	10	—	System GND. Connect to DAP.
HG	14	16	O	Connect to gate of high-side NFET of buck regulator. Use series resistor to limit current slew-rate and mitigate EMI noise.
IADJ	6	6	I	Connect resistor divider from VREF to set analog dimming level. Use NTC resistor from pin to GND as resistor divider to implement thermal foldback operation.
LG	10	12	O	Connect to gate of low-side NFET of buck regulator. Use series resistor to limit current slew-rate and mitigate EMI noise.
RON	2	2	I	Connect a resistor to VIN and capacitor to GND to set switching frequency.
SDIM	—	8	I	PWM dimming input for shunt FET dimming.
SDRV	—	9	O	Connect to gate of external parallel NFET across LED load used for shunt dimming if desired.
SW	13	15	O	Connect to switch node of buck regulator.
UDIM	3	3	I	Connect resistor divider from VIN to set undervoltage lockout threshold.
VCC	11	13	O	Bypass with 2.2-µF ceramic capacitor to provide bias supply for controller.
VIN	1	1	I	Connect to input voltage. Connect 1-µF bypass capacitor
VOUT	4	4	I	Connect resistor divider from V_{OUT}, scaled down feedback of V_{OUT}.
VREF	5	5	O	System reference voltage. Bypass with 100-nF ceramic capacitor.
DAP	—	—	—	Place 6-9 vias from pad to GND plane for thermal relief.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}, UDIM, SW	–0.3	90	V
		–1	mA
BOOT	–0.3	98.5	V
HG	–0.3	90	V
		–2.5 (Pulse < 100 ns)	V
LG, SDRV, CS	–0.3	$+V_{CC}$	V
		–2.5 (Pulse < 100 ns)	V
		V_{CC} + 2.5 (Pulse < 100 ns)	V
V_{CC}	–0.3	15	V
VREF, RON, COMP, VOUT, IADJ, SDIM	–0.3	6	V
	–200	200	µA
GND	–0.3	0.3	V
	–2.5 (Pulse < 100 ns)	2.5 (Pulse < 100 ns)	V
Continuous power dissipation		Internally Limited	
Maximum lead temperature (soldering and reflow) (2)		260	°C
Maximum junction temperature	–40	125	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to TI's packaging website for more detailed information and mounting techniques.

6.2 ESD Ratings

			VALUE	UNIT
TPS92640 PWP PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
TPS92641 PWP PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	7		85	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS92640 PWP (HTSSOP) 14 PINS	TPS92641 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.1	38.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.6	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.9	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.7	16.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified V_{IN} = 24 V. Typical specifications apply for $T_A = T_J$ = 25°C.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
START-UP REGULATOR (V_{CC}, V_{IN})						
V_{CCREG}	V_{CC} Regulation	I_{CC} = 10 mA, V_{IN} = 24 V, 85 V	7.86	8.5	9.14	V
I_{CCLIM}	V_{CC} Current Limit	V_{CC} = 0 V	48	63	78	mA
I_Q	Quiescent Current	V_{UDIM} = 3 V, Static V_{IN} = 7 V, 24 V, 85 V		2	3	mA
I_{SD}	Shutdown Current	V_{UDIM} = 0 V		100		µA
V_{CC-UV}	V_{CC} UVLO Threshold	V_{CC} increasing		5.04	5.9	V
		V_{CC} decreasing	4.5	4.9		
V_{CC-HYS}	V_{CC} UVLO Hysteresis			0.17		V
REFERENCE VOLTAGE (V_{REF})						
V_{REF}	Reference Voltage	No Load, V_{IN} = 7 V, 24 V, 85 V	2.97	3.03	3.09	V
$I_{VREFLIM}$	Current Limit	V_{REF} = 0 V	1.3	2.1	2.9	mA
ERROR AMPLIFIER (CS, COMP)						
V_{CSREF}	CS Reference Voltage	With respect to GND		V_{IADJ}/10		V
$V_{CSREF-OFF}$	Error Amp Input Offset Voltage		–600	0	600	µV
I_{COMP}	COMP Sink Current			85		µA
	COMP Source Current			110		µA
g_{M-CS}	Transconductance			500		µA/V
	Linear Input Range	See (3)		±125		mV
	Transconductance Bandwidth	–6-dB unloaded response(3)		400		kHz
TIMERS / OVERVOLTAGE PROTECTION (RON, VOUT)						
$t_{OFF-MIN}$	Minimum Off-time	CS = 0 V		230		ns
t_{ON-MIN}	Minimum On-time			235		ns
t_{ON}	Programmed On-time	V_{VOUT} = 2 V, R_{ON} = 25 kΩ, C_{ON} = 1 nF		2.08		µs
R_{RON}	RON Pulldown Resistance			35	120	Ω
t_{CL}	Current Limit Off-time			270		µs
t_{D-ON}	RON Thresh - HG Falling Delay			25		ns
V_{TH-OVP}	VOUT Overvoltage Threshold	VOUT rising	2.85	3.05	3.25	V
$V_{HYS-OVP}$	VOUT Overvoltage Hysteresis			0.13		V
GATE DRIVER (HG, LG, BOOT, SW)						
R_{SRC-LG}	LG Sourcing Resistance	LG = High		1.5	6	Ω
R_{SNK-LG}	LG Sinking Resistance	LG = Low		1	4.5	Ω
R_{SRC-HG}	HG Sourcing Resistance	HG = High		3.9	6	Ω
R_{SNK-HG}	HG Sinking Resistance	HG = Low		1.1	4.5	Ω
$V_{TH-BOOT}$	BOOT UVLO Threshold	BOOT-SW rising	1.9	3.4	4.5	V
$V_{HYS-BOOT}$	BOOT UVLO Hysteresis	BOOT-SW falling		1.8		V
T_{D-HL}	HG to LG deadtime	HG fall to LG rise		60		ns
T_{D-LH}	LG to HG deadtime	LG fall to HG rise		60		ns

(1) All limits specified at room temperature (TYP values) and at temperature extremes (MIN/MAX values). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) These electrical parameters are specified by design, and are not verified by test.

Electrical Characteristics (continued)

Unless otherwise specified V_{IN} = 24 V. Typical specifications apply for $T_A = T_J$ = 25°C.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
PWM DIMMING (SDIM, SDRV) (TPS92641 only)						
$R_{SRC-DDRV}$	SDRV Sourcing Resistance	SDRV = High		5.6	30	Ω
$t_{SDIM-RIS}$	SDIM to SDRV Rising Delay	SDIM rising		68	100	ns
$t_{SDIM -FALL}$	SDIM to SDRV Falling Delay	SDIM falling		29	70	ns
$V_{SDIM-RIS}$	SDIM Rising Threshold	SDIM rising		1.29	1.74	V
$V_{SDIM -FALL}$	SDIM Falling Threshold	SDIM falling	0.5			V
$R_{SDIM-PU}$	SDIM Pullup Resistance			90		kΩ
ANALOG ADJUST (IADJ)						
$V_{ADJ-MAX}$	IADJ Clamp Voltage		2.46	2.54	2.62	V
R_{ADJ}	IADJ Input Impedance			1		MΩ
UNDERVOLTAGE / PWM (UDIM)						
$V_{TH-UDIM}$	UDIM Start-up Threshold	UDIM rising	1.21	1.276	1.342	V
$I_{HYS-UDIM}$	UDIM Hysteresis Current		12	21	30	µA
$t_{UDIM-RIS}$	UDIM to HG/LG Rising Delay	UDIM rising		168	260	ns
$t_{UDIM-FALL}$	UDIM to HG/LG Falling Delay	UDIM falling		174	280	ns
$V_{UDIM-LP}$	UDIM Low Power Threshold			370		mV
$T_{UDIM-DET}$	UDIM Shutdown Detect Timer	UDIM falling	8.5	13		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold	See (3)		165		°C
T_{HYS}	Thermal Shutdown Hysteresis	See (3)		20		°C

6.6 Typical Characteristics

Unless otherwise stated, –40°C ≤ $T_A = T_J$ ≤ 125°C, V_{IN} = 24 V, V_{IADJ}= 2 V, I_{LED} = 1 A, C_{VCC} = 2.2 µF, C_{COMP} = 0.47 µF

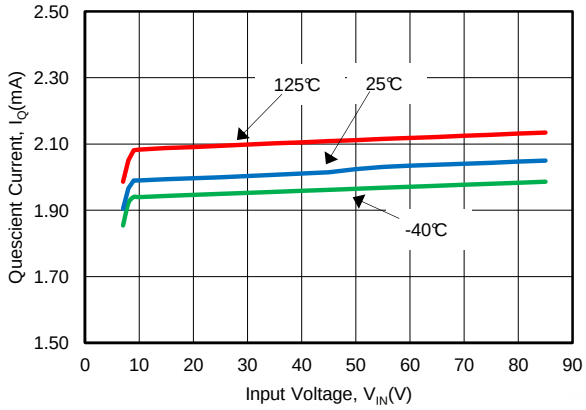


Figure 1. Quescient Current, I_Q vs Input Voltage, V_{IN}

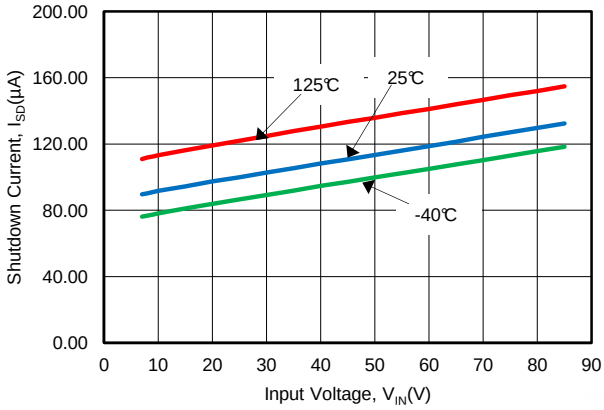


Figure 2. Shutdown Current, I_{SD}vs Input Voltage , V_{IN}

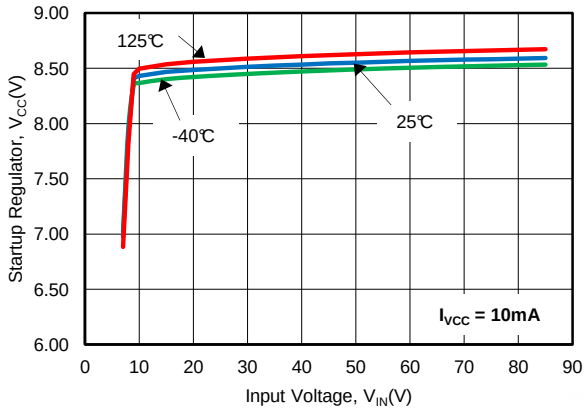


Figure 3. Start-Up Regulator, V_{CC} vs Input Voltage, V_{IN}

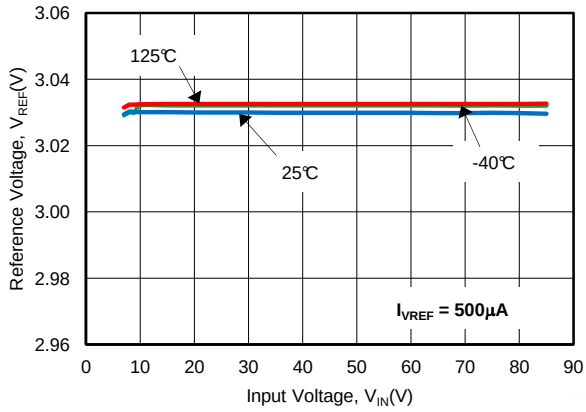


Figure 4. Reference Voltage, V_{REF} vs Input Voltage, V_{IN}

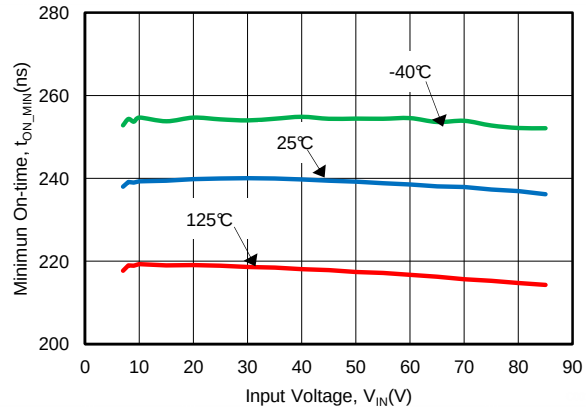


Figure 5. Minimum On-time, t_{ON_MIN} vs Input Voltage, V_{IN}

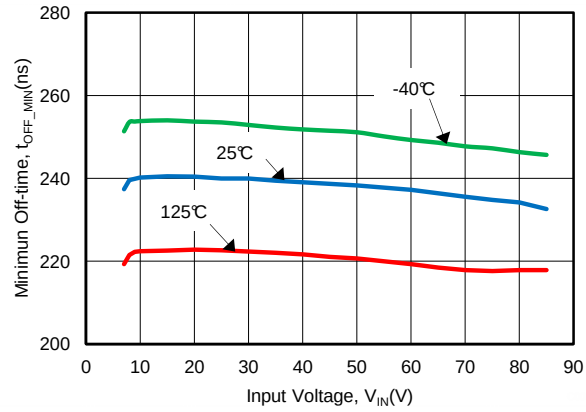


Figure 6. Minimum Off-time, t_{OFF_MIN} vs Input Voltage, V_{IN}

Typical Characteristics (continued)

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ 125°C, V_{IN} = 24 V, V_{IADJ}= 2 V, I_{LED} = 1 A, C_{VCC} = 2.2 µF, C_{COMP} = 0.47 µF

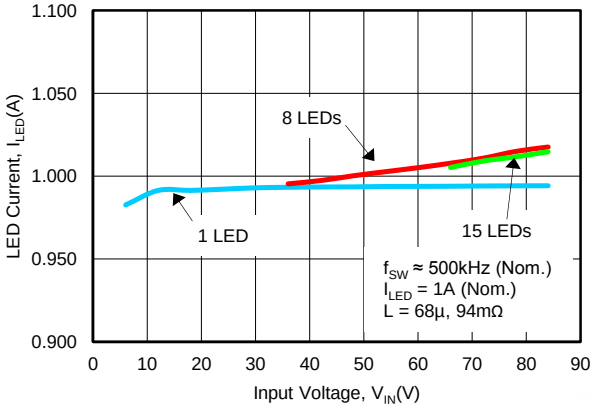


Figure 7. LED Current, I_{LED} vs Input Voltage, V_{IN}

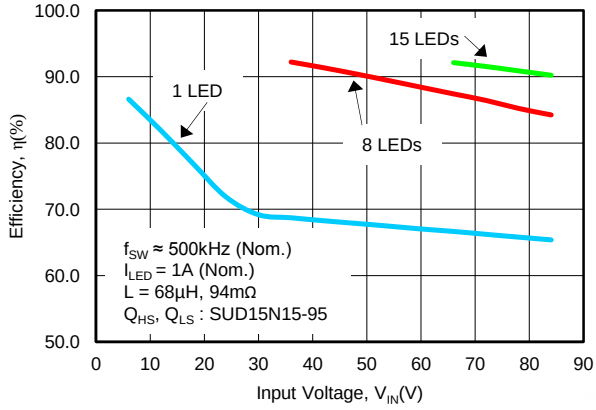


Figure 8. Conversion Efficiency, η vs Input Voltage, V_{IN}

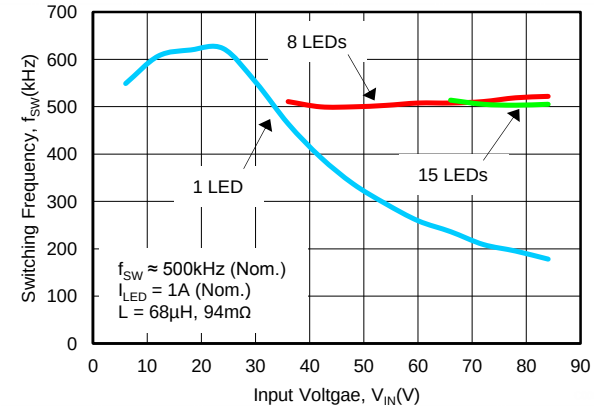


Figure 9. Converter Switching Frequency, f_{SW} vs Input Voltage, V_{IN}

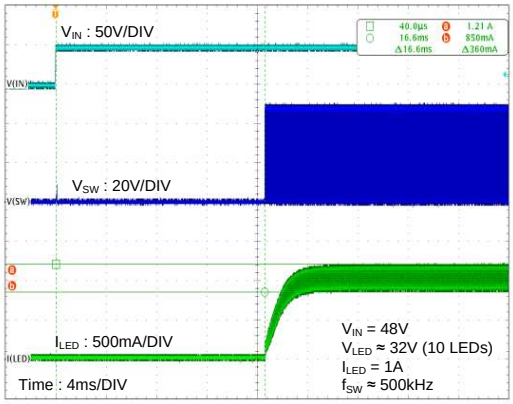


Figure 10. Waveforms of Power-Up Transient

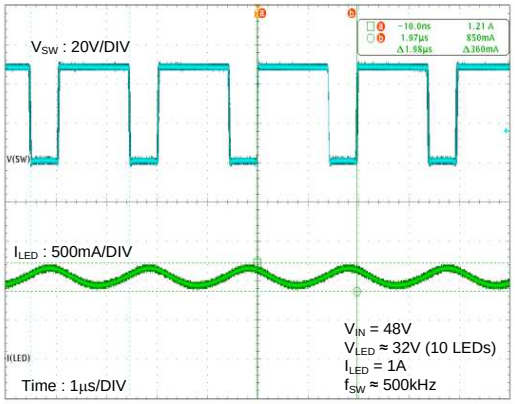


Figure 11. Waveforms of Steady-State Operation

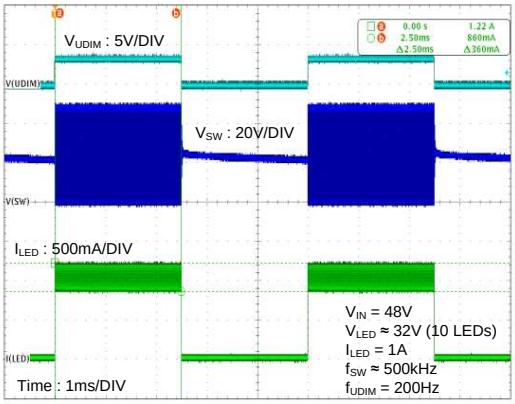


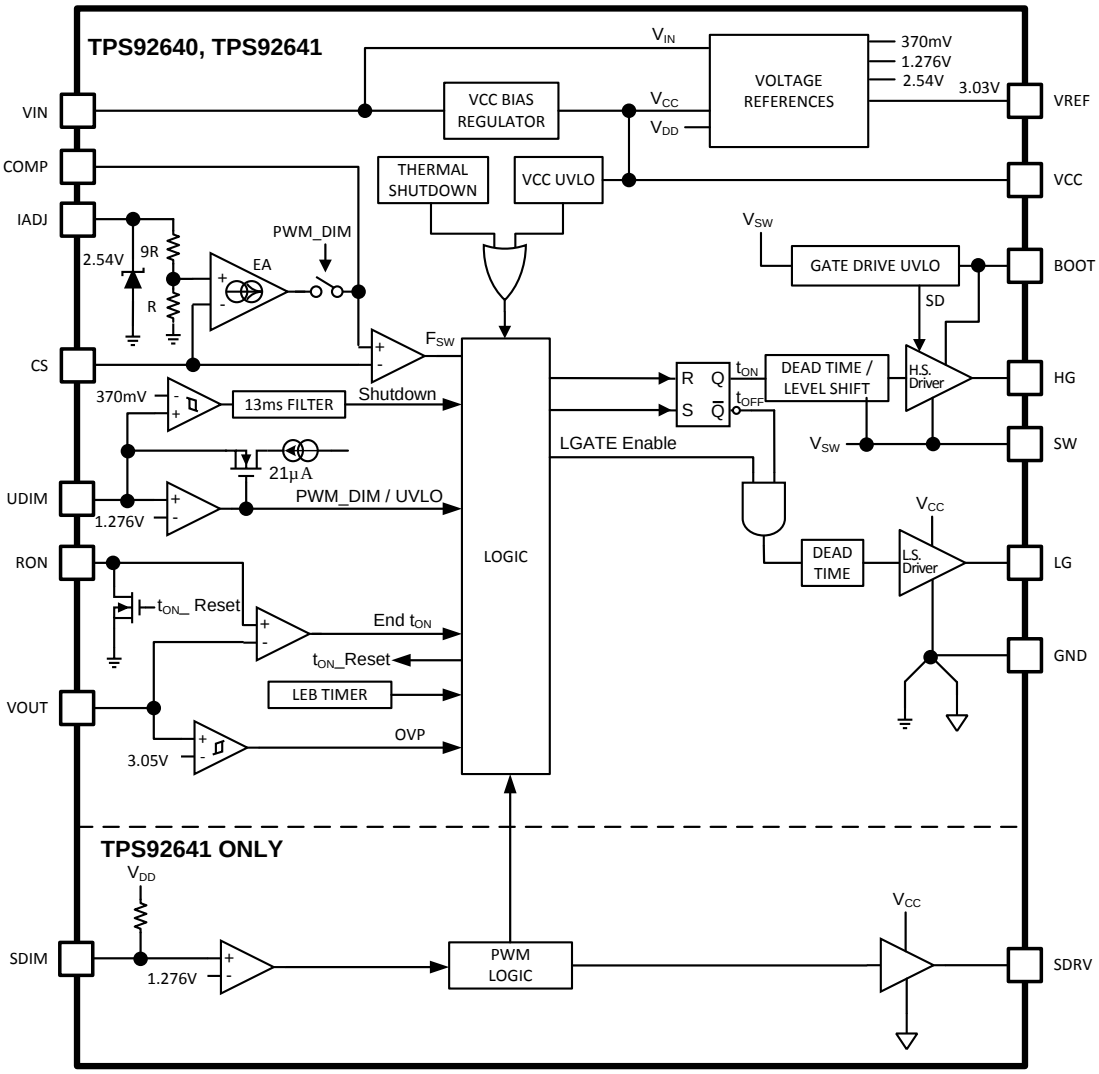
Figure 12. Waveforms of UDIM Operation (D_{DIM} = 0.5)

7 Detailed Description

7.1 Overview

The TPS92640 and TPS92641 devices are synchronous N-channel MOSFET (NFET) controllers for step-down (buck) current regulators, which are ideal for driving LED loads. They can accept wide input voltage range allowing for greater flexibility in powering different series connected LED string combinations. The single current sense pin with low adjustable threshold voltage provides an excellent method for regulating LED current while maintaining high system efficiency. The TPS92640 and TPS92641 devices use valley current control with a controlled on-time architecture that allows the converter to be operated at nearly constant switching frequency without the need for slope compensation. The extremely accurate adjustable current sense threshold together with the synchronous operation provides the capability to amplitude (analog) dim the LED current with high contrast ratios. Excellent PWM dimming is attainable using the main NFETs or the external shunt FET driver (TPS92641 only). The TPS92640 and TPS92641 devices incorporate 2-Ω, 1-A internal gate drivers and supports constant current operation up to 5 A. This simple controller contains all the features necessary to implement a high-efficiency, versatile LED driver with precise dimming response.

7.2 Functional Block Diagram



7.3 Feature Description

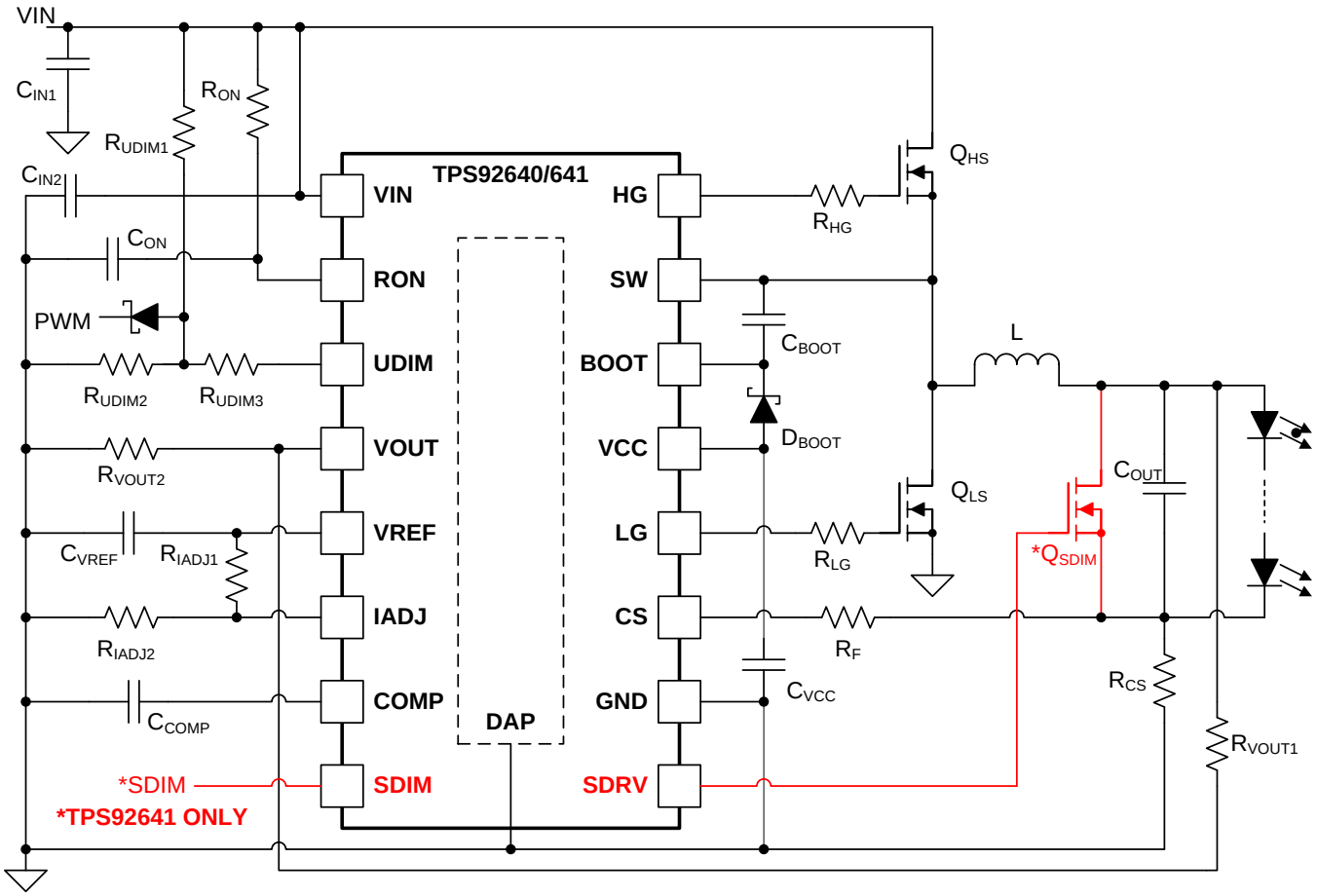


Figure 13. Synchronous Buck LED Driver

7.3.1 Controlled On-Time Architecture

The control architecture is a combination of valley current control and a one-shot on-timer that varies with input and output voltage. The TPS92640 and TPS92641 devices use a series resistor in the LED path to sense both average LED current and valley inductor current. During the time that the high side NFET is turned on (t_{ON}), the input voltage charges up the inductor. When it is turned off (t_{OFF}) and the low side NFET is turned on, the inductor discharges. During both intervals, the current is supplied to the load keeping the LEDs forward biased. Figure 14 shows the inductor current (i_L) waveform for a buck converter operating in continuous conduction mode (CCM). As the system changes input voltage or output voltage, duty cycle D is varied indirectly by changing both t_{ON} and t_{OFF} to regulate I_L and ultimately I_{LED}. For any buck regulator, duty cycle, D, is calculated using Equation 1.

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{V_{OUT}}{\eta \times V_{IN}}$$

$$V_{OUT} = V_{LED} + V_{CS}$$

where

- V_{CS} is the voltage measured at the CS pin of the IC and η is the estimated or actual converter efficiency. (1)

Feature Description (continued)

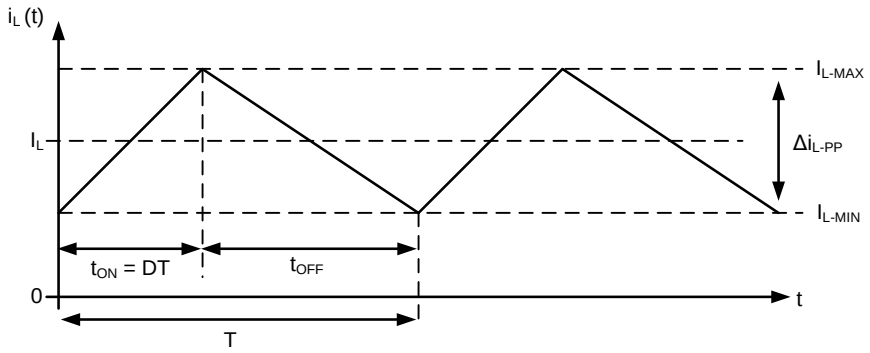


Figure 14. Ideal CCM Buck Converter Inductor Current I_L Waveform

7.3.2 Switching Frequency

The on-time is determined based on the external resistor (R_{ON}) connected between RON and VIN pins in combination with a capacitor (C_{ON}) between RON and GND pins. The input voltage and the R_{ON} resistor set the current sourced into the R_{ON} capacitor which governs the ramp speed. The ramp threshold is proportional to scaled down feedback of V_{OUT} at VOUT pin. The proportionality of V_{OUT} is set by an external resistor divider (R_{VOUT1}, R_{VOUT2}) from V_{OUT}. The switching frequency, f_{SW} can be calculated based on on-time and off-time using Equation 2.

$$\frac{V_{IN}}{R_{ON}} = C_{ON} \times \frac{V_{OUT} \times \frac{R_{VOUT\,2}}{\left(R_{VOUT\,1} + R_{VOUT\,2}\right)}}{t_{ON}}$$

$$\frac{V_{IN}}{R_{ON}} = C_{ON} \times \frac{V_{IN} \times \frac{t_{ON}}{T} \times \frac{R_{VOUT\,2}}{\left(R_{VOUT\,1} + R_{VOUT\,2}\right)}}{t_{ON}}$$

$$f_{SW} = \frac{1}{T} = \frac{\left(R_{VOUT\,1} + R_{VOUT\,2}\right)}{R_{VOUT\,2}} \times \frac{1}{R_{ON} \times C_{ON}} \quad (2)$$

Even though the on-time control is quasi-hysteretic, the input and output voltage proportionality creates a nearly constant switching frequency over the entire operating range. Quasi-hysteretic control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. It also mitigates current mode instability (also known as sub-harmonic oscillation) found in standard fixed frequency current mode control when operating near or above 50% duty cycle. The inductor current sensing and averaging mechanism in the valley detection control loop provides highly accurate LED current regulation over the entire operating range and temperature.

7.3.3 Average LED Current

Average LED current regulation is set using a sense resistor in series with the LEDs. The internal error-amplifer regulates the voltage across the sense resistor (V_{CS}) to the IADJ voltage divided by 10. The error amplifier input offset voltage has been minimized using auto-zero calibration technique as shown in . In this chopping scheme, the noninverting and inverting inputs and outputs change polarity every switching cycle to cancel the offset, providing near zero input offset voltage.

Feature Description (continued)

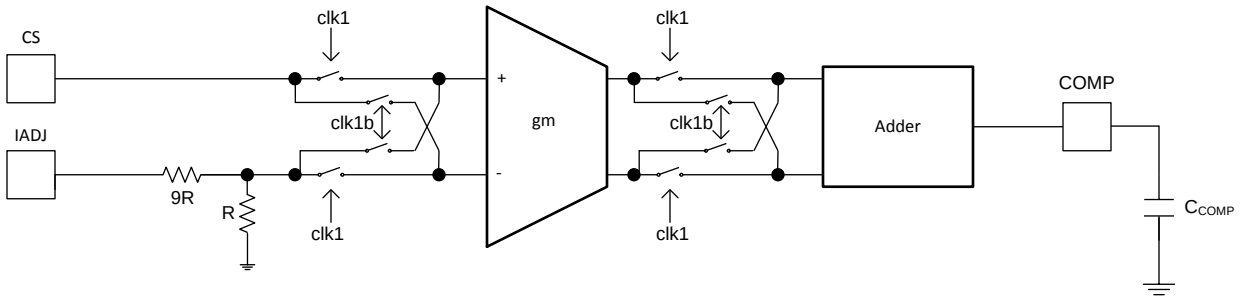


Figure 15. Working Principle of the Chopper OTA to Minimize Input Offset Voltage

IADJ can be set to any value up to 2.54 V by connecting it to VREF through a resistor divider for static output current settings. IADJ can also be used to change the regulation point if connected to a controlled voltage source or potentiometer to provide analog dimming. It is also possible to configure IADJ to be used for thermal foldback functions.

$$I_{LED} = \frac{V_{CS}}{R_{CS}} \quad (3)$$

$$V_{CS} = \frac{V_{IADJ}}{10} \quad (4)$$

7.3.4 Analog Dimming and True-Zero Operation

In traditional Buck converters, discontinuous conduction mode (DCM) operation of inductor current results in loss of linearity at low dimming levels and limits the analog dimming range. When using TPS92640 and TPS92641 devices to implement synchronous buck converter, the inductor current is forced to maintain continuous conduction mode (CCM). As a result, it is possible to maintain linearity and achieve true-zero LED current operation with respect to analog dimming command. For true zero application, an external capacitor is required across the LED string to provide a negative current path for the inductor current loop. Figure 16 shows the inductor current (I_L) and output voltage (V_{OUT}) waveform for a buck converter operating at true zero average current level.

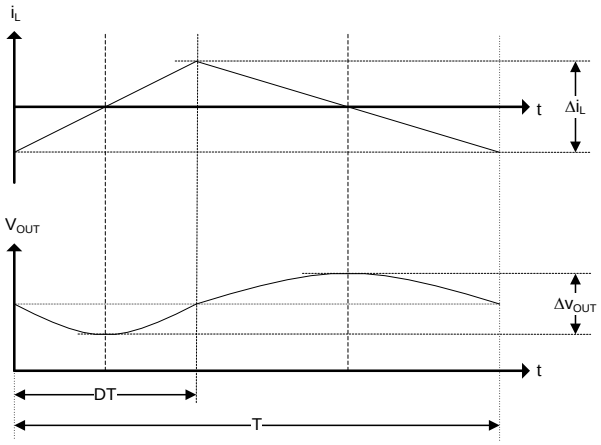


Figure 16. True Zero CCM Buck Converter Inductor Current I_L and Output Voltage V_{OUT} Waveform

In true zero application (V_{IADJ}=0 V), there will be a certain amount of I_{LED} passing the LEDs even though the average inductor current is well-regulated at 0-A set-point. The shaped area in Figure 17 shows the current that will pass through the LED string (i_{LED}).

Feature Description (continued)

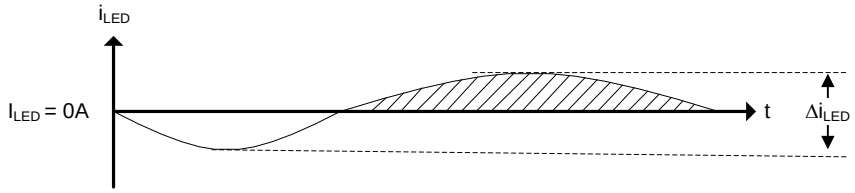


Figure 17. Output Current Waveform in True Zero Application with V_{IADJ} = 0 V

An external resistor, R_{OFF} as shown in Figure 18 is recommended from V_{OUT} to CS to shunt the positive current ripple while maintaining the operation of error amplifier to cancel input offset voltage. The shunt current (I_{OFF}) should be at least half of the output current ripple to ensure proper operation.

$$I_{OFF} = \frac{V_{OUT}}{R_{OFF} + R_F + R_{CS}} > 0.5 \times \Delta I_{LED}$$

$$R_{OFF} < \frac{V_{OUT}}{0.5 \times \Delta I_{LED}} - (R_F + R_{CS}) \quad (5)$$

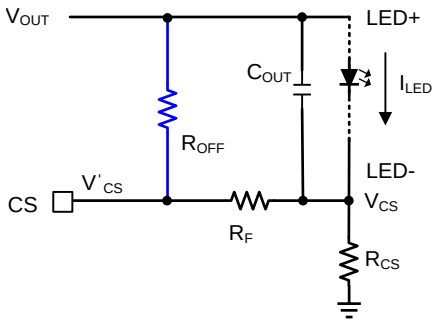


Figure 18. R_{OFF} for True Zero Application

The resistor R_{OFF} also impacts the start-up behavior of the circuit as it creates an DC shift in the voltage sensed at CS pin. To ensure proper start-up sequence and monotonic LED current behavior, the voltage V'_{CS} should exceed a threshold voltage based on the native offset of the error amplifier before V_{OUT} exceeding the LED forward voltage, V_{LED}. Assuming a worst case native off-set (non-chopping) of error amplifier to be less than ±10 mV, the voltage V'_{CS} must be greater than this threshold to initiate switching and auto-zero operation. Therefore, R_{OFF} should be sized to also meet following condition.

$$V'_{CS} = V_{OUT} \times \left(\frac{R_F + R_{CS}}{R_{OFF} + R_F + R_{CS}} \right) > 0.01$$

$$R_{OFF} < \left[V_{OUT} \times \left(\frac{R_F + R_{CS}}{0.01} \right) - (R_F + R_{CS}) \right]$$

$$R_F >> R_{CS}$$

$$R_{OFF} < (100 \times V_{OUT}) \times R_F \quad (6)$$

Feature Description (continued)

To conclude, an external resistor (R_{OFF}) from V_{OUT} to CS pin is required for true zero application, where R_{OFF} should be:

$$R_{OFF} = \min \left[\frac{V_{OUT}}{0.5 \times \Delta I_{LED}} - (R_F + R_{CS}); (100 \times V_{OUT}) \times R_F \right] \quad (7)$$

7.3.5 Undervoltage Lockout (UVLO)

The UDIM pin of the TPS92640 and TPS92641 devices is a dual function input that features an accurate 1.276-V threshold with programmable hysteresis. This pin functions as both the PWM dimming input of the LEDs and as an input UVLO with built-in hysteresis. When the pin voltage rises and exceeds the 1.276-V threshold, 21 µA (typical) of current is driven out of the UDIM pin into the resistor divider (R_{UDIM1}, R_{UDIM2}) providing programmable hysteresis. The UVLO turnon threshold, $V_{TURN-ON}$, is defined using Equation 8.

$$V_{TURN\_ON} = 1.276V \times \left(\frac{R_{UDIM1} + R_{UDIM2}}{R_{UDIM2}} \right) \quad (8)$$

Once the input voltage is above V_{TURN_ON}, the current source is active and the UVLO hysteresis is determined by Equation 9.

$$V_{HYS} = 21\mu A \times (R_{UDIM1}) \quad (9)$$

When using the UDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra resistor (R_{UDIM3}) to set the hysteresis. This allows the standard resistor divider to have smaller values minimizing delays that can incur with additional external PWM dimming circuitry. In general, at least 3 V of hysteresis is preferable when PWM dimming if operating near the UVLO threshold. Under these conditions, the UVLO hysteresis is defined using Equation 10.

$$V_{HYS} = 21\mu A \times \left(R_{UDIM1} + \frac{R_{UDIM3} \times (R_{UDIM1} + R_{UDIM2})}{R_{UDIM2}} \right) \quad (10)$$

7.3.6 PWM Dimming Using the UDIM Pin

The UDIM pin can be driven with a PWM signal, which controls the synchronous NFET operation. The brightness of the LEDs can be varied by modulating the duty cycle (D_{DIM}) of this signal using a Schottky diode with anode connected to UDIM pin, as shown in Figure 13.

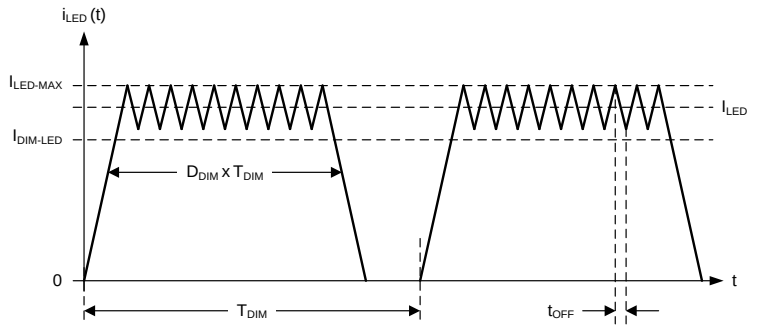


Figure 19. LED Current During UDIM Pin PWM Dimming

Figure 19 shows the LED current waveform during PWM dimming where duty cycle (D_{DIM}) is the percentage of the dimming period (T_{DIM}) that the synchronous NFETs are switching. For the remainder of T_{DIM}, the NFETs are disabled. The resulting dimmed LED current (I_{DIM_LED}) is:

$$I_{DIM\_LED} = D_{DIM} \times I_{LED} \quad (11)$$

Feature Description (continued)

7.3.7 External Shunt FET PWM Dimming

Extremely high dimming range and linearity can be achieved by using TPS92641 device for Shunt FET dimming operation with SDIM and SDRV pin. When higher frequency and time resolution PWM dimming signal is applied to the SDIM pin, the SDRV pin provides an inverted signal of the same frequency and duty cycle that can be used to drive the gate of a Shunt NFET directly across the LED load. Because the output voltage will go to near zero when the Shunt NFET is turned on, the internal on-timer at the RON pin will switch to a fixed minimum on-time during the off-time of the dimming cycle. This method keeps the inductor current slewed up and the converter regulating, without the presence of extremely high switching frequencies. During the on-time of the dimming cycle, the converter will switch in its regular fashion with the programmed on-time at the RON pin. An internal resistor pulls the SDIM pin to logic high if left open. In this case, the SDRV driver will be off.

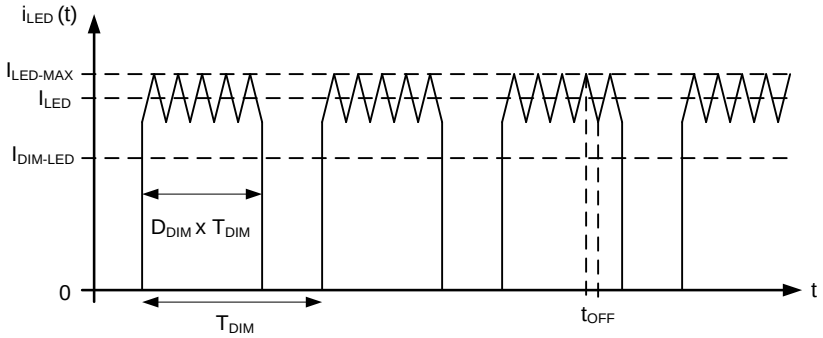


Figure 20. Ideal LED Current During Shunt FET PWM Dimming

Figure 20 shows the ideal LED current waveform during Shunt FET PWM dimming which is very similar to the internal PWM dimming described and shown previously except with much faster rise and fall of the LED current. With this method, only the speed of the parallel Shunt NFET limits the dimming frequency and dimming duty cycle.

7.3.8 VCC Regulation and Start-up

The TPS92640 and TPS92641 devices include a high voltage, low-dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor (C_{VCC}) connected to the VCC pin. The recommended bypass capacitance for the VCC regulator is 2.2 µF to 3.3 µF. This capacitor should be rated for 10 V or greater and an X7R dielectric ceramic is recommended. The output of the VCC regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage, and the supply current is also internally current-limited. When V_{IN} is close or lower than 8.5 V, the regulator will enter the by-pass mode and the VCC will closely follow V_{IN}. This linear regulator is the primary heat source generator of the device. The amount of heat generated is a function of input voltage (V_{IN}), switching frequency (F_{SW}) and the characteristics of the power MOSFET used. The thermal handling capability of the device imposes a limit on the maximum switching frequency can be used, especially when V_{IN} is higher than 48 V and high current power MOSFET is used.

7.3.9 Precision Reference

The device includes a precision 3-V reference. This can be used in conjunction with a resistor divider to set voltage levels for the IADJ pin and other external circuitry requiring a reference. It can also be used to supply current to low power micro-controllers. The source current capability from VREF pin is internally limited 2.1 mA. For the VREF regulator, TI recommends a bypass capacitance from 0.1 µF to 1 µF.

7.3.10 Control Loop Compensation

Compensating the TPS92640 and TPS92641 devices is relatively simple for most applications. The only compensation needed is a compensation capacitor, C_{COMP} across the COMP pin and ground to place a low-frequency dominant pole in the system. The pole must be placed low enough to ensure adequate phase margin at the crossover frequency. For most of the applications, C_{COMP} of 100 nF to 470 nF is good enough. Additionally, TI recommends a high quality ceramic capacitor with X7R dielectric rated for 25 V.

Feature Description (continued)

7.3.11 Overcurrent Protection

The TPS92640 and TPS92641 devices has overcurrent protection to protect the high side NFET (HS-NFET) along with the rest of the system from overcurrent conditions. This peak current limit of 1.28 V (with V_{IN} = 85 V at room temperature) is sensed across the high side FET R_{DS-ON} (from SW to VIN). If the threshold is reached or exceeded, HS-NFET will turn off and the low side NFET (LS-NFET) will turn on for approximately 800 ns. Then HS-NFET will turn on again, if the threshold is still reached or exceeded, both FETs are shutoff for 270-µs typical. Figure 21 shows the waveforms of HG and LG under overcurrent protection.

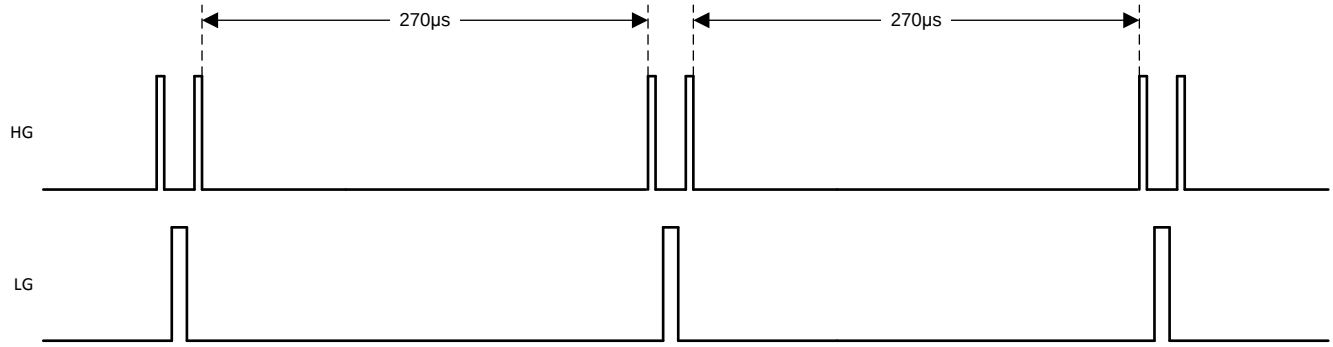


Figure 21. HG and LG Waveforms Under Overcurrent Protection

7.3.12 Overvoltage Protection (OVP)

The TPS92640 and TPS92641 devices have programmable overvoltage protection by using the resistor divider at the VOUT pin. The OVP limit, V_{OVP_ON}, is defined using Equation 12.

$$V_{OVP\_ON} = 3.05V \times \left(\frac{R_{VOUT1} + R_{VOUT2}}{R_{VOUT2}} \right) \quad (12)$$

If the output voltage reaches V_{OVP_ON}, the HG, LG and SDRV pins are pulled low to prevent damage to the LEDs or the rest of the circuit. The OVP circuit has a fixed hysteresis of 100 mV before the driver attempts to switch again.

7.3.13 Boot Undervoltage Lockout (UVLO)

The BOOT UVLO circuit is implemented to ensure proper operation of the high-side gate driver under all operating conditions. The switching operation is commenced once the BOOT voltage exceeds 3.4 V above the SW pin. Comparator hysteresis of 1.8 V is included to prevent false tripping due to high-frequency switching noise. When the BOOT falls below the low voltage threshold (1.6 V typical), the high side NFET is disabled by pulling HG pin to SW pin. The next turnon transition of low-side NFET pulls SW pin down and charges the BOOT capacitor (C_{BOOT}) through VCC. Normal operation is commenced once BOOT capacitor (C_{BOOT}) is charged above BOOT UVLO turnon threshold of 3.4 V.

The boostrap circuit behavior impacts the circuit behavior near dropout (V_{IN}= V_{OUT}) conditions. A minimum off-time is implemented to restrict the maximum duty cycle and maintain charge on the external BOOT capacitor, C_{BOOT}. As the input voltage, V_{IN}, approachs close to the output voltage, V_{OUT}, the output current will fall with the switching frequency, as in conventional Buck regulator. This behavior ensures smooth operation in and out of dropout region while ensuring proper operation of high side gate driver and bootstrap circuit.

7.4 Device Functional Modes

7.4.1 Low Power Shutdown Using the UDIM Pin

The TPS92640 and TPS92641 devices can be placed into a low power shutdown mode by grounding the UDIM pin directly (any voltage below 370 mV) for more than 13 ms (typical).

7.4.2 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the device in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 165°C with a 20°C hysteresis (both values typical). During thermal shutdown the NFETs and drivers are disabled.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Switching Frequency

Switching frequency is selected based on the trade-offs between efficiency, solution size/cost and the range of output voltage that can be regulated. Many applications place limits on switching frequency due to EMI sensitiviy. The on-time of the TPS92640 and TPS92641 devices can be programmed for switching frequencies ranging from the tens of kHz to over 1 MHz. This on-time varies in proportion to both V_{IN} and V_{OUT}, as described in Switching Frequency. However, in practice the switching frequency will shift in response to large swings in input or output voltage. The maximum switching frequency is limited only by the minimum on-time and minimum off-time requirements.

8.1.2 LED Ripple Current

The LED manufacturers generally recommend values of current ripple, ΔI_{LED}, to achieve optimal optical efficiency. The peak-to-peak current ripple values typically range from ±10% to ±40% of DC current, I_{LED}. Higher LED ripple current allows the use of smaller inductors, smaller output capacitors, or no output capacitors at all. Lower ripple current requires more inductance, higher switching frequency, or additional output capacitance. Based on the LED current ripple specification and desired switching frequency, the inductor value can be calculated using Equation 13.

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{LED}} \times t_{ON} \tag{13}$$

It is important to ensure that the rated inductor saturation current is greater than the worst case operating current ($I_{LED}+\Delta I_{LED}/2$) under the wide operating temperature range.

8.1.3 Buck Converters Without Output Capacitor

A Buck regulator is ideal for regulating current because of the direct connection between the inductor and the LED load. Because the current is being regulated, not voltage, a buck current regulator is free of load current transients, and has no need of output capacitance to supply the load and maintain output voltage. This is of great benefit when driving LEDs as large electrolytic capacitors impact the lifetimes and PWM dimming performance. The output capacitor can be eliminated by using a large inductor or higher switching frequency as discussed in LED Ripple Current

A capacitor placed in parallel with the LED or array of LEDs can be used to reduce Δi_{LED} while keeping the same average current through both the inductor and the LED array. With this topology the inductance can be lowered, making the magnetics smaller and less expensive. Alternatively, the circuit can be run at lower frequency with the same inductor value, improving the efficiency and expanding the range of output voltage that can be regulated.

Figure 22 shows the equivalent impedances presented to the $\Delta i_{L\text{-}PP}$ when an output capacitor, C_{OUT}, and its equivalent series resistance (R_{ESR}) are placed in parallel with the LED array.

Application Information (continued)

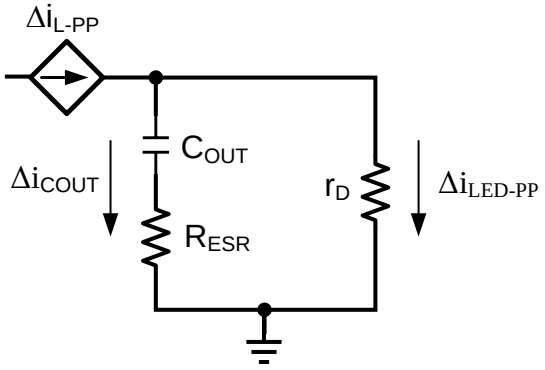


Figure 22. LED Ripple Current With C_{OUT}

To calculate the respective ripple currents, the LED array is represented as the dynamic resistance, (r_D). LED's dynamic resistance is not always specified on the manufacturer's data sheet, but it can be calculated as the inverse slope of the LED's V_{LED} vs I_{LED} curve at the operating point. However, this method only gives an rough estimate of r_D. Total dynamic resistance for a string of n LEDs connected in series can be calculated as the r_D of one device multiplied by n. Inductor ripple current, $\Delta i_{L\text{-}PP}$ is still calculated as before. The following equations can then be used to estimate peak-to-peak LED current ripple, $\Delta i_{LED\text{-}PP}$, when using a parallel capacitor:

$$\Delta i_{LED-PP} = \frac{\Delta i_{L-PP}}{1 + \frac{r_D}{Z_{COUT}}} \qquad Z_{COUT} = \frac{1}{2 \times \pi \times f_{SW} \times C_{OUT}} \tag{14}$$

The calculation for Z_{COUT} assumes that the shape of the inductor ripple current is approximately sinusoidal. Small values of C_{OUT} that do not significantly reduce $\Delta i_{LED\text{-}PP}$ can also be used to control EMI generated by the switching action of the TPS92640 and TPS92641 devices. EMI reduction becomes more important as the length of the connections between the LED and the rest of the circuit increase.

8.1.4 Input Capacitor

Input capacitor is selected using requirements for minimum capacitance and rms ripple current. The input capacitor supply pulses of current approximately equal to I_{LED} while the high-side NFET is on, and is charged up by the input voltage while the high-side NFET is off. Switching converters such as the TPS92640 and TPS92641 devices have a negative input impedance due to the decrease in input current as input voltage increases. This inverse proportionality of input current to input voltage can cause oscillations (sometimes called power supply interaction) if the magnitude of the negative input impedance is greater than the input filter impedance. Minimum capacitance can be selected by comparing the input impedance to the converter's negative resistance; however, this requires accurate calculation of the input voltage source inductance and resistance, quantities which can be difficult to determine. An alternative method to select the minimum input capacitance ($C_{IN\text{-}MIN}$) is to select the maximum voltage ripple ($\Delta v_{IN\text{-}MAX}$), which can be tolerated. $\Delta v_{IN\text{-}MAX}$ is equal to the change in voltage across C_{IN} during t_{ON} when it supplies the load current. A good starting point for selection of C_{IN} is to use an input voltage ripple of 2% to 10% of V_{IN}. $C_{IN\text{-}MIN}$ can be selected using Equation 15.

$$C_{IN\_MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN\_MAX}} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF} \right)}{\Delta v_{IN\_MAX}} \tag{15}$$

TI recommends a minimum input capacitance at least 75% greater than the $C_{IN\text{-}MIN}$ value. To determine the RMS input current rating ($I_{IN\text{-}RMS}$), use Equation 16.

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1-D)} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}} \tag{16}$$

Application Information (continued)

Because this approximation assumes there is no inductor ripple current, the value should be increased by 10-30% depending on the amount of ripple that is expected. Ceramic capacitors are the best choice for the input to the TPS92640 and TPS92641 devices due to their high ripple current rating, low ESR, low cost, and small size compared to other types. When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose one-half or more of their capacitance at their rated DC voltage bias and also lose capacitance with extremes in temperature. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature.

8.1.5 NFETs

The TPS92640 and TPS92641 devices require two external NFETs for the switching regulator. The FETs should have a voltage rating at least 20% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node. In practice, all switching converters have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The NFETs should also have a current rating at least 50% higher than the average transistor current. Once NFETs are chosen, the power rating is verified by calculating the power loss.

8.2 Typical Applications

8.2.1 TPS92640: Design Procedure

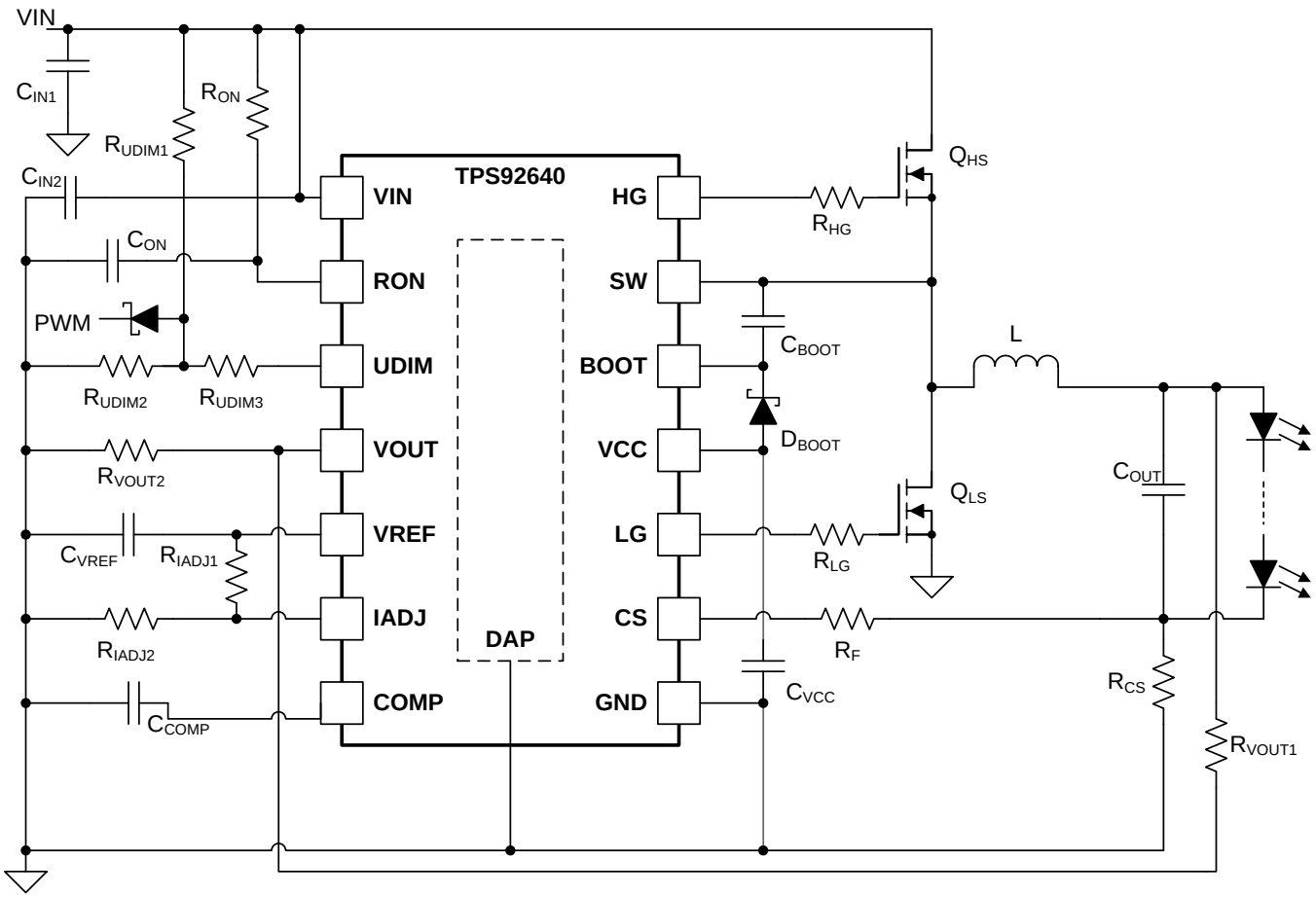


Figure 23. TPS92640 Design Procedure Schematic

8.2.1.1 Design Requirements

- V_{IN}
- V_{LED}
- Number of LEDs in Series
- I_{LED}
- f_{SW}
- V_{CS}
- Δi_{LED-PP}
- ΔV_{IN-PP}
- $V_{TURN-ON}$
- V_{HYS}

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Set Output Voltage Feedback Ratio

For the desired output (V_{OUT}), R_{VOUT1} and R_{VOUT2} is calculated first with the desired feedback voltage, V_{VOUT} at approximately 2.5 V:

Typical Applications (continued)

$$V_{OUT} \times \frac{R_{VOUT2}}{R_{VOUT1} + R_{VOUT2}} = 2.5V$$

$$\frac{R_{VOUT2}}{R_{VOUT1} + R_{VOUT2}} = \frac{2.5}{V_{OUT}}$$

$$V_{OUT} = V_{LED} + I_{LED} \times R_{SNS} \quad (17)$$

8.2.1.2.2 Set Switching Frequency

The switching frequency is set as follows:

$$f_{SW} = \frac{\frac{R_{VOUT1} + R_{VOUT2}}{R_{VOUT2}}}{R_{ON} \times C_{ON}} \quad (18)$$

8.2.1.2.3 Set Average LED Current

The average LED current (I_{LED}) is set by:

$$I_{LED} = \frac{V_{IADJ}}{10 \times R_{CS}}$$

$$V_{IADJ} = V_{REF} \times \frac{R_{IADJ2}}{R_{IADJ1} + R_{IADJ2}}$$

$$V_{REF} = 3.03V \quad (19)$$

8.2.1.2.4 Set Inductor Ripple Current

First, the expected duty cycle, D must be determined:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \qquad \eta \text{ : expected efficiency} \quad (20)$$

With the inductor ripple current, $\Delta i_{L\text{-}PP}$ specified and the expected duty cycle, the inductance (L) can be chosen:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta i_{L-PP} \times f_{SW}} \quad (21)$$

8.2.1.2.5 Set LED Ripple Current and Determine Output Capacitance, C_{OUT}

The LED ripple current ($\Delta i_{LED\text{-}PP}$) is specified. With the target ripple current determined, the output capacitance (C_{OUT}) can be chosen using Equation 22.

$$C_{OUT} = \frac{\Delta i_{L-PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED-PP}} \quad (22)$$

8.2.1.2.6 Choose N-Channel MOSFETs

The suggested minimum voltage rating, $V_{T\text{-}MAX}$ and current rating, $I_{T\text{-}MAX}$ are:

$$V_{T-MAX} = 1.2 \times V_{IN-MAX}$$

$$I_{T-MAX} = 1.5 \times D_{MAX} \times I_{LED} \quad (23)$$

Selecting a proper power MOSFET is critical in a power application, other than the SOA limits, the gate characteristic and the R_{DSON} can affect the system performance seriously.

Typical Applications (continued)

Also, the peak current limit (I_{LIMIT}) is governed by:

$$I_{LIMIT} \approx \frac{1.28V}{R_{DSON}} \qquad V_{IN} = 85V, \text{ at room temperature} \tag{24}$$

Both the current limit threshold and MOSFET R_{DSON} are loosely specified and can vary a lot with temperature, input voltage and other operating conditions.

8.2.1.2.7 Choose Input Capacitance

Input capacitance is necessary to provide instantaneous current to the discontinuous portions of the circuit during the high side NFET on-time. The allowable input voltage ripple (Δv_{IN-PP}) is specified at approximately 3% Pk-Pk of V_{IN}. The minimum required capacitance (C_{IN_MIN}) to achieve this specification is:

$$C_{IN\_MIN} = \frac{I_{LED} \times D}{\Delta v_{IN-PP} \times f_{SW}} \tag{25}$$

The necessary RMS input current rating (I_{IN-RMS}) can be approximated as follows:

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1-D)} \tag{26}$$

8.2.1.2.8 Set the Turnon Voltage and Undervoltage Lockout Hysteresis

With the desired turnon threshold voltage (V_{TURN_ON}) stated, the resistor divider network composing with R_{UDIM1} and R_{UDIM2} can be calculated with the equation in below.

$$V_{TURN\_ON} = 1.276V \times \left(\frac{R_{UDIM1} + R_{UDIM2}}{R_{UDIM2}} \right)$$

$$R_{UDIM2} = \frac{1.276V \times R_{UDIM1}}{V_{TURN\_ON} - 1.276V} \tag{27}$$

Then R_{UDIM3} is optional and recommended for PWM. The R_{UDIM3} can be calculated based on Equation 10 to provide the desired undervoltage lockout hysteresis (V_{HYS}).

Typical Applications (continued)

8.2.2 TPS92640 – PWM Dimming Application

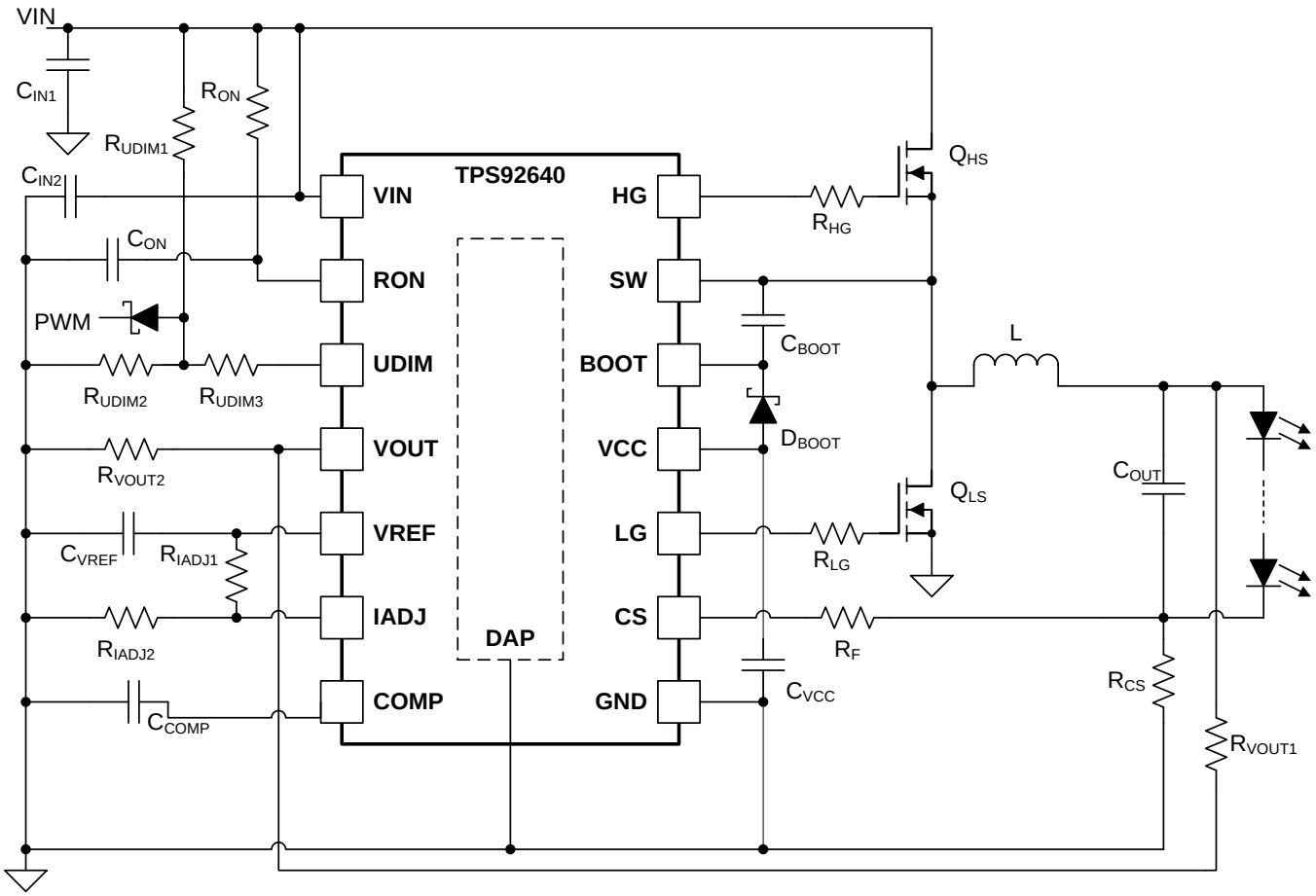


Figure 24. PWM Dimming Using UDIM Pin Schematic

8.2.2.1 Design Requirements

- V_{IN} = 48 V ± 10%
- V_{LED} = 3.25 V, 325-mΩ dynamic resistance
- 10 LEDs in Series, r_D = 3.25 Ω
- I_{LED} = 1 A
- f_{SW} = 500 kHz
- V_{CS} = 200 mV
- $\Delta i_{LED-PP} \leq$ 300 mA
- $\Delta V_{IN-PP} \leq$ 1.5 V
- $V_{TURN-ON}$ = 40 V
- V_{HYS} = 15 V

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Calculate Operating Points

Calculate the operating points using Equation 28 to Equation 30, and assume approximately 90% conversion efficiency (η = 0.9).

$$V_{OUT} = n \times V_{LED} + 200mV = 10 \times 3.25V + 200mV = 32.7V \quad (28)$$

Typical Applications (continued)

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} = \frac{32.7}{0.9 \times 48V} = 0.76 \quad (29)$$

$$D_{MAX} = \frac{V_{OUT}}{\eta \times V_{IN\text{-}MIN}} = \frac{32.7}{0.9 \times 43.2V} = 0.84 \quad (30)$$

8.2.2.2.2 Output Voltage Feedback

Calculate the VOUT pin resistors by setting $\mathbf{R_{VOUT2} = 10\ k\Omega}$ and calculating R_{VOUT1}.

$$R_{VOUT1} = \frac{R_{VOUT2} \times V_{OUT}}{2.5V} - R_{VOUT2} = \frac{10k\Omega \times 32.7V}{2.5V} - 10k\Omega = 120.8k\Omega \quad (31)$$

Choose $\mathbf{R_{VOUT1} = 120\ k\Omega}$.

8.2.2.2.3 Switching Frequency

Using the values calculated above choose a value of $\mathbf{C_{ON} = 1\ nF}$ and calculate the value of R_{ON}:

$$R_{ON} = \frac{\frac{R_{VOUT1} + R_{VOUT2}}{R_{VOUT2}}}{C_{ON} \times f_{SW}} = \frac{\frac{120k\Omega + 10k\Omega}{10k\Omega}}{1nF \times 500kHz} = 26k\Omega \quad (32)$$

Choose the closest standard resistor value of $\mathbf{R_{ON} = 26.1\ k\Omega}$.

8.2.2.2.4 Set the Feedback Reference and LED Current

To get a value of V_{CS} = 200 mV V_{IADJ} must be set to 2 V. Choose a value of $\mathbf{R_{IADJ1} = 10\ k\Omega}$ and solve for R_{IADJ2}:

$$R_{IADJ2} = \frac{V_{IADJ} \times R_{IADJ1}}{V_{REF} - V_{IADJ}} = \frac{2V \times 10k\Omega}{3.03V - 2V} = 19.4k\Omega \quad (33)$$

Choose the standard resistor value of $\mathbf{R_{IADJ2} = 19.6\ k\Omega}$ and solve for R_{CS} using Equation 34.

$$R_{CS} = \frac{V_{IADJ}}{10 \times I_{LED}} = \frac{2V}{10 \times 1A} = 0.2\Omega \quad (34)$$

$\mathbf{R_{CS} = 0.2\ \Omega}$ is a standard resistor value.

8.2.2.2.5 Calculate the Inductor Value

Because this is a PWM dimming application, TI does not recommend much output capacitance for faster current rise and fall times, so the inductor ripple current should be close to the 300-mA peak-to-peak LED ripple current. Calculate and inductor value that will give you 350-mA peak-to-peak inductor ripple current or less:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} = \frac{(48V - 32.7V) \times 0.76}{350mA \times 500kHz} = 66.4\mu H \quad (35)$$

Choose the standard value of $\mathbf{L = 68\ \mu H}$ which results in an actual $\Delta i_{L\text{-}PP}$ of 342 mA.

8.2.2.2.6 Calculate the Output Capacitor Value

Given the actual inductor ripple current of 342-mA peak-to-peak, use Equation 36 to calculate the required output capacitor value.

$$C_{OUT} = \frac{\Delta i_{L\text{-}PP}}{8 \times r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}} = \frac{342mA}{8 \times 3.25\Omega \times 300mA \times 500kHz} = 88nF \quad (36)$$

Choose $\mathbf{C_{OUT} = 0.1\ \mu F}$.

8.2.2.2.7 Calculate the MOSFET Parameters

The MOSFETs must have a minimum voltage and current rating for the application. The minimum ratings are calculated using Equation 37 and Equation 38.

Typical Applications (continued)

$$V_{T\text{-}MAX} = 1.2 \times V_{IN\text{-}MAX} = 1.2 \times 52.8V = 63V \quad (37)$$

$$I_{T\text{-}MAX} = 1.5 \times D_{MAX} \times I_{LED} = 1.5 \times 0.84 \times 1A = 1.26A \quad (38)$$

Choose MOSFETs that have a drain-to-source voltage rating of greater than 63 V and a current rating greater than 1.26 A.

8.2.2.2.8 Calculate the Minimum Input Capacitance

The minimum input capacitance to achieve 1.5-V peak-to-peak input voltage ripple is calculated using Equation 39.

$$C_{IN\_MIN} = \frac{I_{LED} \times D}{\Delta V_{IN\text{-}PP} \times f_{SW}} = \frac{1A \times 0.76}{1.5V \times 500kHz} = 1\mu F \quad (39)$$

For PWM dimming applications more input voltage ripple will be present at the PWM dimming frequency. For these applications, TI recommends using 10 times the amount of minimum input capacitance or more. Choose **C_{IN} = 10 µF**.

8.2.2.2.9 Undervoltage Lockout and Hysteresis

Choose a value of **R_{UDIM1} = 100 kΩ** and calculate the values of R_{UDIM2} and R_{UDIM3} using Equation 40 and Equation 41.

$$R_{UDIM2} = \frac{1.276V \times R_{UDIM1}}{V_{TURN\text{-}ON} - 1.276V} = \frac{1.276V \times 100k\Omega}{40V - 1.276V} = 3.3k\Omega \quad (40)$$

$$R_{UDIM3} = \frac{\left(\frac{V_{HYS}}{21\mu A} - R_{UDIM1}\right) \times R_{UDIM2}}{R_{UDIM1} + R_{UDIM2}} = \frac{\left(\frac{15V}{21\mu A} - 100k\Omega\right) \times 3.24k\Omega}{100k\Omega - 3.24k\Omega} = 19.3k\Omega \quad (41)$$

Choose the nearest standard resistor values of **R_{UDIM2} = 3.32 kΩ** and **R_{UDIM3} = 19.1 kΩ**.

8.2.2.3 Application Curve

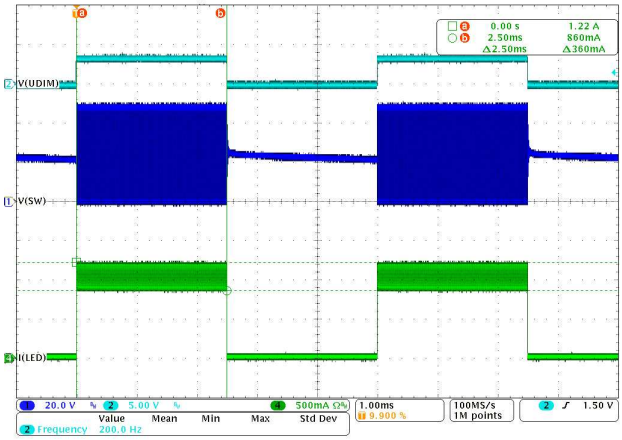


Figure 25. UDIM Dimming Waveform

9 Power Supply Recommendations

Any DC output power supply may be used provided it has a high enough voltage and current range for the particular application required.

10 Layout

10.1 Layout Guidelines

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximize noise rejection and minimize the generation of EMI within the circuit.

Discontinuous currents are the most likely to generate EMI, therefore take care when routing these paths. The main path for discontinuous current in the TPS92640 and TPS92641 buck converters contain the input capacitor (C_{IN}), the low side MOSFET (Q_{LS}), and the high side MOSFET (Q_{HS}). This loop should be kept as small as possible and the connections between all three components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L, Q_{LS} and Q_{HS} connect) should be just large enough to connect the components without excessive heating from the current it carries. The current sense trace (CS pin) should be run along with a ground plane or have differential traces run for CS and ground.

In some applications, the LED or LED array can be far away (several inches or more) from the circuit, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the converter, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

10.2 Layout Example

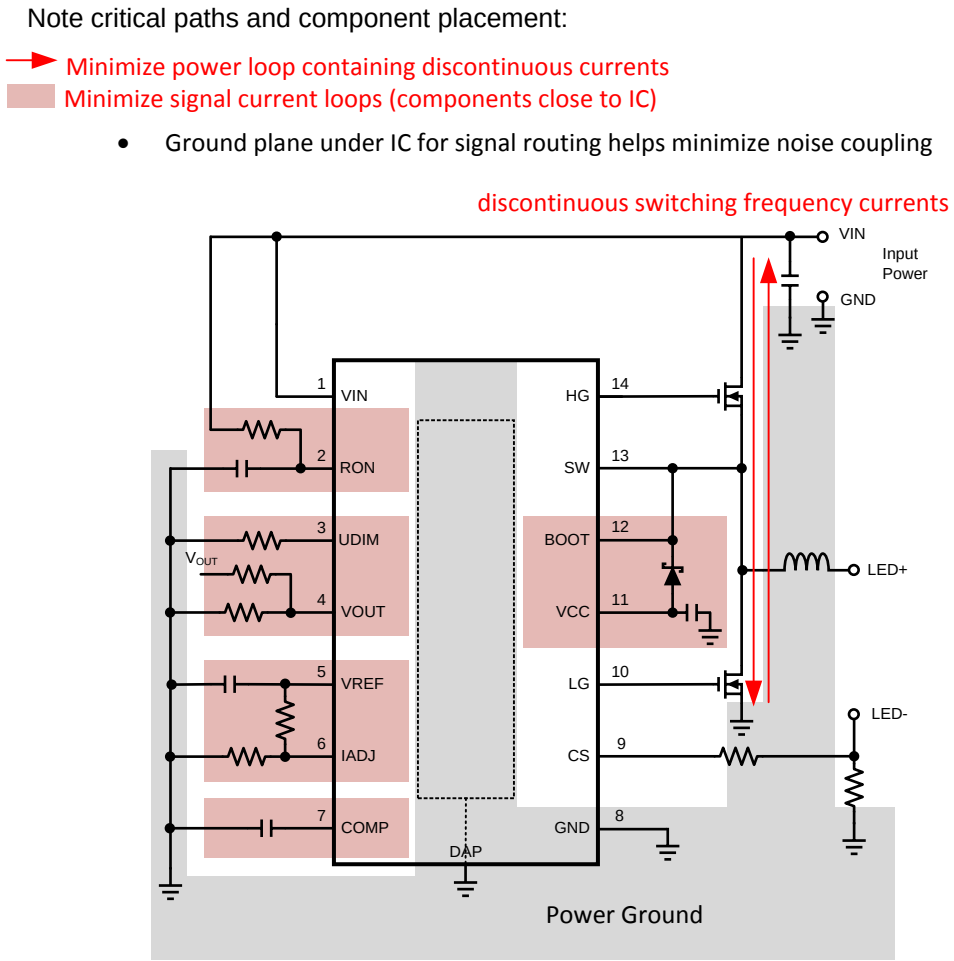


Figure 26. Layout Recommendation

10.3 EMI and Noise Considerations

In synchronous rectifier, the high speed gate drive signals can generate significant conducted and radiated EMI. This noise can couple with high impedance nodes of the IC and result in undesirable operation. A small (4 Ω to 10 Ω) resistors, R_{HG} and R_{LG}, in series with the gate drive signals are recommended to slow the slew-rate of the SW node and reduce the noise signature. They also improve the robustness of the circuit by reducing the noise coupling in to sensitive nodes such as UDIM, CS, RON and IADJ.

In other to further reduce EMI signature, good PCB layout techniques must be implemented. The loop area between the synchronous NFET, inductor and output capacitor should be minimized to reduce radiated EMI due to switching action. The trace lengths of high impedance nodes (UDIM, CS, RON and IADJ) should be minimized and shielded from switching noise. The parasitic capacitance between switching node and ground node should be minimized to reduce common mode noise. Other common layout techniques such as star ground and noise suppression using local bypass capacitors should be followed to maximize noise rejection and minimize EMI within the circuit.

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS92640	Click here	Click here	Click here	Click here	Click here
TPS92641	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92640PWP/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TP92640 PWP	Samples
TPS92640PWPR/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TP92640 PWP	Samples
TPS92640PWPT/NOPB	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TP92640 PWP	Samples
TPS92641PWP/NOPB	ACTIVE	HTSSOP	PWP	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TP92641 PWP	Samples
TPS92641PWPR/NOPB	ACTIVE	HTSSOP	PWP	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TP92641 PWP	Samples
TPS92641PWPT/NOPB	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TP92641 PWP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

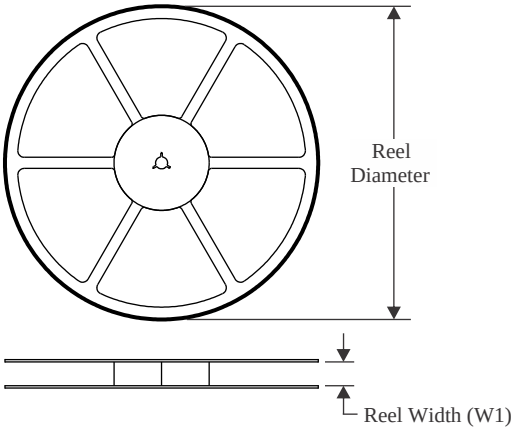
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

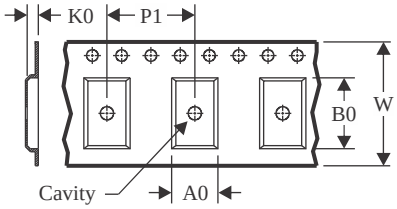
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

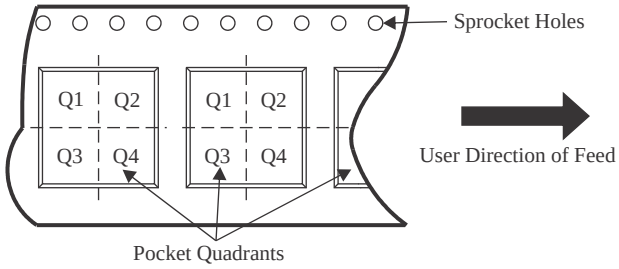


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

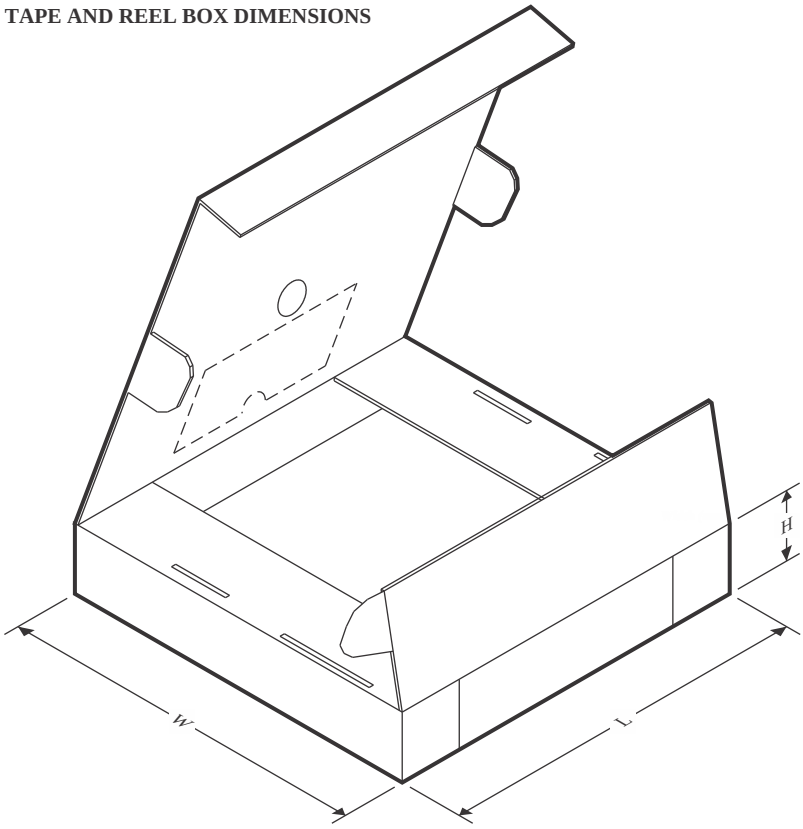
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92640PWPR/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS92640PWPT/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS92641PWPR/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS92641PWPT/NOPB	HTSSOP	PWP	16	250	178.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

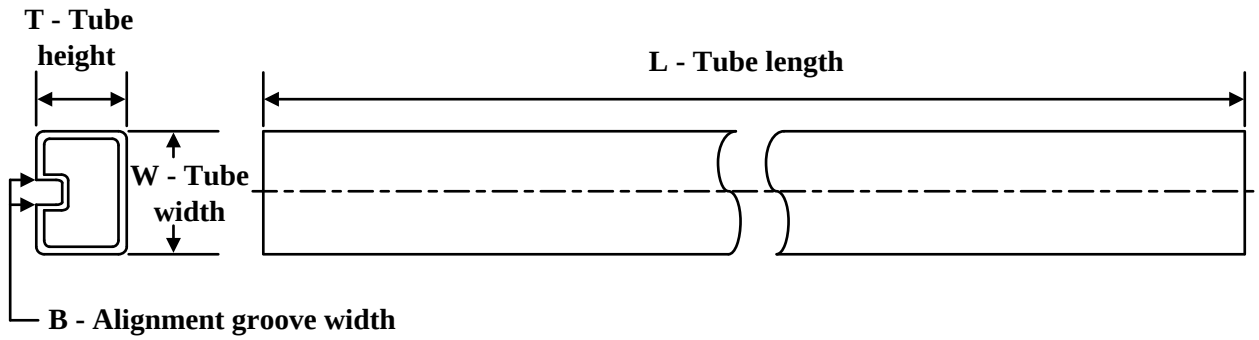
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92640PWPR/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
TPS92640PWPT/NOPB	HTSSOP	PWP	14	250	208.0	191.0	35.0
TPS92641PWPR/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
TPS92641PWPT/NOPB	HTSSOP	PWP	16	250	208.0	191.0	35.0

TUBE



*All dimensions are nominal

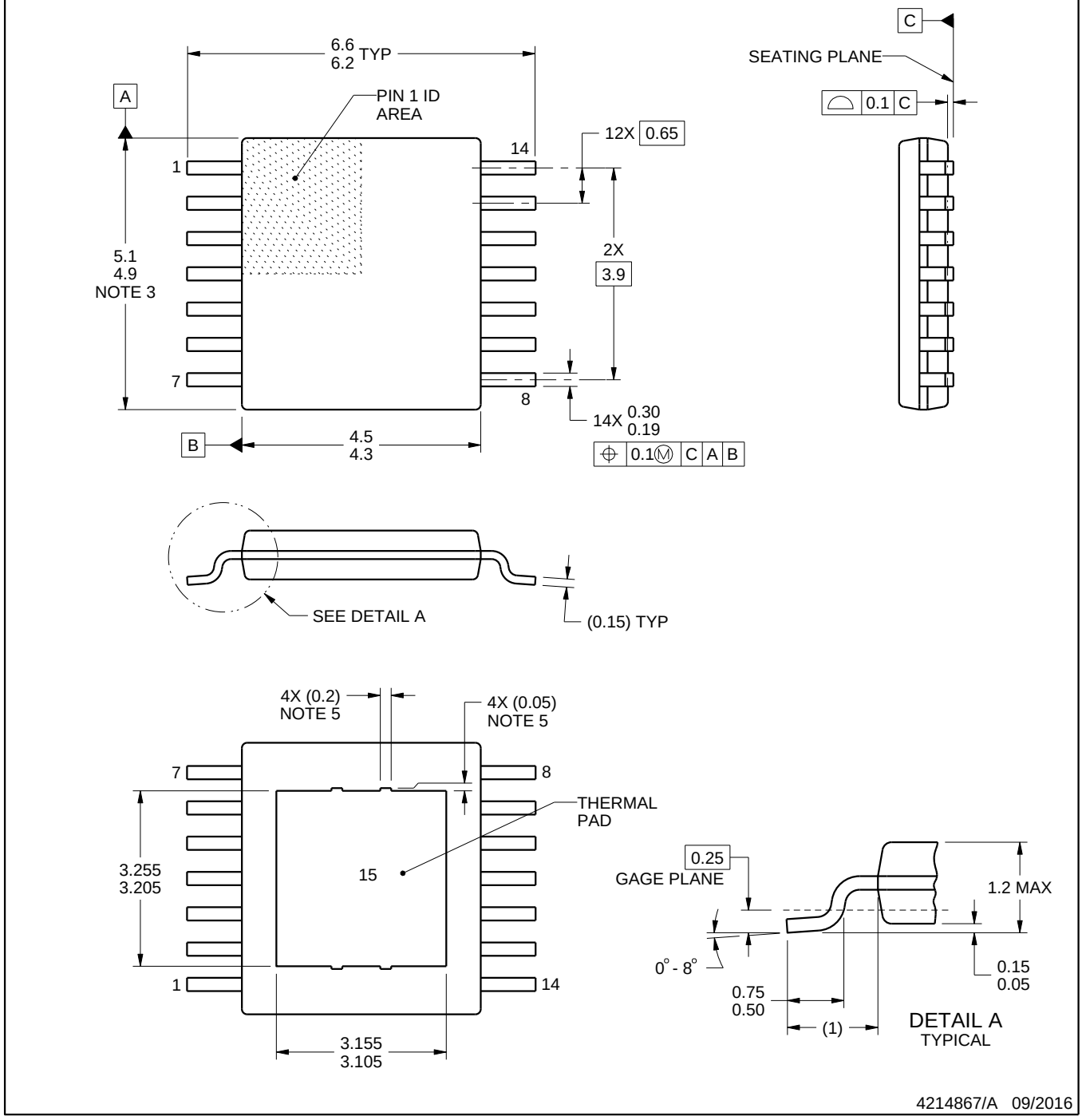
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92640PWP/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
TPS92641PWP/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

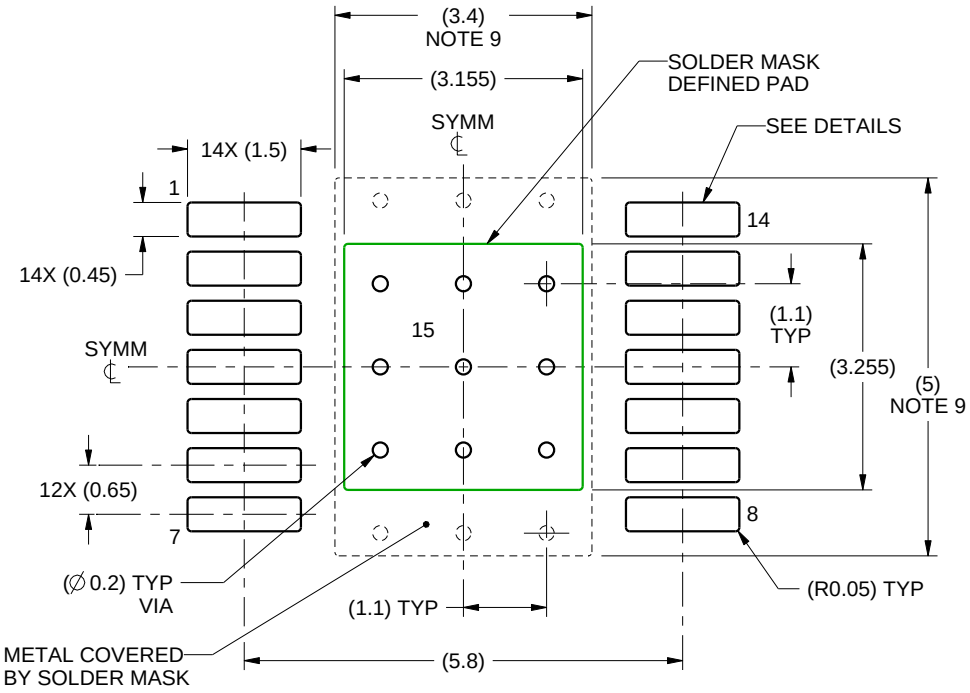
PLASTIC SMALL OUTLINE



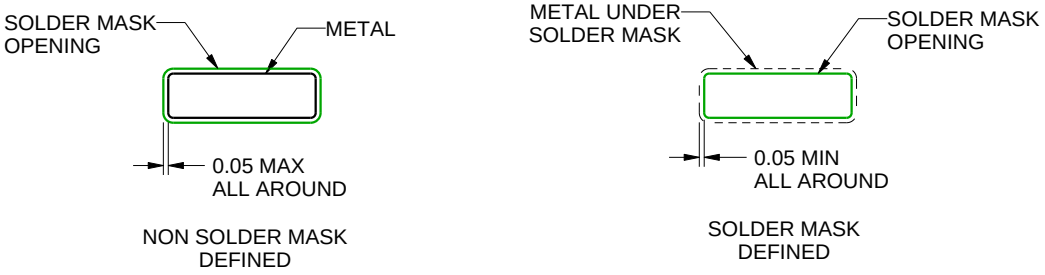
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

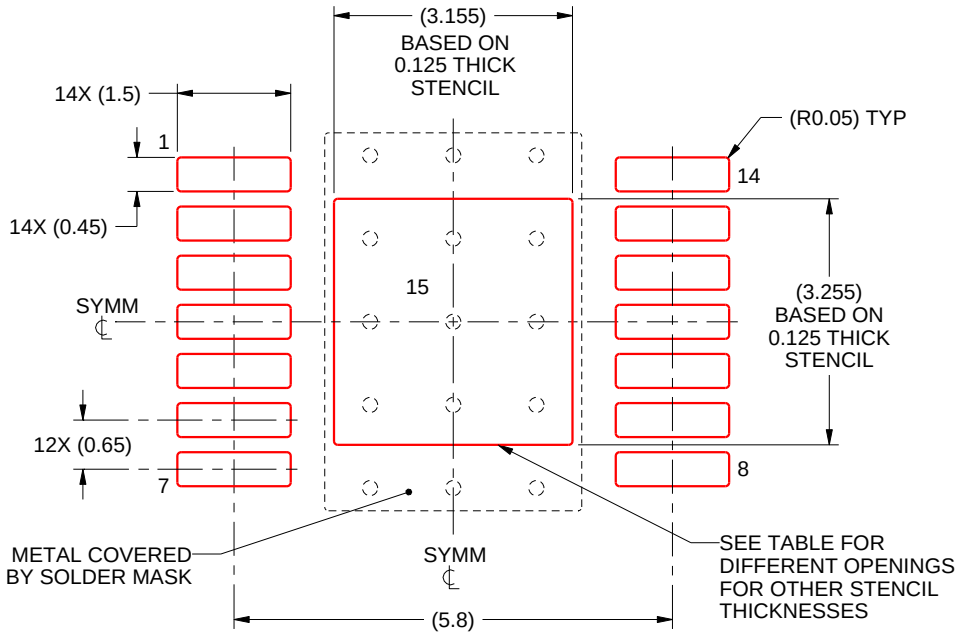


SOLDER MASK DETAILS
PADS 1-14

4214867/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



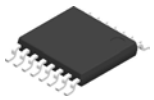
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

4214867/A 09/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

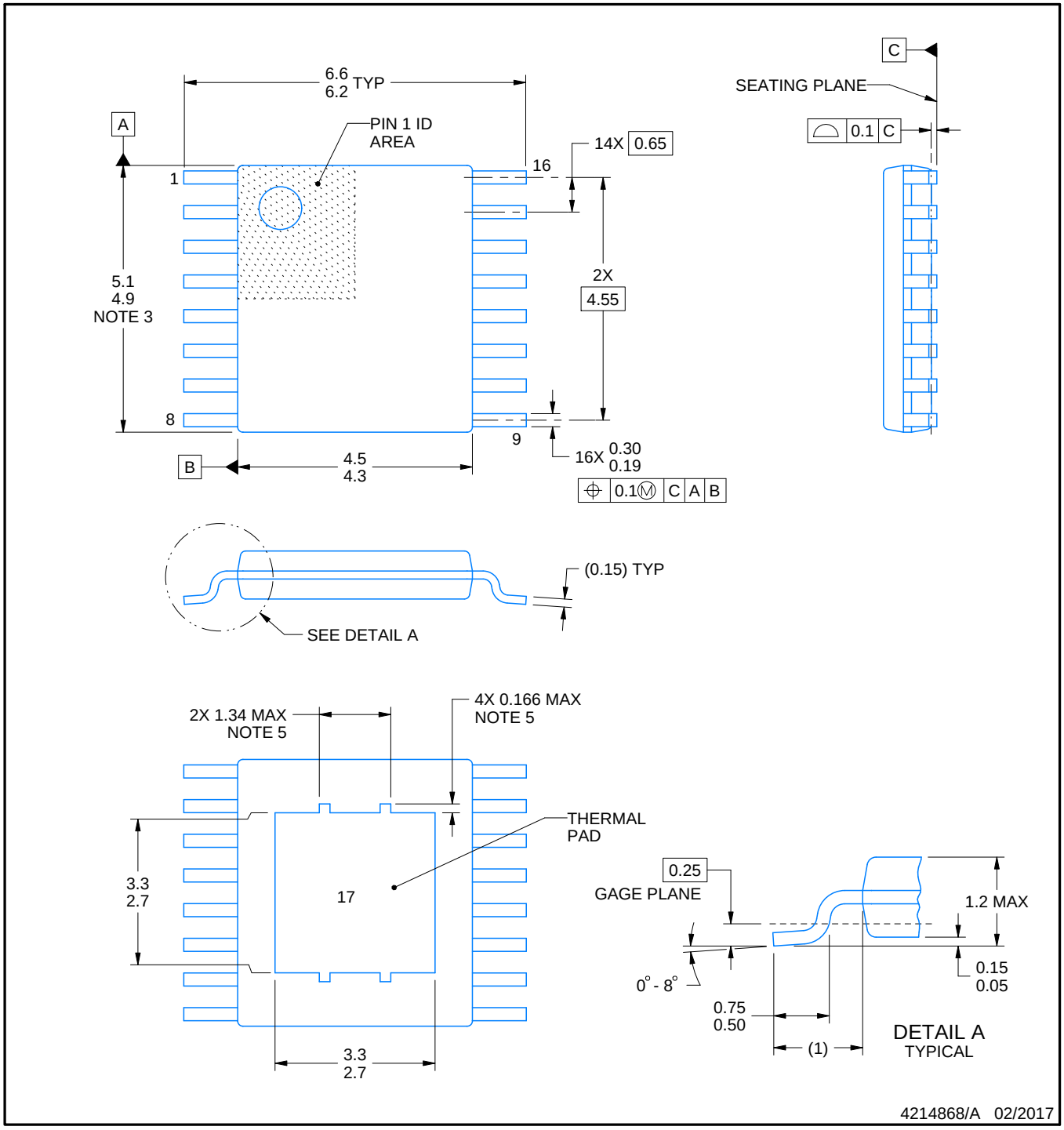


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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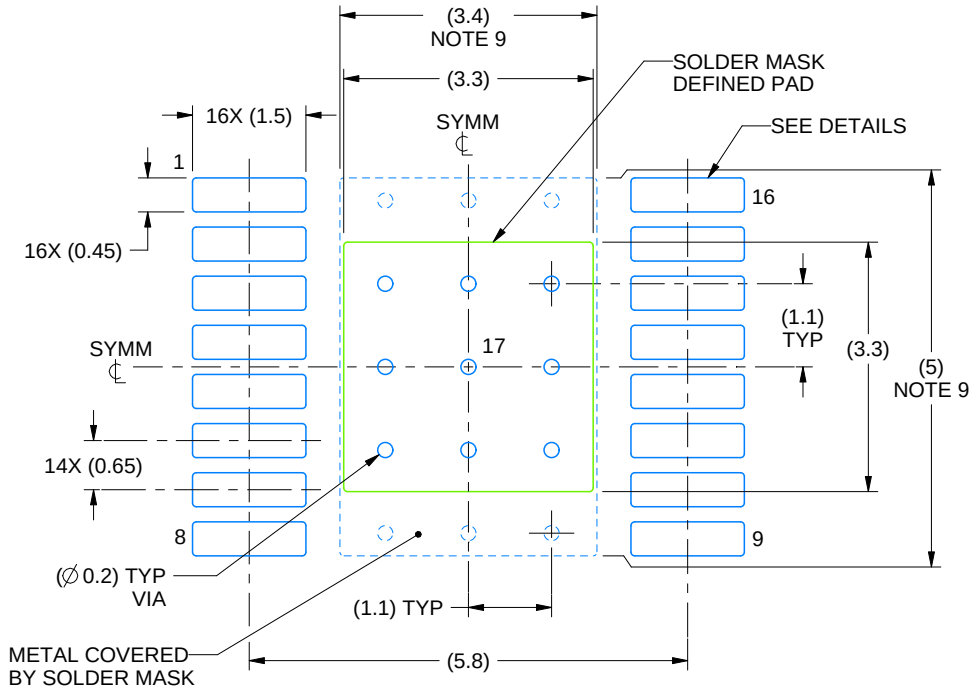
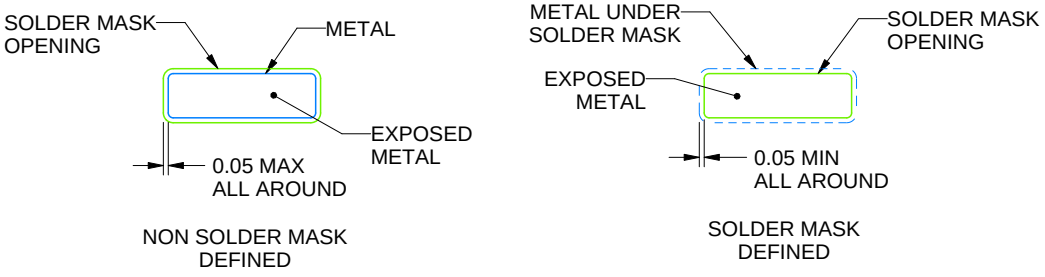
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

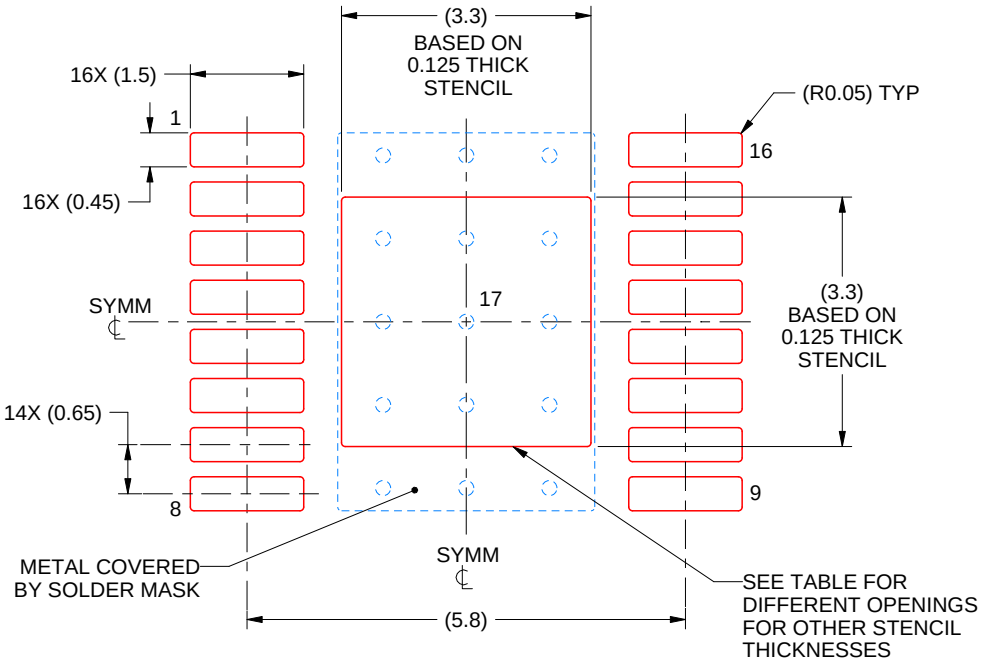


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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