5-A, 20-V High-Current Load Switch

Check for Samples: TPS2590

FEATURES

- **Integrated Pass MOSFET**
- **Up to 20-V Bus Operation**
- **Programmable Fault Timer**
- **Programmable Fault Current**
- **Programmable Hard Current-Limit**
- **Fast Disable**
- **Thermal Shutdown**
- **Load Fault Alert**
- **Latching and Auto-retry Operation**
- **4-mm x 4-mm QFN**
- **–40°C to 125°C Junction Temperature Range**
- **UL2367 Recognized - File Number E169910**

APPLICATIONS

- **RAID Arrays**
- **Telecommunications**
- **Plug-In Circuit Boards**
- **Disk Drives**
- **SSDs**
- **PCIE**
- **Fan Control**
- **Notebooks and Netbooks**

DESCRIPTION

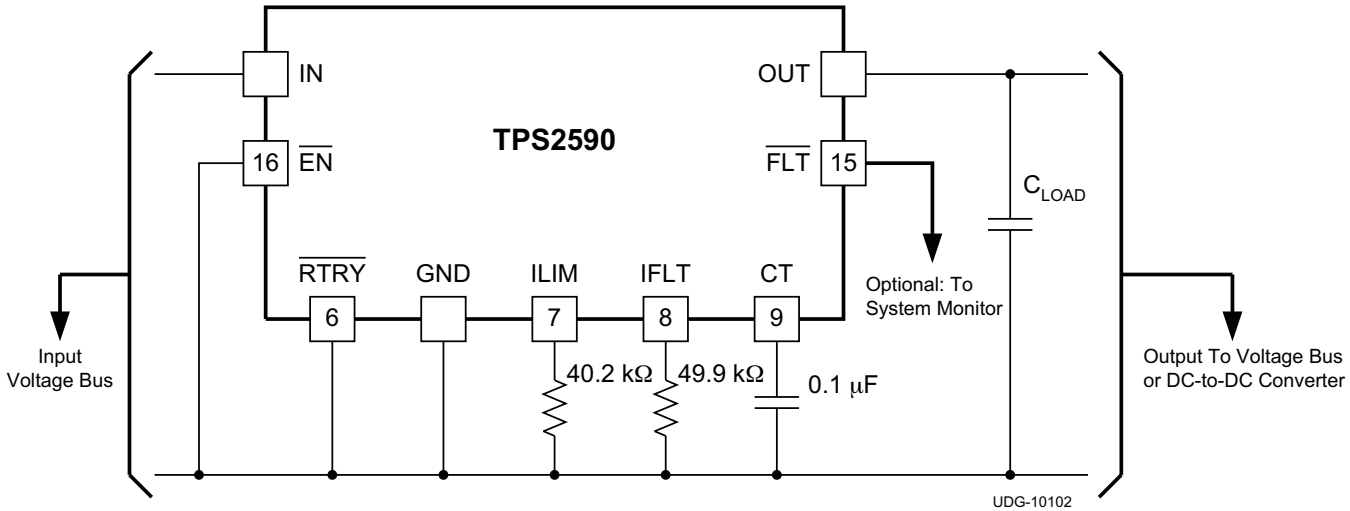
The TPS2590 device provides highly integrated hot-swap power management and superior protection in applications where the load is powered by busses up to 20 V. The maximum UV turn-on threshold of 2.9 V makes the TPS2590 device well suited to standard bus voltages as low as 3.3 V. This device is intended for systems where a voltage bus must be protected to prevent load shorts from interrupting or damaging other system components. The TPS2590 device is in a 16-pin QFN package.

The TPS2590 device has multiple programmable protection features. Load protection is accomplished by a non-current-limiting fault threshold, a hard current-limit threshold, and a fault timer. The dual current thresholds allow the system to draw high current for short periods without causing a voltage droop at the load. An example of this is a disk drive startup. This technique is ideal for loads that experience brief high demand, but benefit from protection levels consistent with average current draw.

Hotswap MOSFET protection is provided by power limit circuitry which protects the internal MOSFET against SOA related failures.

The TPS2590 device provides a fault indicator output and allows latch off or retry on fault.

12-V, 3.5-A APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage range IN, OUT		–0.3	25	V
Voltage range $\overline{FLT}$		–0.3	20	V
Output sink current $\overline{FLT}$			10	mA
Input voltage range, $\overline{EN}$		–0.3	6	V
Input current, $\overline{RTRY}$ ($\overline{RTRY}$ internally clamped to 3 V) $\overline{RTRY}$ = 0 V			35	uA
Voltage range CT(3), IFLT(3) ,ILIM(3), $\overline{RTRY}$		–0.3	3	V
ESD rating	Human body model (HBM)		2.5	kV
	Charged device model (CDM)		400	V
Operating junction temperature range, T_J		Internally Limited		°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to pin.

DISSIPATION RATINGS(1) (2) (3) (4)

PACKAGE	θ_{JA} LOW K, °C/W	θ_{JA} HIGH K, °C/W	θ_{JA} BEST 4, °C/W
RSA	211	55	50

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7and JESD 51-3.
(2) Low-k (2 signal - no plane, 3-inch by 3-inch board, 0.062-inch thick, 1-oz copper) test board with the pad soldered, and an additional 0.12 inch. 2 of top-side copper added to the pad.
(3) High-k is a (2 signal – 2 plane) test board with the pad soldered.
(4) The best case thermal resistance is obtained using the recommendations per SLMA002A (2 signal - 2 plane with the pad connected to the plane).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage range IN, OUT	3		20	V
Voltage range $\overline{EN}$	0		5	V
Voltage range $\overline{FLT}$	0		20	V
Output sink current $\overline{FLT}$	0		1	mA
Voltage range $\overline{RTRY}$	0		3	V
CCT	0.1			nF
Output current, IOUT	0		5.5	A
R_{RFLT}	49.9		200	kΩ
R_{RLIM}	40.2		100	kΩ
Junction temperature	–40		125	°C

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ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, V_{IN} = 3 V – 20 V, $\overline{EN}$ = 0 V, $\overline{FLT}$ = open, $\overline{RTRY}$ = open, CT = open, R_{RLIM} = 40.2 kΩ, R_{RFLT} = 49.9 kΩ, No external capacitor connected to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
	UVLO	V_{IN} ↑	2.6	2.85	2.9	V
		Hysteresis		150		mV
	Bias current	$\overline{EN}$ = 2.4 V		25	100	µA
		$\overline{EN}$ = 0 V		3.9	5	mA
OUT						
	RON	R_{IN-OUT}, I_{OUT} < I_{LIM}, 1 A ≤ I_{OUT} ≤ 4.5 A		29.5	42	mΩ
		I_{OUT} V_{IN}: 12 V, C_{LOAD} = 1000 µF, $\overline{EN}$: 3 V → 0 V	3	5	7.5	W
	Reverse diode voltage	V_{OUT} > V_{IN} , $\overline{EN}$ = 5 V, I_{IN} = –1 A		0.77	1	V
IFLT						
I_{FAULT}	Fault current threshold	I_{OUT} ↑, I_{CT}: sinking → sourcing, pulsed test (R_{RFLT} = 200 kΩ)	0.8	1	1.2	A
		I_{OUT} ↑, I_{CT}: sinking → sourcing, pulsed test (R_{RFLT} = 100 kΩ)	1.8	2	2.2	
		I_{OUT} ↑, I_{CT}: sinking → sourcing, pulsed test (R_{RFLT} = 49.9 kΩ)	3.6	4	4.4	
ILIM						
I_{LIM}	Current-limit program I_{VOUT} –, V_{VIN}–V_{OUT} = 0.3 V, pulsed test	R_{RLIM} = 100 kΩ	1.6	2	2.4	A
		R_{RLIM} = 66.5 kΩ	2.6	3	3.4	
		R_{RLIM} = 40.2 kΩ	4.6	5	5.4	
CT						
	Charge/discharge current	I_{CT} sourcing, V_{CT} = 1 V	29	35	41	µA
		I_{CT} sinking, V_{CT} = 1 V, $\overline{RTRY}$ = 0 V	1	1.4	1.8	
	Threshold voltage	V_{CT} ↑	1.3	1.4	1.5	V
		V_{CT} ↓	0.1	0.16	0.3	
	ON/OFF fault duty cycle	V_{VOUT} = 0 V	2.8	3.7	4.6	%
$\overline{EN}$						
	Threshold voltage	$V_{\overline{EN}}$↓	0.8	1	1.5	V
		Hysteresis	50	150	250	mV
	Input bias current	$V_{\overline{EN}}$ = 2.4 V (sinking)	–1.5	0	0.5	µA
		$V_{\overline{EN}}$ = 0.2 V (sourcing)	2	1	0.5	
	Turn on propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 2.4 V→ 0.2 V, V_{OUT}: ↑ 90% × VI_N		350	500	µs
	Turn off propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 0.2 V→ 2.4 V, V_{OUT}: ↓10% × V_{IN}		10	20	
$\overline{FLT}$						
	VOUT LOW	V_{CT} = 1.8 V, $I_{\overline{FLT}}$ = 1 mA		0.2	0.4	V
	Leakage current	V_{FLT} = 18 V			1	µA
$\overline{RTRY}$						
	Low threshold voltage	Auto Retry Mode			0.8	V
	High threshold	Latch mode	2.0			
	Input bias current	$V_{\overline{RTRY}}$ = 3 V	–1	0.2	1	mA
		$V_{\overline{RTRY}}$ = 0.2 V	50	25	0	
THERMAL SHUTDOWN						
	Thermal shutdown	T_J		160		°C
		Hysteresis		10		

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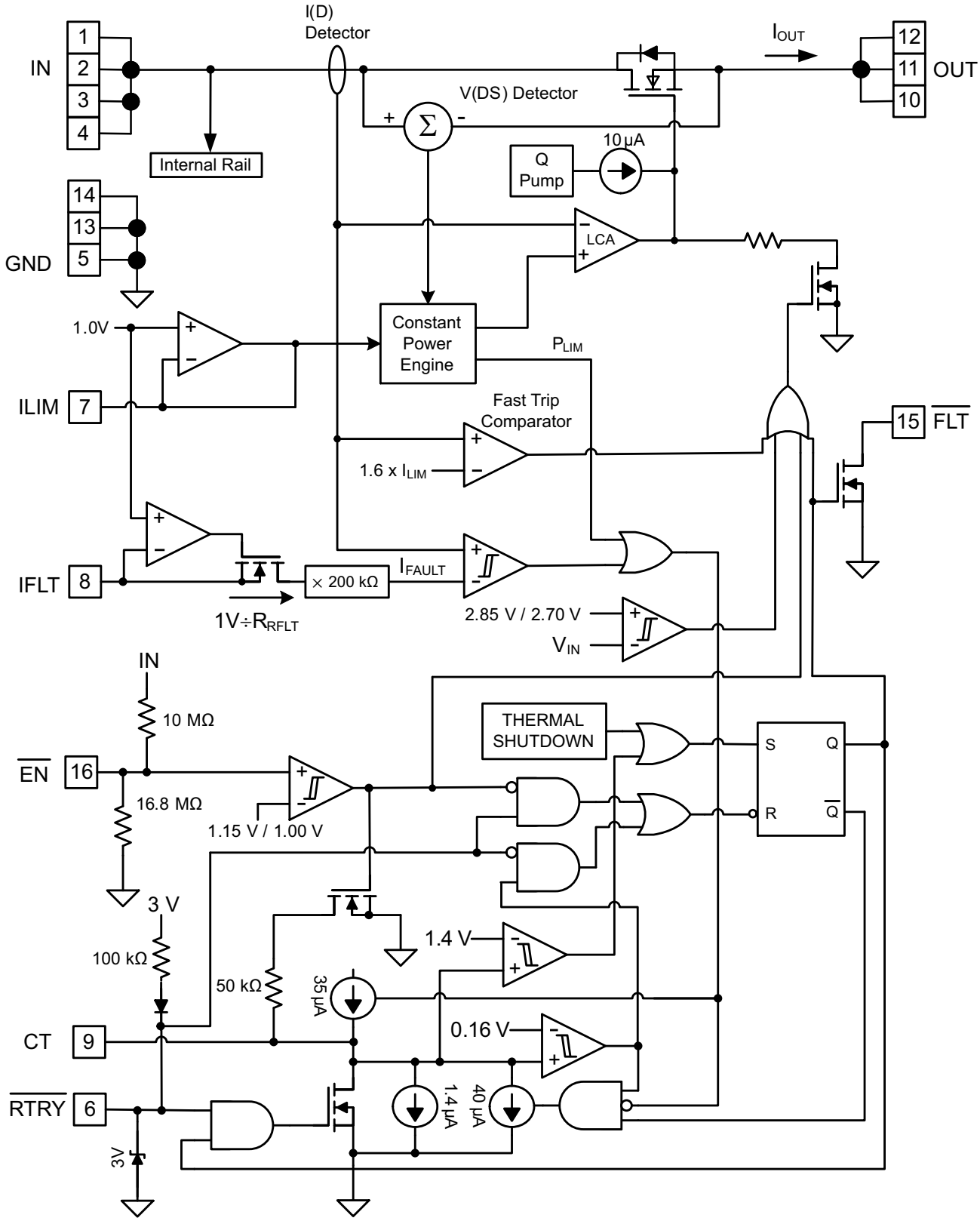
DEVICE INFORMATION

TPS2590 FUNCTIONAL BLOCK DIAGRAM



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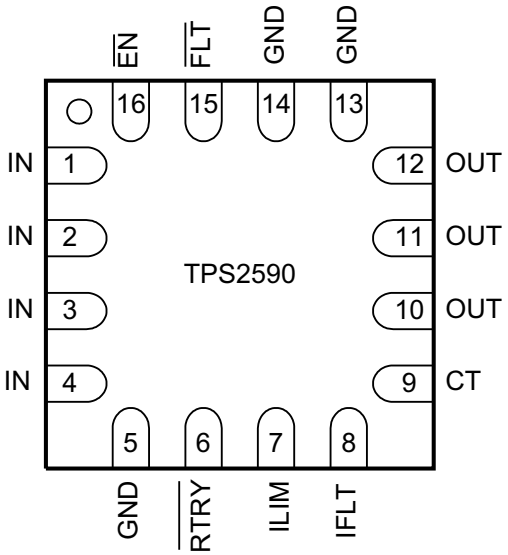
TPS2590 PINOUT



TERMINAL FUNCTIONS

FUNCTION	TPS2590	DESCRIPTION
$\overline{EN}$	16	Device is enabled when this pin is pulled low.
IN	1-4	Power In and control supply voltage.
$\overline{RTRY}$	6	If low, the TPS2590 will attempt to restart after an overcurrent fault. If floating (high) the device will latch off after an overcurrent fault and will not attempt to restart until $\overline{EN}$ or Vin is cycled off and on.
ILIM	7	A resistor to ground sets the current-limit level.
IFLT	8	A resistor to ground sets the fault current level.
CT	9	A capacitor to ground sets the fault time.
GND	5, 13, 14	GND
OUT	10, 11, 12	Output to the load.
$\overline{FLT}$	15	Fault low indicated the fault time has expired and the FET is switched off.

PIN DESCRIPTION

CT: Connect a capacitor from CT to GND to set the fault time. The fault timer starts when I_{OUT} exceeds I_{FAULT} or when SOA protection mode is active, charging the capacitor with 35 µA from GND towards an upper threshold of 1.4 V. If the capacitor reaches the upper threshold, the internal pass MOSFET is turned off. If $\overline{RTRY}$ > 2 V, the MOSFET remains off until $\overline{EN}$ is cycled. If $\overline{RTRY}$ ≤ 0.8 V, the capacitor will discharge at 1.4 µA to 0.16 V and then re-enable the pass MOSFET. If the upper threshold is not crossed, the capacitor will discharge at 40 µA to 0.16 V and then to 0 V at 1.4 µA. When the device is disabled, CT is pulled to GND through a 50-kΩ resistor.

The timer period must be chosen long enough to allow the external load capacitance to charge. The nominal (not including component tolerances) fault timer period is selected using Equation 1 where T_{FAULT} is the minimum timer period in seconds and C_{CT} is in Farads.

$$C_{CT} = \frac{T_{FAULT}}{40 \times 10^3} \quad (1)$$

If $\overline{RTRY}$ < 0.8 V, the second and subsequent retry timer periods will be slightly shorter than the first retry period. CT nominal (not including component tolerances) discharge time, t_{SD} from 1.4 V to 0.16 V is shown in Equation 2, where C_{CT} is in Farads and t_{SD} is in seconds.

$$t_{SD} = 885.7 \times 10^3 \times C_{CT} \quad (2)$$

The nominal ratio of on-to-off times represents about a 3.7% duty cycle when a hard fault is present on the output.

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$\overline{\text{FLT}}$: Open-drain output that pulls low on any condition that causes the output to open. These conditions are either an overload with a fault time-out, or a thermal shutdown. $\overline{\text{FLT}}$ becomes operational before UV, when IN is greater than 1 V. I_{FAULT} may not be set below 1 A to maintain the Fault Current-Limit threshold accuracy listed in Electrical Characteristics. $\overline{\text{FLT}}$ will pulse low momentarily prior to the onset of OUT ramp up during IN or $\overline{\text{EN}}$ based start-up.

GND: This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified.

IFLT: A resistor connected from this pin to ground sets the fault current threshold (I_{FAULT}). Currents between the fault current threshold and the current-limit are permitted to flow unimpeded for the period set by the fault timer programmed on CT. This permits loads to draw momentary surges while maintaining the protection provided by a lower average-current-limit.

The fault timer described in the CT section starts when I_{OUT} exceeds I_{FAULT}. The fault current resistor is set using Equation 3 where I_{FAULT} is in Amperes and R_{RFLT} is in Ohms.

$$R_{RFLT} = \frac{200\ k\Omega}{I_{FAULT}} \tag{3}$$

ILIM: A resistor connected from this pin to ground sets I_{LIM}. The TPS2590 device limits current to I_{LIM}. If the current doesn't drop below the I_{FAULT} level before the timer times out then the output will be shut off. R_{RLIM} is set by Equation 4:

$$R_{RLIM} = \frac{201\ k\Omega}{I_{LIM}} \tag{4}$$

I_{LIM} must be set sufficiently larger than I_{FAULT} to ensure that I_{LIM} could never be less than I_{FAULT}, even after taking tolerances into account.

$\overline{\text{EN}}$: When this pin is pulled low, the IC is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{\text{EN}}$ is pulled to IN with a 10 MΩ resistor and to GND with a 16.8 MΩ resistor. Because high impedance pullup/down resistors are used to reduce current draw, any external FET controlling this pin should be low leakage.

IN: Input voltage to the TPS2590 device. The recommended operating voltage range is 3 V to 20 V. All IN pins should be connected together and to the power source.

OUT: Output connection for the TPS2590 device. V_{OUT} in the ON condition considering the ON resistance of the internal MOSFET, RON is shown in Equation 5.

$$V_{OUT} = V_{IN} - RON \times I_{OUT} \tag{5}$$

All OUT pins should be connected together and to the load.

$\overline{\text{RTRY}}$: When pulled low the TPS2590 device attempts to restart after a fault. If left floating or pulled high the TPS2590 device latches off after a fault. This pin is internally clamped at 3 V and is pulled to the internal 3-V supply by a diode in series with a 100-kΩ resistor.

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TYPICAL CHARACTERISTICS

CURRENT-LIMIT
vs
JUNCTION TEMPERATURE

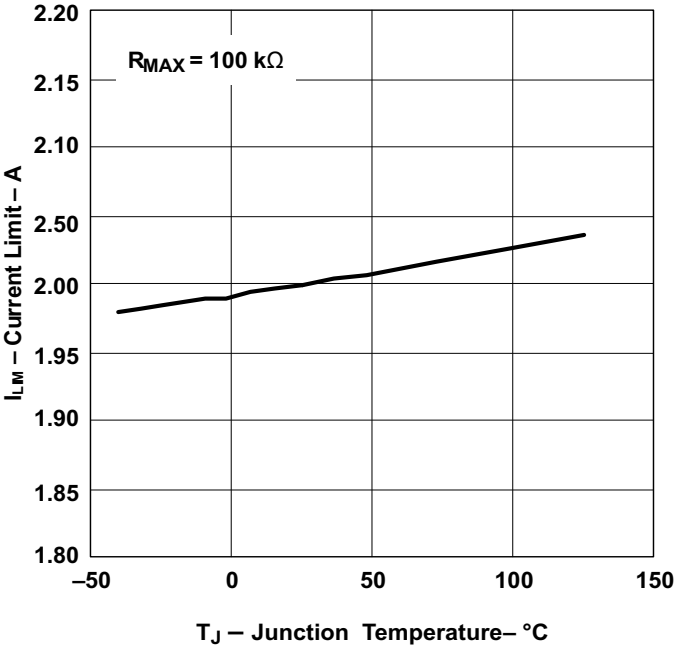

Figure 1.

FAULT CURRENT
vs
JUNCTION TEMPERATURE

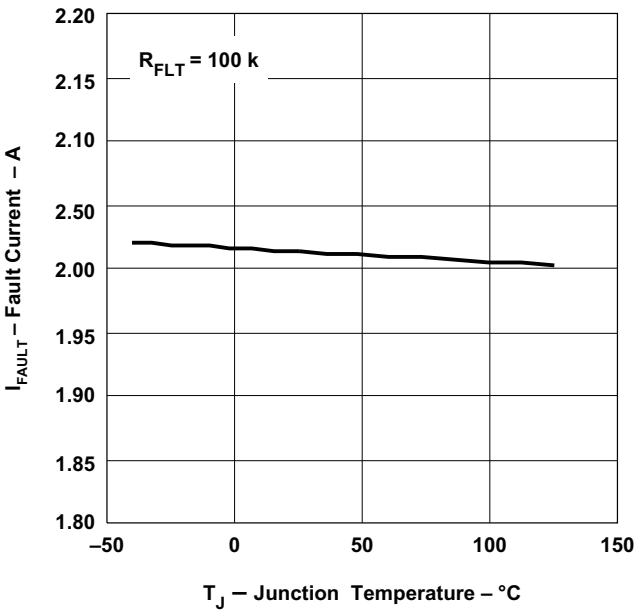

Figure 2.

POWER LIMIT
vs
JUNCTION TEMPERATURE

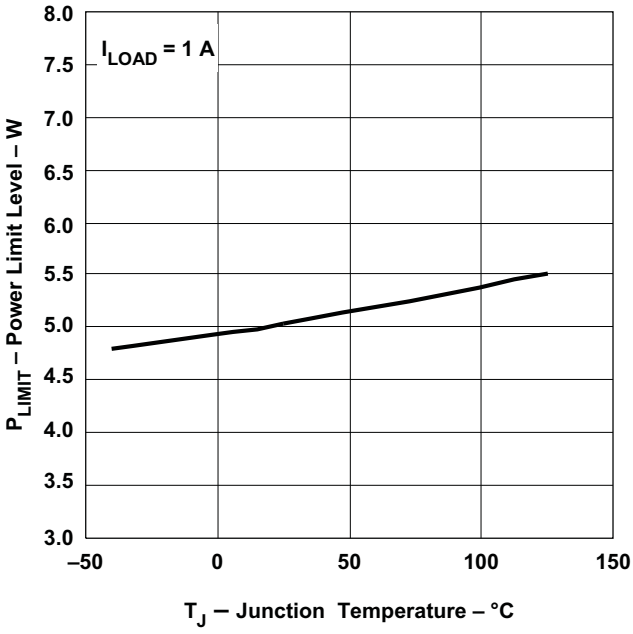

Figure 3.

SLEEP-MODE SUPPLY CURRENT
(VCC = 12 V)
vs
JUNCTION TEMPERATURE

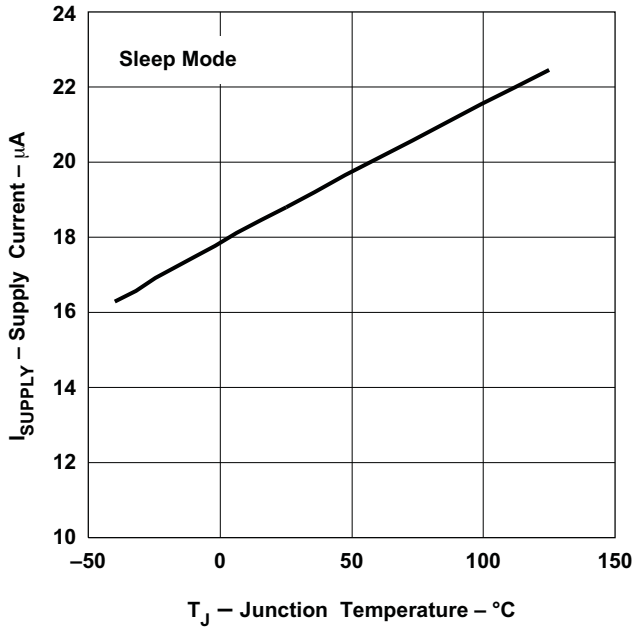

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

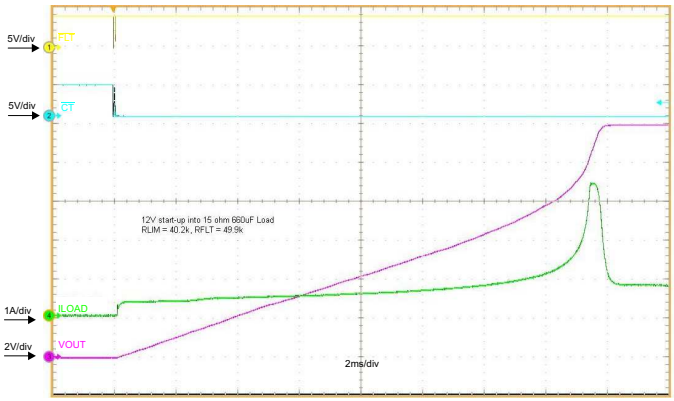

Figure 5. 12-V Startup into 15-Ω, 700-µF Load

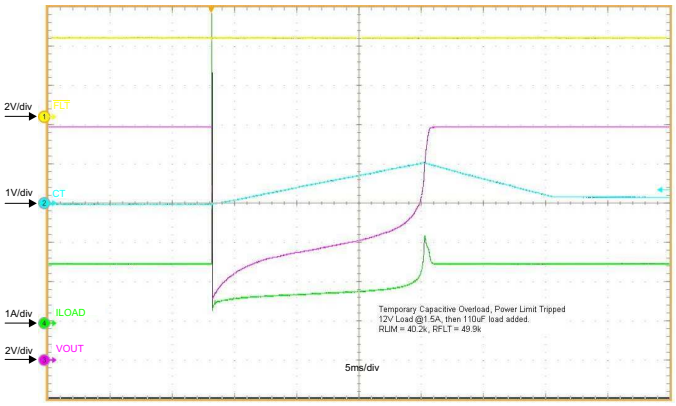

Figure 6. 12-V Input Added to an 8-Ω Load

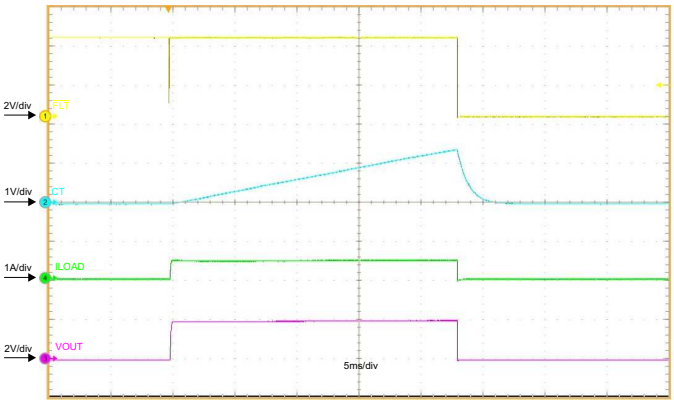

Figure 7. Failed Startup into a 4-Ω Load

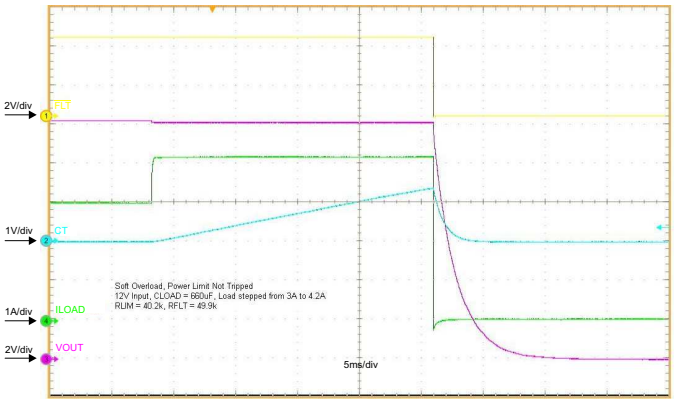

Figure 8. 12-V Soft Overload, 3-A to 4.2-A, Power Limit Not Tripped

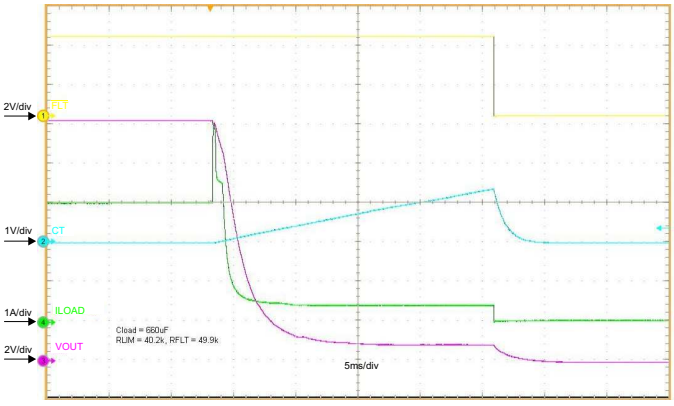

Figure 9. Firm Overload, 3-A to 5.4 A, Power Limit Tripped

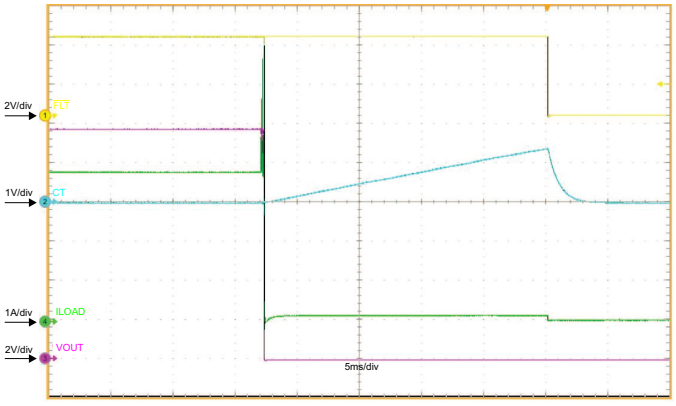

Figure 10. 12-V Hard Overload, 3.6-A Load then Short

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TYPICAL CHARACTERISTICS (continued)

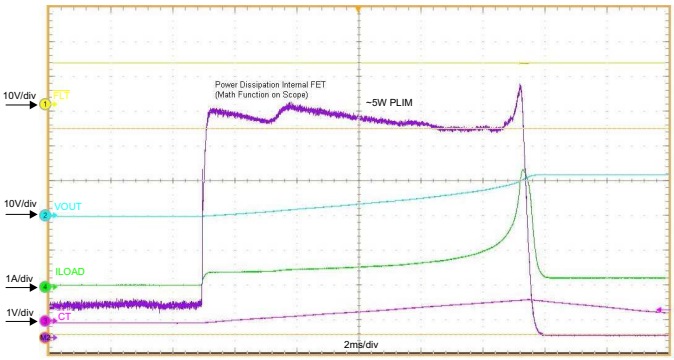

Figure 11. Power Dissipation During 12-V Startup into a 60-Ω, 660-µF Load

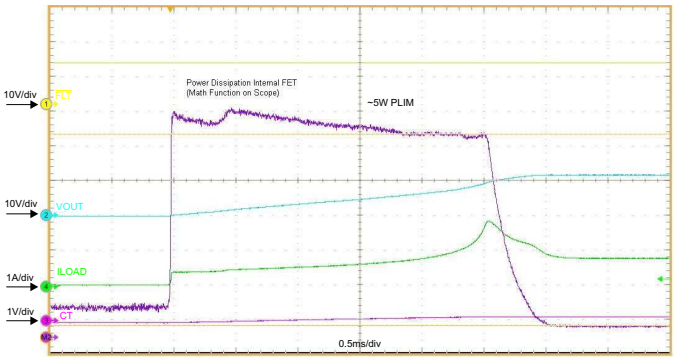

Figure 12. Power Dissipation During 12-V Startup into a 15-Ω, 110-µF Load

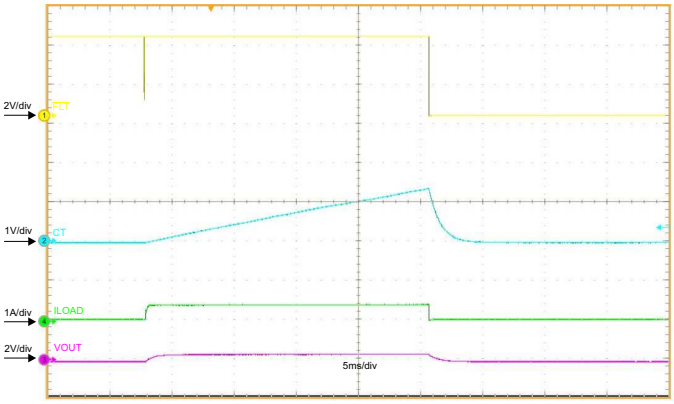

Figure 13. Startup into a 1-Ω Load

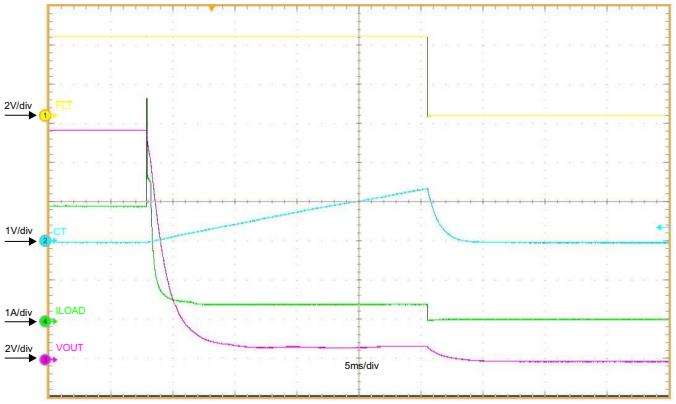

Figure 14. Firm Overload, Load Stepped From 3.8 A to 5.5 A

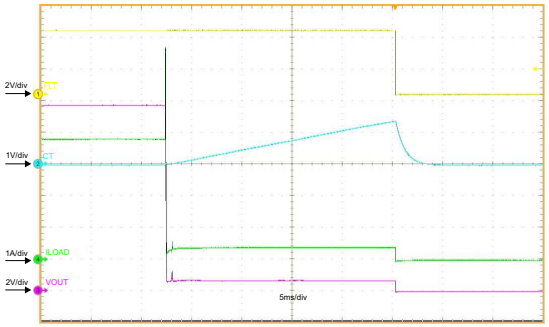

Figure 15. Hard Overload, Load Stepped from 3.8 A to 7.1 A

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APPLICATION INFORMATION

Startup

Large inrush current occurs when power is applied to discharged capacitors and load. During the inrush period, the TPS2590 device operates in power limit (or SOA protect mode) managing the current as VOUT rises. In SOA protect mode, the internal MOSFET power dissipation ($[V_{IN} – V_{OUT}] \times I_{OUT}$) is regulated at 5 W typical while the fault timer starts and C_{CT} ramps up. As the charge builds on C_{LOAD}, the current increases towards I_{LIM}. When the capacitor is fully charged, I_{OUT} drops to the dc load value, the fault timer stops, and C_{CT} ramps down. In order for the TPS2590 device to start properly, the fault timer duration must exceed C_{LOAD} startup time, t_{ON}. Startup time without additional dc loading can be determined using Equation 6 where P_{LIM} = 5 W (typical).

$$t_{ON} = \frac{C_{LOAD} \times P_{LIM}}{2 \times I_{LIM}^2} + \frac{C_{LOAD} \times V_{IN}^2}{2 \times P_{LIM}} \quad (6)$$

When the load has a resistive component in addition to C_{LOAD}, the fault time must be extended because the resistive load current is unavailable to charge C_{LOAD}. Table 1 and Table 2 can be used to predict start-up time in the presence of resistive dc loading.

Refer to the TPS2590 Design Calculator Tool (SLUC398) for assistance with design calculations.

Table 1. Start-up Time (ms) With DC Loading: V_{IN} = 5 V, P_{LIM} = 3 W, I_{LIM} = 5 A

R_{LOAD} (Ω)	C_{LOAD} = 100 µF	C_{LOAD} = 220 µF	C_{LOAD} = 470 µF	C_{LOAD} = 1000 µF
1000	0.43	0.95	2.03	4.33
10	0.5	1.11	2.36	5.03
5	0.61	1.34	2.87	6.1
3	0.91	2	4.28	9.11
2.5	1.31	2.88	6.14	13.07

Table 2. Start-up Time (ms) With DC Loading: V_{IN} = 12 V, P_{LIM} = 3 W, I_{LIM} = 5 A

R_{LOAD} (Ω)	C_{LOAD} = 100 µF	C_{LOAD} = 220 µF	C_{LOAD} = 470 µF	C_{LOAD} = 1000 µF
10000	2.46	5.41	11.56	24.59
100	2.67	5.87	12.55	26.69
50	2.93	6.45	13.79	29.34
15	6.7	14.74	31.5	67.01
13	11.68	25.69	54.87	116.75

Maximum Allowable Load to Ensure Successful Start-Up

The power limiting function of the TPS2590 device provides very effective protection for the internal FET. Expectedly, there is a supply voltage dependent maximum allowable load required for successful startup. Loads above this can cause the output to shut off because of CT timeout or thermal shutdown because V_{OUT} hangs at an intermediate voltage below V_{IN}. The equation for maximum load (or R_{MIN} is derived using the circuit equations for V_{OUT} as a function of V_{IN}, R_{LOAD}, P_{LIM}, and the result is quadratic in form.

$$R_{MIN} \times I^2 - V_{IN} \times I + P_{LIM\_MIN} = 0 \quad (7)$$

$$I = \frac{V_{IN} \pm \sqrt{V_{IN}^2 - 4 \times R_{MIN} \times P_{LIM\_MIN}}}{2 \times R_{MIN}} \quad (8)$$

$$R_{MIN} \times I = V_{OUT} = \frac{V_{IN} \pm \sqrt{V_{IN}^2 - 4 \times R_{MIN} \times P_{LIM\_MIN}}}{2} \quad (9)$$

When $R_{LOAD} < R_{MIN}$, the numerical result for V_{OUT} is real ($V_{IN}^2 – 4 \times R_{LOAD} \times P_{LIM} > 0$) and less than V_{IN} meaning the circuit will not start (CT or thermal shutdown). When $R_{LOAD} > R_{MIN}$, the numerical result for V_{OUT} is imaginary ($V_{IN}^2 – 4 \times R_{LOAD} \times P_{LIM} < 0$) and the circuit will start ($V_{OUT} = V_{IN}$). Ensure that R_{LOAD} is > R_{MIN} per Equation 11.

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$$4 \times R_{MIN} \times P_{LIM\_MIN} > V_{IN}^2 \quad (10)$$

$$R_{LOAD} > R_{MIN} = \frac{V_{IN}^2}{4 \times P_{LIM\_MIN}} = \frac{V_{IN}^2}{12} \quad (11)$$

Enable Pin Considerations

For the case when $\overline{EN}$ is simply connected to GND, TPS2590 device begins ramping the voltage on OUT as IN rises above UVLO (~2.85V typical). If IN does not ramp monotonically, the TPS2590 device can momentarily turn off then on during startup if IN falls below approximately 2.7 V. To avoid this problem, $\overline{EN}$ assertion can be delayed until IN is sufficiently above UVLO. A simple approach is shown in Figure 16. The 100-kΩ pullup resistor de-asserts $\overline{EN}$ when IN is above approximately 1.75 V maximum which is well below the minimum UVLO of approximately 2.6 V. The Zener diode ensures that $\overline{EN}$ remains below 5 V. User control to enable the TPS2590 device can be applied at the ON node to turn on the FET once IN has risen sufficiently above UVLO.

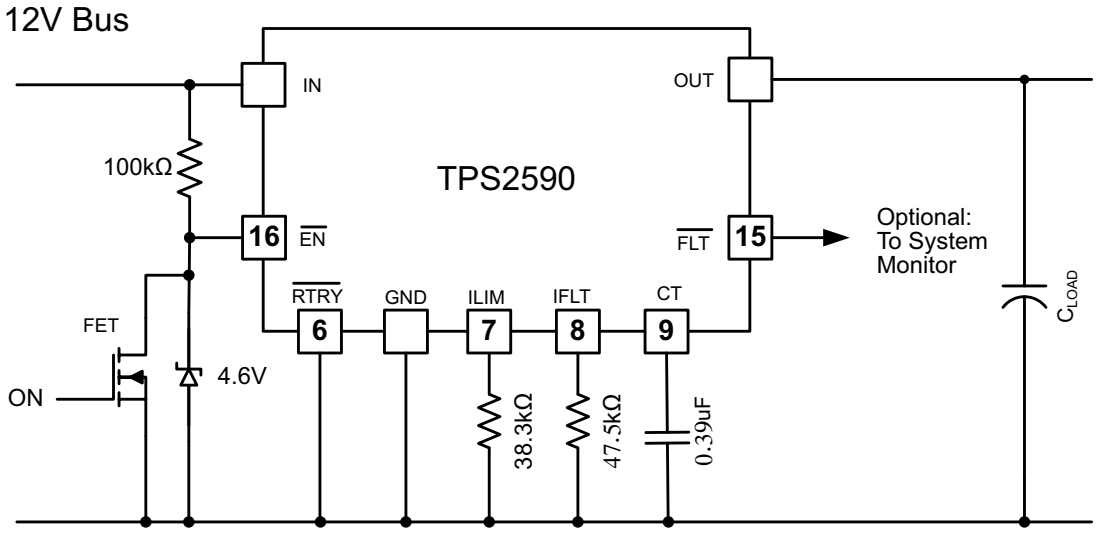

Figure 16. EN Delay Circuit

Fault Timer

The fault timer is active when the TPS2590 device is in SOA protect mode or the current is above I_{FAULT}. Figure 17 illustrates operation during non-faulted start-up (C_{LOAD} = 470 µF and I_{OUT} = 1 A in a 12-V system). C_{CT} charges at approximately 35 µA until the TPS2590 device exits SOA-protect mode, discharges quickly (approximately 40 µA) to approximately 0.16 V, and then decays slowly (approximately 1.4 µA) towards zero.

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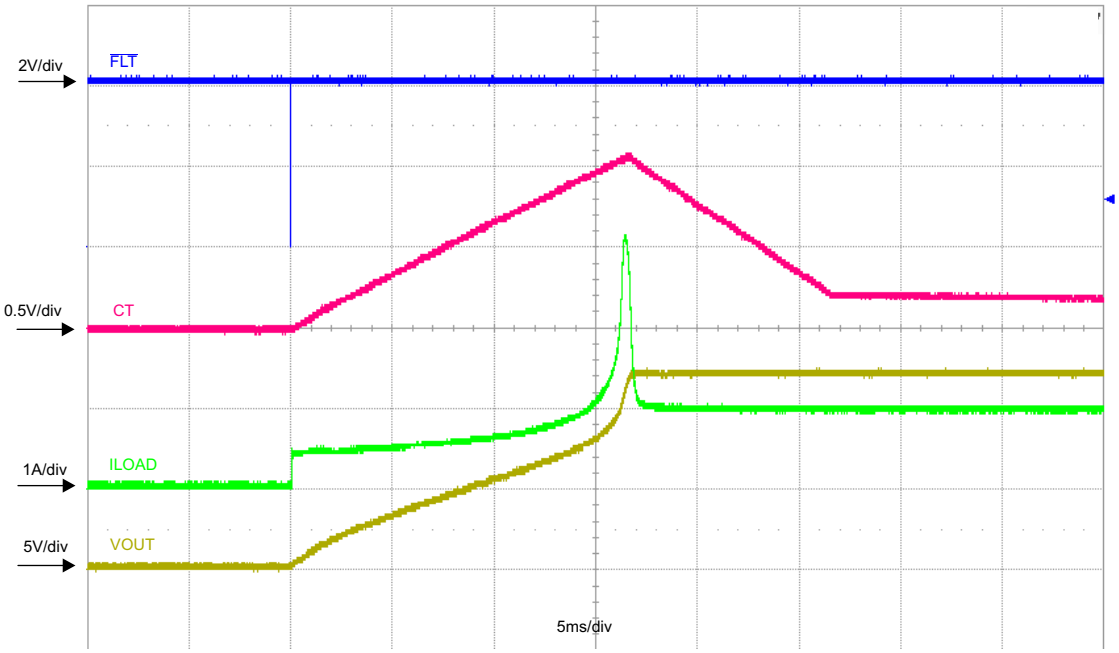

Figure 17. Fault Timer Operation During Start-Up

C_{CT} can be chosen for fault-free start-up including expected C_{LOAD} and C_{CT} capacitance tolerance as shown in Equation 12.

$$C_{CT} = \frac{(1 + C_{LOAD\_TOL} + C_{CT\_TOL}) \times t_{ON}}{40000} \quad (12)$$

Normal Operation

When load current exceeds I_{FAULT} during normal operation the fault timer starts. If load current drops below I_{FAULT} before the fault timer expires, normal operation continues. If load current stays above the I_{FAULT} threshold the fault timer expires and a fault is declared. When a fault is declared a device operating in latched mode ($\overline{RTRY}$ > 2 V) turns off and can be restarted by cycling power or toggling the $\overline{EN}$ signal. A device operating in retry mode ($\overline{RTRY}$ < 0.8 V) attempts to turn on at a 3.7% duty cycle until the fault is cleared. When I_{LIM} is reached during a fault the device goes into current-limit and the fault timer keeps running.

Start-Up into a Short

The controller attempts to power on into a short for the duration of the timer. Figure 13 shows a small current resulting from power limiting the internal MOSFET. This happens only once in latched mode. In Retry mode, the cycle repeats at a 3.7% duty cycle.

Shutdown Modes

Hard Overload - Fast Trip

When a hard overload causes the load current to exceed approximately 1.6 × I_{LIM} the TPS2590 device immediately shuts off current to the load without waiting for the fault timer to expire. After such a shutoff the TPS2590 device enters startup mode and attempts to apply power to the load. If the hard overload was caused by a transient, then normal startup can be expected. If the hard overload is caused by a persistent, continuous failure then the TPS2590 device goes into current-limit during the restart attempt and either latches off or attempts retry depending on the state of the $\overline{RTRY}$ input.

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Overcurrent Shutdown

Overcurrent shutdown occurs when the output current exceeds I_{FAULT} for the duration of the fault timer. Figure 8 shows a step rise in output current which exceeds the I_{FAULT} threshold but not the I_{LIM} threshold. The increased current is on for the duration of the timer. When the timer expires, the output is turned off.

Programming the Fault (I_{FAULT}) and Current-limit (I_{LIM}) Thresholds

The I_{FAULT} and I_{LIM} thresholds are user programmable with an external resistor. The TPS2590 device uses an internal regulation loop to provide a regulated voltage on the IFLT and ILIM pins. The current-limit thresholds are proportional to the current sourced out of IFLT and ILIM. The recommended 1% resistor range is 49.9 kΩ ≤ R_{RFLT} ≤ 200 kΩ and 40.2 kΩ ≤ R_{RLIM} ≤ 100 kΩ to ensure the rated accuracy. Many applications require that minimum fault and current-limits are known or that maximum current-limit is bounded. It is important to consider the tolerance of the fault and current-limit thresholds, as well as R_{RFLT} and R_{RLIM} when selecting values. See the ELECTRICAL CHARACTERISTICS table for specific fault and current-limit settings.

Using the data for I_{FAULT} and I_{LIM} from the ELECTRICAL CHARACTERISTICS table, equations can be generated and used for other set points. Equation 13 and Equation 14 are used to calculate minimum and maximum I_{FAULT} where $R_{RFLT,max}$ and $R_{RFLT,min}$ include R_{RFLT} tolerances. Equation 15 and Equation 16 calculate $R_{RFLT,max}$ and $R_{RFLT,min}$ where R_{TOL} is the 1% resistor tolerance.

$$I_{FAULT,min} = \frac{185.58}{R_{RFLT,max}} - 0.13 \quad (13)$$

$$I_{FAULT,max} = \frac{213.68}{R_{RFLT,min}} + 0.13 \quad (14)$$

$$R_{RFLT,min} = (1 + R_{TOL}) \times \frac{213.68}{I_{FAULT,max} - 0.13} \quad (15)$$

$$R_{RFLT,max} = (1 - R_{TOL}) \times \frac{185.58}{I_{FAULT,min} + 0.13} \quad (16)$$

Equation 17 and Equation 18 are used to calculate minimum and maximum I_{LIM} where $R_{RLIM,max}$ and $R_{RLIM,min}$ include R_{RLIM} tolerances. Equation 19 and Equation 20 calculate $R_{RLIM,max}$ and $R_{RLIM,min}$ where R_{TOL} is the 1% resistor tolerance.

$$I_{LIM,min} = \frac{201.9}{R_{RLIM,max}} - 0.44 \quad (17)$$

$$I_{LIM,max} = \frac{201.9}{R_{RLIM,min}} + 0.38 \quad (18)$$

$$R_{RLIM,min} = (1 + R_{TOL}) \times \frac{201.9}{I_{LIM,max} - 0.38} \quad (19)$$

$$R_{RLIM,max} = (1 - R_{TOL}) \times \frac{201.9}{I_{LIM,min} + 0.44} \quad (20)$$

Design Example

A typical design is shown in Figure 18 with the following requirements:

- Nominal input voltage, V_{IN}: 12 V
- Maximum expected load current, I_{OUT}: 3.7 A
- Load capacitance, C_{LOAD}: 100 µF
- Expected resistive load, R_{LOAD} during start-up: 13 Ω
- Current-limit, $I_{LIM,\ min}$: > $I_{FAULT,\ max}$
- Example calculations are shown in the TPS2590 Design Calculator Tool (SLUC398).

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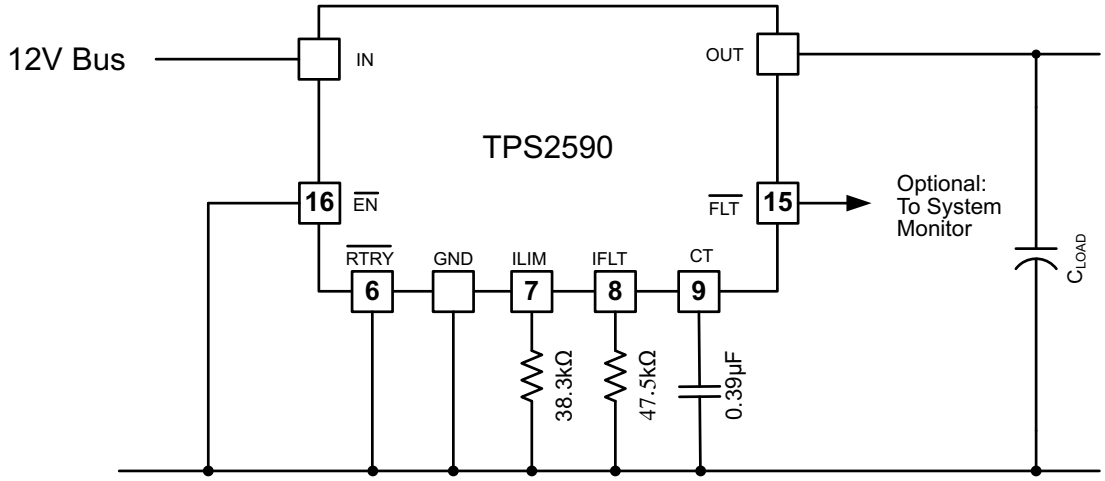

Figure 18. Design Example Schematic

1. Calculate maximum R_{RFLT} to ensure that minimum I_{FAULT} is above maximum operating load current using Equation 16 as shown below in Equation 21.

$$R_{RFLT,max} = 0.99 \times \frac{185.58}{3.7 + 0.13} = 47.97k\Omega \quad (21)$$

   - Choose a standard 1% value below $R_{RFLT,max}$ for R_{RFLT} = 47.5 kΩ
   - $I_{FAULT,min}$ = 3.738 A using Equation 13 and meets the maximum operating current requirement of 3.7 A without starting the fault timer during maximum steady state operation for R_{RFLT} = 47.5 kΩ, 1%.
   - $I_{FAULT,max}$ = 4.674 A using Equation 14 for R_{RFLT} = 47.5 kΩ, 1%.
2. Based on maximum I_{FAULT} = 4.674 A, choose minimum I_{LIM} = 4.7 A.
   - Calculate $R_{RLIM,max}$ = 38.9 kΩ using Equation 20 and 1% tolerance.
   - Choose a standard 1% value below $R_{RLIM,max}$ for R_{RLIM} = 38.3 kΩ.
   - $I_{LIM,min}$ = 4.779 A and $I_{LIM,max}$ = 5.705 A using Equation 17 and Equation 18 for R_{RLIM} = 38.3 kΩ, 1%.
3. Minimum R_{LOAD} at start-up using Equation 11 is 12 Ω. Because R_{LOAD} = 13 Ω is present during circuit start-up, use t_{ON} = 12 ms from Table 2 for C_{LOAD} = 100 µF and R_{LOAD} = 13 Ω.
   - Calculate C_{CT} = 0.39 µF including C_{LOAD} and C_{CT} tolerances (C_{LOAD_TOL} = 20% and C_{CT_TOL} = 10%) using Equation 22.

$$C_{CT} = \frac{(1 + C_{LOAD\_TOL} + C_{T\_TOL}) \times t_{ON}}{40000} = \frac{(1 + 0.2 + 0.1) \times 0.012}{40000} = 0.39\mu F \quad (22)$$

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2590 device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device.
- Transient Voltage Suppressors (TVS) on the input to absorb inductive spikes.
- Schottky diode across the output to absorb negative spikes.
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy.

The following equation estimates the magnitude of these voltage spikes:

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Where;

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C}$$

- V_{NOM} equals the nominal supply voltage
- I_{LOAD} equals the load current
- C equals the capacitance present at the input or output of the TPS2590
- L equals the effective inductance seen looking into the source or the load (23)

The inductance because of a straight length of wire equals approximately.

Where;

$$L_{straightwire} \approx 0.2 \times L \times \ln\left(\frac{4 \times L}{D} - 0.75\right) (nH)$$

- L equals the length of the wire
- D equals wire diameter (24)

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

Layout

Support Components

Locate all TPS2590 support components, R_{RFLT}, R_{RLIM}, C_{CT}, or any input or output voltage clamps, close to their connection pin. Connect the other end of the component to the inner layer GND without trace length. The traces routing the R_{RFLT} and R_{RLIM} resistors to the TPS2590 device must be as short as possible to reduce parasitic effects on fault and current-limit accuracy.

PowerPad™

When properly mounted the PowerPad package provides significantly greater cooling ability than an ordinary package. To operate at rated power the Power Pad must be soldered directly to the PC board GND plane directly under the device. The PowerPad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to *Technical Briefs: PowerPAD™ Thermally Enhanced Package* (TI Literature Number SLMA002) and *PowerPAD™ Made Easy* (TI Literature Number SLMA004) for more information on using this PowerPad package. These documents are available at www.ti.com (Search by Keyword).

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REVISION HISTORY

Changes from Original (July 2009) to Revision A **Page**

- Changed the Application diagram 1

Changes from Revision A (July 2010) to Revision B **Page**

- Added Feature: UL Listed - File Number E169910 1
- Changed the Application diagram 1

Changes from Revision B (August 2010) to Revision C **Page**

- Added the IFLT description 6
- Changed current-limit vs Junction Temperature graph 7

Changes from Revision C (September 2011) to Revision D **Page**

- Changed Figure 5 through Figure 15. 7

Changes from Revision D (October 2011) to Revision E **Page**

- Changed the RECOMMENDED OPERATING CONDITIONS table 2
- Changed the ELECTRICAL CHARACTERISTICS table 3
- Changed the PIN DESCRIPTION, CT section 5
- Changed the PIN DESCRIPTION, ILIM section 6
- Changed the PIN DESCRIPTION, $\overline{EN}$ section 6
- Changed the PIN DESCRIPTION, VIN section: 18 V to 20 V and VIN to IN 6
- Changed the PIN DESCRIPTION, OUT section 6
- Changed the APPLICATION INFORMATION SECTION. Deleted the Maximum Load at Startup section. 10
- Changed the Transient Protection section 14

Changes from Revision E (April 2013) to Revision F **Page**

- Deleted Voltage IFAULT, ILIM from the ABSOLUTE MAXIMUM RATINGS table 2

Changes from Revision F (May 2013) to Revision G **Page**

- Deleted the minimum voltage from the voltage range listed in the document title, features list and description 1
- Added 5-A to document title 1
- Changed *listed* to *recognized* in last Features bullet. Also added 2367 to UL number 1
- Added SSDs, PCIE, and Fan Control list items to the *APPLICATIONS* list 1
- Added UV turn-on threshold and bus voltage text to the first paragraph of the *DESCRIPTION* 1
- Deleted *ORDERING INFORMATION* table 2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2590RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 2590	Samples
TPS2590RSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 2590	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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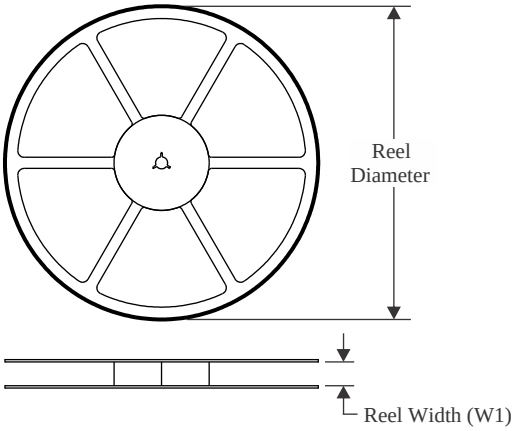
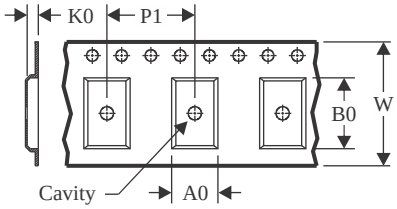
TAPE AND REEL INFORMATION

REEL DIMENSIONS

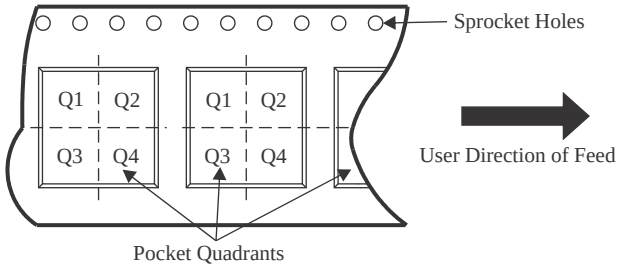


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2590RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2590RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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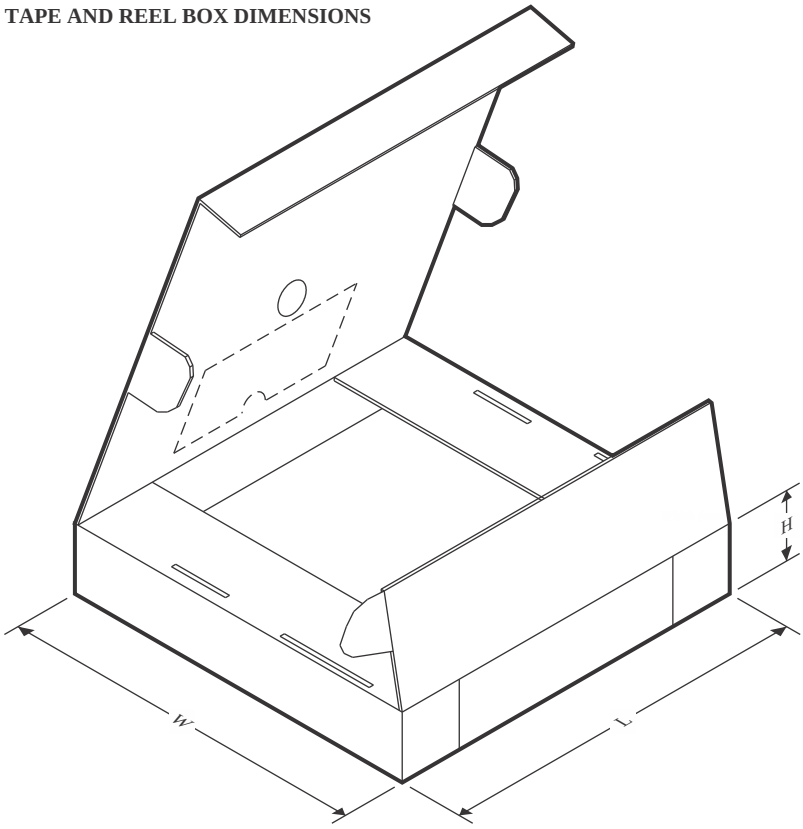
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2590RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
TPS2590RSAT	QFN	RSA	16	250	210.0	185.0	35.0

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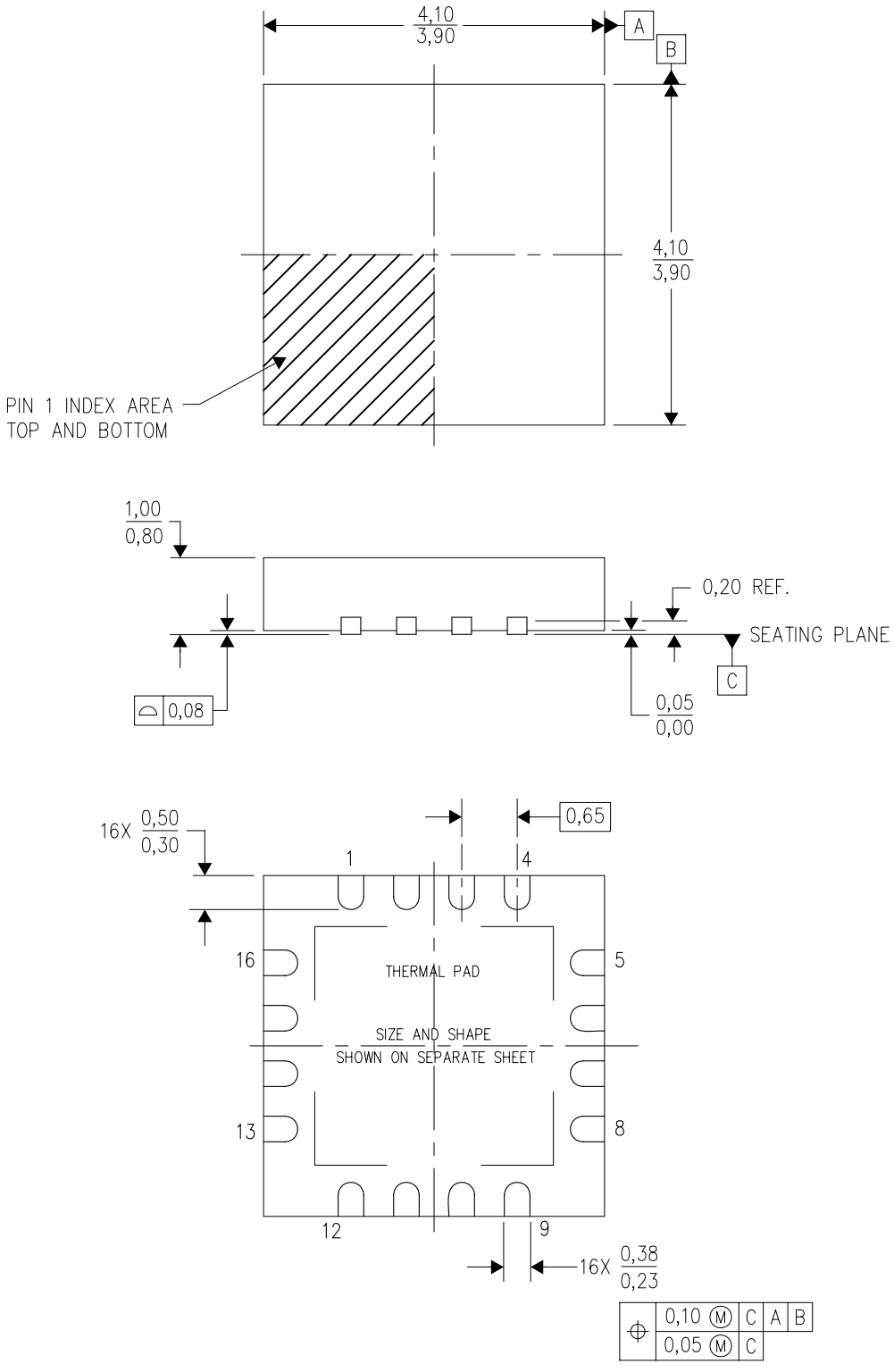
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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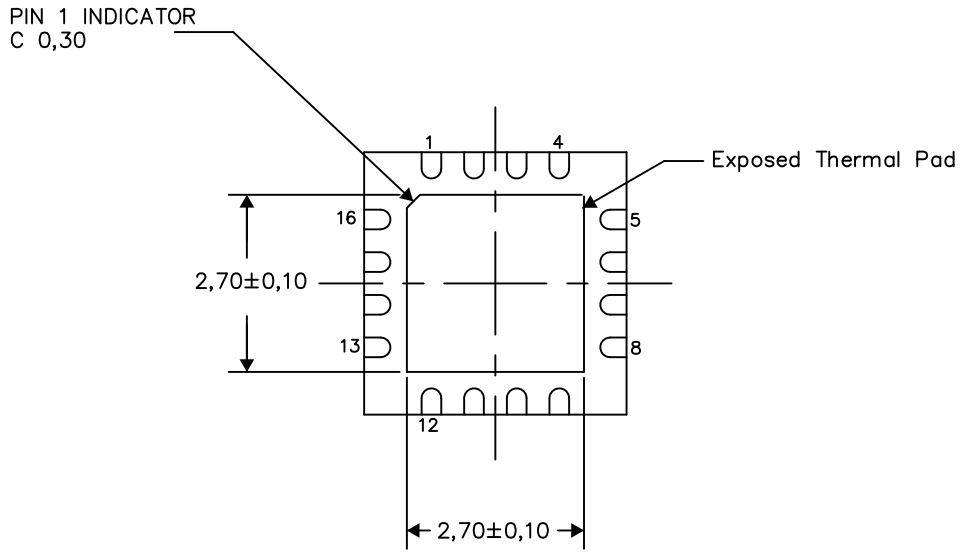
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

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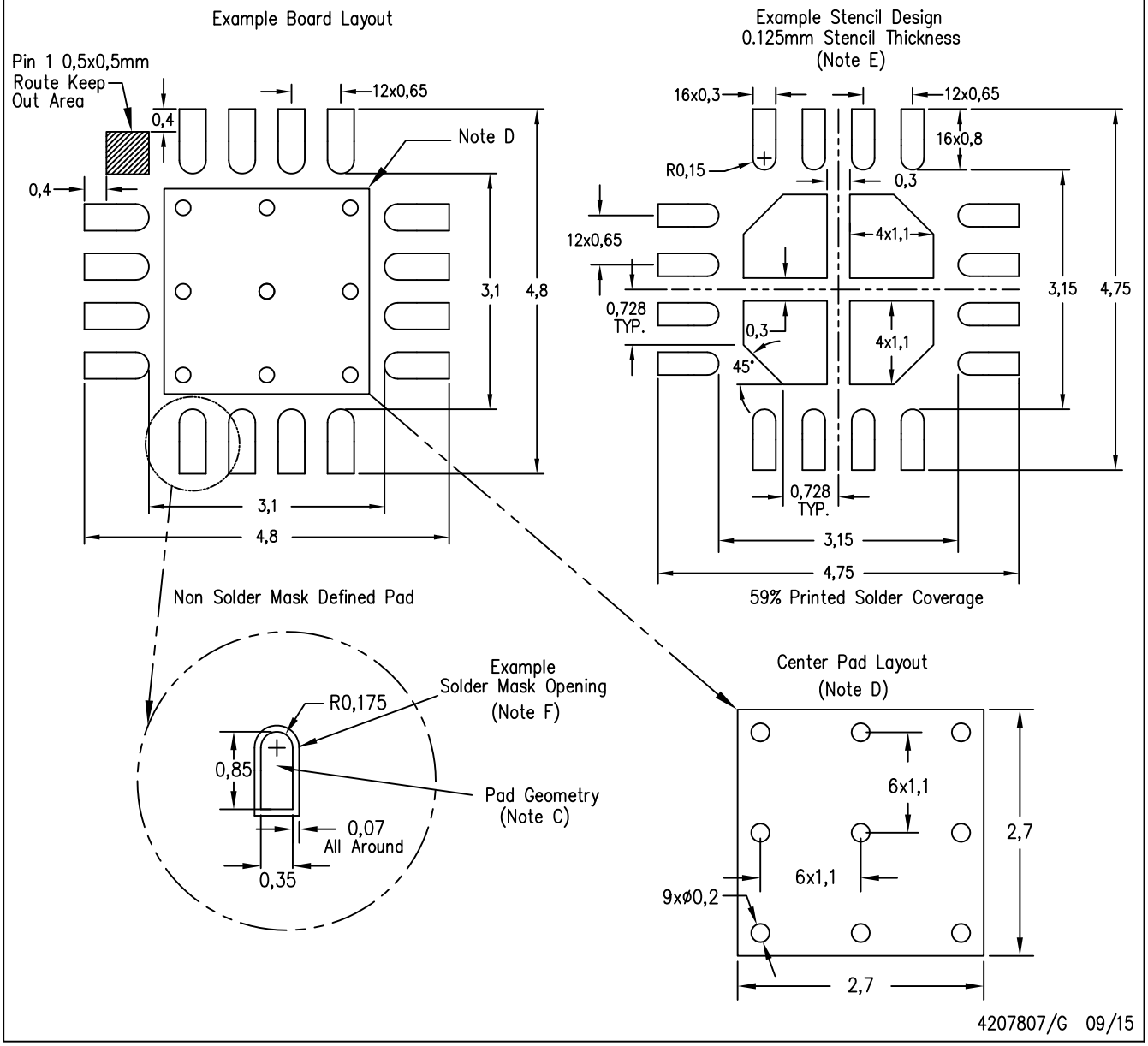
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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