TEXAS INSTRUMENTS

LM5010

SNVS307G –SEPTEMBER 2004–REVISED APRIL 2016

LM5010 High-Voltage 1-A Step-Down Switching Regulator

1 Features

- Input Voltage Range: 8 V to 75 V
- Valley Current Limit At 1.25 A
- Switching Frequency Can Exceed 1 MHz
- Integrated N-Channel Buck Switch
- Integrated Start-Up Regulator
- No Loop Compensation Required
- Ultra-Fast Transient Response
- Operating Frequency Remains Constant With Load and Line Variations
- Maximum Duty Cycle Limited During Start-Up
- Adjustable Output Voltage
- Precision 2.5-V Feedback Reference
- Thermal Shutdown
- Exposed Thermal Pad for Improved Heat Dissipation

2 Applications

- High Efficiency Point-of-Load (POL) Regulator
- Non-Isolated Telecommunications Buck Regulator
- Secondary High Voltage Post Regulator
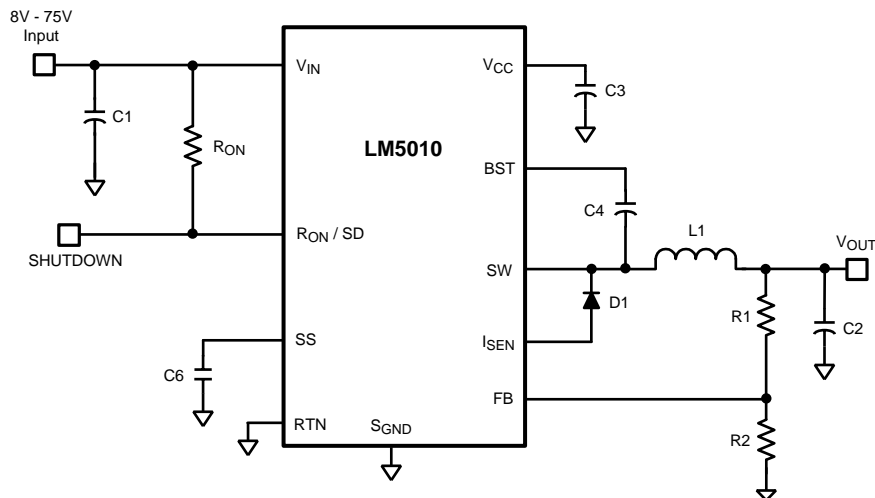- Automotive Systems

3 Description

The LM5010 step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck bias regulator capable of supplying in excess of 1-A load current. This high-voltage regulator contains an N-Channel Buck Switch, and is available in thermally enhanced 10-pin WSON and 14-pin HTSSOP packages. The hysteretic regulation scheme requires no loop compensation, resulting in fast load transient response, and simplifies circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the ON-time. The valley current limit detection is set at 1.25 A. Additional features include: VCC undervoltage lockout, thermal shutdown, gate drive undervoltage lockout, and maximum duty cycle limiter.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5010	WSON (10)	4.00 mm × 4.00 mm
	HTSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Basic Step-Down Regulator

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2013) to Revision G   **Page**

• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision E (February 2013) to Revision F   **Page**

• Changed layout of National Data Sheet to TI format 1

5 Pin Configuration and Functions

**DPR Package
10-Pin WSON
Top View**

**PWP Package
14-Pin HTSSOP
Top View**

Pin Functions

PIN			I/O	DESCRIPTION
NAME	WSON	HTSSOP		
BST	2	3	I	Boost pin for bootstrap capacitor: Connect a 0.022-µF capacitor from SW to this pin. The capacitor is charged from VCC through an internal diode during each OFF-time.
EP	—	—	—	Exposed pad
FB	6	9	I	Feedback input from the regulated output: Internally connected to the regulation and overvoltage comparators. The regulation level is 2.5 V.
I_{SEN}	3	4	I	Current sense: The recirculating current flows through the internal sense resistor, and out of this pin to the free-wheeling diode. Current limit is nominally set at 1.25 A.
NC	—	1, 7, 8, 14	—	No connection
R_{ON}/SD	8	11	I	ON-time control and shutdown: An external resistor from VIN to this pin sets the buck switch ON-time. Grounding this pin shuts down the regulator.
RTN	5	6	—	Circuit ground: Ground for all internal circuitry other than the current limit detection.
S_{GND}	4	5	—	Sense ground: Recirculating current flows into this pin to the current sense resistor.
SS	7	10	I	Soft start: An internal 11.5-µA current source charges an external capacitor to 2.5 V, providing the soft start function.
SW	1	2	O	Switching node: Internally connected to the buck switch source. Connect to the inductor, free-wheeling diode, and bootstrap capacitor.
VCC	9	12	I	Output from the startup regulator: Nominally regulates at 7 V. An external voltage (7.5 V to 14 V) can be applied to this pin to reduce internal dissipation. An internal diode connects VCC to VIN.
VIN	10	13	I	Input supply: Nominal input range is 8 V to 75 V.

Product Folder Links: *LM5010*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
VIN	8	75	V
VIN to GND		76	V
BST to GND		90	V
SW to GND (steady state)		−1.5	V
BST to VCC		76	V
BST to SW		14	V
VCC to GND		14	V
S_{GND} to RTN	−0.3	0.3	V
SS to RTN	−0.3	4	V
VIN to SW		76	V
All other inputs to GND	−0.3	7	V
Lead temperature (soldering, 4 s)[2]		260	°C
Junction temperature, T_J	−40	150	°C
Storage temperature, T_{stg}	−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For detailed information on soldering plastic HTSSOP and WSON packages, see *Mechanical, Packaging, and Orderable Information*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	8	75	V
I_O	Output current		1	A
Ext-V_{CC}	External bias voltage	8	13	V
T_J	Operating junction temperature	−40	125	°C

Product Folder Links: *LM5010*

6.4 Thermal Information

THERMAL METRIC[1]	LM5010 DPR (WSON) 10 PINS	LM5010 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	36	41.1	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	31.9	26.5	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	13.2	22.5	°C/W
ψ_{JT} Junction-to-top characterization parameter	0.3	0.7	°C/W
ψ_{JB} Junction-to-board characterization parameter	13.5	22.2	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	3	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C, minimum and maximum limits apply over T_J = –40°C to 125°C, V_{IN} = 48 V, and R_{ON} = 200 kΩ (unless otherwise noted). [1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} REGULATOR						
V_{CC}Reg	VCC regulated output		6.6	7	7.4	V
	V_{IN} - V_{CC}	I_{CC} = 0 mA, F_S < 200 kHz, 7.5 V ≤ V_{IN} ≤ 8 V		1.3		V
	V_{CC} output impedance (0 mA ≤ I_{CC} ≤ 5 mA)	V_{IN} = 8 V		140		Ω
		V_{IN} = 48 V		2.5		
	V_{CC} current limit	V_{CC} = 0 V		10		mA
UVLO$_{VCC}$	V_{CC} undervoltage lockout threshold	V_{CC} increasing		5.8		V
	UVLO$_{VCC}$ hysteresis	V_{CC} decreasing		145		mV
	UVLO$_{VCC}$ filter delay	100-mV overdrive		3		µs
	I_{IN} operating current	Non-switching, FB = 3 V		650	850	µA
	I_{IN} shutdown current	R_{ON}/SD = 0 V		95	200	µA
SOFT-START PIN						
	Pullup voltage			2.5		V
	Internal current source			11.5		µA
CURRENT LIMIT						
I_{LIM}	Threshold	Current out of I_{SEN}	1	1.25	1.5	A
	Resistance from I_{SEN} to S_{GND}			130		mΩ
	Response time			150		ns
R_{ON}/SD PIN						
	Shutdown threshold	Voltage at R_{ON}/SD rising	0.35	0.65	1.1	V
	Threshold hysteresis	Voltage at R_{ON}/SD falling		40		mV
HIGH-SIDE FET						
$R_{DS(ON)}$	Buck switch	I_{TEST} = 200 mA		0.35	0.8	Ω
UVLO$_{GD}$	Gate drive UVLO	V_{BST} - V_{SW} Increasing	3	4.3	5	V
	UVLO$_{GD}$ Hysteresis			440		mV
REGULATION AND OVERVOLTAGE COMPARATORS (FB PIN)						
V_{REF}	FB regulation threshold	SS pin = steady state	2.45	2.5	2.55	V
	FB overvoltage threshold			2.9		V
	FB bias current			1		nA

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \times R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in *Thermal Information*.

Product Folder Links: *LM5010*

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C, minimum and maximum limits apply over T_J = –40°C to 125°C, V_{IN} = 48 V, and R_{ON} = 200 kΩ (unless otherwise noted).[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			175		°C
	Thermal shutdown hysteresis			20		°C

6.6 Switching Characteristics

Typical values correspond to T_J = 25°C, minimum and maximum limits apply over T_J = –40°C to 125°C and V_{IN} = 48 V (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Buck switch	I_{TEST} = 200 mA		0.35	0.8	Ω
$UVLO_{GD}$	Gate drive UVLO	V_{BST} - V_{SW} Increasing	3	4.3	5	V
	$UVLO_{GD}$ Hysteresis			440		mV
OFF TIMER						
t_{OFF}	Minimum OFF-time			265		ns
ON TIMER						
t_{ON} - 1	ON-time	V_{IN} = 10 V, R_{ON} = 200 kΩ	2.1	2.75	3.4	µs
t_{ON} - 2	ON-time	V_{IN} = 75 V, R_{ON} = 200 kΩ	290	390	490	ns

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations while applying statistical process control.

Product Folder Links: *LM5010*

6.7 Typical Characteristics
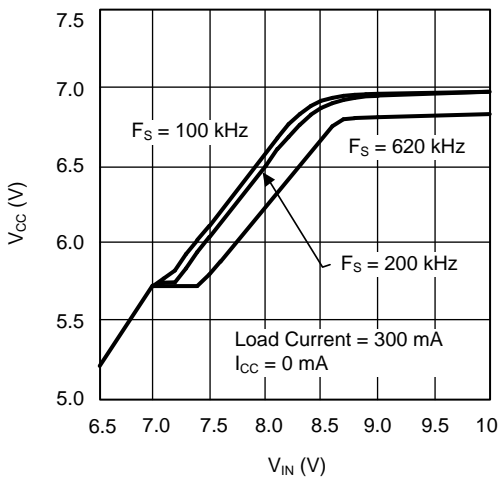
at T_A = 25°C (unless otherwise noted)
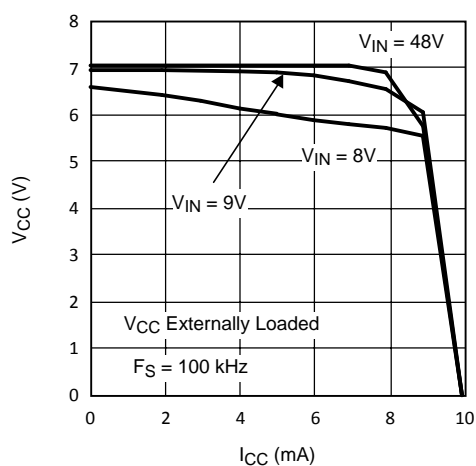

Figure 1. V_{CC} vs V_{IN}

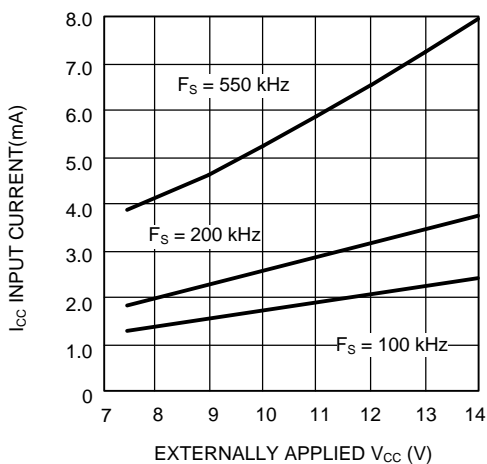Figure 2. V_{CC} vs I_{CC}

Figure 3. I_{CC} vs Externally Applied V_{CC}
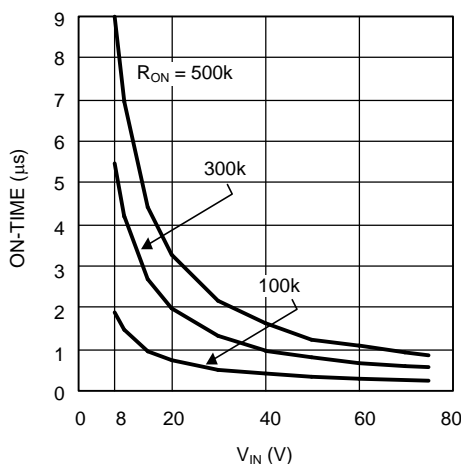

Figure 4. ON-Time vs V_{IN} and R_{ON}
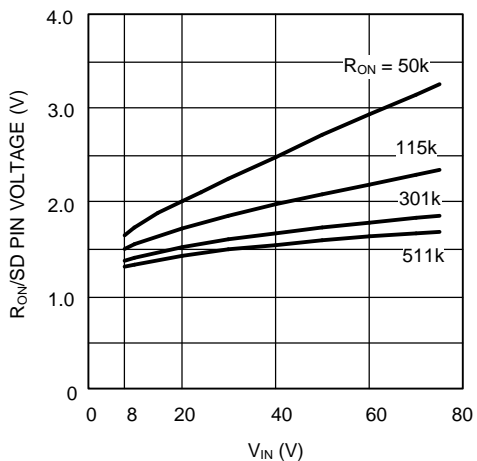
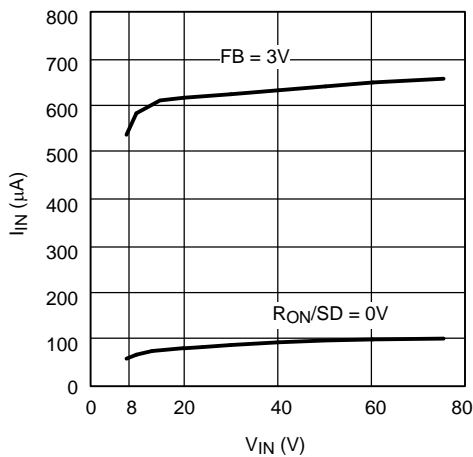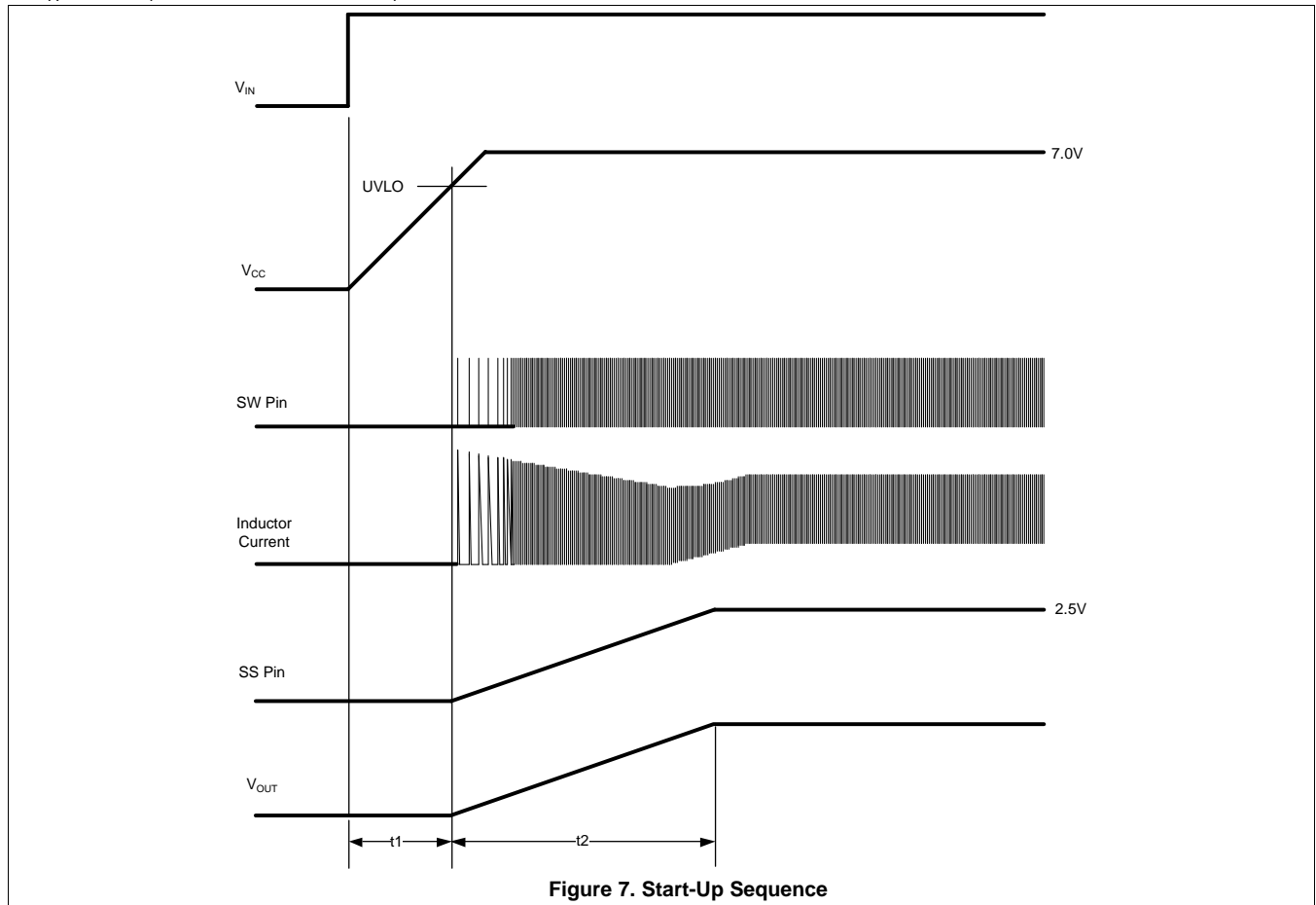Figure 5. Voltage at R_{ON}/SD Pin

Figure 6. I_{IN} vs V_{IN}

Product Folder Links: *LM5010*

Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

Figure 7. Start-Up Sequence
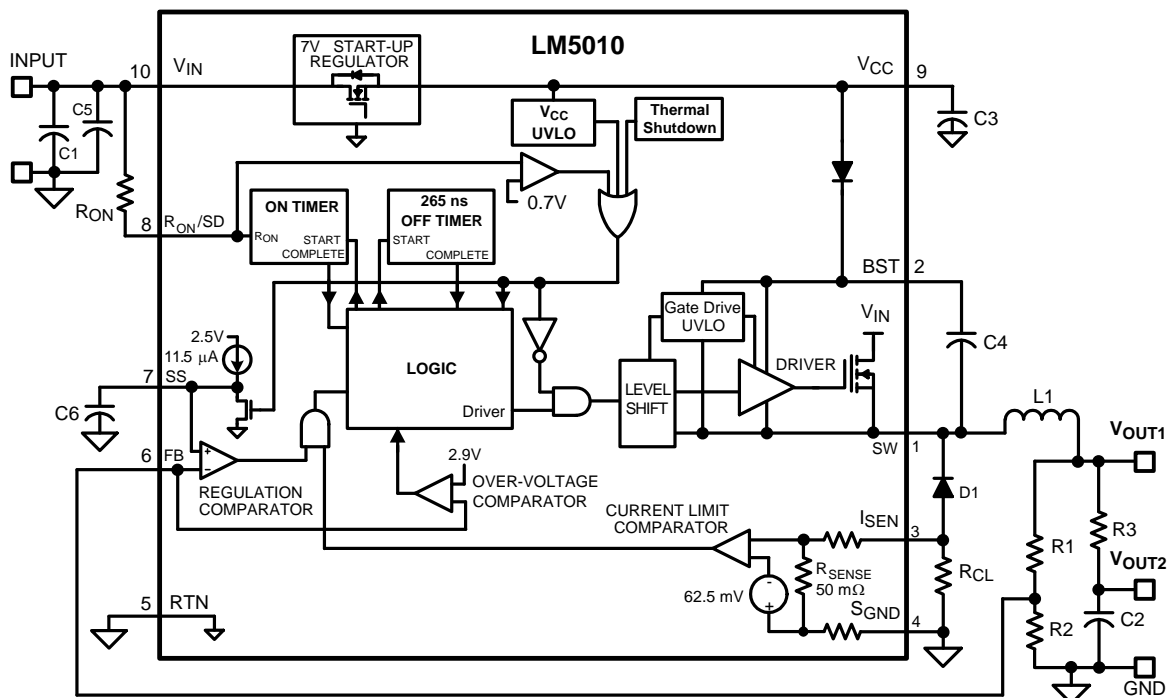
Product Folder Links: *LM5010*

7 Detailed Description

7.1 Overview

The LM5010 step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck bias power converter. This high-voltage regulator contains a 75-V N-channel buck switch, is easy to implement, and is provided in HTSSOP and thermally-enhanced, WSON packages. The regulator is based on a control scheme using an ON-time inversely proportional to V_{IN}. The control scheme requires no loop compensation. The functional block diagram of the LM5010 is shown in the *Functional Block Diagram*.

The LM5010 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well-suited for 48-V telecom and 42-V automotive power bus ranges. Additional features include: thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limit timer, and the valley current limit functionality.

7.2 Functional Block Diagram

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Pin numbers are for the WSON (10) package

7.3 Feature Description

The LM5010 step-down switching regulator features all the functions needed to implement a low-cost, efficient buck bias power converter capable of supplying in excess of 1 A to the load. This high voltage regulator contains an N-Channel buck switch, is easy to implement, and is available in the thermally enhanced 10-pin WSON and 14-pin HTSSOP packages. The regulator's operation is based on a constant ON-time control scheme, where the ON-time varies inversely with V_{IN}. This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The switching frequency can range from 100 kHz to > 1 MHz. The hysteretic control requires no loop compensation, resulting in very fast load transient response. The valley current limit detection circuit, internally set at 1.25 A, holds the buck switch off until the high current level subsides. The LM5010 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48-V telecom applications, as well as the new 42-V automotive power bus. Implemented as a point-of-load regulator following a highly-efficient intermediate bus converter can result in high overall system efficiency. Features include: Thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, and maximum duty cycle limit.

Feature Description (continued)

7.3.1 Control Circuit Overview

The LM5010 buck DC-DC regulator employs a control scheme based on a comparator and a one-shot ON timer, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB voltage is below the reference the buck switch is turned on for a time period determined by the input voltage and a programming resistor (R_{ON}). Following the ON-time the switch remains off for 265 ns, or until the FB voltage falls below the reference, whichever is longer. The buck switch then turns on for another ON-time period. Typically when the load current increases suddenly, the OFF-times are temporarily at the minimum of 265 ns. Once regulation is established, the OFF-time resumes its normal value. The output voltage is set by two external resistors (R1, R2). The regulated output voltage is calculated with Equation 1.

$$V_{OUT} = 2.5 \text{ V} \times (R1 + R2) / R2 \tag{1}$$

Output voltage regulation is based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. The LM5010 requires a minimum of 25-mV of ripple voltage at the FB pin. In cases where the capacitor's ESR is insufficient, additional series resistance may be required (R3 in *Functional Block Diagram*).

When in regulation, the LM5010 operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode current always flows through the inductor, never reaching zero during the OFF-time. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. Calculate the approximate operating frequency with Equation 2.

$$F_S = \frac{V_{OUT}}{1.18 \times 10^{-10} \times R_{ON}} \tag{2}$$

The buck switch duty cycle is approximately equal to Equation 3.

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

At low load current, the circuit operates in discontinuous conduction mode, during which the inductor current ramps up from zero to a peak during the ON-time, then ramps back to zero before the end of the OFF-time. The next ON-time period starts when the voltage at FB falls below the reference until then the inductor current remains zero, and the load current is supplied by the output capacitor (C2). In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained at light loads because the switching losses reduce with the reduction in load and frequency. Calculate the approximate discontinuous operating frequency with Equation 4.

$$F_S = \frac{V_{OUT}^2 \times L1 \times 1.4 \times 10^{20}}{R_L \times (R_{ON})^2}$$

where

- R_L = the load resistance $\tag{4}$

For applications where lower output voltage ripple is required, the output can be taken directly from a low ESR output capacitor as shown in Figure 8. However, R3 slightly degrades the load regulation.

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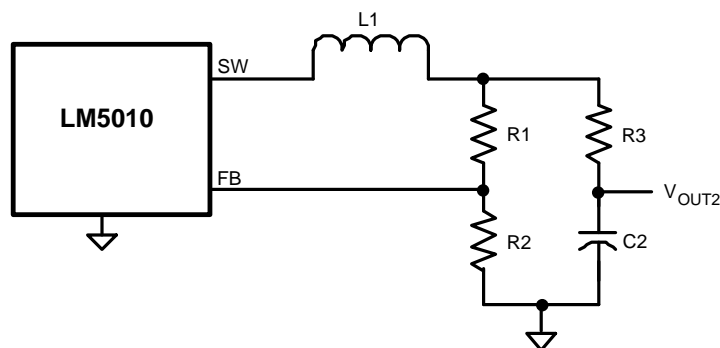
Feature Description (continued)

Figure 8. Low Ripple Output Configuration

7.3.2 Start-Up Regulator (VCC)

The start-up regulator is integral to the LM5010. The input pin (VIN) can be connected directly to line voltages up to 75 V. The VCC output is regulated at 7 V, ±6%, and is current-limited to 10 mA. Upon power up the regulator sources current into the external capacitor at VCC (C3). With a 0.1-µF capacitor at VCC, approximately 58 µs are required for the VCC voltage to reach the undervoltage lockout threshold (UVLO) of 5.8 V (t1 in Figure 7), at which time the buck switch is enabled, and the soft-start pin is released to allow the soft-start capacitor (C6) to charge up. V_{OUT} then increases to its regulated value as the soft-start voltage increases (t2 in Figure 7).

The minimum input operating voltage is determined by the regulator's dropout voltage, the V_{CC} UVLO falling threshold (≈5.65 V), and the frequency. When V_{CC} falls below the falling threshold the V_{CC} UVLO activates to shut off the buck switch and ground the soft-start pin. If VCC is externally loaded, the minimum input voltage increases since the output impedance at VCC is ≈140 Ω at low V_{IN}. See Figure 1 and Figure 2. In applications involving a high value for V_{IN} where power dissipation in the start-up regulator is a concern, an auxiliary voltage can be diode connected to the VCC pin (Figure 9). Setting the auxiliary voltage to between 7.5 V and 14 V shuts off the internal regulator, reducing internal power dissipation. Figure 3 shows the current required into the VCC pin. A diode connects VCC to VIN internally.
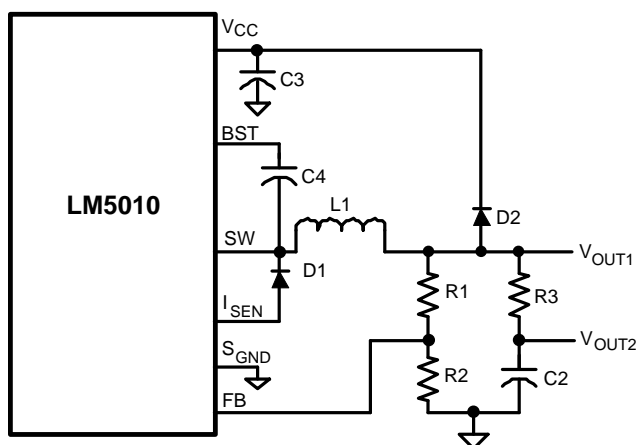

Figure 9. Self Biased Configuration

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to the voltage at the soft-start pin (2.5 V, ±2%). In normal operation (the output voltage is regulated) an ON-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch stays on for the ON-time causing the FB voltage to rise above 2.5 V. After the ON-time period the buck switch stays off until the FB voltage falls below 2.5 V. Bias current at the FB pin is less than 5 nA over temperature.

Product Folder Links: *LM5010*

Feature Description (continued)

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.9-V reference. If the voltage at FB rises above 2.9 V, the ON-time is immediately terminated. This condition can occur if the input voltage or the output load changes suddenly. The buck switch will not turn on again until the voltage at FB falls below 2.5 V.

7.3.5 ON-Time Control

The ON-time of the internal switch (see Figure 4) is determined by the R_{ON} resistor and the input voltage (V_{IN}), calculated with Equation 5.

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R_{ON} + 1.4k)}{V_{IN} - 1.4V} + 67 \text{ ns}$$

(5)

The inverse relationship of t_{ON} vs V_{IN} results in a nearly constant frequency as V_{IN} is varied. If the application requires a high frequency, the minimum value for t_{ON}, and consequently R_{ON}, is limited by the OFF-time (265 ns, ±15%) which limits the maximum duty cycle at minimum V_{IN}. The tolerance for Equation 5 is ±25%. Frequencies in excess of 1 MHz are possible with the LM5010.

7.3.6 Current Limit

Current limit detection occurs during the OFF-time by monitoring the recirculating current through the free-wheeling diode (D1). The detection threshold is 1.25 A, ±0.25 A. Referring to *Functional Block Diagram*, when the buck switch is off the inductor current flows through the load, into S_{GND}, through the sense resistor, out of I_{SEN} and through D1. If that current exceeds the threshold the current limit comparator output switches to delay the start of the next ON-time period. The next ON-time starts when the current out of I_{SEN} is below the threshold and the voltage at FB is below 2.5 V. If the overload condition persists causing the inductor current to exceed the threshold during each ON-time, that is detected at the beginning of each OFF-time. The operating frequency is lower due to longer-than-normal OFF-times.

Figure 10 illustrates the inductor current waveform. During normal operation the load current is I_O, the average of the ripple waveform. When the load resistance decreases the current ratchets up until the lower peak attempts to exceed the threshold. During the Current Limited portion of Figure 10, the current ramps down to the threshold during each OFF-time, initiating the next ON-time (assuming the voltage at FB is < 2.5 V). During each ON-time the current ramps up an amount equal to Equation 6.

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L1}$$

(6)

During this time the LM5010 is in a constant current mode, with an average load current (I_{OCL}) equal to the threshold + ΔI / 2.

The valley current limit technique allows the load current to exceed the current limit threshold as long as the lower peak of the inductor current is less than the threshold.

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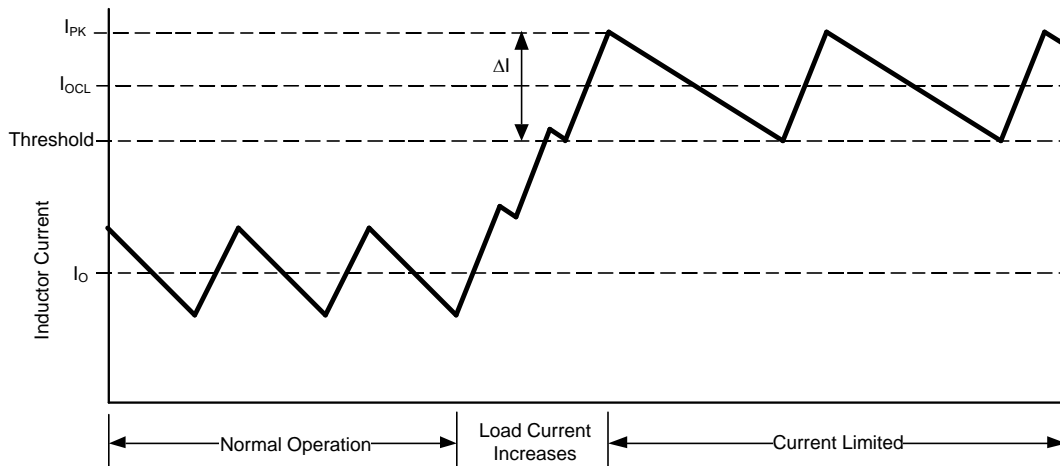
Feature Description (continued)

Figure 10. Inductor Current, Current Limit Operation

The current limit threshold can be increased by connecting an external resistor (R_{CL}) between S_{GND} and I_{SEN}. The external resistor typically is less than 1 Ω, and its calculation is explained in *Application and Implementation*.

The peak current out of SW and I_{SEN} must not exceed 3.5 A. The average current out of SW must be less than 3 A, and the average current out of I_{SEN} must be less than 2 A.

7.3.7 Soft Start

The soft-start feature allows the converter to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. Upon turnon, after V_{CC} reaches the undervoltage threshold (t1 in Figure 7), an internal 11.5-μA current source charges the external capacitor at the soft-start pin to 2.5 V (t2 in Figure 7). The ramping voltage at SS (and at the non-inverting input of the regulation comparator) ramps up the output voltage in a controlled manner. This feature keeps the load current from going to current limit during start-up, thereby reducing inrush currents.

An internal switch grounds the soft-start pin if V_{CC} is below the undervoltage lockout threshold, if a thermal shutdown occurs, or if the circuit is shutdown using the R_{ON}/SD pin.

7.3.8 N-Channel Buck Switch and Driver

The LM5010 integrates an N-Channel buck switch and associated floating high voltage gate driver. The peak current through the buck switch must not be allowed to exceed 3.5 A, and the average current must be less than 3 A. The gate driver circuit is powered by the external bootstrap capacitor between BST and SW (C4). During each OFF-time, the SW pin is at approximately −1 V, and C4 is recharged from VCC through the internal high voltage diode. The minimum OFF-time of 265 ns ensures a minimum time each cycle to recharge the bootstrap capacitor. TI recommends a 0.022-μF ceramic capacitor for C4.

7.3.9 Thermal Shutdown

The LM5010 should be operated so the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal Thermal Shutdown circuit activates (typically) at 175°C, taking the controller to a low-power reset state by disabling the buck switch and the ON timer, and grounding the soft-start pin. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 155°C (typical hysteresis = 20°C), the softstart pin is released and normal operation resumes.

7.4 Device Functional Modes

7.4.1 Shutdown

The LM5010 can be remotely shut down by taking the R_{ON}/SD pin below 0.65 V. See Figure 11. In this mode the soft-start pin is internally grounded, the ON timer is disabled, and the input current at V_{IN} is reduced (Figure 6). Releasing the R_{ON}/SD pin allows normal operation to resume. When the switch is open, the nominal voltage at R_{ON}/SD is shown in Figure 5.
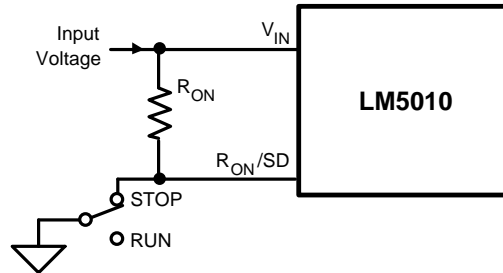

Figure 11. Shutdown Implementation

8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5010 is a non-synchronous buck regulator converter designed to operate over a wide input voltage and output current range. Spreadsheet-based calculator tools, available on the TI product website at Quick-Start Calculator, can be used to design a single output non-synchronous buck converter.

Alternatively, online WEBENCH® software is available to create a complete buck design and generate the bill of materials, estimated efficiency, solution size, and cost of the complete solution.

8.2 Typical Application

The final circuit is shown in Figure 12, and its performance is shown from Figure 14 to Figure 17.
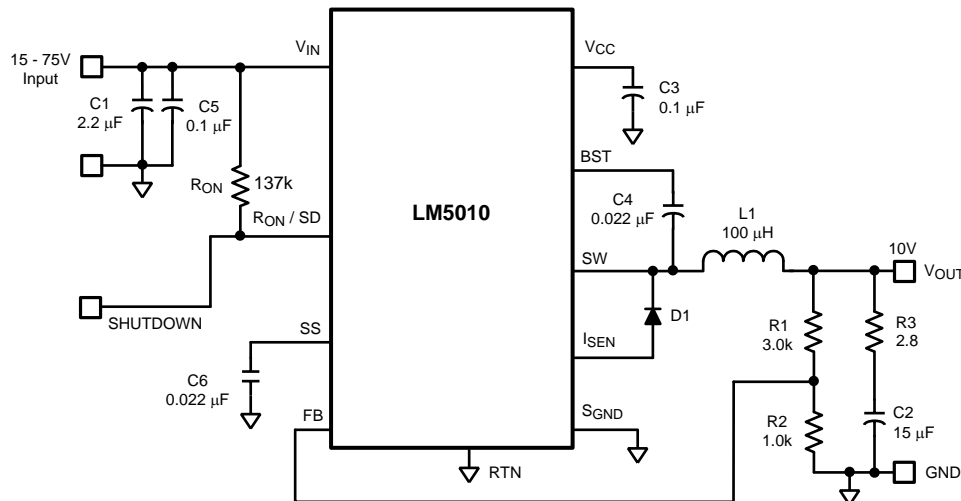
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Figure 12. LM5010 Example Circuit

8.2.1 Design Requirements

Table 1 lists the operating parameters for Figure 12.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	15 V to 75 V
Output voltage	10 V
Load current	150 mA to 1 A
Soft-start time	5 ms

8.2.2 Detailed Design Procedure

The procedure for calculating the external components is illustrated with a design example. Configure the circuit in Figure 12 according to the components listed in Table 2.

Product Folder Links: LM5010

Table 2. List of Components for LM5010 Example Circuit

COMPONENT	DESCRIPTION	VALUE
C1	Ceramic Capacitor	2.2 µF, 100 V
C2	Ceramic Capacitor	15 µF, 25 V
C3	Ceramic Capacitor	0.1 µF, 16 V
C4, C6	Ceramic Capacitor	0.022 µF, 16 V
C5	Ceramic Capacitor	0.1 µF, 100 V
D1	Ultra-fast diode	100 V, 2 A
L1	Inductor	100 µH
R1	Resistor	3 kΩ
R2	Resistor	1 kΩ
R3	Resistor	2.8 Ω
R_{ON}	Resistor	137 kΩ
U1	Switching regulator	—

8.2.2.1 Component Selection

8.2.2.1.1 R1 and R2

Calculate the ratio of these resistors with Equation 7.

$$R1 / R2 = (V_{OUT} / 2.5 \text{ V}) - 1 \tag{7}$$

R1 and R2 calculates to 3. The resistors should be chosen from standard value resistors in the range of 1 kΩ to 10 kΩ. Values of 3 kΩ for R1, and 1 kΩ for R2 are used.

8.2.2.1.2 R_{ON}, F_S

R_{ON} sets the ON-time, and can be chosen using Equation 2 to set a nominal frequency, or from Equation 5 if the ON-time at a particular V_{IN} is important. A higher frequency generally means a smaller inductor and capacitors (value, size and cost), but higher switching losses. A lower frequency means a higher efficiency, but with larger components. If PC board space is tight, a higher frequency is better. The resulting ON-time and frequency have a ±25% tolerance, rearranging Equation 2 to Equation 8.

$$R_{ON} = \frac{10V}{1.18 \times 10^{-10} \times 625 \text{ kHz}} = 136 \text{ k}\Omega \tag{8}$$

The next larger standard value (137 kΩ) is chosen for R_{ON}, yielding a nominal frequency of 618 kHz.

8.2.2.1.3 L1

The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$). See Figure 13.
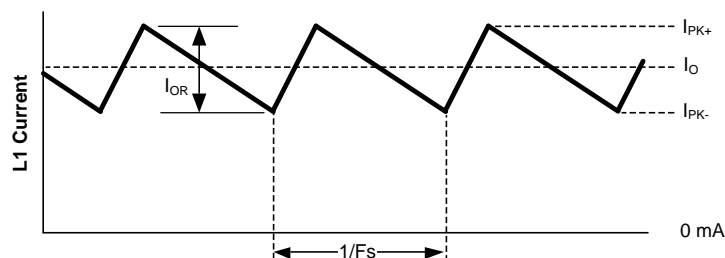
Figure 13. Inductor Current

To keep the circuit in continuous conduction mode, the maximum allowed ripple current is twice the minimum load current, or 300 mA$_{P-P}$. Using this value of ripple current, the inductor (L1) is calculated using Equation 9 and Equation 10.

$$L1 = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{I_{OR} \times F_{S(min)} \times V_{IN(max)}}$$

where

- $F_{S(min)}$ is the minimum frequency (F_S - 25%)   (9)

$$L1 = \frac{10V \times (75V - 10V)}{0.30A \times 463 \text{ kHz} \times 75V} = 63 \text{ } \mu H$$

(10)

Equation 10 provides the minimum value for inductor L1. When selecting an inductor, use a higher standard value (100 uH). L1 must be rated for the peak current (I_{PK+}) to prevent saturation. The peak current occurs at maximum load current with maximum ripple. The maximum ripple is calculated by rearranging Equation 9 using $V_{IN(max)}$, $F_{S(min)}$, and the minimum inductor value, based on the manufacturer's tolerance. Assume for Equation 11, Equation 12, and Equation 13 that the inductor's tolerance is ±20%.

$$I_{OR(max)} = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{L1_{MIN} \times F_{S(min)} \times V_{IN(max)}}$$

(11)

$$I_{OR(max)} = \frac{10V \times (75V - 10V)}{80 \text{ } \mu H \times 463 \text{ kHz} \times 75V} = 234 \text{ mAp-p}$$

(12)

$$I_{PK+} = 1 \text{ A} + 0.234 \text{ A} / 2 = 1.117 \text{ A}$$ (13)

8.2.2.1.4 R_{CL}

Since it is obvious that the lower peak of the inductor current waveform does not exceed 1 A at maximum load current (see Figure 13), it is not necessary to increase the current limit threshold. Therefore R_{CL} is not needed for this exercise. For applications where the lower peak exceeds 1 A, see *Increasing The Current Limit Threshold*.

8.2.2.1.5 C2 and R3

Since the LM5010 requires a minimum of 25 mV_{P-P} of ripple at the FB pin for proper operation, the required ripple at V_{OUT1} is increased by R1 and R2. This necessary ripple is created by the inductor ripple current acting on C2's ESR + R3. First, determine the minimum ripple current with Equation 14.

$$I_{OR(min)} = \frac{V_{OUT1} \times (V_{IN(min)} - V_{OUT1})}{L1_{MAX} \times F_{S(max)} \times V_{IN(min)}}$$

$$= \frac{10V \times (15V - 10V)}{120 \text{ } \mu H \times 772 \text{ kHz} \times 15V} = 36 \text{ mA}$$

(14)

The minimum ESR for C2 is then equal to Equation 15.

$$ESR_{(min)} = \frac{25 \text{ mV} \times (R1 + R2)}{R2 \times I_{OR(min)}} = 2.8\Omega$$

(15)

If the capacitor used for C2 does not have sufficient ESR, R3 is added in series as shown in Figure 12. C2 should generally be no smaller than 3.3 µF, although that is dependent on the frequency and the allowable ripple amplitude at V_{OUT1}. Experimentation is usually necessary to determine the minimum value for C2, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C2 than a non-varying load.

Product Folder Links: *LM5010*

8.2.2.1.6 D1

The important parameters are reverse recovery time and forward voltage drop. The reverse recovery time determines how long the current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is mainly this diode's voltage (plus the voltage across the current limit sense resistor) which forces the inductor current to decrease during the OFF-time. For this reason, a higher voltage is better, although that affects efficiency. A reverse recovery time of ≅30 ns, and a forward voltage drop of ≅0.75 V are preferred. The reverse leakage specification is important as that can significantly affect efficiency. Other types of diodes may have a lower forward voltage drop, but may have longer recovery times, or greater reverse leakage. D1 should be rated for the maximum V_{IN}, and for the peak current when in current limit (I_{PK} in Figure 11) which is equal to Equation 16.

$$I_{PK} = 1.5\ A + I_{OR(max)} = 1.734\ A$$

where

- 1.5 A is the maximum guaranteed current limit threshold
- the maximum ripple current was previously calculated as 234 mA$_{P-P}$ (16)

This calculation is only valid when R_{CL} is not required.

8.2.2.1.7 C1

Assuming the voltage supply feeding VIN has a source impedance greater than zero, this capacitor limits the ripple voltage at VIN while supplying most of the switch current during the ON-time. At maximum load current, when the buck switch turns on, the current into VIN increases to the lower peak of the output current waveform, ramps up to the peak value, then drops to zero at turnoff. The average current into VIN during this ON-time is the load current. For a worst case calculation, C1 must supply this average load current during the maximum ON-time. The maximum ON-time is calculated using Equation 5, with a 25% tolerance added in Equation 17.

$$t_{ON(max)} = \frac{1.18 \times 10^{-10} \times (137k + 1.4k) \times 1.25}{15V - 1.4V} + 67\ ns = 1.57\ \mu s$$

(17)

C1 is calculated with Equation 18.

$$C1 = \frac{I_O \times t_{ON}}{\Delta V} = \frac{1.0A \times 1.57\ \mu s}{1V} = 1.57\ \mu F$$

where

- I_O is the load current
- ΔV is the allowable ripple voltage at VIN (1 V for this example) (18)

TI recommends quality ceramic capacitors with a low ESR for C1. To allow for capacitor tolerances and voltage effects, use a 2.2-µF capacitor.

8.2.2.1.8 C3

The capacitor at the VCC pin provides not only noise filtering and stability, but also prevents false triggering of the V_{CC} UVLO at the buck switch ON and OFF transitions. For this reason, C3 should be no smaller than 0.1 µF, and should be a good quality, low ESR, ceramic capacitor. This capacitor also determines the initial start-up delay (t1 in Figure 7).

8.2.2.1.9 C4

TI recommends a value of 0.022 µF for C4. TI recommends a high-quality ceramic capacitor with low ESR, because C4 supplies the surge current to charge the buck switch gate at turnon. A low ESR also ensures a complete recharge during each OFF-time.

8.2.2.1.10 C5

This capacitor suppresses transients and ringing due to long lead inductance at VIN. TI recommends a low ESR, 0.1-µF ceramic chip capacitor, placed physically close to the LM5010.

Product Folder Links: *LM5010*

8.2.2.1.11 C6

The capacitor at the SS pin determines the soft-start time (that is the time for the reference voltage at the regulation comparator and the output voltage), to reach their final value. Determine the time with Equation 19.

$$t_{SS} = \frac{C6 \times 2.5V}{11.5\ \mu A}$$

(19)

For a 5-ms soft-start time, C6 calculates to 0.022 µF.

8.2.2.2 *Increasing The Current Limit Threshold*

The current limit threshold is nominally 1.25 A, with a minimum guaranteed value of 1 A. If, at maximum load current, the lower peak of the inductor current (I_{PK-} in Figure 13) exceeds 1 A, resistor R_{CL} must be added between S_{GND} and I_{SEN} to increase the current limit threshold to be equal or exceed that lower peak current. This resistor diverts some of the recirculating current from the internal sense resistor so that a higher current level is needed to switch the internal current limit comparator. Calculate I_{PK-} with Equation 20.

$$I_{PK-} = I_{O(max)} - \frac{I_{OR(min)}}{2}$$

where

- $I_{O(max)}$ is the maximum load current
- $I_{OR(min)}$ is the minimum ripple current calculated using Equation 14

(20)

R_{CL} is calculated with Equation 21.

$$R_{CL} = \frac{1.0A \times 0.11\Omega}{I_{PK-} - 1.0A}$$

where

- 0.11 Ω is the minimum value of the internal resistance from S_{GND} to I_{SEN}

(21)

The next smaller standard value resistor should be used for R_{CL}. With the addition of R_{CL} it is necessary to check the average and peak current values to ensure they do not exceed the LM5010 limits. At maximum load current the average current through the internal sense resistor is calculated with Equation 22.

$$I_{AVE} = \frac{I_{O(max)} \times R_{CL} \times (V_{IN(max)} - V_{OUT})}{(R_{CL} + 0.11\Omega) \times V_{IN(max)}}$$

(22)

If I_{AVE} is less than 2 A, no changes are necessary. If it exceeds 2 A, R_{CL} must be reduced. The upper peak of the inductor current (I_{PK+}), at maximum load current, is calculated using Equation 23.

$$I_{PK+} = I_{O(max)} + \frac{I_{OR(max)}}{2}$$

where

- $I_{OR(max)}$ is calculated using Equation 11

(23)

If I_{PK+} exceeds 3.5 A , the inductor value must be increased to reduce the ripple amplitude. This necessitates recalculation of $I_{OR(min)}$, I_{PK-}, and R_{CL}.

When the circuit is in current limit, the upper peak current out of the SW pin is calculated with Equation 24.

$$I_{PK+(CL)} = \frac{1.5A \times (150\ m\Omega + R_{CL})}{R_{CL}} + I_{OR(MAX)}$$

(24)

The inductor L1 and diode D1 must be rated for this current.
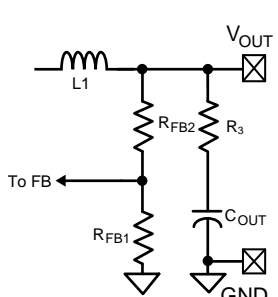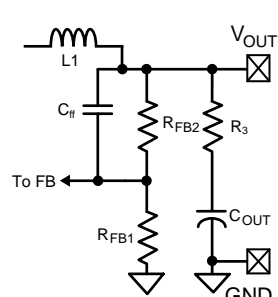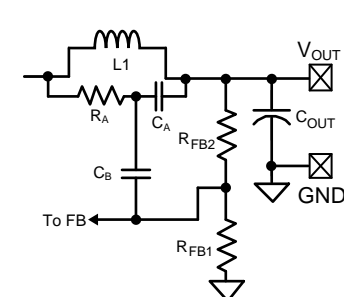
Product Folder Links: *LM5010*

8.2.2.3 Ripple Configuration

The LM5010 uses a constant-ON-time (COT) control scheme where the ON-time is terminated by a one-shot and the OFF-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the OFF-time. Furthermore, this change in feedback voltage (V_{FB}) during OFF-time must be large enough to dominate any noise present at the feedback node.

Table 3 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging or discharging the output capacitor.
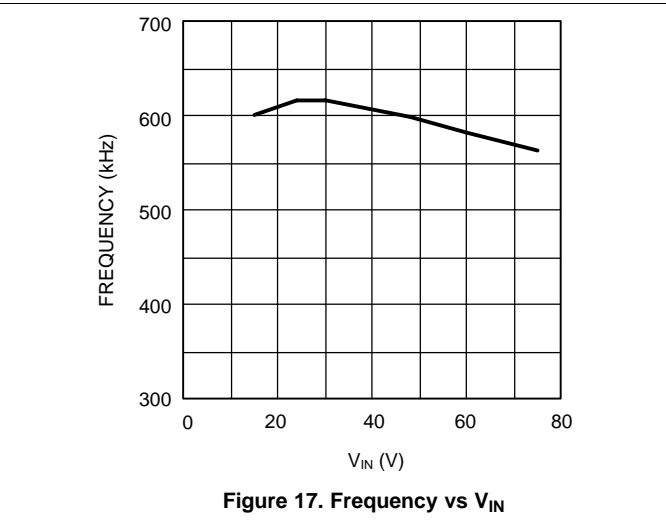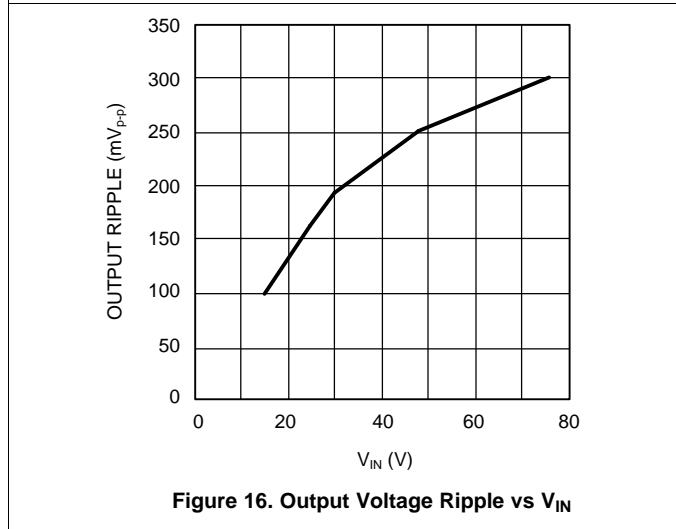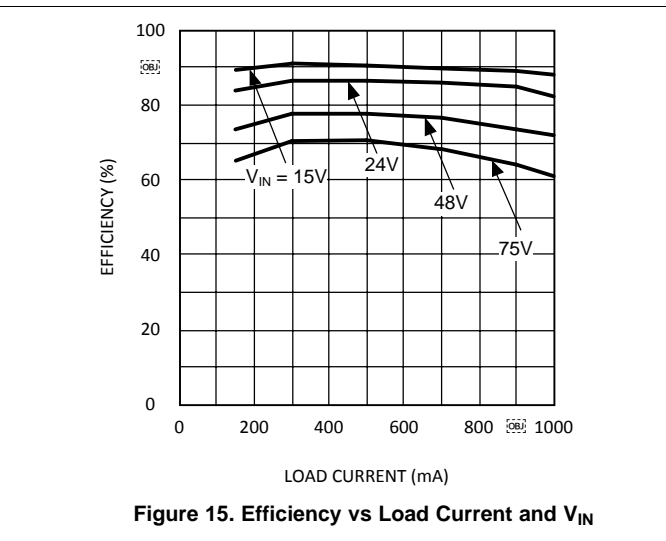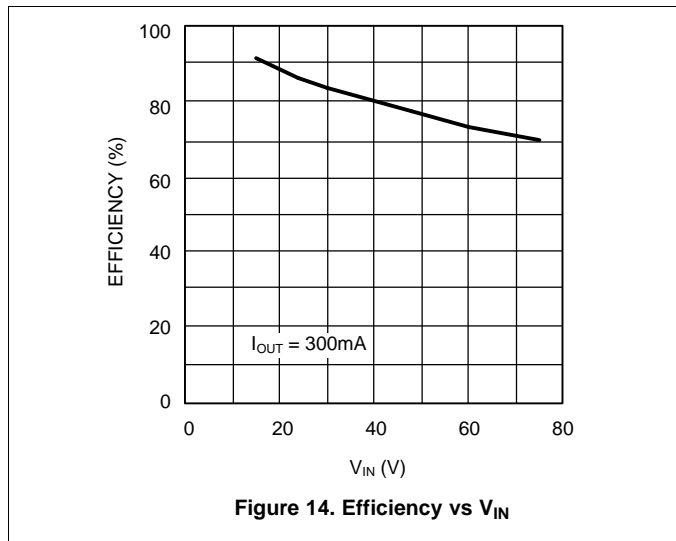2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and R3.

Table 3. Ripple Configuration

TYPE 1	TYPE 2	TYPE 3
Lowest cost	Reduced ripple	Minimum ripple
$$R_3 \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$$ (25)	$$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2}\,\|R_{FB1})}$$ $$R_3 \geq \frac{25\ mV}{\Delta I_{L1,min}}$$ (26)	$$R_A C_A \leq \frac{(V_{IN,min} - V_O) \times T_{ON(@\ V_{IN,min})}}{25mV}$$ (27)

The capacitive ripple is out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the OFF-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the OFF-time. The resistive ripple must exceed the capacitive ripple at output (V_{OUT}) for stable operation. If this condition is not satisfied, then unstable switching behavior is observed in COT converters with multiple ON-time bursts in close succession followed by a long OFF-time.

The type 3 ripple method uses a ripple injection circuit with R_A, C_A, and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then AC-coupled into the feedback node (FB) using the capacitor C_B. This circuit is suited for applications where low output voltage ripple is imperative because this circuit does not use the output voltage ripple. See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant ON-Time (COT) Regulator Designs*, (SNVA166) for more details on each ripple generation method.

8.2.3 Application Curves

Figure 14. Efficiency vs V$_{IN}$

Figure 15. Efficiency vs Load Current and V$_{IN}$

Figure 16. Output Voltage Ripple vs V$_{IN}$

Figure 17. Frequency vs V$_{IN}$

8.3 Do's and Don'ts

A minimum load current of 1 mA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor can discharge during the long OFF-time and the circuit either shuts down or cycles ON and OFF at a low frequency. If the load current is expected to drop below 1 mA in the application, choose the feedback resistors to be low enough in value to provide the minimum required current at nominal V$_{OUT}$.

Product Folder Links: *LM5010*

9 Power Supply Recommendations

The LM5010 is designed to operate with an input power supply capable of supplying a voltage range from 8 V to 75 V. The input power supply must be well-regulated and capable of supplying sufficient current to the regulator during peak load operation. Also, like in all applications, the power-supply source impedance must be small compared to the module input impedance to maintain the stability of the converter.

10 Layout

10.1 Layout Guidelines

The LM5010 regulation, overvoltage, and current limit comparators are very fast, and respond to short duration noise pulses. Therefore, layout considerations are critical for optimum performance. The layout must be as neat and compact as possible, and all the components must be as close as possible to their associated pins. The current loop formed by D1, L1 (L_{IND}), C2 (C_{OUT}), and the S_{GND} and I_{SEN} pins should be as small as possible. The ground connection from C2 (C_{OUT}) to C1 (C_{IN}) should be as short and direct as possible. If it is expected that the internal dissipation of the LM5010 will produce high junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the IC package bottom can be soldered to a ground plane, and that plane should both extend from beneath the IC, and be connected to exposed ground plane on the board's other side using as many vias as possible. The exposed pad is internally connected to the IC substrate.

The use of wide PC board traces at the pins, where possible, can help conduct heat away from the IC. The four no connect pins on the HTSSOP package are not electrically connected to any part of the IC, and may be connected to ground plane to help dissipate heat from the package. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.
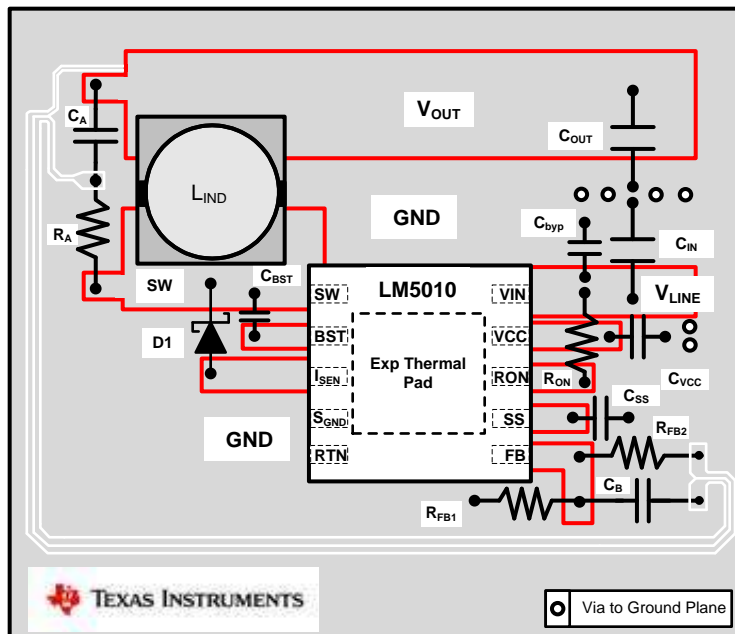
10.2 Layout Example

Figure 18. LM5010 Buck Layout Example With the WSON Package

Product Folder Links: *LM5010*

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Submit Documentation Feedback   23

Product Folder Links: *LM5010*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5010MH	LIFEBUY	HTSSOP	PWP	14	94	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L5010 MH	
LM5010MH/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5010 MH	Samples
LM5010MHX/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5010 MH	Samples
LM5010SD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L00057B	Samples
LM5010SDX/NOPB	ACTIVE	WSON	DPR	10	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L00057B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5010MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5010SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5010SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5010MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM5010SD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5010SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

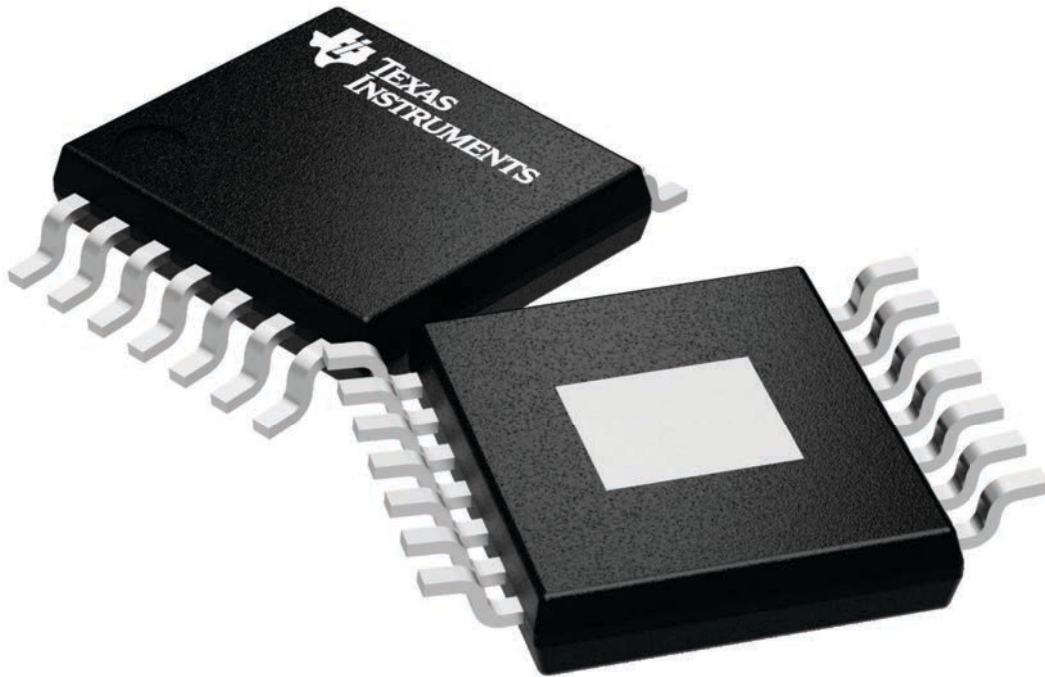| Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM5010MH	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010MH	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010MH/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06

PWP 14

PowerPAD TSSOP - 1.2 mm max height

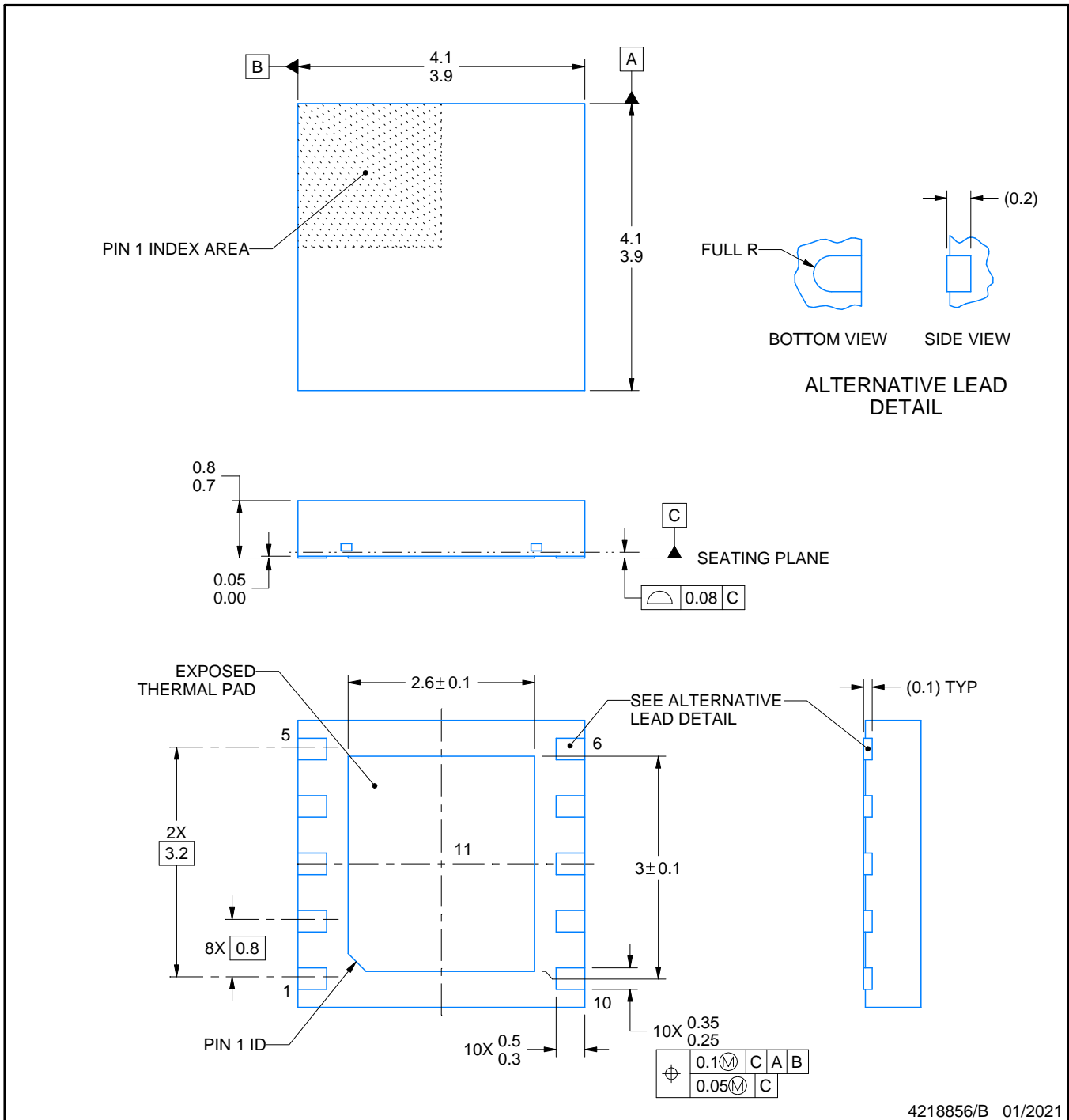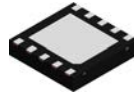**4.4 x 5.0, 0.65 mm pitch**

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224995/A

4.1
3.9

4.1
3.9

PIN 1 INDEX AREA

FULL R

(0.2)

BOTTOM VIEW   SIDE VIEW

ALTERNATIVE LEAD
DETAIL

0.8
0.7

0.05
0.00

C

SEATING PLANE

0.08 C

EXPOSED
THERMAL PAD

2.6±0.1

SEE ALTERNATIVE
LEAD DETAIL

(0.1) TYP

5

6

2X
3.2

11

3±0.1

8X 0.8

1

10

PIN 1 ID

10X 0.5
0.3

10X 0.35
0.25

0.1 (M) C A B

0.05 (M) C
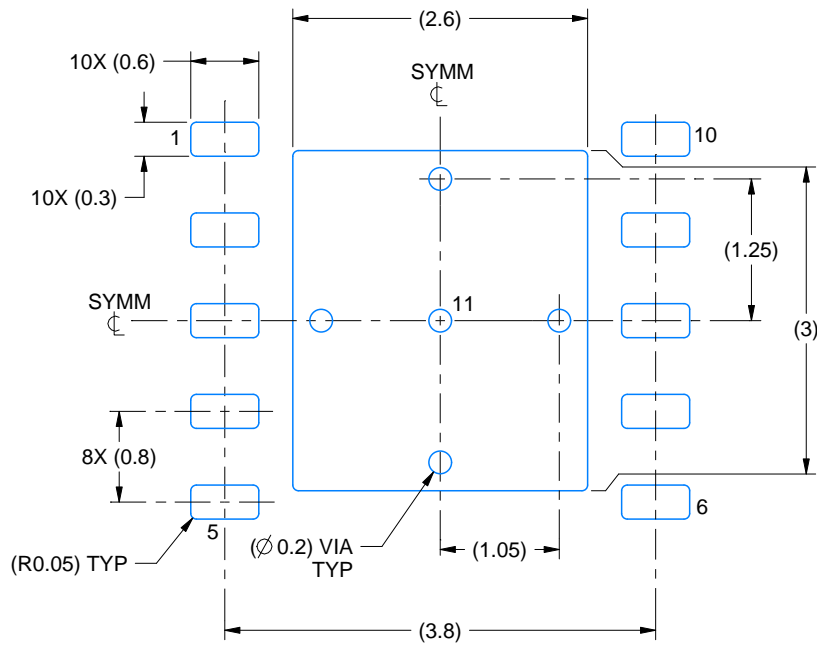
4218856/B   01/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
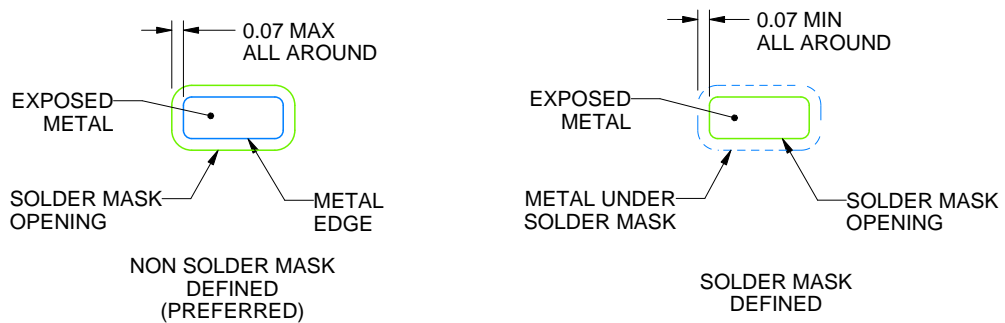
TEXAS
INSTRUMENTS

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

10X (0.6)

10X (0.3)

SYMM

8X (0.8)

5

(R0.05) TYP

(⌀ 0.2) VIA
TYP

(2.6)

SYMM

1

11

10

6

(1.25)

(3)

(1.05)

(3.8)

SOLDER MASK DETAILS

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL
EDGE

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

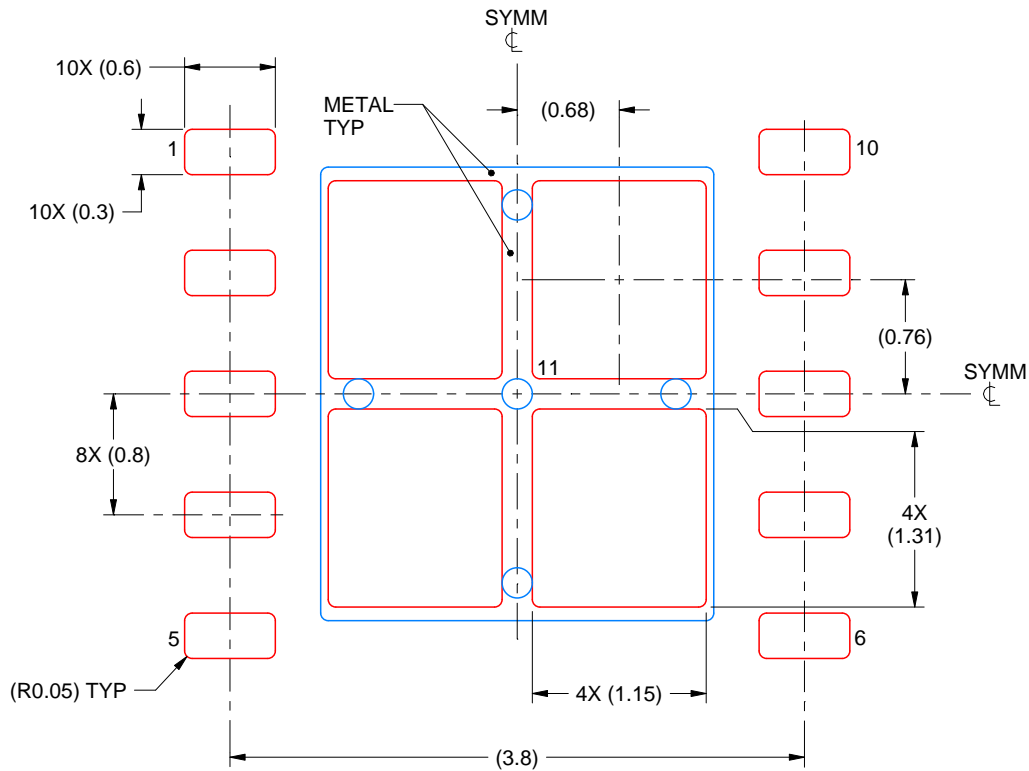4218856/B   01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).

TEXAS
INSTRUMENTS

SYMM

10X (0.6)

METAL
TYP

(0.68)

1

10

10X (0.3)

(0.76)

SYMM

11

8X (0.8)

4X
(1.31)

5

6

(R0.05) TYP

4X (1.15)

(3.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B   01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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