DS90UB983-Q1 4K DisplayPort/eDP to FPD-Link IV Bridge Serializer

1 Features

- DisplayPort receiver
  - DP/eDP v1.4 compatible
  - Supports data lane swap and polarity inversion
  - HBR3/HBR2/HBR/RBR link bit rates
  - Main link: 1, 2, or 4 lanes
  - Each lane up to 8.1 Gbps
  - AUX CH 1 Mbps
  - Hot plug detect (HPD)
  - Multi-display (MST) and SST support
  - Supports Symmetric and Asymmetric MST
  - Daisy chaining and splitting
  - SuperFrame unpacking capability
  - Suitable for 4K at 60 Hz video resolution
- FPD-Link IV interface
  - Supports 13.5/12.528/10.8/6.75/3.375 Gbps per channel; Up to 27 Gbps over dual channels
  - Coax/STP interconnect support
  - Port splitting to enable Y-cable interfaces
  - MST and SuperFrame based data splitting to different FPD channels
- Ultra-low latency control channel
  - Three fast-mode plus I^2C up to 1 MHz (up to 3.4 MHz for local bus access)
  - High speed GPIOs
- Backwards compatibility
  - IVI 94x and 92x product families
- Security and diagnostics
  - Link diagnostics
  - Voltage and temperature monitoring
  - Line fault detection
  - BIST and pattern generation
  - CRC and error diagnostics
  - ECC error correction for control bits
  - Replica mode for redundancy
- Advanced link robustness and EMC control
  - Spread spectrum clocking (SSC) input support
  - Spread spectrum clocking generation (SSCG)
  - Data scrambling
- Low power operation
  - 1.8V and 1.15V dual power supply
- AEC-Q100 qualified for automotive applications
  - AEC-Q grade-level 2, -40°C to 105°C
  - 64-pin QFN wettable flanks 9 mm x 9 mm
  - ISO 10605 and IEC 61000-4-2 ESD compliant

2 Applications

- Automotive displays:
  - Central Information Displays (CID)
  - Rear Seat Entertainment (RSE)
  - Digital instrument clusters
  - Head units and HMI modules
  - Head Up Display (HUD)
  - Rear view and side mirror displays

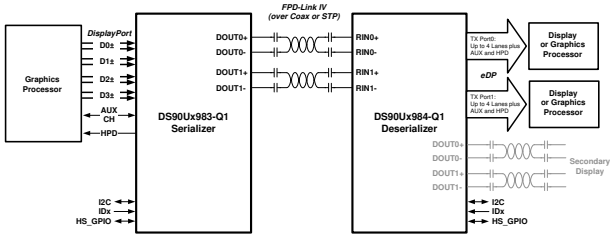
3 Description

The DS90UB983-Q1 is a DisplayPort/eDP to FPD-Link III/IV bridge device. In conjunction with an FPD-Link IV deserializer, the chipset provides a high-speed serialized interface over low-cost 50Ω coax or STP cables. The DS90UB983-Q1 is a VESA DP Standard v1.4 compatible device that supports advanced features such as MST, HBR3, and SuperFrame formats. The device is capable of supporting video resolution up to 4K resolutions with 30-bit color. 8b10b encoded DP data is serialized onto an FPD-Link IV interface output. The FPD-Link IV interface supports video and audio data transmission and full duplex control, including I^2C, and GPIO data over a single channel or dual channels. Consolidation of video data and control over FPD-Link IV lanes reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, SSCG, and randomization. In backward compatible mode, the device supports up to 720p and 1080p resolutions with 24-bit color depth over a single/dual link.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DS90UB983-Q1	VQFN (64)	9.0 mm × 9.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Application Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (May 2022)	Page
• Changed power supply voltage label 1.1V to 1.15V in DC power consumption table	9
• AC electrical table was updated to include higher FPD-Link III mode speed capability when paired with 98x deserializer	9
• Clarified SSCG specification	9
• Clarified video input reset, and removed DPRX setting. The recommendation to set 0xA0C and 0xB0C during DP initialization was removed	44
• Clarified that payload ID configuration needs to be done after DP is locked; added DTG enable for each MST stream; fixed a typo in the sequence of writing to the MST_PAYLOAD_ID	44
• Updated FPD-Link IV PLL settings table, BC_DOWNSAMPLING_RATE = 0x0 for 3.375Gbps and 6.75Gbps table, added 12.528 Gbps section	48
• SSCG section updated with constraints for backward compatible operation	50
• SSCG section updated to fix center spread diagram and revised equations	50
• Updated incorrect video processor block diagram	55
• Added video stream buffers topic	56
• Added a recommendation for minimum total horizontal blanking	57
• Dual MST with daisy-chain topic was moved from MST section to VP section	61
• Added dual serializers and dual deserializer topic	66
• Added section for FPD-Link polarity swap	67
• Added reference to App Note for internal ADC	69
• Changed V_SF to CF for Pin_Voltage equation	70
• Updated lower and upper thresholds for supply voltages table	70
• Clarified REM_INTB functionality does not support multiple ports in independent FPD-Link mode	72
• Added new section description for ABUFF	76
• Added new section description for audio functionality	78
• Removed FPD-Link III I2S Audio section, and referenced to Parallel I2S	79
• Added support for higher FPD-Link III PCLK between 98x devices	93
• New section to include back channel optimizations for FPD Mode changes	96
• Removed FPD-Link III I2S Audio section, and referenced to new audio section	100

- Removed comment (Port 0 Only) in IDx table; The IDX sets the VDDI2C for all I2C ports.....105
- Added I2C considerations when hot plugging..... 108
- Unique ID section updated to reflect 12 byte registers instead of 10.....116
- Main page register 0x1, 0x2, 0xC, 0x3F, 0x5A,0x6A, 0x6E which were modified; removed register 0x45, 0x6C 116
- Added APB default values registers after POR..... 381
- Updated the APB register map; changed 0x18, 0x20, 0x30, 0x58, 0x70, 0x74, 0x94, 0x98, 0x188, 0x208, 0x430, 0x480, 0x538; APB registers removed: 0x4, 0x34, 0x38, 0x3C, 0x40, 0x9C, 0xA0, 0xA8, 0xB0, 0xB4, 0xB8, 0xBC, 0xC4, 0xCC, 0xD0, 0xD4, 0xD8, 0xDC, 0xE0, 0xE4, 0xE8, 0xEC, 0xF8, 0x100, 0x104, 0x114, 0x118, 0x120, 0x200, 0x224, 0x408, 0x438, 0x444, 0x458, 0x45C, 0x460, 0x464, 0x468, 0x46C, 0x470, 0x474, 0x478, 0x488, 0x710, 0x714, 0x718, 0x71C, 0x720, 0x800, 0x804, 0x808, 0x80C, 0x810, 0x814, 0x818, 0x81C, 0x900, 0x930; virtual sink 0 registers removed: 0xA04, 0xA08, 0xA18, 0xA1C, 0xA20, 0xA24, 0xA28, 0xA2C, 0xA30, 0xA34, 0xA38, 0xA3C, 0xA88, 0xAA8, 0xAE0; virtual sink 1 registers were removed: 0xB04, 0xB08, 0xB18, 0xB1C, 0xB20, 0xB24, 0xB28, 0xB2C, 0xB30, 0xB34, 0xB38, 0xB3C, 0xB88, 0xBA8, 0xBE0..... 381
- Changed oscillator RMS jitter from 1ps to 1.5ps, removed SSC percentage and frequency in oscillator table... 419
- Added recommended oscillators table, removed load capacitance for oscillator table..... 419
- Added figure for coax line fault circuit, removed ADC Threshold tables.....422
- Added GPIO pin on power up sequencing diagram..... 423
- Added coax layout recommendation..... 439

5 Pin Configuration and Functions

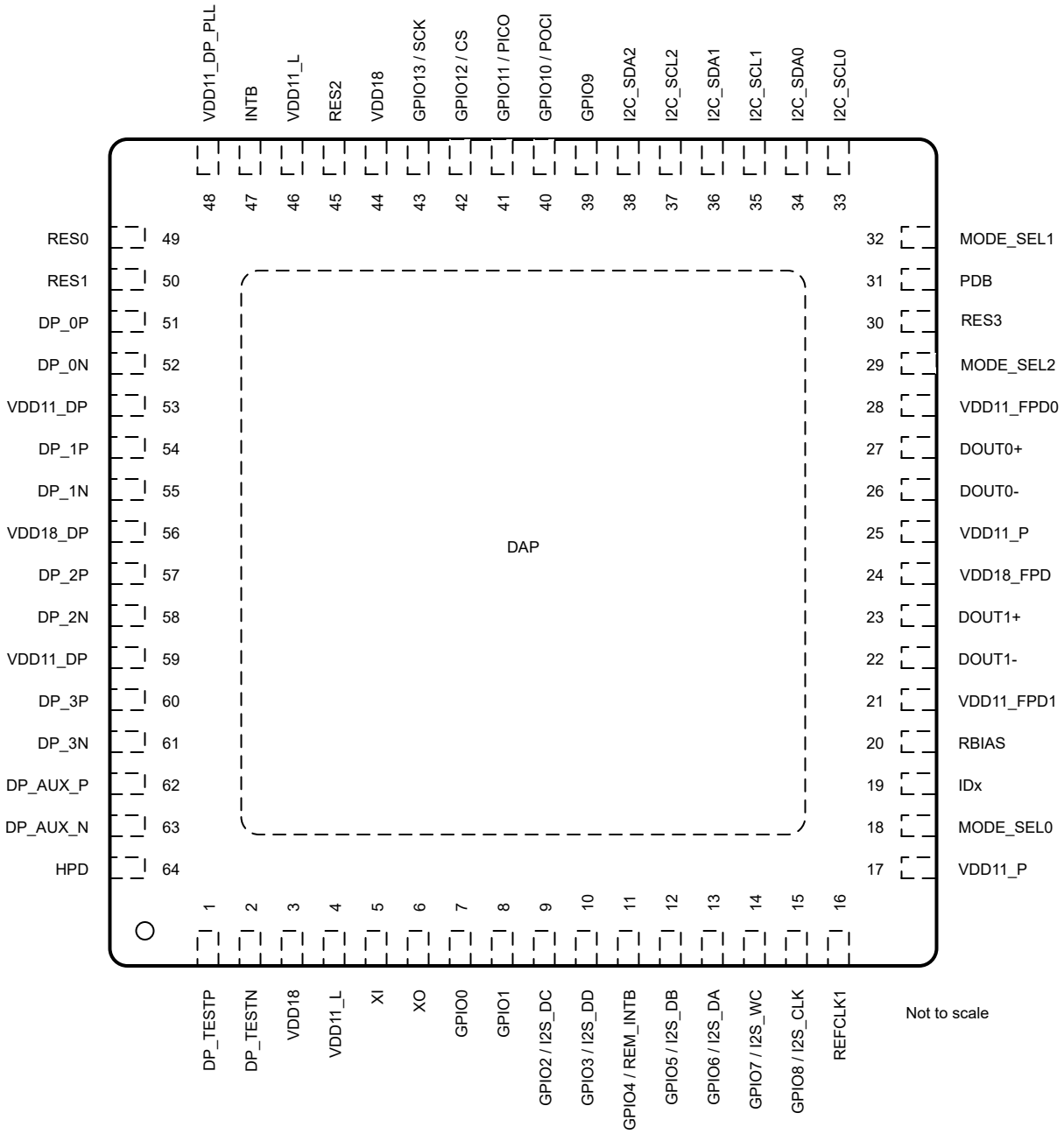


Figure 5-1. Package
64-Pin QFN
Top View

Table 5-1. Pin Functions

NAME	PIN NUMBER	I/O, TYPE	DESCRIPTION
DISPLAYPORT INPUT			
DP_0P	51	I, DP	DisplayPort/eDP Main Link Lane Input. Differential signal from DisplayPort/eDP source. Place 0.1µF AC coupling capacitors on the DisplayPort receiver side close to the device for each lane. If a lane is unused, leave floating. For eDP configuration, only one set of AC coupling capacitors is required between source and sink. Sink side AC coupling capacitors are optional.
DP_0N	52		
DP_1P	54		
DP_1N	55		
DP_2P	57		
DP_2N	58		
DP_3P	60		
DP_3N	61		
OTHER DISPLAYPORT			
HPD	64	O	Hot Plug Detect output signal to DisplayPort source. The reference voltage is 3.3V. Tie 100kΩ resistor to GND. For DP source's supporting only 1.8V HPD, a strap mode in MODE_SEL1 is available. When perform strap mode override, a soft reset requires to obtain the new value. The HPD connection is optional for eDP connections. If HPD is supported by the eDP or DP source, it is recommended to connect HPD. If pin is unused, leave floating.
DP_AUX_P	62	IO	AUX Channel Differential Input/Output for DisplayPort source. Refer to DP/eDP Implementation for details connection.
DP_AUX_N	63		
FPD-LINK IV INTERFACE			
DOUT0+	27	IO	FPD-Link IV Input/Output Channel 0 and 1: It can interface with a compatible FPD-Link III / FPD-Link IV deserializer RX through a STP or coaxial cable in Typical Application Connection - STP and Typical Application Connection - Coax.The pin must be AC-coupled with a 0.1µF capacitor, and must be placed as close as possible to the device. It is recommended these PCB traces maintain 100 Ω differential impedance. For single-ended configurations, connect DOUT0- and DOUT1- to 50Ω resistor terminator after the AC coupling capacitor. The 50Ω termination resistor placement must be as close as possible to the output connector. AC coupling capacitors for DOUT0+ and DOUT1+ must be 0.1µF, and DOUT0- and DOUT1- must be 47nF. If pin is unused, leave floating.
DOUT0-	26		
DOUT1+	23		
DOUT1-	22		
I²C BUS			
I2C_SDA0	34	IO, Open-Drain	I²C bus data signal. If I²C pull-up is connected to 3.3V, only the upper four addresses can be used. If I²C pull-up is connected to 1.8V, only the lower four addresses can be used. If these pins are unused, a pull-up resistor is required since the pin is open drain. Refer to "*I2C Bus Pullup Resistor Calculation*, SLVA689" to determine the pull-up resistor value.
I2C_SDA1	36		
I2C_SDA2	38		
I2C_SCL0	33	IO, Open-Drain	I²C bus clock signal. If I²C pull-up is connected to 3.3V, only the upper four addresses can be used. If I²C pull-up is connected to 1.8V, only the lower four addresses can be used. If these pins are unused, a pull-up resistor is required since the pin is open drain. Refer to "*I2C Bus Pullup Resistor Calculation*, SLVA689" to determine the pull-up resistor value.
I2C_SCL1	35		
I2C_SCL2	37		
IDx	19	S	I²C target address selection. Connect to external pull-up and pull-down resistors to create a voltage divider. Connect a pull-up resistor node to after filter VDD18_FPD (pin 24). **DO NOT LEAVE INPUT FLOATING** . See I2C Device Addresses.
CONTROL			
MODE_SEL0	18	S	Mode Select: Connect to external pull-up and pull-down resistors to create a voltage divider. Connect a pull-up resistor node to after filter VDD18_FPD (pin 24) under all conditions. **DO NOT LEAVE INPUT FLOATING** . See Strap Mode Selection. For MODE_SEL2: MODE_SEL2 = 0, FPD4 mode MODE_SEL2 = 1, FPD3 mode.
MODE_SEL1	32		
MODE_SEL2	29		
PDB	31	I, LVCMOS	Power-Down Mode Input Pin. Add RC on PDB to ensure that the delay for the PDB pin comes up once all supplies have settled properly. If PDB is High, the device is enabled (normal operation). If PDB is Low, the device is powered down, and resets the entire device including registers. See section Power Down. The PDB pin has power sequence timing requirements described in Power Sequence.

Table 5-1. Pin Functions (continued)

NAME	PIN NUMBER	I/O, TYPE	DESCRIPTION
INTB	47	O, Open-Drain	Interrupt INTB = H, Normal Operation INTB = L, Interrupt Request Recommended pull-up: 4.7kΩ to VDD18. **DO NOT LEAVE INPUT FLOATING** .
BIDIRECTIONAL CONTROL CHANNEL (BCC) GPIO PINS			
GPIO0	7	IO, LVCMOS	General Purpose Input/Output 0 (GPIO0). The pin has an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO1	8	IO, LVCMOS	General Purpose Input/Output 1 (GPIO1). The pin has an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO2 / I2S_DC	9	IO, LVCMOS	General Purpose Input/Output 2 (GPIO2) or Peripheral Mode I2S Data Input. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO3 / I2S_DD	10	IO, LVCMOS	General Purpose Input/Output 3 (GPIO3) or Peripheral Mode I2S Data Input. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO4 / REM_INTB	11	Input (default), IO, LVCMOS	General Purpose Input/Output 4 (GPIO4) or Remote Interrupt Pin. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. GPIO4 defaults to an input state. At device startup this pin must be left floating or pulled to GND. The remote interrupt function must be enabled manually after startup. When used as remote interrupt, REM_INTB will directly mirror the status of the INTB_IN signal from the remote device. No separate serializer register read will be required to reset and change the status of this pin. If pin is unused, leave floating. See General-purpose I/O.
GPIO5 / I2S_DB	12	IO, LVCMOS	General Purpose Input/Output 5 (GPIO5) or I2S Data Input. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO6 / I2S_DA	13	IO, LVCMOS	General Purpose Input/Output 6 (GPIO6) or I2S Data Input. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When used as an input, this pin can be used for monitoring of external voltage source. If pin is unused, leave floating. See General-purpose I/O.
GPIO7 / I2S_WC	14	IO, LVCMOS	General Purpose Input/Output 7 (GPIO7) or I2S Word Clock Input. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO8 / I2S_CLK	15	IO, LVCMOS	General Purpose Input/Output 8 (GPIO8) or I2S Clock Input. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When used as an input, this pin can be used for monitoring of external voltage source. If pin is unused, leave floating. See General-purpose I/O.
GPIO9	39	IO, LVCMOS	General Purpose Input/Output 9 (GPIO9). The pin has an internal 25 kΩ pull down resistor. If pin is unused, leave floating. See General-purpose I/O.
GPIO10 / POCI	40	IO, LVCMOS	General Purpose Input/Output 10 (GPIO10) or SPI Peripheral OUT Controller IN (POCI). Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When configured as an input, this pin can be used for sensing the input voltage of Line-Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. If pin is unused, leave floating. See General-purpose I/O.
GPIO11 / PICO	41	IO, LVCMOS	General Purpose Input/Output 11 (GPIO11) or SPI Peripheral IN Controller OUT (PICO). Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When configured as an input, this pin can be used for sensing the input voltage of Line-Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. If pin is unused, leave floating. See General-purpose I/O.
GPIO12 / CS	42	IO, LVCMOS	General Purpose Input/Output 12 (GPIO12) or SPI Chip Select. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When configured as an input, this pin can be used for sensing the input voltage of Line Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. If pin is unused, leave floating. See General-purpose I/O.

Table 5-1. Pin Functions (continued)

NAME	PIN NUMBER	I/O, TYPE	DESCRIPTION
GPIO13 / SCK	43	IO, LVCMOS	General Purpose Input/Output 13 (GPIO13) or SPI Clock. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When configured as an input, this pin can be used for sensing the input voltage of Line Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. If pin is unused, leave floating. See General-purpose I/O.
POWER and GROUND			
VDD18_DP	56	Power	1.8 V (±5%) supply Requires 10-µF, 1-µF and 0.1-µF capacitors to GND. See Typical Application Connection - STP and Typcial Application Connection - Coax.
VDD18_FPD	24		
VDD18	44		
VDD18	3		
VDD11_L	46	Power	1.15V (±5%) supply Requires 1-µF and 0.1-µF capacitors to GND. See Typical Application Connection - STP and Typcial Application Connection - Coax.
VDD11_L	4		
VDD11_P	17		
VDD11_P	25		
VDD11_FPD0	28		
VDD11_FPD1	21		
VDD11_DP	59		
VDD11_DP	53		
VDD11_DP_PLL	48		
GND	DAP	GND	DAP is the large metal contact at the bottom side, located at the center of the QFN package. Connect the exposed pad to the ground plane (GND) with recommended vias per package drawing in Mechanical, Packaging, and Orderable Information.
OTHER			
XI	5	I	Crystal Input / External Oscillator Reference input. See Oscillator Reference Clock Requirements and Crystal Reference Clock Requirements. A 27 MHz reference clock must be connected, either a parallel resonance crystal between this pin and XO or a 27 MHz 1.8V LVCMOS-level oscillator (+/- 50 ppm) to the XI pin only. Refer to Oscillator Reference Clock Requirements for details information. Ensure matching capacitance (CL_1 and CL_2) calculation is as close as possible to the load capacitance of the crystal. The crystal must be placed as close as possible to the serializer device.
XO	6	O	Crystal Output. Output pin for providing crystal reference. A resistor must be added in series with XO pin for current limiting to maintain the power level to 100µW RMS maximum. The selection of series resistor value is based on crystal specification. Refer to Table 8-5 for details about resistor value selection. Leave this pin NC when reference clock input is driving XI with oscillator. See Crystal Reference Clock Requirements.
REFCLK1	16	I	Reference Clock Input For Backward Compatibility. This clock is an optional reference clock that can be when connecting to FPD-Link III devices requiring a specific PCLK frequency; however XI pin can still be used for backwards compatibility. It supports SSC input in . Note that XI pin is always required, even if REFLCK1 is used as the PLL source. The clock frequency XI Oscillator Reference Clock Requirements is 16.5-33MHz (+/-100 ppm). Total capacitance must be <20pF. This is optional. If unused leave as No Connect.
RBIAS	20	I	Resistor Bias Connect a 10 kΩ (±1% tol) resistor to GND. This resistor is used for internal reference current calibration and must be a high accuracy resistor ±1% to ensure proper operation.
DP_TESTP	1	O	DisplayPort test mode port High speed 100Ω differential output drivers. Place 0.1µF AC coupling caps in series both pins. DP_TESTx pins are used to monitor the eye of the recovered clock, as required by the DisplayPort specification. These pins are available for debugging purposes only. Test point must be placed at the termination resistor. If not used, terminate with external 100Ω.
DP_TESTN	2		

Table 5-1. Pin Functions (continued)

NAME	PIN NUMBER	I/O, TYPE	DESCRIPTION
RES0	49	-	These pin names are reserved pins. These pins must be left floating (No Connect).
RES1	50		
RES2	45		
RES3	30		

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD18 (VDD18_DP, VDD18_FPD, VDD18, VDD18)	–0.3	2.16	V
Supply voltage	VDD11 (VDD11_L, VDD11_L, VDD11_P, VDD11_P, VDD11_FPD0, VDD11_FPD1, VDD11_DP, VDD11_DP, VDD11_DP_PLL)	–0.3	1.32	V
FPD-Link IV output voltage	DOUT0+, DOUT0-, DOUT1+, DOUT1-	–0.3	1.32	V
LVCMOS IO voltage	GPIO0, GPIO1, GPIO2 / I2S_DC, GPIO3 / I2S_DD, GPIO4 / REM_INTB, GPIO5 / I2S_DB, GPIO6 / I2S_DA, GPIO7 / I2S_WC, GPIO8 / I2S_CLK, GPIO9, GPIO10 / MISO, GPIO11 / MOSI, GPIO12 / SS, GPIO13 / SCK	–0.3	2.16	V
Reserved pin voltage	RES0, RES1, RES2, RES3	–0.3	1.32	V
Analog voltage	RBIAS	–0.3	2.16	V
HPD	HPD	–0.3	3.96	V
DP input voltage	DP0_P, DP0_N, DP1_P, DP1_N, DP2_P, DP2_N, DP3_P, DP3_N, AUX_P, AUX_N, DP_TESTP, DP_TESTN	–0.3	1.32	V
Configuration input voltage	MODE_SEL0, MODE_SEL1, MODE_SEL2, IDx	–0.3	2.16	V
Open-Drain voltage	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1, I2C_SDA2, I2C_SCL2	–0.3	3.96	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	DOUT0+, DOUT0-, DOUT1+, DOUT1-	±2	kV
			All pins except DOUT0+, DOUT0-, DOUT1+, DOUT1-	±2	
		Charged device model (CDM), per AEC Q100-011	Charged device model (CDM), per AEC Q100-011	±1	
		IEC 61000-4-2, R_D = 330 Ω, C_S = 150 pF	Contact Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)	±4	
			Air Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)	±8	
		ISO 10605 R_D = 330 Ω, C_S = 150 pF and 330 pF R_D = 2 kΩ, C_S = 150 pF and 330 pF	Contact Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)	±4	
			Air Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)	±8	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC (1)		DS90UB983-Q1 RTD (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	18.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.3	°C/W

(1) Thermal data in accordance with JESD51. For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
RECOMMENDED OPERATING CONDITIONS					
Supply voltage	VDD18 (VDD18_DP, VDD18_FPD, VDD18, VDD18, RES2)	1.71	1.8	1.89	V
Supply voltage	VDD11 (VDD11_L, VDD11_L, VDD11_P, VDD11_P, VDD11_FPD0, VDD11_FPD1, VDD11_DP, VDD11_DP, VDD11_DP_PLL)	1.09	1.15	1.21	V
I2C supply voltage	I2C_SDA2, I2C_SCL2, I2C_SDA1, I2C_SCL1, I2C_SDA0, I2C_SCL0 = $V_{(I2C)}$ = 1.8 V	1.71	1.8	1.89	V
I2C supply voltage	I2C_SDA0, I2C_SCL0 = $V_{(I2C)}$ = 3.3 V	3	3.3	3.6	V
Operating free air temperature, T_A	Operating free air temperature, T_A	–40	25	105	°C
DP data rate(2)	HBR3	8.05707	8.1	8.10243	Gbps
DP data rate(2)	HBR2	5.37138	5.4	5.40162	Gbps
DP data rate(2)	HBR	2.68569	2.7	2.70081	Gbps
DP data rate(2)	RBR	1.611414	1.62	1.620486	Gbps
Local I2C clock frequency, f_{SCL}	Local I2C frequency Standard Mode			0.1	MHz
Local I2C clock frequency, f_{SCL}	Local I2C frequency Fast Mode			0.4	MHz
Local I2C clock frequency, f_{SCL}	Local I2C frequency Fast Plus Mode			1	MHz
Local I2C clock frequency, f_{SCL}	Local I2C frequency High-Speed Mode			3.4	MHz
Supply noise(1)	VDD11			25	mV_{PP}
Supply noise(1)	VDD18			50	mV_{PP}
Supply noise(1)	$V_{(VDDI2C)}$ = 1.8V			50	mV_{PP}
Supply noise(1)	$V_{(VDDI2C)}$ = 3.3V			100	mV_{PP}

(1) DC - 50 MHz at supply pin
(2) per DP lane

6.5 DC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
POWER CONSUMPTION & SUPPLY CURRENTS							
P_T	Total power consumption, normal operation	2x FPD Tx @ 13.5Gbps DP 4 Lanes @8.1Gbps	VDD18(1), VDD11 (2)			1.951	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.2	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.164	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.3	A
I_{DD-11}	Supply current		VDD11_L			0.768	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.071	A
I_{DD-11}	Supply current		VDD11_FPD1			0.071	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 13.5Gbps DP 4 Lanes @5.4Gbps	VDD18(1), VDD11 (2)			1.878	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.24	A
I_{DD-11}	Supply current		VDD11_L			0.762	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.071	A
I_{DD-11}	Supply current		VDD11_FPD1			0.071	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 13.5Gbps DP 4 Lanes @2.7Gbps	VDD18(1), VDD11 (2)			1.830	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.2	A
I_{DD-11}	Supply current		VDD11_L			0.752	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.071	A
I_{DD-11}	Supply current		VDD11_FPD1			0.071	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	2x FPD Tx @ 13.5Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.770	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.15	A
I_{DD-11}	Supply current		VDD11_L			0.718	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.071	A
I_{DD-11}	Supply current		VDD11_FPD1			0.071	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 10.8 Gbps DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.927	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.28	A
I_{DD-11}	Supply current		VDD11_L			0.766	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.062	A
I_{DD-11}	Supply current		VDD11_FPD1			0.062	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 10.8 Gbps DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.818	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.19	A
I_{DD-11}	Supply current		VDD11_L			0.730	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.062	A
I_{DD-11}	Supply current		VDD11_FPD1			0.062	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	2x FPD Tx @ 10.8 Gbps DP 4 Lanes @2.7Gbps	VDD18[1], VDD11 [2]			1.770	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.15	A
I_{DD-11}	Supply current		VDD11_L			0.720	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.062	A
I_{DD-11}	Supply current		VDD11_FPD1			0.062	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 10.8 Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.709	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.2	A
I_{DD-18}	Supply current		VDD18			0.034	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.165	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.1	A
I_{DD-11}	Supply current		VDD11_L			0.686	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.062	A
I_{DD-11}	Supply current		VDD11_FPD1			0.062	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 6.75 Gbps DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.9321	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.255	A
I_{DD-11}	Supply current		VDD11_L			0.763	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.051	A
I_{DD-11}	Supply current		VDD11_FPD1			0.051	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	2x FPD Tx @ 6.75Gbps DP 4 Lanes @5.4Gbps	VDD18(1), VDD11 (2)			1.763	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.16	A
I_{DD-11}	Supply current		VDD11_L			0.722	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.051	A
I_{DD-11}	Supply current		VDD11_FPD1			0.051	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 6.75Gbps DP 4 Lanes @2.7Gbps	VDD18(1), VDD11 (2)			1.714	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.12	A
I_{DD-11}	Supply current		VDD11_L			0.712	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.051	A
I_{DD-11}	Supply current		VDD11_FPD1			0.051	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 6.75Gbps DP 4 Lanes @1.62Gbps	VDD18(1), VDD11 (2)			1.605	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.03	A
I_{DD-11}	Supply current		VDD11_L			0.638	A
I_{DD-11}	Supply current		VDD11_P			0.03	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.051	A
I_{DD-11}	Supply current		VDD11_FPD1			0.051	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.375Gbps DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.823	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.21	A
I_{DD-11}	Supply current		VDD11_L			0.738	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.375Gbps DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.726	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.13	A
I_{DD-11}	Supply current		VDD11_L			0.712	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.375Gbps DP 4 Lanes @2.7Gbps	VDD18[1], VDD11 [2]			1.642	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.06	A
I_{DD-11}	Supply current		VDD11_L			0.672	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.375Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.545	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			0.98	A
I_{DD-11}	Supply current		VDD11_L			0.608	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.823	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.21	A
I_{DD-11}	Supply current		VDD11_L			0.738	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.726	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.13	A
I_{DD-11}	Supply current		VDD11_L			0.712	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @2.7Gbps	VDD18(1), VDD11 (2)			1.642	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.06	A
I_{DD-11}	Supply current		VDD11_L			0.672	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A
P_T	Total power consumption, normal operation	2x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @1.62Gbps	VDD18(1), VDD11 (2)			1.545	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			0.98	A
I_{DD-11}	Supply current		VDD11_L			0.608	A
I_{DD-11}	Supply current		VDD11_P			0.028	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.042	A
I_{DD-11}	Supply current		VDD11_FPD1			0.042	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 13.5Gbps DP 4 Lanes @8.1Gbps	VDD18(1), VDD11 (2)			1.860	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.24	A
I_{DD-11}	Supply current		VDD11_L			0.768	A
I_{DD-11}	Supply current		VDD11_P			0.026	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.043	A
I_{DD-11}	Supply current		VDD11_FPD1			0.043	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 13.5Gbps DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.763	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.16	A
I_{DD-11}	Supply current		VDD11_L			0.742	A
I_{DD-11}	Supply current		VDD11_P			0.026	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.043	A
I_{DD-11}	Supply current		VDD11_FPD1			0.043	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 13.5Gbps DP 4 Lanes @2.7Gbps	VDD18[1], VDD11 [2]			1.739	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.14	A
I_{DD-11}	Supply current		VDD11_L			0.752	A
I_{DD-11}	Supply current		VDD11_P			0.026	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.043	A
I_{DD-11}	Supply current		VDD11_FPD1			0.043	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 13.5Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.666	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.08	A
I_{DD-11}	Supply current		VDD11_L			0.708	A
I_{DD-11}	Supply current		VDD11_P			0.026	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.043	A
I_{DD-11}	Supply current		VDD11_FPD1			0.043	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 10.8Gbps DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.835	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.19	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.154	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.22	A
I_{DD-11}	Supply current		VDD11_L			0.757	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.04	A
I_{DD-11}	Supply current		VDD11_FPD1			0.04	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 10.8Gbps DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.657	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.15	A
I_{DD-18}	Supply current		VDD18			0.037	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.112	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.135	A
I_{DD-11}	Supply current		VDD11_L			0.726	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.04	A
I_{DD-11}	Supply current		VDD11_FPD1			0.04	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 10.8Gbps DP 4 Lanes @2.7Gbps	VDD18[1], VDD11 [2]			1.554	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.15	A
I_{DD-18}	Supply current		VDD18			0.037	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.112	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.05	A
I_{DD-11}	Supply current		VDD11_L			0.671	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.04	A
I_{DD-11}	Supply current		VDD11_FPD1			0.04	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 10.8Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.530	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.15	A
I_{DD-18}	Supply current		VDD18			0.037	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.112	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.03	A
I_{DD-11}	Supply current		VDD11_L			0.667	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.04	A
I_{DD-11}	Supply current		VDD11_FPD1			0.04	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 6.75Gbps DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.717	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.2	A
I_{DD-11}	Supply current		VDD11_L			0.754	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.032	A
I_{DD-11}	Supply current		VDD11_FPD1			0.032	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 6.75Gbps DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.608	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.11	A
I_{DD-11}	Supply current		VDD11_L			0.718	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.032	A
I_{DD-11}	Supply current		VDD11_FPD1			0.032	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 6.75Gbps DP 4 Lanes @2.7Gbps	VDD18[1], VDD11 [2]			1.511	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.03	A
I_{DD-11}	Supply current		VDD11_L			0.668	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.032	A
I_{DD-11}	Supply current		VDD11_FPD1			0.032	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 6.75Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.475	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1	A
I_{DD-11}	Supply current		VDD11_L			0.654	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.032	A
I_{DD-11}	Supply current		VDD11_FPD1			0.032	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.375Gbps DP 4 Lanes @8.1Gbps	VDD18[1], VDD11 [2]			1.680	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.17	A
I_{DD-11}	Supply current		VDD11_L			0.732	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.028	A
I_{DD-11}	Supply current		VDD11_FPD1			0.028	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.375Gbps DP 4 Lanes @5.4Gbps	VDD18[1], VDD11 [2]			1.535	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1.05	A
I_{DD-11}	Supply current		VDD11_L			0.666	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.028	A
I_{DD-11}	Supply current		VDD11_FPD1			0.028	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.375Gbps DP 4 Lanes @2.7Gbps	VDD18[1], VDD11 [2]			1.475	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			1	A
I_{DD-11}	Supply current		VDD11_L			0.646	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.028	A
I_{DD-11}	Supply current		VDD11_FPD1			0.028	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.375Gbps DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.421	W
I_{DDT}	1.8 V Total Supply Current		VDD18[1]			0.15	A
I_{DD-18}	Supply current		VDD18			0.037	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.112	A
I_{DDT}	1.15 V Total supply current		VDD11 [2]			0.94	A
I_{DD-11}	Supply current		VDD11_L			0.602	A
I_{DD-11}	Supply current		VDD11_P			0.022	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.028	A
I_{DD-11}	Supply current		VDD11_FPD1			0.028	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @8.1Gbps	VDD18(1), VDD11 (2)			1.680	W
I_{DDT}	1.8 V Total Supply Current		VDD18 Rail (1)			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.17	A
I_{DD-11}	Supply current		VDD11_L			0.729	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.36	A
I_{DD-11}	Supply current		VDD11_FPD0			0.029	A
I_{DD-11}	Supply current		VDD11_FPD1			0.029	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @5.4Gbps	VDD18(1), VDD11 (2)			1.535	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1.05	A
I_{DD-11}	Supply current		VDD11_L			0.663	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.306	A
I_{DD-11}	Supply current		VDD11_FPD0			0.029	A
I_{DD-11}	Supply current		VDD11_FPD1			0.029	A
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @2.7Gbps	VDD18(1), VDD11 (2)			1.475	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail (1)			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail (2)			1	A
I_{DD-11}	Supply current		VDD11_L			0.643	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.276	A
I_{DD-11}	Supply current		VDD11_FPD0			0.029	A
I_{DD-11}	Supply current		VDD11_FPD1			0.029	A

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_T	Total power consumption, normal operation	1x FPD Tx @ 3.675 Gbps (FPD-Link III) DP 4 Lanes @1.62Gbps	VDD18[1], VDD11 [2]			1.402	W
I_{DDT}	1.8 V Total supply current		VDD18 Rail [1]			0.14	A
I_{DD-18}	Supply current		VDD18			0.035	A
I_{DD-18}	Supply current		VDD18_DP			0.001	A
I_{DD-18}	Supply current		VDD18_FPD			0.104	A
I_{DDT}	1.15 V Total supply current		VDD11 Rail [2]			0.94	A
I_{DD-11}	Supply current		VDD11_L			0.599	A
I_{DD-11}	Supply current		VDD11_P			0.023	A
I_{DD-11}	Supply current		VDD11_DP			0.260	A
I_{DD-11}	Supply current		VDD11_FPD0			0.029	A
I_{DD-11}	Supply current		VDD11_FPD1			0.029	A
P_Z	Total power consumption, Power Down Mode	PDB = LOW	VDD18[1], VDD11 [2]			422.64	mW
I_{DDZ}	1.8 V Total shutdown current	PDB = LOW	VDD18 Rail [1]			45	mA
I_{DD-18Z}	Powerdown current	PDB = LOW	VDD18			18	mA
I_{DD-18Z}	Powerdown current	PDB = LOW	VDD18_DP			0	mA
I_{DD-18Z}	Powerdown current	PDB = LOW	VDD18_FPD			27	mA
I_{DDZ}	1.15 V Total shutdown current	PDB = LOW	VDD11 Rail [2]			279	mA
I_{DD-11Z}	Powerdown current	PDB = LOW	VDD11_L			206.46	mA
I_{DD-11Z}	Powerdown current	PDB = LOW	VDD11_P			11.16	mA
I_{DD-11Z}	Powerdown current	PDB = LOW	VDD11_DP			36.828	mA
I_{DD-11Z}	Powerdown current	PDB = LOW	VDD11_FPD0			12.276	mA
I_{DD-11Z}	Powerdown current	PDB = LOW	VDD11_FPD1			12.276	mA
1.8 V LVCMOS I/O							
V_{OH}	High-level output voltage	I_{OH} = –4 mA, VDD18 = 1.71 V to 1.89 V	GPIO0, GPIO1, GPIO2 / I2S_DC, GPIO3 / I2S_DD, GPIO4 / REM_INTB, GPIO5 / I2S_DB, GPIO6 / I2S_DA, GPIO7 / I2S_WC, GPIO8 / I2S_CLK, GPIO9, GPIO10 / MISO, GPIO11 / MOSI, GPIO12 / SS, GPIO13 / SCK	VDD18 – 0.45		VDD18	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, VDD18 = 1.71 V to 1.89 V		GND		0.45	V
V_{IH}	High-level input voltage	VDD18 = 1.71 V to 1.89 V		0.65 × VDD18		VDD18	V
V_{IL}	Low-level input voltage	VDD18 = 1.71 V to 1.89 V		GND		0.35 × VDD18	V
I_{IH}	Input high current	V_{IN} = VDD18 = 1.71 V to 1.89 V, Internal pulldown enabled				100	µA
I_{IH}	Input high current	V_{IN} =VDD18 = 1.71 V to 1.89 V, Internal pulldown disabled				25	µA
I_{IL}	Input low current	V_{IN} = 0 V		–25			µA
I_{IN_STRAP}	Strap pin input current	V_{IN} = 0 V to VDD18	IDX, MODE_SEL0, MODE_SEL1, MODE_SEL2	–2		2	µA

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{OS}	Output short circuit current	V_{OUT} = 0 V	GPIO0, GPIO1, GPIO2 / I2S_DC, GPIO3 / I2S_DD, GPIO4 / REM_INTB, GPIO5 / I2S_DB, GPIO6 / I2S_DA, GPIO7 / I2S_WC, GPIO8 / I2S_CLK, GPIO9, GPIO10 / MISO, GPIO11 / MOSI, GPIO12 / SS, GPIO13 / SCK		–35		mA
I_{OZ}	TRI-STATE output current	V_{OUT} = 0 V or VDD18, PDB = L		–20		20	µA
OPEN DRAIN OUTPUT							
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, VDD18 = 1.71 V to 1.89 V	INTB	GND		0.45	V
I_{IN}	Leakage current	V_{IN} = VDD18		-65		65	µA
SERIAL CONTROL BUS							
V_{IL}	Input low-level	Standard/Fast/ Fast Plus Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1, I2C_SDA2, I2C_SCL2	GND		0.3 × $V_{(I2C)}$	V
V_{IH}	Input high-level	Standard/Fast/ Fast Plus Mode		0.7 × $V_{(I2C)}$		$V_{(I2C)}$	V
V_{HYS}	Input hysteresis	Standard/Fast/ Fast Plus Mode			70		mV
V_{OL1}	Output low-level	Standard-mode/ Fast-mode, I_{OL} = 3 mA, $V_{(I2C)}$ = 3.0 V to 3.6 V		0		0.4	V
V_{OL2}	Output low-level	Standard-mode/ Fast-mode I_{OL} = 3 mA, $V_{(I2C)}$ = 1.71 V to 1.89 V		0		0.2 x $V_{(I2C)}$	V
V_{OL1}	Output low-level	Fast-mode Plus, I_{OL} = 20 mA		0		0.4	V
I_{IL}	Input low current	V_{IN} = 0V		-40			µA
I_{IH}	Input high current	V_{IN} = $V_{(I2C)}$				40	µA
I_{OL}	Output low-level current	Standard/Fast Mode, V_{OL} = 0.2 x $V_{(I2C)}$, $V_{(I2C)}$ = 1.71 V to 1.89 V		3			mA
I_{OL}	Output low-level current	Standard/Fast Mode, V_{OL} = 0.4, $V_{(I2C)}$ = 3.0 V to 3.6 V		3			mA
I_{OL}	Output low-level current	Fast Plus Mode		20			mA
C_{IN}	Input capacitance				5		pF
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)		0.1 × $V_{(I2C)}$			V
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)		0.2 × $V_{(I2C)}$			V
SERIAL CONTROL BUS HIGH-SPEED MODE							

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{IL}	Input low-level	High-Speed Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1, I2C_SDA2, I2C_SCL2	GND		0.3 × $V_{(I2C)}$	V
V_{IH}	Input high-level	High-Speed Mode		0.7 × $V_{(I2C)}$		$V_{(I2C)}$ + 0.5	V
V_{HYS}	Input hysteresis	High-Speed Mode			70		mV
V_{OL}	Output low-level	High-Speed Mode, I_{OL} = 3 mA, $V_{(I2C)}$ = 1.71 V to 1.89 V		0		0.2 x $V_{(I2C)}$	V
I_{IL}	Input low current	V_{IN} = 0V		-65		65	µA
I_{IH}	Input high current	V_{IN} = $V_{(I2C)}$		-65		65	µA
C_{IN}	Input capacitance				5		pF
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)		0.2 × $V_{(I2C)}$			V
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)		0.1 × $V_{(I2C)}$			V
VOLTAGE AND TEMPERATURE SENSING							
V_{ACC}	Voltage sensor accuracy			-2.5	±1	+2.5	%

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
T_{ACC}	Temperature sensor accuracy	T_J = -40 to 150°C Junction Temperature		-5.5	±2.5	+5.5	°C
FPD-LINK DC SPECIFICATIONS							
$\|V_{OUT}\|$	Single-ended output amplitude		DOUT0+, DOUT0–, DOUT1+, DOUT1–	470	575	670	mV
$\|V_{OD}\|$	Differential output amplitude			940	1150	1340	mV
ΔV_{OD}	Output differential voltage unbalance	RL=100Ω			1	50	mV
V_{OS}	Output offset voltage	RL=100Ω,			VDD11/2		V
ΔV_{OS}	Offset voltage mismatch	RL=100Ω,			1	50	mV
$V_{CM\Delta}$	Common mode voltage noise					20	mV
V_{IN-BC}	Single-ended back channel input amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate= 168.75 Mbps. (FPD-Link IV mode)		110			mV
V_{ID-BC}	Differential back channel input amplitude	R_L = 100 Ω. Differential configuration. Back channel rate = 168.75 Mbps. (FPD-Link IV mode)		220			mV
V_{IN-BC}	Single-ended back channel input amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III mode)		130			mV
V_{ID-BC}	Differential back channel input amplitude	R_L = 100 Ω. Differential configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III mode)		260			mV
R_T	Internal termination resistor	Single-ended	DOUT0+, or DOUT0–, and DOUT1+, or DOUT1–	40	50	60	Ω
		Differential	Between DOUT0+/–, and between DOUT1+/–	80	100	120	Ω

(1) VDD18 = 1.8 V for typical, and 1.89 V for max
(2) VDD11 = 1.15 V for typical, and 1.21 V for max

6.6 AC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O						

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
FC_GPIO_{Jit}	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over one 13.5 Gbps FC (1 des)				39.12	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over two 13.5 Gbps FC (2 daisy-chained des), jitter at second des output				78.24	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over three 13.5 Gbps FC (3 daisy-chained des), jitter at third des output				117.36	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over four 13.5 Gbps FC (4 daisy-chained des), jitter at fourth des output				156.48	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over one 13.5 Gbps FC (1 des)				78.24	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over two 13.5 Gbps FC (2 daisy-chained des), jitter at second des output				156.48	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over three 13.5 Gbps FC (3 daisy-chained des), jitter at third des output				234.72	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over four 13.5 Gbps FC (4 daisy-chained des), jitter at fourth des output				312.96	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over one 13.5 Gbps FC (1 des)				117.36	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over two 13.5 Gbps FC (2 daisy-chained des), jitter at second des output				234.72	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over three 13.5 Gbps FC (3 daisy-chained des), jitter at third des output				352.08	ns
FC_GPIO_{Jit}	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over four 13.5 Gbps FC (4 daisy-chained des), jitter at fourth des output				469.44	ns
FC_GPIO_{Lat}	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over one 13.5 Gbps FC (1 des)				0.222	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over two 13.5 Gbps FC (2 daisy-chained des), latency before second des output				0.444	us

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
FC_GPIO_{Lat}	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over three 13.5 Gbps FC (3 daisy-chained des), latency before third des output				1.333	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over four 13.5 Gbps FC (4 daisy-chained des), latency before fourth des output				5.333	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over one 13.5 Gbps FC (1 des)				0.444	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over two 13.5 Gbps FC (2 daisy-chained des), latency before second des output				0.889	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over three 13.5 Gbps FC (3 daisy-chained des), latency before third des output				2.667	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over four 13.5 Gbps FC (4 daisy-chained des), latency before fourth des output				10.667	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over one 13.5 Gbps FC (1 des)				1.778	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over two 13.5 Gbps FC (2 daisy-chained des), latency before second des output				3.556	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over three 13.5 Gbps FC (3 daisy-chained des), latency before third des output				10.667	us
FC_GPIO_{Lat}	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over four 13.5 Gbps FC (4 daisy-chained des), latency before fourth des output				42.667	us
BC_GPIO_{Jit}	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output				177.778	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output				213.333	ns

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
BC_GPIO_{Jit}	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output				248.889	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output				284.444	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output				711.238	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output				853.485	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output				995.733	us
BC_GPIO_{Jit}	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output				1137.980	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output				1422.222	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output				1706.667	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output				1991.111	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output				2275.556	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output				2844.440	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output				3413.328	ns

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
BC_GPIO_{Jit}	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output				3982.217	ns
BC_GPIO_{Jit}	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output				4551.105	ns
BC_GPIO_{Lat}	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				1	us
BC_GPIO_{Lat}	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				2	us
BC_GPIO_{Lat}	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				3	us
BC_GPIO_{Lat}	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				4	us
BC_GPIO_{Lat}	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				1	us
BC_GPIO_{Lat}	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				2	us
BC_GPIO_{Lat}	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				3	us
BC_GPIO_{Lat}	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				4	us
BC_GPIO_{Lat}	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				2	us
BC_GPIO_{Lat}	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				4	us

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
BC_GPIO_{Lat}	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				6	us
BC_GPIO_{Lat}	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				8	us
BC_GPIO_{Lat}	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				3	us
BC_GPIO_{Lat}	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				6	us
BC_GPIO_{Lat}	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				9	us
BC_GPIO_{Lat}	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				12	us
t_{CLH}	LVCMOS low-to-high transition-time	VDD18, C_L = 8pF, Default Registers			2		ns
t_{CHL}	LVCMOS high-to-low transition-time				2		ns
t_{PDB}	PDB reset pulse width	Voltage supplies applied and stable	PDB	500			us
t_{PDB_D}	Delay between PDB pulses	Minimum time between reset pulses		2			ms
t_{PDB_Glitch}	PDB glitch filtering	Glitches less than the specificied maximum will be ignored (device will not go into reset)		500			ns
FPD-Link IV AC SPECIFICATIONS							
f_{FC}	Forward channel data rate	FPD-Link IV	DOUT0+, DOUT0–, DOUT1+, DOUT1–		13.5		Gbps
					12.528		Gbps
					10.8		Gbps
f_{FC}	Forward channel data rate	FPD-Link IV	DOUT0+, DOUT0–, DOUT1+, DOUT1–		6.75		Gbps
					3.375		Gbps
f_{FC}	Forward channel data rate	FPD-Link III(3)	DOUT0+, DOUT0–, DOUT1+, DOUT1–		5.67		Gbps

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
f_{BC}	Back channel data rate(1)	FPD-Link IV FC rate = 13.5 Gbps, 10.8 Gbps, 6.75 Gbps or 3.375 Gbps	DOUT0+, DOUT0–, DOUT1+, DOUT1–		168.75		Mbps
f_{BC}	Back channel data rate(1)	FPD-Link IV FC rate = 12.528 Gbps	DOUT0+, DOUT0–, DOUT1+, DOUT1–		156.6		Mbps
f_{BC}	Back channel data rate(1)	FPD-Link III	DOUT0+, DOUT0–, DOUT1+, DOUT1–		20		Mbps
f_{BC}	Back channel data rate(1)		DOUT0+, DOUT0–, DOUT1+, DOUT1–		10		Mbps
f_{BC}	Back channel data rate(1)		DOUT0+, DOUT0–, DOUT1+, DOUT1–		5		Mbps
t_{JIT}	Output Total Jitter - 13.5 Gbps (FPD-Link IV)	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (2)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.35	UI_{FC}
t_{JIT}	Output Total Jitter - 12.528 Gbps (FPD-Link IV)		DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.35	UI_{FC}
t_{JIT}	Output Total Jitter - 10.8 Gbps (FPD-Link IV)		DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.30	UI_{FC}
t_{JIT}	Output Total Jitter - 6.75 Gbps (FPD-Link IV)	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (2)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.25	UI_{FC}
t_{JIT}	Output Total Jitter - 3.375 Gbps (FPD-Link IV)					0.25	UI_{FC}
t_{JIT}	Output Total Jitter - 3.675 Gbps (FPD-Link III)	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (2)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.25	UI_{FC}
t_{RF}	Forward Channel Rise/Fall Time	20% to 80%,			30		ps
E_{FCH}	Output Eye Height - 13.5 Gbps (FPD-Link IV)	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. Correlation to eye height with video data required to use PRBS15.(2)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	225			mVpp
E_{FCH}	Output Eye Height - 12.528 Gbps (FPD-Link IV)			335			mVpp
E_{FCH}	Output Eye Height - 10.8 Gbps (FPD-Link IV)			335			mVpp
E_{FCH}	Output Eye Height - 6.75 Gbps (FPD-Link IV)	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. Correlation to eye height with video data required to use PRBS15.(2)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	510			mVpp
E_{FCH}	Output Eye Height - 3.375 Gbps (FPD-Link IV)			640			mVpp

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
E_{FCH}	Output Eye Height - 3.675 Gbps (FPD-Link III)	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. Correlation to eye height with video data required to use PRBS15.(2)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	640			mVpp
$f_{DEV\_DOWN-FC}$	Forward Channel Spread Spectrum Clocking Generation Deviation Frequency Magnitude	Down Spread (-0.25%)	DOUT0±, DOUT1±			0.25	%
$f_{DEV\_CENTER\_SUM}$	Spread Spectrum Clocking Generation Deviation Frequency Magnitude Sum on Forward Channel	Foward Channel Center Spread (+/-0.25%)	DOUT0±, DOUT1±			0.5	%
$f_{DEV\_CENTER\_HALF}$	Forward Channel Spread Spectrum Clocking Generation Deviation Frequency Magnitude	Center Spread (+/-0.25%) (SSCG only applied to foward channel)	DOUT0±, DOUT1±			0.5	%
f_{MOD}	Spread Spectrum Clocking Generation Modulation Frequency		DOUT0±, DOUT1±	30		33	kHz
t_{TSD}	Serializer Delay	Data in to Data out			245		ns
t_{PLL-LT}	Lock Time	PDB to Valid FPD Out				2	ms
S_{11}	Return loss of TX	f_{FCMAX}= 6.75GHz			-12.1		dB
S_{11}	Return loss of TX	f_{BCMIN} = 84.375MHz			-42		dB

(1) The backchannel data rate (Mbps) listed is for the encoded back channel data stream. For the 94x, the internal reference frequency used to generate the encoded back channel data stream is two times the back channel datarate. For the 98x, the internal reference frequency used to generate the encoded back channel data stream is the same as the back channel datarate.
(2) Measurement includes PCB and recommended external components
(3) Refer to partner deserializer for maximum data rate. Certain deserializers support up to 96 MHz (3.36 Gbps) or lower PCLK.

6.7 DisplayPort Electrical Characteristics

At typical condition (T=25ºC, nominal VDD). Tested according to DP 1.4a PHY CTS r1.0.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DP V1.4 MAIN LINK RX SYSTEM PARAMETERS						
f_{HBR3}	Frequency for high bit rate 3	HBR3 rate @ +300ppm / -5300ppm	8.05707	8.1	8.10243	Gbps
f_{HBR2}	Frequency for high bit rate 2	HBR2 rate @ +300ppm / -5300ppm	5.37138	5.4	5.40162	Gbps
f_{HBR}	Frequency for high bit rate	HBR rate @ +300ppm / -5300ppm	2.68569	2.7	2.70081	Gbps
f_{RBR}	Frequency for reduced bit rate	RBR rate @ +300ppm / -5300ppm	1.611414	1.62	1.620486	Gbps
Down_Spread_Amplitude	Link clock down-spreading	Modulation frequency range of 30kHz to 33kHz	0		0.5	%
DP V1.4 RX TP3 PARAMETERS						
t_{RX-EYE_CONN}	Minimum Receiver EYE Width at RX-side connector pins	RBR	0.25			UI
$t_{RX-SKEW-INTRA\_PAIR\ HBR3}$	Lane Intra-pair Skew Tolerance	HBR3			50	ps
$t_{RX-SKEW-INTRA\_PAIR\ HBR2}$	Lane Intra-pair Skew Tolerance	HBR2			50	ps

6.7 DisplayPort Electrical Characteristics (continued)

At typical condition (T=25ºC, nominal VDD). Tested according to DP 1.4a PHY CTS r1.0.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{RX-SKEW-INTRA\_PAIR\ High-Bit-Rate}$	Lane Intra-pair Skew Tolerance	HBR. Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3.			60	ps
$t_{RX-SKEW-INTRA\_PAIR\ Reduced-Bit-Rate}$	Lane Intra-pair Skew Tolerance	RBR. For RBR. Represents the skew contribution from the cable in addition to the stressed EYE at TP3.			260	ps
$f_{RX-TRACKING-BW\_HBR3}$	Jitter Closed-Loop Tracking Bandwidth	Minimum CDR closed-loop tracking bandwidth at the receiver when the input is an 8b/10b pattern, such as a TPS4. 3dB BW @0.5UI SJ	7.2			MHz
$f_{RX-TRACKING-BW\_HBR2}$	Jitter Closed-Loop Tracking Bandwidth	Minimum CDR closed-loop tracking bandwidth at the receiver when the input is an 8b/10b pattern, such as a TPS4. 3dB BW @0.5UI SJ	5.4			MHz
$f_{RX-TRACKING-BW\_HBR}$	Jitter Closed-Loop Tracking Bandwidth		1.8			MHz
$f_{RX-TRACKING-BW\_RBR}$	Jitter Closed-Loop Tracking Bandwidth		0.65			MHz
DP V1.4 MAIN LINK RX TP3_EQ						
$t_{RX-TJ\_TPS4\_HBR3}$	Minimum Receiver EYE Width	HBR3. Measured at 1E-9 BER using TPS4.	0.35			UI
$V_{RX-DIFFp-p\_HBR3}$	RX Differential Peak-to- Peak EYE Voltage	HBR3. Measured at 1E-9 BER using TPS4.	75			mV
$t_{RX-NonISI\_TPS4\_HBR3}$	Minimum Receiver Non-ISI Jitter	HBR3. Measured at 1E-9 BER.	0.56			UI
$t_{TX-RJ\_TPS4\_HBR3}$	Random Jitter Contribution from TX	For HBR3 without cross talk. Measured at 1E-9 BER.	0.16			UI
$t_{RX-TJ\_CP2520\_HBR2}$	Minimum Receiver EYE Width	HBR2. Measured at 1E-9 BER using the CP2520 PHY Layer Compliance EYE pattern.	0.38			UI
$V_{RX-DIFFp-p\_HBR2}$	RX Differential Peak-to- Peak EYE Voltage		70			mV
$t_{RX-DIFFp-p\_RANGE\_HBR2\_HBR3}$	RX Differential Peak-to-Peak EYE Voltage Measurement Range	HBR2, HBR3. Uses 0.5 CDF of the jitter distribution as the 0UI reference point. RX Differential Peak-to-Peak EYE Voltage requirement can be met anywhere within this UI range.	0.375		0.625	UI
DP V1.4 AUX CHANNEL ELECTRICAL SPECIFICATIONS						
UI_{MAN}	Manchester transaction unit interval		0.4	0.5	0.6	us
Pre-charge Pulses	Number of pre-charge pulses		10		16	
$PULSE_{SYNC}$	Number of Pulses before SYNC end symbol (DP mode)			16		pulses
$PULSE_{SYNC}$	Number of Pulses before SYNC end symbol (eDP mode)			8		pulses
$T_{AUX-BUS-PARK}$	AUX CH bus park time		10			ns

6.7 DisplayPort Electrical Characteristics (continued)

At typical condition (T=25°C, nominal VDD). Tested according to DP 1.4a PHY CTS r1.0.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{AUX-BUS-PARK}$	Maximum allowable UI variation within a single transaction at connector pins of a transmitting device				0.08	UI
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a transmitting device				0.04	UI
	Maximum allowable UI variation within a single transaction at connector pins of a receiving device				0.1	UI
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device				0.05	UI
$V_{AUX-DIFFp-p\_TX}$	eDP mode AUX peak-to-peak voltage at a transmitting device when transmitting		0.14		1.36	V
$V_{AUX-DIFFp-p\_TX}$	DP mode AUX peak-to-peak voltage at a transmitting device when transmitting		0.29		0.4	V
	DP mode AUX peak-to-peak voltage at a receiving device when transmitting		0.27		0.38	V
$V_{AUX-DIFFp-p\_RX}$	DP mode AUX peak-to-peak voltage at a transmitting device when receiving		0.29		1.38	V
	DP mode AUX peak-to-peak voltage at a receiving device when receiving		0.27		1.36	V
$V_{AUX-DC-CM}$	eDP mode AUX DC common mode voltage		0		1.2	V
$V_{AUX-DC-CM}$	DP mode AUX DC common mode voltage		0		2	V
$V_{AUX-TURN-CM}$	AUX turn around common mode voltage				0.3	V
I_{AUX_SHORT}	AUX short circuit current limit				90	mA
C_{AUX}	AUX AC-coupling capacitor		75		200	nF
DP V1.4 HPD SIGNAL SPECIFICATIONS						
V_{OH_3p3}	HPD HIGH-level output voltage		2.25		3.6	V
V_{OL_3p3}	HPD LOW-level output voltage				0.4	V
V_{OH_1p8}	HPD HIGH-level output voltage at Vdd of 1.8V		VDD18 - 0.45		VDD18	V
V_{OL_1p8}	HPD LOW-level output voltage at Vdd of 1.8V				0.45	V
HPD_TERM	HPD Downstream Device Termination		100			kΩ
t_{IRQ_HPD1}	IRQ_HPD Pulse/Glitch Detection Threshold for Upstream Device		0.25			ms
t_{IRQ_HPD2}	IRQ_HPD Pulse/ Hot Unplug Event Detection Threshold for Upstream Device		2			ms

6.7 DisplayPort Electrical Characteristics (continued)

At typical condition (T=25°C, nominal VDD). Tested according to DP 1.4a PHY CTS r1.0.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{IRQ_HPD3}	IRQ_HPD Minimum Spacing		2			ms

6.8 Recommended Timing for the Serial Control Bus

Over I2C supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode Plus	>0		1	MHz
		High-speed-mode	>0		3.4	MHz
t_{LOW}	SCL Low Period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
		High-speed-mode	0.16			µs
t_{HIGH}	SCL High Period	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.06			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.16			µs
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.16			µs
$t_{HD:DAT}$	Data hold time	Standard-mode	0		3.45	µs
		Fast-mode	0		0.9	µs
		Fast-mode Plus	0		0.45	µs
		High-speed-mode	0		0.07	µs
$t_{SU:DAT}$	Data set up time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
		High-speed-mode	10			ns
$t_{SU:STO}$	Set up time for STOP condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.16			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
	Bus free time between STOP and START (FPD-Link IV, FPD-Link III with PCLK ≥ 50 MHz)	Fast-mode Plus	0.5			µs
	Bus free time between STOP and START (FPD-Link III mode, PCLK < 50 MHz)	Fast-mode Plus	1			µs

6.8 Recommended Timing for the Serial Control Bus (continued)

Over I2C supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
t_r	SCL and SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
		High-speed-mode			40	ns
t_f	SCL and SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
		High-speed-mode			40	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
		High-speed-mode			100	pF
$t_{VD:DAT}$	Data valid time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
$t_{VD:ACK}$	Data vallid acknowledge time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
t_{SP}	Input filter	Standard-mode			50	ns
		Fast-mode			50	ns
		Fast-mode Plus			50	ns
		High-speed-mode			10	ns

6.9 Timing Diagrams

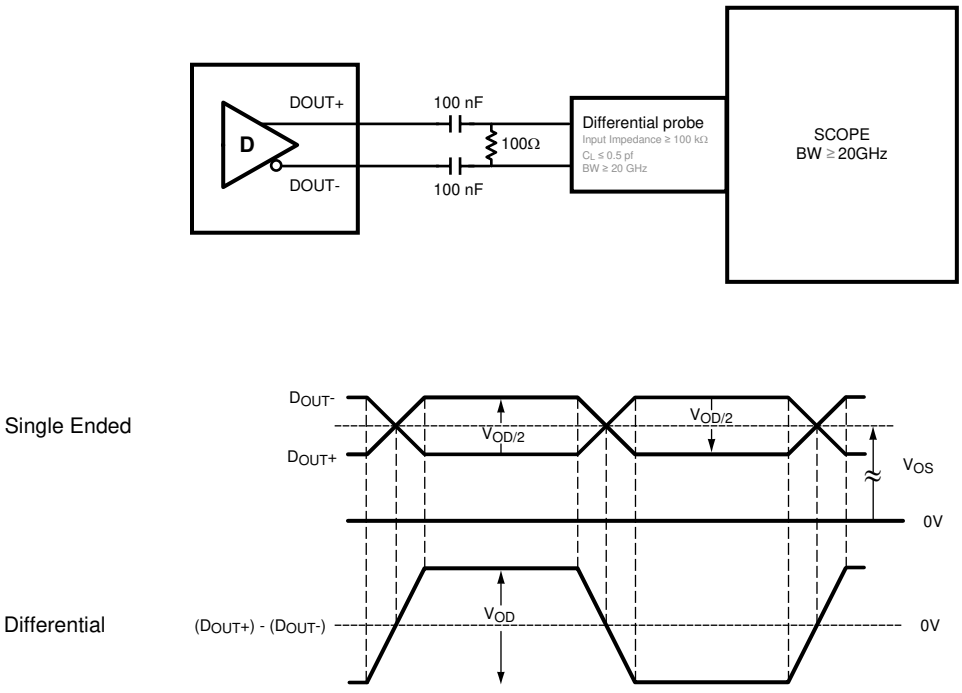


Figure 6-1. Serializer V_{OD} Output

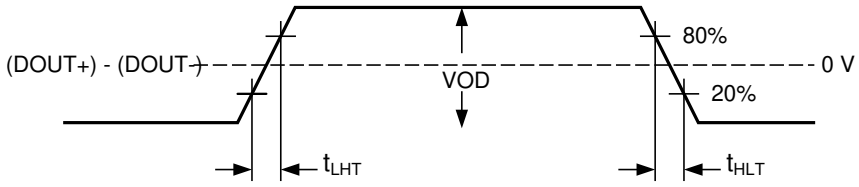


Figure 6-2. Output Transition Times

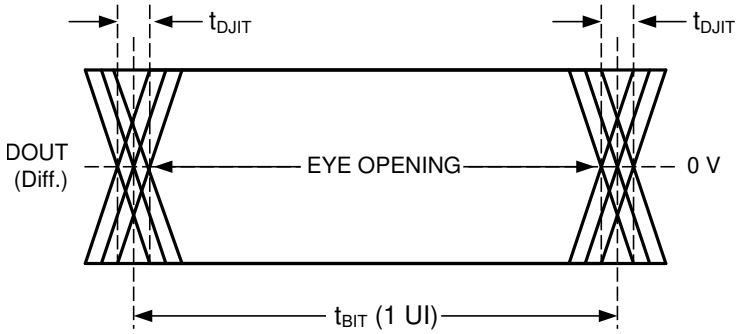


Figure 6-3. Serializer Output Jitter

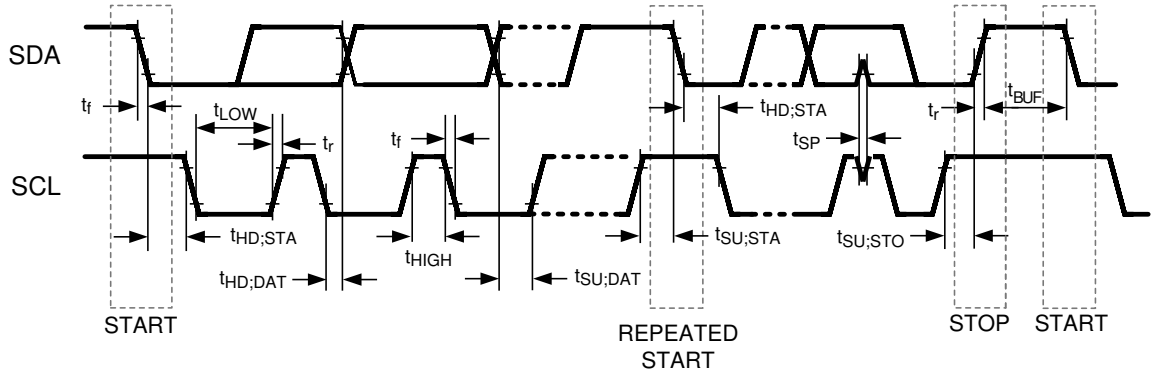


Figure 6-4. Serial Control Bus Timing Diagram

7 Detailed Description

7.1 Overview

The DS90UB983-Q1 converts a DisplayPort interface (1, 2, or 4 lanes) to an FPD-Link IV interface. The DisplayPort receiver supports up to HBR3 speed, a data rate of 8.1 Gbps with a total bandwidth of 32.4 Gbps link rate. This device transmits an FPD-Link IV output over a single coax/STP cable operating up to 13.5 Gbps line rate or Dual Coax/STP cable operating up to 27 Gbps line rate. The serial stream contains an embedded clock, video control signals, DP video data, control information, and audio data. The payload is DC-balanced to enhance signal quality and supports AC coupling. The DS90UB983-Q1 serializer is intended for use with a DS90UB984-Q1, and DS90UB988-Q1 deserializers, or the DS90Ux924-Q1, DS90Ux926-Q1, DS90Ux928-Q1, DS90Ux940-Q1, DS90Ux940N-Q1, and DS90Ux948-Q1 deserializers in backwards compatible mode.

The DS90UB983-Q1 serializer and companion deserializer incorporate an I^2C compatible interface. The I^2C interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer and deserializer as well as remote I^2C target devices. The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I^2C transactions across the serial link from one I^2C bus to another. The implementation allows for arbitration with other I^2C compatible controllers at either side of the serial link.

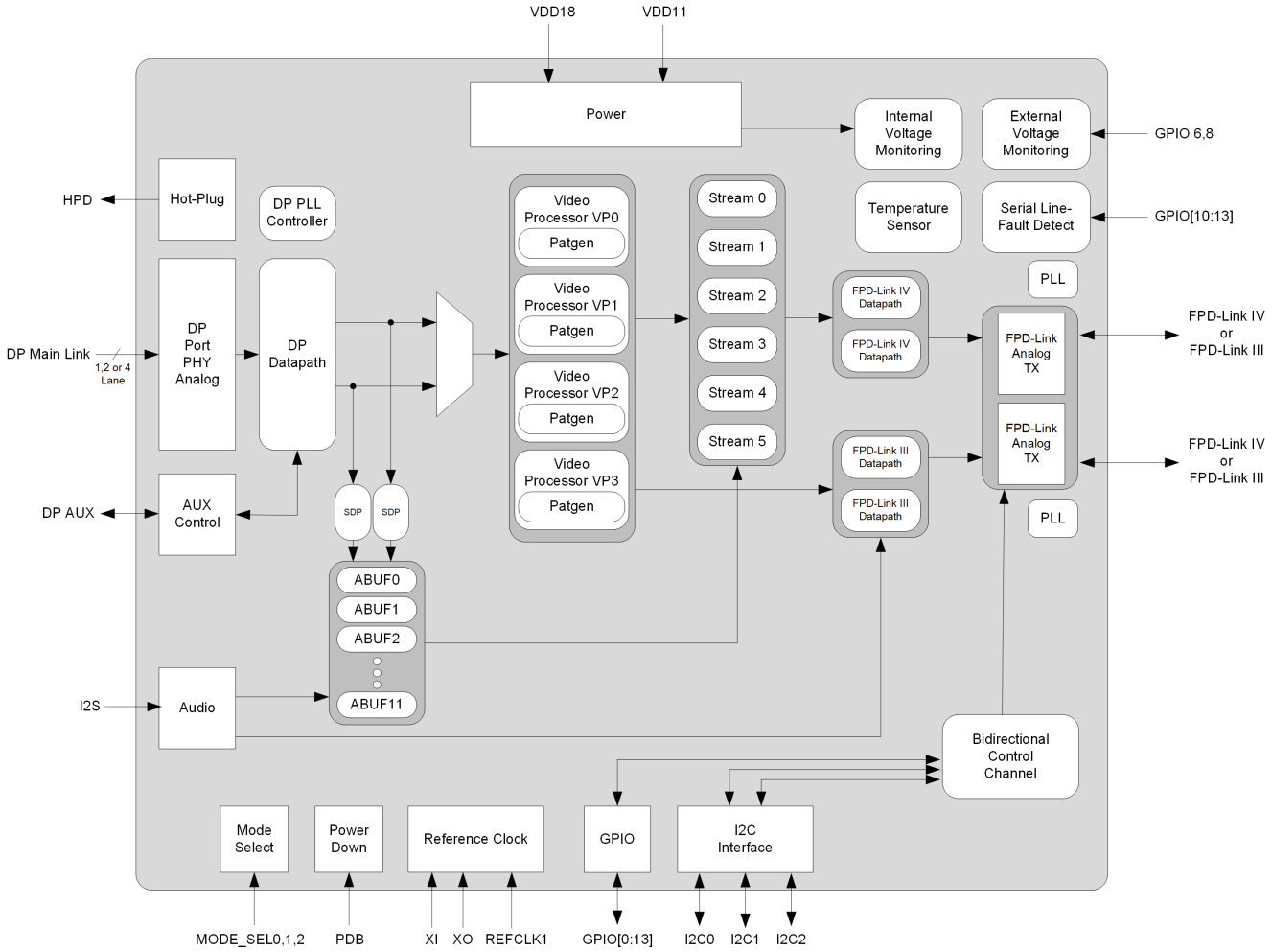
Table 7-1. Features

FUNCTION	DESCRIPTION
DATA RATES	
Forward Channel Line Rate	• Up to 27 Gbps over STQ/Dual-coax or up to 13.5 Gbps per STP/Coax (including frame and coding overhead) • Discrete rates of 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps and 3.375 Gbps available per FPD-Link IV lane
Forward DP Rate	• 6.48 Gbps per DP lane (8.1 Gbps with 8b10b overhead)
Back Channel Rate	• 168.75 Mbps for FPD-Link IV • 156.6 Mbps for FPD-Link IV (12.528 Gbps)
INTERFACE	
Cable	FPD-Link IV, NRZ signaling • 50Ω coaxial single-ended cable • 100Ω differential STP
System	DP v1.4 HBR3 • Configurable 1, 2 or 4 lanes • 6.48 Gbps per lane (8.1 Gbps with 8b10b overhead) eDP v1.4b HRB3 • Supports 1, 2, or 4 lanes • 6.48 Gbps per lane (8.1 Gbps with 8b10b overhead)
Control	I^2C, GPIO, and SPI • Up to 1 Mbps I^2C (up to 3.4 Mbps for local bus access) • High-Speed GPIO • Supports SPI and UART passthrough on GPIOs
NETWORKING TOPOLOGIES	

Table 7-1. Features (continued)

FUNCTION	DESCRIPTION
Topologies	• Point-to-point topology • Daisy chain (when used with DS90UB98x deserializer) • One –to –Many Y topology • SuperFrame splitting • Video aggregation
DATA PROTECTION	
Video	• Error detection on serializer input with error counter and alarm signal
Control	• Errors are communicated back to deserializer via I^2C NACK and link alarm bit.
BACKWARD COMPATIBILITY	
Forward Channel Line Rate	• Backward compatible 875 Mbps to 3.675 Gbps available per FPD-Link III lane • Backward compatible mode supports a PCLK range of 25 MHz to 105 MHz single or 210 MHz in dual mode (limited by deserializer capability)
Back Channel Rate	• Backwards compatible rates of 5, 10, 20 Mbps for FPD-Link III
HEALTH MONITORING AND DIAGNOSTICS	
Alarm	• Alarm bit configurable to trigger on link status, bit errors, etc
Voltage & Temperature	• Measures up to 2 external voltages • Measure internal die temperature • 8-bit resolution
BIST	• Pseudo-random bit sequence (PRBS) Built-in self test (BIST) function
Line-Fault Detect	• Serial link line fault monitor to detect power supply short, short to ground, or open.
ESD Event Counter	• Detects and tracks number of ESD events trigger the devices ESD protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DisplayPort (DP) / embedded DisplayPort (eDP) Receiver

The DP interface is capable of transmitting high-definition video as well as various control and status data that travel bidirectionally. The DP interface consists of four data lanes, one auxiliary channel and a HPD line. Some DP interfaces include a 3.3V DP power line, but this is not used by the DS90UB983-Q1. The DP Receiver is a DP version 1.4 compatible receiver. The DP receiver (DP RX) is capable of operation with 4K resolutions at 60 Hz. The DS90UB983-Q1 includes DP support for 18-bit, 24-bit and 30-bit RGB data formats. The DP RX supports up to four differential pairs to transmit video data. Each of the four pairs carry data with an embedded clock. The DP data lanes can operate at 1.62 Gbps (Reduced Bit Rate or RBR), 2.7 Gbps (High Bit Rate or HBR), 5.4 Gbps (High Bit Rate 2 or HBR2) or 8.1 Gbps (High Bit Rate 3 or HBR3). The DP interface incorporates a form of 8b/10b encoding, and the differential signaling reduces electromagnetic interference (EMI) and improves skew tolerance.

The embedded DisplayPort (commonly referred to eDP) is related to the external DisplayPort interface and based on the VESA standard. The embedded DisplayPort is an internal interface where the system function is fully integrated within the SoC. Both of these interfaces have slightly different hardware implementation as shown in DP/eDP Implementation. A proper shielded cable can be used for the eDP interconnect connecting both SoC and the DS90UB983-Q1 in the system application. The DS90UB983-Q1 can be integrated within the same board as the SoC where the cable is omitted.

7.3.1.1 DisplayPort Initialization

Through DP AUX and HPD control signals, DPRX can respond to DPTX upon connection and complete link training automatically. In both SST and MST mode, after link training is complete, a video reset is recommended in DS90UB983-Q1 DPRX. Set APB register 0x054[0] = 1 to reset the video reception only when the incoming video are not synchronized from the input source.

Example code to check if the video timings are synchronized.

```
    # Select/set global flag for desired VPs
    VP0_enabled = 1
    VP1_enabled = 0
    VP2_enabled = 0
    VP3_enabled = 0

    # Select VP page
    board.WriteI2C(serAddr, 0x40, 0x31)

    # Check VP0 status
    board.WriteI2C(serAddr, 0x41, 0x30)
    VP0sts= board.ReadI2C(serAddr, 0x42)

    # Check VP1 status
    board.WriteI2C(serAddr, 0x41, 0x70)
    VP1sts = board.ReadI2C(serAddr, 0x42)

    # Check VP2 status
    board.WriteI2C(serAddr, 0x41, 0xB2)
    VP2sts = board.ReadI2C(serAddr, 0x42)

    # Check VP3 status
    board.WriteI2C(serAddr, 0x41, 0xF0)
    VP3sts = board.ReadI2C(serAddr, 0x42)

    if (VP0_enabled and VP0sts == 0) or (VP1_enabled and VP1sts == 0) or (VP2_enabled and VP2sts ==
0) or (VP3_enabled and VP3sts == 0):
        board.WriteI2C(serAddr, 0x49, 0x54)  # Video Input Reset
        board.WriteI2C(serAddr, 0x4a, 0x0)
        board.WriteI2C(serAddr, 0x4b, 0x1)
        board.WriteI2C(serAddr, 0x4c, 0x0)
        board.WriteI2C(serAddr, 0x4d, 0x0)
        board.WriteI2C(serAddr, 0x4e, 0x0)
```

7.3.1.2 Multi-Display Transport Support

Multi-stream transport (MST) enables the transport of multiple streams from multiple stream sources device in one or more DP source devices to multiple stream sinks in one or more DP sink devices. The DP interface supports two streams of Multi-Stream Transport (MST) or Single-Stream Transport (SST), allowing multiple video streams to be sent through a single DP interface. The DS90UB983-Q1 supports up to two video streams on its DP receiver. Each stream can contain multiple images in SuperFrame format which can be extracted by the video processors to support up to 4 screens. The MST supports both symmetric and asymmetric video stream resolutions with independent frame rates. The MST feature requires bypassing sideband messaging/ topology discovery inside the DP source.

7.3.1.2.1 MST Configuration

The DS90UB983-Q1 DPRX supports both SST mode and MST mode. The mode is selected upon power up through MODE_SEL1 strap setting. The alternative way is to overrite the MST enable bit of APB register 0x018[8] = 1. Write 1 to enable MST mode or 0 to disable MST mode. MST mode does not support automatic topology management, so the DP source must be configured to bypass automatic MST topology discovery and force the desired MST configuration for virtual sink 0 and virtual sink 1.

In order to configure the DS90UB983-Q1 to support MST mode, the DPRX MST Payload ID and virtual sink settings need to be applied via APB register configuration after DP link is locked. The DPRX sink settings are shown in the snippet of code below for 2-stream MST configuration. The settings are the same for all 2-stream MST regardless the video source timing.

```
devAddr = 0x18
board.WriteI2C(devAddr, 0x01, 0x01) # soft reset
board.WriteI2C(devAddr, 0x2D, 0x01) # write port select to port 0 initially

board.WriteI2C(devAddr,0x49,0x4) #Set MST_PAYLOAD_ID APB reg 0x904 value 0x1
board.WriteI2C(devAddr,0x4a,0x9)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x8) #Set MST_PAYLOAD_ID APB reg 0x908 value 0x2
board.WriteI2C(devAddr,0x4a,0x9)
board.WriteI2C(devAddr,0x4b,0x2)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x4) #Set MST_PAYLOAD_ID APB reg 0x904 value 0x1
board.WriteI2C(devAddr,0x4a,0x9)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x8) #Set MST_PAYLOAD_ID APB reg 0x908 value 0x2
board.WriteI2C(devAddr,0x4a,0x9)
board.WriteI2C(devAddr,0x4b,0x2)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)

board.WriteI2C(devAddr,0x49,0x0) #Set DP Virtual Sink 0 Settings APB reg 0xA00 value 0x1
board.WriteI2C(devAddr,0x4a,0xa)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x4) #Set DP Virtual Sink 0 Settings APB reg 0xA04 value 0x4
board.WriteI2C(devAddr,0x4a,0xa)
board.WriteI2C(devAddr,0x4b,0x4)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x18) #Set DP Virtual Sink 0 Settings APB reg 0xA18 value 0x1
board.WriteI2C(devAddr,0x4a,0xa)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x14) #Enable DTG for stream 0 APB reg 0xA14 value 0x1
board.WriteI2C(devAddr,0x4a,0xa)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)

board.WriteI2C(devAddr,0x49,0x0) #Set DP Virtual Sink 0 Settings APB reg 0xB00 value 0x1
board.WriteI2C(devAddr,0x4a,0xb)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x4) #Set DP Virtual Sink 0 Settings APB reg 0xB04 value 0x4
board.WriteI2C(devAddr,0x4a,0xb)
board.WriteI2C(devAddr,0x4b,0x4)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x18) #Set DP Virtual Sink 0 Settings APB reg 0xB18 value 0x1
board.WriteI2C(devAddr,0x4a,0xb)
board.WriteI2C(devAddr,0x4b,0x1)
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
board.WriteI2C(devAddr,0x49,0x14) #Enable DTG for stream 0 APB reg 0xB14 value 0x1
board.WriteI2C(devAddr,0x4a,0xb)
board.WriteI2C(devAddr,0x4b,0x1)
```

```
board.WriteI2C(devAddr,0x4c,0x0)
board.WriteI2C(devAddr,0x4d,0x0)
```

7.3.1.3 Hot Plug Detect (HPD)

The HPD line is asserted by the sink to let the source know that it is ready for AUX transactions. The HPD line can also be used for an interrupt request (IRQ) assertion by a downstream (e.g. sink) device. Similarly, the downstream device monitors AUX+ and AUX- DC voltage levels to detect the presence of an upstream device and its power state. After the HPD pin is asserted, the AUX channel will be used to perform link training which consist of configuring drive current and equalization levels. DS90UB983-Q1's Hot Plug Detect (HPD) signal line is configured to 1.8V or 3.3V voltage levels through the MODE_SEL1 strap pin in Table 7-42.

For eDP, the HPD (Hot Plug Detect) signal is optional but TI recommends connecting HPD if HPD functionality is supported by the eDP source. If HPD is not used, link training and re-training needs to be manually performed by the DP source.

7.3.1.4 DP Auxiliary (AUX) Channel

The DP RX supports a 1 Mbps Manchester-encoded AUX channel which is used for link management and device control. The AUX channel is a half-duplex bidirectional channel, meaning that communication can only travel in one direction at a time. AUX transactions are initiated by an upstream (e.g. source) device, but a downstream device can prompt an AUX transaction via an IRQ pulse assertion over the HPD line.

7.3.1.5 DisplayPort Configuration Data (DPCD)

The DP RX includes a set of standard registers used to determine receiver capability and perform link training. These registers are accessible via the AUX channel of the DP interface. The data for some of these registers can also be read indirectly via registers in APB (DP RX) Registers.

7.3.2 FPD-Link IV High Speed Forward Channel Data Transfer

The High Speed Forward Channel transmits data according to the FPD-Link IV protocol. FPD-Link IV consists of 132-bit units of data transmission, referred to as frames. FPD-Link IV frames can transmit RGB data, sync signals, I^2C, and GPIOs transmitted from serializer to deserializer. Each 132-bit frame can include up to 128 bits of RGB data. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. FPD-Link IV protocol allows for up to four distinct streams to be transferred over a single link. To manage the bandwidth allocation of the FPD-Link, each FPD-Link includes 65 different time slots which are divided up between the different FPD-Link streams.

The FPD-Link IV serial stream rate supports fixed-rates of 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps and 3.375 Gbps. When operating over both FPD-Link channels, a total data rate of 27 Gbps, 25.056 Gbps, 21.6 Gbps, 13.5 Gbps and 6.75 Gbps is supported, respectively.

7.3.2.1 FPD-Link Streams

FPD-Link IV protocol supports transferring up to six distinct streams over a single link. FPD-Link FPD-Link streams can be used to transmit video or other data. Up to four streams can be used to send video data by mapping the outputs of the four video processors (VPs) to an FPD-Link stream. See Section 7.3.4.3.

7.3.2.2 FPD-Link Timeslots

There are 65 total timeslots in dual mode and 65 total slots per link layer in independent mode, which are used to divide the available FPD-Link bandwidth between different streams. The number of timeslots allocated to each stream are configured through the LINK0_SLOT_REQx and LINK1_SLOT_REQx in Page_11 registers (0x06, 0x07, 0x08, 0x09, 0x16, 0x17, 0x18, and 0x19). Video streams can be assigned based on system needs (i.e. all four video streams can be assigned to Link Layer 0 or split across both Link Layer 0 and Link Layer 1). When assigning time slots, if fewer than 65 timeslots are requested, the additional timeslots will be assigned to Stream 0. If greater than 65 timeslots are requested (an invalid configuration), priority is given to lower stream numbers. Timeslot assignments are updated only after the EN_NEW_TSLOTx bit is set. In Dual FPD-Link mode only the Link Layer 0 registers are used. In general, timeslots can be assigned based on the proportion of the available bandwidth required by the individual stream. For example with a FPD-Link single link or independent with a data rate of 13.5 Gbps which supports up to 13.09 Gbps throughput (13.5 Gbps x 128/132), each timeslot accounts for a bandwidth of 201 Mbps (13.09 Gbps / 65). For a system configured to dual FPD-Link with 13.5 Gbps data rate per lane, the total bandwidth is 26.18 Gbps (2 x (13.5Gbps x 128/132)). Each timeslot acounts for 402

Mbps (26.18 Gbps / 65). The time slot assignments are considered static and can not be modified during video transmission. It is recommended to adhere to the following procedure when modifying time slot assignments:

1. Disable the link layer (set LINK_LAYER_x_EN = 0)
2. Disable all video processors used on the link (set VPx_ENABLE= 0)
3. Configure time slots through LINK0_SLOT_REQx and LINK1_SLOT_REQx registers
4. Set EN_NEW_TSLOTx = 1
5. Enable the link layer (set LINK_LAYER_x_EN = 1)
6. Enable all video processors used on the link (set VPx_ENABLE= 1)

7.3.2.2.1 Example Timeslot Assignment

1. Calculate the required bandwidth for each image by multiplying the PCLK by the number of bits per pixel.
   - EX: Stream 0: PCLK = 200 MHz with 30 bpp. Required bandwidth = 200 MHz * 30 bpp = 6.0 Gbps
     Stream 1: PCLK = 112 MHz with 24 bpp. Required bandwidth = 112 MHz * 24 bpp = 2.688 Gbps
2. Calculate the proportion of the available bandwidth needed for each stream and the corresponding number of timeslots (Stream Bandwidth / Available Bandwidth * Total Number of Timeslots rounded up).
   - EX: Stream 0: Proportion of Available Bandwidth = 6.0 Gbps / 10.47 Gbps = 0.57.
     Number of Timeslots = 65*0.57 = 37.05 ≈ 38 Timeslots
     Stream 1: Proportion of Available Bandwidth = 2.688 Gbps / 10.47 Gbps = 0.25.
     Number of Timeslots = 65*0.25 = 16.25 ≈ 17 Timeslots
3. Verify the total number of timeslots is less than 65.
   - EX: 38 Timeslots for Stream 0 + 17 Timeslots for Stream 1 = 55
     Timeslots is < 65 Timeslots so this configuration is valid.
4. (Optional) Assign extra timeslots evenly between streams. If this step is skipped, the remaining timeslots will be assigned to Stream 0.
   - EX: 65 - 55 = 10 remaining timeslots. Add 5 timeslots to Stream 0 and 5 timeslots to Stream 1. Stream 0 can be assigned 43 timeslots total (LINKx_SLOT_REQ0 = 43) and Stream 1 can be assigned 22 timeslots total (LINKx_SLOT_REQ1= 22).

7.3.2.3 FPD-Link PLL

The V^{3}Link forward channel is generated based on a phase locked loop (PLL) as shown in Figure 7-1. In general, this PLL can select between XI and REFCLK1 for the reference source. For FPD-Link IV, the 27 MHz connected to XI must be used as the reference source. The PLL settings are automatically set at device start up according to the devices MODE_SEL settings. This is the default setting and can be confirmed by checking the register CHx_FPD3_REFCLK1 = 0 (0x5[7] or 0x5[6]). In FPD-Link IV mode, the output of the PLL must be 6.75 GHz (13.5 Gbps/2 bits), 6.264 GHz (12.528 Gbps/2 bits), 5.4 GHz (10.8 Gbps/2 bits), 3.375 GHz (6.75 Gbps/2 bits or 3.375 Gbps/1 bit) as a result of FPD-Link mode set to full-rate mode in HALFRATE_MODE_CHx[7:6]. This output frequency is generated using the following settings, programmable via Page 2 of the indirect access registers. After modifying PLL values, reset the PLL using either PLL_CH0_RESET or PLL_CH1_RESET Field in RESET_CTL register 0x01.

The following equation is used to calculate the VCO frequency:

- f_{VCO} is the VCO frequency
- P is the post-divider value (1, 2, 4, 8, 16)

$$f_{VCO} = f_{REF} \times 2 \times \left[N + \left(\frac{NUM}{DEN} \right) \right] \quad (1)$$

where

- f_{REF} is the reference frequency, either from the XI or REFCLK1
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206), NUM ≤ DEN
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

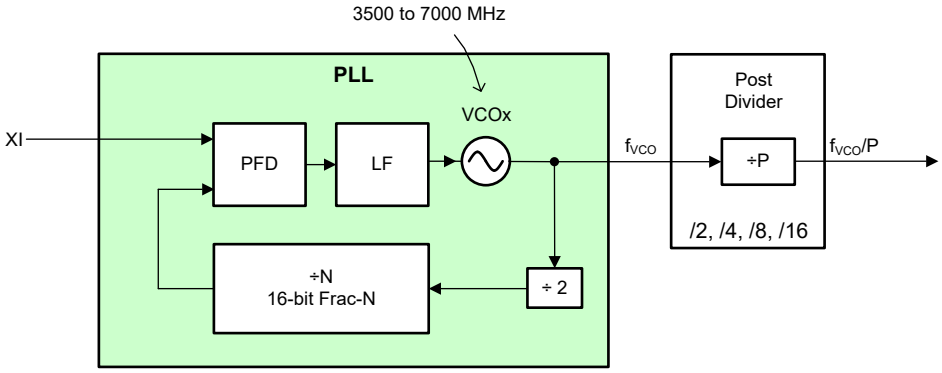


Figure 7-1. FPD-Link IV PLL

Table 7-2. FPD-Link IV PLL Settings for 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps and 3.375 Gbps

FPD-Link Data Rate	13.5 Gbps	12.528 Gbps	10.8 Gbps	6.75 Gbps	3.375 Gbps
FPD-Link Back Channel Rate	168.75 Mbps	156.6 Mbps	168.75 Mbps		
Reference Source	XI (CHx_FPD3_REFCLK1 = 0)				
N-Divider	125 (NDIV[7:0] = 0x7D, NDIV[15:8] = 0x00)	116 (NDIV[7:0] = 0x74, NDIV[15:8] = 0x00)	100 (NDIV[7:0] = 0x64, NDIV[15:8] = 0x00)	125 (NDIV[7:0] = 0x7D, NDIV[15:8] = 0x00)	
Numerator	0 (NUM[7:0] = 0x00, NUM[15:8] = 0x00, NUM[23:16] = 0x00)				
Denominator	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)				
MASH Order	Integer (MASH_ORDER = 0x0)				
Post-Divider	1 (POST_DIV = 0x0)			2 (POST_DIV = 0x1)	
FPD-Link PLL Frequency	6.75 GHz	6.264 GHz	5.4 GHz	3.375 GHz	3.375 GHz
Nyquist Frequency	6.75 GHz	6.264 GHz	5.4 GHz	3.375 GHz	1.6875 GHz
Back Channel Sampling Rate	2 (BC_DOWNSAMPLING_RATE = 0x1)		1 (BC_DOWNSAMPLING_RATE = 0x0)		
Back Channel Configuration	0 (BC_CONFIG = 0x0)		6 (BC_CONFIG = 0x6)	0 (BC_CONFIG = 0x0)	
Half Rate Mode	1 (HALFRATE_MODE_CHx = 0x1)				0 (HALFRATE_MODE_CHx = 0x0)

The DS90UB983-Q1 12.528 Gbps linerate is not pre-defined in the preset mode strap settings. The 12.528 Gbps linerate can be programmed via I^2C access registers setting in order to convert the current mode to 12.528 Gbps. Changing the 12.528 Gbps FPD-Link mode requires setting the PLL settings in Table 7-2.

Setting 12.528 Gbps FPD-Link mode

1. Strap the desired 12.528Gbps data rate for deserializer (1)
2. Power up serializer (DS90UB983-Q1) and deserializer (DS90Ux984 or DS90Ux988)
3. Set up PLL settings and enable PLLs on serializer
4. Perform a serializer PLL reset
5. Perform a deserializer reset

The following snippet code shows how to set up the PLL settings.

```
board.WriteI2C(serAddr,0x40,0x8) #Select PLL reg page
board.WriteI2C(serAddr,0x41,0x1b)
board.WriteI2C(serAddr,0x42,0x8) #Disable PLL0
board.WriteI2C(serAddr,0x41,0x5b)
board.WriteI2C(serAddr,0x42,0x8) #Disable PLL1
board.WriteI2C(serAddr,0x2,0xd1) #Enable mode overwrite
board.WriteI2C(serAddr,0x2d,0x1)
board.WriteI2C(serAddr,0x40,0x24) #Select digital reg page
board.WriteI2C(serAddr,0x40,0x8) #Select PLL page
board.WriteI2C(serAddr,0x41,0x5) #Select Ncount Reg
board.WriteI2C(serAddr,0x42,0x74) #Set Ncount
board.WriteI2C(serAddr,0x41,0x13) #Select post div reg
board.WriteI2C(serAddr,0x42,0x80) #Set post div for 12.528 Gbps
board.WriteI2C(serAddr,0x2d,0x1) #Select write reg to port 0
board.WriteI2C(serAddr,0x6a,0x4a) #set BC sampling rate
board.WriteI2C(serAddr,0x6e,0x80) #set BC configuration
board.WriteI2C(serAddr,0x40,0x4) #Select FPD page and set BC settings for FPD IV port 0
board.WriteI2C(serAddr,0x41,0x6)
board.WriteI2C(serAddr,0x42,0x0)
board.WriteI2C(serAddr,0x41,0xd)
board.WriteI2C(serAddr,0x42,0x34)
board.WriteI2C(serAddr,0x41,0xe)
board.WriteI2C(serAddr,0x42,0x53)
board.WriteI2C(serAddr,0x40,0x8) #Select PLL page
board.WriteI2C(serAddr,0x41,0x45) #Select Ncount Reg
board.WriteI2C(serAddr,0x42,0x74) #Set Ncount
board.WriteI2C(serAddr,0x41,0x53) #Select post div reg
board.WriteI2C(serAddr,0x42,0x80) #Set post div for 12.528 Gbps
board.WriteI2C(serAddr,0x2d,0x12) #Select write reg to port 1
board.WriteI2C(serAddr,0x6a,0x4a) #set BC sampling rate
board.WriteI2C(serAddr,0x6e,0x80) #set BC configuration
board.WriteI2C(serAddr,0x40,0x4) #Select FPD page and set BC settings for FPD IV port 1
board.WriteI2C(serAddr,0x41,0x26)
board.WriteI2C(serAddr,0x42,0x0)
board.WriteI2C(serAddr,0x41,0x2d)
board.WriteI2C(serAddr,0x42,0x34)
board.WriteI2C(serAddr,0x41,0x2e)
board.WriteI2C(serAddr,0x42,0x53)
board.WriteI2C(serAddr,0x2,0xd1) #Set HALFRATE_MODE
```

7.3.2.4 Spread Spectrum Clock Generation (SSCG)

If desired, spread spectrum clocking can be enabled for the FPD-Link IV forward channel ranging between 30 kHz and 33 kHz modulation frequency. FPD-Link IV forward channel and back channel SSCG cannot exceed 0.5% frequency deviation. When paired in backward compatible mode with DS90Ux948-Q1 deserializers in FPD-Link III, the frequency deviation cannot exceed 0.3%. Both center-spread and down-spread ramps are supported. The deserializer spread spectrum capabilities must be checked to ensure proper spread spectrum compatibility. It is recommended to use center-spread SSC such that the average FPD-Link rate is maintained. If down-spread is desired, this will reduce the FPD-Link bandwidth and must be considered in bandwidth calculations. SSC configurations must be chosen such that the final display can tolerate the variation in the PCLK. In FPD-Link IV mode, the effects of SSC must be considered when choosing the appropriate M and N values.

The FPD PLL must be configured in fractional mode to enable SSCG. If the PLL was originally configured in integer mode (NUM[23:0] = 0), set NUM[23:0] equal to the value of DEN[23:0], and subtract one from the original NDIV[15:0] value. Additionally, set MASH_ORDER to fractional mode (e.g. MASH_ORDER[2:0] = 2). For instance, to enable SSCG using the default FPD-Link IV PLL settings set NDIV = 124 and NUM[23:0] = 16,777,206. To configure spread spectrum clock generation, the following equations can be used to calculate the RAMPX_STOP and RAMPX_INC.

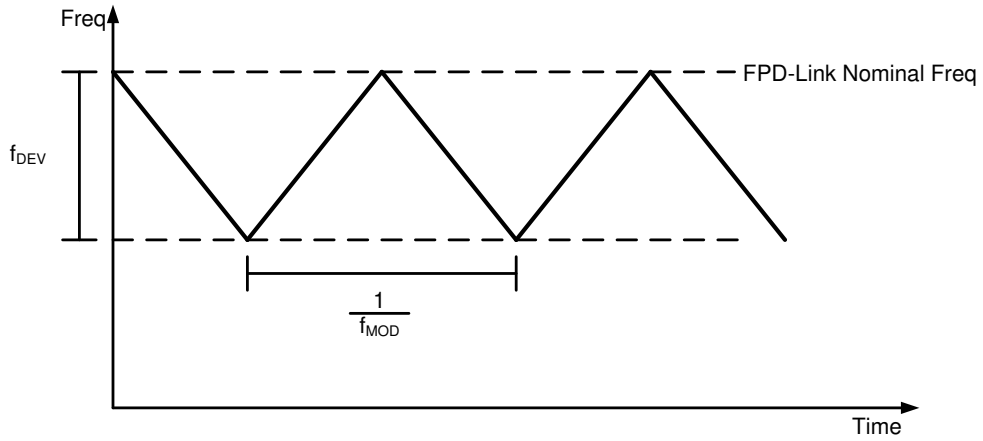


Figure 7-2. Down Spread SSCG

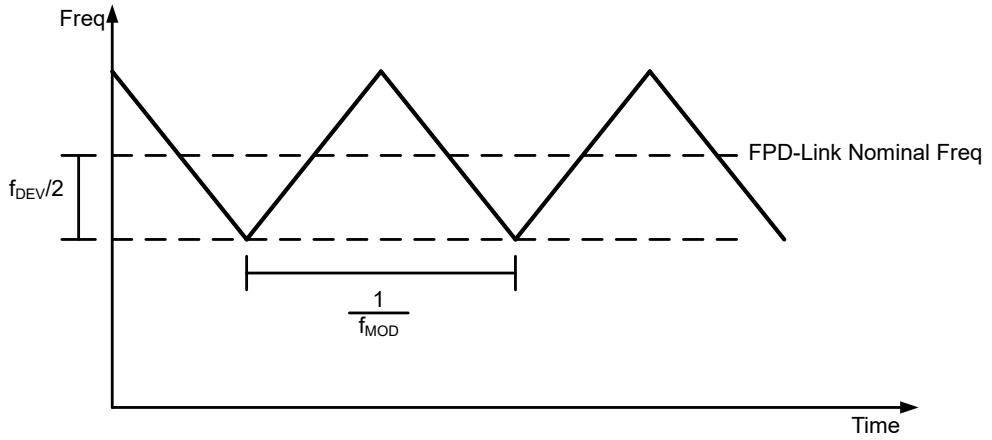


Figure 7-3. Center Spread SSCG

$$RAMPX\_STOP = \frac{f_{REF}}{(4 \times f_{MOD})} \quad (2)$$

where

- f_{REF} is the reference clock in kHz (27 MHz in FPD-Link IV Mode)
- f_{MOD} is the modulation frequency in kHz

$$RAMPX\_INC_{Initial} = \frac{(VCO\_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX\_STOP)} \quad (3)$$

- $RAMPX\_INC_{Initial}$ must be rounded to an integer number

where

- f_{DEV} is the deviation frequency as a percentage of the forward channel frequency (Example: deviation frequency = 0.5% corresponds to f_{DEV} = 0.5)
- i_{SPREAD} = 2
- $DEN_{Initial}$ is the denominator of the N-divider in the FPD PLL (16,777,206 for FPD-Link IV Mode)
- REFCLK is the reference clock frequency in MHz (27)
- VCO_freq is the VCO frequency in MHz

$$x = \begin{cases} \log_2 \dfrac{RAMPX\_INC_{Initial}}{32767}, & RAMPX\_INC_{Initial} > 32767 \\ 0, & RAMPX\_INC_{Initial} \le 32767 \end{cases} \quad (4)$$

where

- x must be rounded up to the nearest integer

$$RAMPX\_INC_{Final} = \frac{(VCO\_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX\_STOP \times 2^x)} \quad (5)$$

$$DEN_{Final} = \left(\frac{DEN_{Initial}}{2^x}\right) \quad (6)$$

$$NUM_{Final} = \left(\frac{NUM_{Initial}}{2^x}\right) \quad (7)$$

where

- Initial numerator and denominator are determined based on the FPD-Link rate. If the original PLL setting is integer mode (numerator = 0) then the first step of applying SSCG is to convert to fractional mode (subtract one from the integer part of the n divider and set both numerator and denominator to 16,777,206).

$$VCO_{Freq,Final} = f_{REF} \times 2\left[Ndiv + \left(\frac{NUM_{Final}}{DEN_{Final}}\right)\right] \quad (8)$$

$$f_{DEV,Final} = \left[\frac{(RAMPX\_INC_{Final} \times REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX\_STOP)}{(VCO_{Freq,Final} \times DEN_{Final})}\right] \quad (9)$$

For instance, to configure SSCG with f_{MOD} = 30 KHz SSCG with down-spread f_{DEV} = 0.5% frequency deviation and a reference clock of 27 MHz in FPD-Link IV Mode at a VCO frequency of 6.75 GHz.

$$RAMPX\_STOP = \frac{f_{REF}}{(4 \times f_{MOD})} \quad (10)$$

$$RAMPX\_STOP = \frac{27 \times 10^6}{(4 \times 30 \times 10^3)} = 225$$

$$RAMPX\_INC_{Initial} = \frac{(VCO\_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX\_STOP)} \quad (11)$$

$$RAMPX\_INC_{Initial} = \frac{(6.75 \times 10^9 \times 0.5 \times 16{,}777{,}206)}{(27 \times 10^6 \times 2 \times 100 \times 2 \times 225)} = 23301.675 \approx 23302$$

$$x = \log_2\left(\frac{23302}{32767}\right) = -0.49179 \approx 0$$

$$RAMPX\_INC_{Final} = \frac{\left(VCO\_freq \times f_{DEV} \times DEN_{Initial}\right)}{\left(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX\_STOP \times 2^{x}\right)} \quad (12)$$

$$RAMPX\_INC_{Final} = \frac{\left(6.75 \times 10^{9} \times 0.5 \times 16{,}777{,}206\right)}{\left(27 \times 10^{6} \times 2 \times 100 \times 2 \times 225 \times 2^{0}\right)} = 23301.675 \approx 23302$$

$$DEN_{Final} = \left(\frac{DEN_{Initial}}{2^{x}}\right) \quad (13)$$

$$DEN_{Final} = \left(\frac{16{,}777{,}206}{2^{0}}\right) = 16{,}777{,}206$$

$$NUM_{Final} = \left(\frac{NUM_{Initial}}{2^{x}}\right) \quad (14)$$

$$NUM_{Final} = \left(\frac{16{,}777{,}206}{2^{0}}\right) = 16{,}777{,}206$$

$$VCO_{Freq,Final} = f_{REF} \times 2\left[Ndiv + \left(\frac{NUM_{Final}}{DEN_{Final}}\right)\right] \quad (15)$$

$$VCO_{Freq,Final} = 27 \times 10^{6} \times 2\left[124 + \left(\frac{16{,}777{,}206}{16{,}777{,}206}\right)\right] = 27 \times 10^{6} \times 250 = 6.75 \times 10^{9}$$

$$f_{DEV,Final} = \left[\frac{\left(RAMPX\_INC_{Final} \times REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX\_STOP\right)}{\left(VCO_{Freq,Final} \times DEN_{Final}\right)}\right] \quad (16)$$

$$f_{DEV,Final} = \left[\frac{\left(23302 \times 27 \times 10^{6} \times 2 \times 100 \times 2 \times 225\right)}{\left(6.75 \times 10^{9} \times 16{,}777{,}206\right)}\right] = 0.5$$

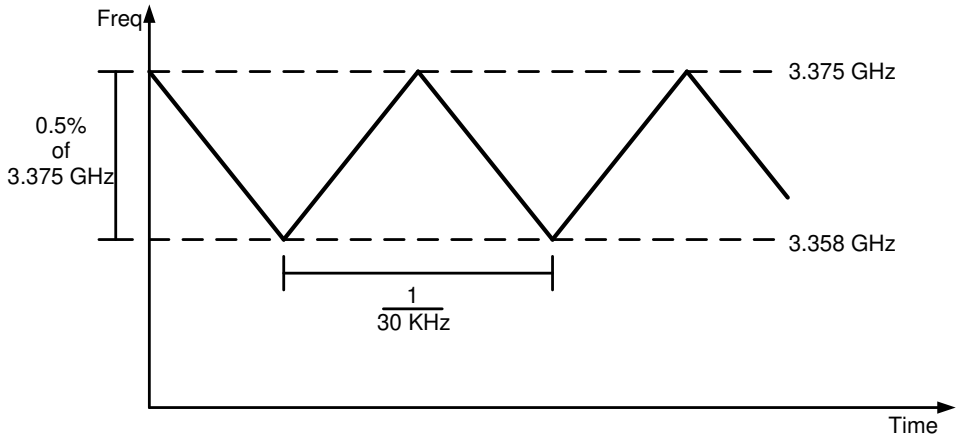


Figure 7-4. Down Spread SSCG Example

7.3.3 Back Channel Data Transfer

The back channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as BCC (Bidirectional Control Channel) frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel frame consists of 30 bits which contain the I^2C, CRC and four bits of standard GPIO information with a 168.75 Mbps line rate (when paired with an FPD-Link IV deserializer).

7.3.4 Video Processor

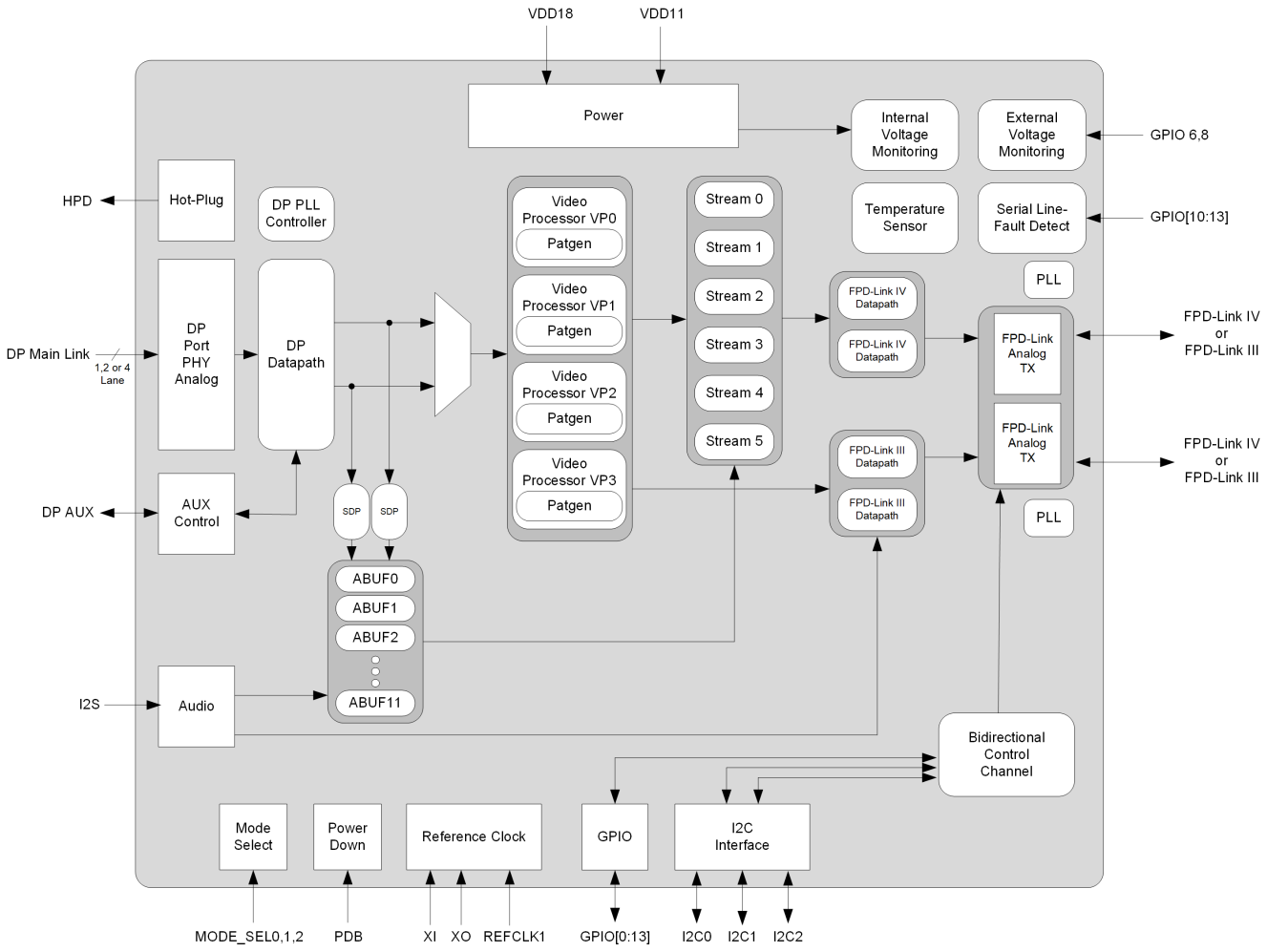


Figure 7-5. Video Processor Block Diagram

The DS90UB983-Q1 contains video processors (VP) to process the input video frames before sending the video across the link. There are four video processors allowing for four different video streams to be sent across the FPD-Link. Each of the video processors can modify and send out only one video stream each. The video processors need to store each active pixel of a single horizontal line of the video the video processor is sending out. The pixel storage for each video processor must be set in the NUM_VID_STREAMS (0x43[2:0]) register. The video processor regenerates the timing of the video being processed. The input videos to the video processors come from the DisplayPort. Each video processors input can be selected independent of each other and more than one video proccessor can share inputs. The video processors can take in SuperFrames and convert the multi image frame into a single image to send across FPD-Link. The video processors can use the following tools to modify the video:

- Vertical Filtering
- Video Cropping
- Timing Generation
- Alternate Pixel Splitting
- Merge

The video processor is where the pattern generator is located. This allows for up to four patterns to be generated and sent out.

7.3.4.1 Video Stream Buffers

The DS90UB983-Q1 supports 4 video streams with a total of 32k buffer. The DS90UB983-Q1 includes multiple video buffers for supporting the multi-stream capability. The serializer device has 4 video processors. Each of the video processors can be assigned to any of the video input streams. The video buffers are assigned to video processors based on the configured number of video streams supported.

In Table 7-3 depicts the video buffer assignments for an active pixels based on the number of the video processors are selected. The VP_CONFIG_REG can be used to control the memory allocation. The default value of NUM_VID_STREAMS bit field in register 0x43[2:0] set to two video processors with 16k each.

Table 7-3. Video Buffer Assignments

Enabled VPs	VP0 Size (pixels)	VP1 Size (pixels)	VP2 Size (pixels)	VP3 Size (pixels)
1	16384			
2	16384	16384		
3	16384	8192	8192	
4	8192	8192	8192	8192

7.3.4.2 Input Configuration

The video processor must first be enabled via the VP_ENABLE_REG register, and then the video stream of interest is selected via VP_SRC_SELECT bit of each video processor. Setting this bit to 0 selects Video Stream 0, and setting this bit to 1 selects Video Stream 1. If the DP port is operating in Single Stream Transport (SST) mode, Video Stream 0 must always be selected. The pixel width must also be specified as 18-bit, 24-bit or 30-bit. For MST applications, VP_SRC_SELECT controls whether the input to the video processer is MST0 or MST1.

Table 7-4. Input Selection Parameters

Enable Video Processor	Select Video Stream	Set Pixel Width
Enable: VPx_ENABLE = 1 Disable: VPx_ENABLE = 0	Video Stream 0: VP_SRC_SELECT = 0 Video Stream 1: VP_SRC_SELECT = 1	18-bit: VPx_WIDTH = 0 24-bit: VPx_WIDTH = 1 30-bit: VPx_WIDTH = 2

7.3.4.3 FPD-Link IV Stream Configuration

Each FPD-Link channel can transmit data from up to four video processors (VP0 to VP3). To forward the video stream from the video processor, the video stream must first be enabled via the LINK0_STREAM_EN register for FPD-Link Port 0 or the LINK1_STREAM_EN register for FPD-Link Port 1 (Page_11 indirect registers 0x01 and 0x11). The LINKx_STREAM_EN register is used to select which video streams are linked to each FPD-Link port. Once the video streams are linked to an FPD-Link port, the video streams must be mapped to the desired FPD-Link streams using the LINK0_MAP_REGx and LINK1_MAP_REGx registers (Page_11 registers 0x02, 0x03, 0x12 and 0x13). In Dual FPD-Link Mode, only LINK0_STREAM registers is used. Video streams can be mapped to multiple video processors to create duplicate copies of one image. In the independent mode, there are six FPD-Link streams available per FPD-Link port. Mapping of VPs and ABUFF are similar to the single/dual mode of operation. For FPD-Link III video stream mapping, see Section 7.3.24.1.1.

Table 7-5. Video Stream Forwarding

Video Processor	FPD-Link Port	Enable
VPx	FPD-Link Port 0	Enable: LINK0_STREAM_EN[x] = 1 Disable: LINK0_STREAM_EN[x] = 0
	FPD-Link Port 1	Enable: LINK1_STREAM_EN[x] = 1 Disable: LINK1_STREAM_EN[x] = 0

Table 7-6. Video Stream Mapping

Video Processor	FPD-Link Port	FPD-Link Stream
VPx	FPD-Link Port 0[1]	Stream 0: LINK0_STREAM_MAP0 = x Stream 1: LINK0_STREAM_MAP1 = x Stream 2: LINK0_STREAM_MAP2 = x Stream 3: LINK0_STREAM_MAP3 = x Stream 4: LINK0_STREAM_MAP4 = x Stream 5: LINK0_STREAM_MAP5 = x
	FPD-Link Port 1[1]	Stream 0: LINK1_STREAM_MAP0 = x Stream 1: LINK1_STREAM_MAP1 = x Stream 2: LINK1_STREAM_MAP2 = x Stream 3: LINK1_STREAM_MAP3 = x Stream 4: LINK1_STREAM_MAP4 = x Stream 5: LINK1_STREAM_MAP5 = x

(1) Each of the four video processors can be mapped to only a single FPD-Link stream, meaning a maximum of four video streams can transmitted by the FPD-Link IV serializer.

Table 7-7. Stream Mapping Input

Stream Map	Stream's Input
LINK0_STREAM_MAPx	0x0 = Video Processor 0
	0x1 = Video Processor 1
	0x2 = Video Processor 2
	0x3 = Video Processor 3

7.3.4.4 Timing Generation

To properly regenerate the video timing, the video processor must be programmed for the correct operating frequency and video parameters. The timing generator runs on a fixed frequency clock and typically inserts or removes pixels prior to the horizontal sync pulse if required. Timing is based on a quad-pixel clock, so pixels are inserted or removed as quad-pixels. The clock generator includes an adaption capability to allow operating slightly faster or slower to minimize the need for correction to blanking intervals. The following parameters must be set for proper timing generation for each video processor via registers on Page_12: VID_H_ACTIVE, VID_H_BACK, VID_H_WIDTH, VID_H_TOTAL, VID_V_ACTIVE, VID_V_BACK, VID_V_WIDTH, and VID_V_FRONT. For HSYNC width, there is a minimum requirement for the video processor of 12 pixels and 8 pixels in FPD-Link IV and FPD-Link III respectively. The total horizontal blanking has a recommended minimum of 100 pixels. The processor computes the horizontal front porch timing from the other horizontal parameters. Video timing parameter requirements are listed in Timing Generation Parameters. Vertical blanking parameters must match the vertical blanking of the SuperFrame after vertical filtering and cropping.

To allow video timing to stabilize, the timing generator can be programmed to drop initial video frames. By default, the timing generator discards the first frame (which can be a partial frame), and can discard up to three frames by programming the VP_DROP_FRAMES field. If the first video line of the subsequent frame is not available at the end of vertical blanking, the timing generator can be programmed either to wait for the video line (default) or to insert additional horizontal sync pulses until the next line arrives.

Timing Generation Parameters

Register Name	Timing Parameter Name	Description	Requirements	Equation
VID_H_ACTIVE	Horizontal Active	The total active horizontal period in number of pixels.		VID_H_ACTIVE = CROP_STOP_X - CROP_START_X + 1
H_ACTIVE_SHADOW	Horizontal Active	The total active horizontal period in number of pixels.		SOURCE_H_ACTIVE = VID_H_ACTIVE
VID_H_BACK	Horizontal Back Porch	The horizontal back porch in number of pixels.	Must be divisible by 4	VID_H_BACK = Desired Horizontal Back Porch

Timing Generation Parameters (continued)

Register Name	Timing Parameter Name	Description	Requirements	Equation
VID_H_WIDTH	Horizontal Sync	The width of the horizontal sync in number of pixels.	• Must be divisible by 4 • For FPD-Link IV must be at least 12 pixels • For FPD-Link III must be at least 8 pixels	VID_H_WIDTH = Desired Horizontal Sync
VID_H_TOTAL	Horizontal Total	The total horizontal width in number of pixels, including the active period, front porch, back porch, and horizontal sync.	Must be divisible by 4	VID_H_TOTAL= VID_H_ACTIVE + VID_H_BACK + VID_H_WIDTH + Desired Horizontal Front Porch
VID_V_ACTIVE	Vertical Active	The total active vertical period in number of lines.		VID_V_ACTIVE = CROP_STOP_Y - CROP_START_Y + 1
V_ACTIVE_SHADOW	Vertical Active	The total active vertical period in number of lines.		SOURCE_V_ACTIVE = VID_V_ACTIVE
VID_V_BACK	Vertical Back Porch	The vertical back porch in number of lines		VID_V_BACK = Original Image Vertical Back Porch x A/N + CROP_START_Y
VID_V_FRONT	Vertical Front Porch	The vertical front porch in number of lines.		VID_V_FRONT = Original Image Vertical Front Porch x A/N + Original Image Active Vertical - CROP_STOP_Y -1
VID_V_WIDTH	Vertical Sync	The width of the vertical sync in number of lines.		VID_V_WIDTH = Original Image Vertical Sync x A/N

7.3.4.4.1 Video Processor Frequency

The maximum PCLK for each video processor is 1080 MHz. In FPD-Link IV mode the video processor operates based on a quad-pixel clock generated based on the forword channel rate divided by 40. An M/N divider is programmed to generate the desired quad-pixel clock. For example, when the FPD-Link IV forward channel is configured for 6.75 Gbps, the reference clock is 6.75 Gbps / 40 bits = 168.75 MHz. The video processor clock operates on a quad-pixel basis so that M/N divider must be programmed to 1/4 of the video stream's pixel clock frequency by setting PCLK_GEN_M and PCLK_GEN_N on Page 12, the video processor register page. PCLK_GEN_M is a 15-bit value, controlling the numerator, while the denominator N is equal to 2^PCLK_GEN_N. PCLK_GEN_N value can range from 0 to 15, allowing a denominator of up to 32,768. Typically, N must be set to 32,768. For example, to create a 150 MHz pixel clock requires a quad-pixel clock of 37.5 MHz. If PCLK_GEN_N is set to the default of 15, PCLK_GEN_M =37.5 * (2^15) / 270 = 4551.111. Choosing an M value of 4551, this produces an effective PCLK of 149.996 MHz, an offset of 31 ppm from the target PCLK.

Video Processor Clock = Target PCLK / 4 (17)

Video Processor Clock = (FC data rate / 40) × PCLK_GEN_M / (2^PCLK_GEN_N) (18)

PCLK_GEN_M = Video Processor Clock × (2^PCLK_GEN_N) / (FC data rate / 40) (19)

If using down spread spectrum the bandwidth of the forward channel data rate is reduced and must be taken into account when calculating the PCLK_GEN_M and PCLK_GEN_N values.

7.3.4.4.2 Blanking Adjustments for Frequency Offset

Since the DS90UB983-Q1 generates timing from a local reference clock, there is the potential for a frequency offset between the actual video stream rate and the regenerated timing. The timing generator uses horizontal sync timing from the input to control regeneration and also uses this to check that the timing is correct. If the incoming horizontal timing is early relative to the generated timing, the generator drops pixels prior to generating the horizontal sync timing pulse.

If the incoming horizontal timing is late relative to the generated timing, the generator adds pixels prior to generating the horizontal sync timing pulse. Since the timing generator operates in four-pixel increments, four pixels are added or removed from the horizontal front porch to correct the offset as needed. This adds some jitter to the horizontal blanking.

Timing corrections are only made during active periods of video. During vertical blanking, an offset in timing can accumulate to the extent that larger compensation is required at the first active line. If there is accumulated error and the regenerated clock is fast (early), extra pixels are inserted to delay the start of the first active line. This delay is the total accumulated difference. A register control (RESYNC_1ST_LINE (0x01[7], 0x41[7], 0x81[7], and 0xC1[7]) on Page_12) allows inserting a single four-pixel delay per video line until the difference is corrected.

If there is accumulated error and the regenerated clock is slow (late), blanking pixels are removed to delay the start of the first active line. Four pixels are removed prior to the first active line, and for each subsequent active line until the accumulated difference is corrected. During active video, the timing generator continues to monitor horizontal sync timing and make corrections of four pixels per line as needed to maintain accurate timing. Since the maximum correction is four pixels per line, the programmed frequency must be accurate within four pixels per line for the timing generator to maintain proper timing.

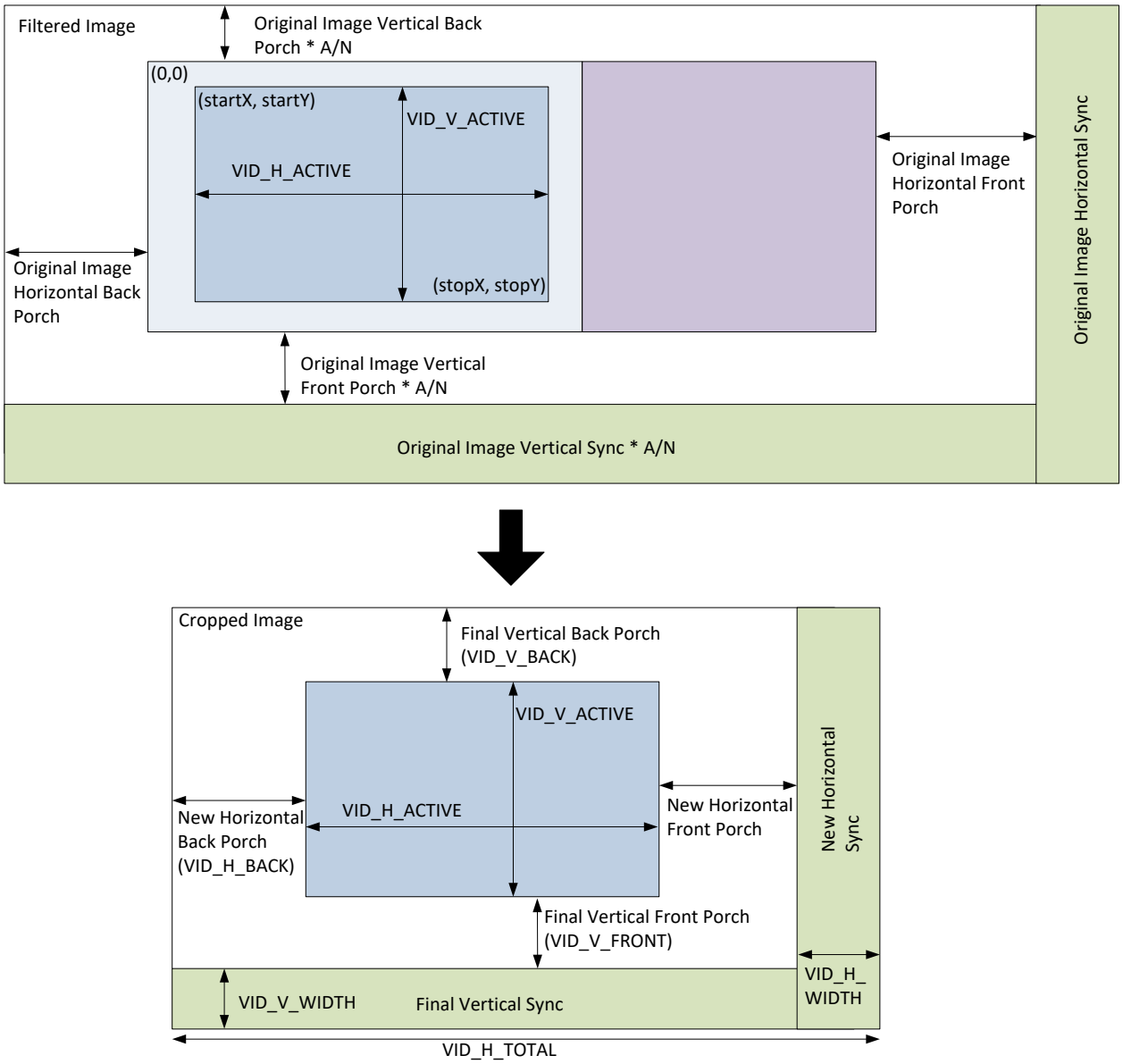


Figure 7-6. Video Cropping and Video Parameters

7.3.4.5 SuperFrame (Multi-Image Frame) Capabilities

The DS90UB983-Q1 supports multi-image frames on each DisplayPort video stream. The support for multi-image frames allows the pixels targeted at different displays to be combined into one frame. Up to four images are supported per frame. These multi-image frames are processed by four video processors, in which each video processor selects a single image (portion of the frame) to be forwarded and generates the timing for the selected image. As there are only four video processors, the total number of images included on the DisplayPort inputs must be 4 or less. As each video processor is independent, forwarded images can be identical or overlapping if desired. The video processors process the multi-image frame splitting in these steps:

1. Input Configuration: Enable video processor, map video stream input to the video processor and set the pixel width.
2. Vertical Filter: Select which lines of the images are forwarded
3. Video Cropping: Crop vertically filtered image to select desired portion of the image to forward
4. Timing Generation: Generate pixel clock and timing for the final image

The video processors process the multi-image frame aggregation in these steps:

1. Input Configuration: Enable video processor, map video stream to the video processor output and set the pixel width.
2. Vertical Filter: Select which lines of the images are forwarded
3. Timing Generation: Generate pixel clock and timing for the final image
4. Merge output of video processor to support aggregation of dual DisplayPort input into an alternating pixel format or left/right format

7.3.4.6 Dual MST with Daisy-chain

In Figure 7-7 depicts the use case of daisy-chain using multiple streams with two similar or different resolution or image video input. The DS90UB983-Q1 takes two video streams in MST mode, where stream 0 contains two synchronous images in SuperFrame format, and stream 1 contains a single image. In MST mode, merging two incoming MSTs video into a single video processor is not supported since the minimum skew requirement is 8 pixels. The DS90UB983-Q1 video processors can be programmed to perform vertical filtering, video cropping, and timing regeneration before forwarding each resultant image to the deserializer devices in the daisy-chain. Each deserializer can extract one (or two) video streams to its desired local display output or it can forward the video streams on the next deserializer in the chain based on register configuration.

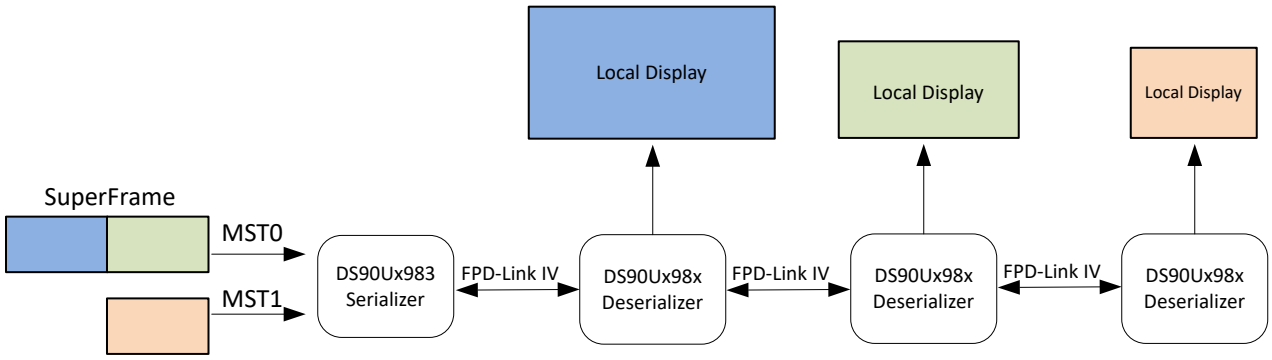


Figure 7-7. Dual MST with Daisy-chain

7.3.4.7 Vertical Filter

The vertical line selects which lines of a given video stream are forwarded. This is done based on the ratio A/N where A is the number of lines forwarded for every N lines of the multi-image frame. The vertical filter ratio values for A and N can be any number from 1 to 63. For proper operation, the number of lines in the multi-image frame must be a multiple of N. The images can be padded to the proper dimensions with additional vertical lines as these can be filtered out in the video cropping step. No horizontal adjustments are performed as part of the vertical filtering. The values for A and N are set via the VFILTER_A and VFILTER_N registers for each video processor on Page_12. The vertical filter applies to both active lines and vertical blanking.

Example: For an A/N image where A=2 and N=3, the multi-image frame has 1.5 times as many lines as the resultant image. The video processor forwards the first two lines and drops the third. The video processor then forwards Lines 4 and 5 and drop the sixth. The vertical filter continues until the last line is reached.

The Vertical Active Input, Vertical Blanking Input and Vertical Total Input must each be divisible by N. The following Equations must be met for the Input parameters;

- Integer number = (Vertical Active Input) / N
- Integer number = (Vertical Blanking Input) / N
- Integer number = (Vertical Total Input) / N

The Vertical Back Porch, Vertical Front Porch, and Vertical Sync are recommended to each be divisible by N as well. In some cases, the Vertical Blanking Total can be too small to support each vertical blanking parameter being divisible by N. In these cases, the Vertical Blanking parameters must be selected using the following equations:

- Vertical Blanking Total Input/N = k where k must be an integer

- Round(VFP_Input * A/N) + Round(VBP_Input * A/N) + Round(VS_Input * A/N) = Vertical Blanking Total Input * A/N
- Vertical Blanking Total Output = (Vertical Blanking Total Input + Number of Lines Cropped) * A/N
- Vertical Blanking Total Output = VFP_output + VBP_output + VS_output where VFP_output, VBP_ouput, and VS_output can be selected as any integer value meeting this equation (e.g. the output value is not required to equal Round(Vertical Blanking parameter*A/N).

Example of correct blanking:

- A/N =5/6
- Vertical Blanking Total input = 6
- VFP_Input = 1, VBP_Input = 1, VS_Input = 4
- Round(VFP_Input * A/N) + Round(VBP_Input * A/N) + Round(VS_Input * A/N) = Vertical Blanking Total Input * A/N
- Round(1 * 5/6) + Round(1 * 5/6) + Round(4 * 5/6) = 6 * 5/6
- Round(0.833) + Round(0.833) + Round(3.333) = 5
- 1 + 1 + 3 = 5
- VFP_output = 1, VBP_output = 1, VS_output =3

Example of incorrect blanking:

- A/N =5/6
- Vertical Blanking Total input = 6
- VFP_Input = 1, VBP_Input = 2, VS_Input = 3
- Round(VFP_Input * A/N) + Round(VBP_Input * A/N) + Round(VS_Input * A/N) = Vertical Blanking Total Input * A/N
- Round(1 * 5/6) + Round(2 * 5/6) + Round(3 * 5/6) = 6 * 5/6
- Round(0.833) + Round(1.666) + Round(2.5) = 5
- 1 + 2 + 3 ≠ 5

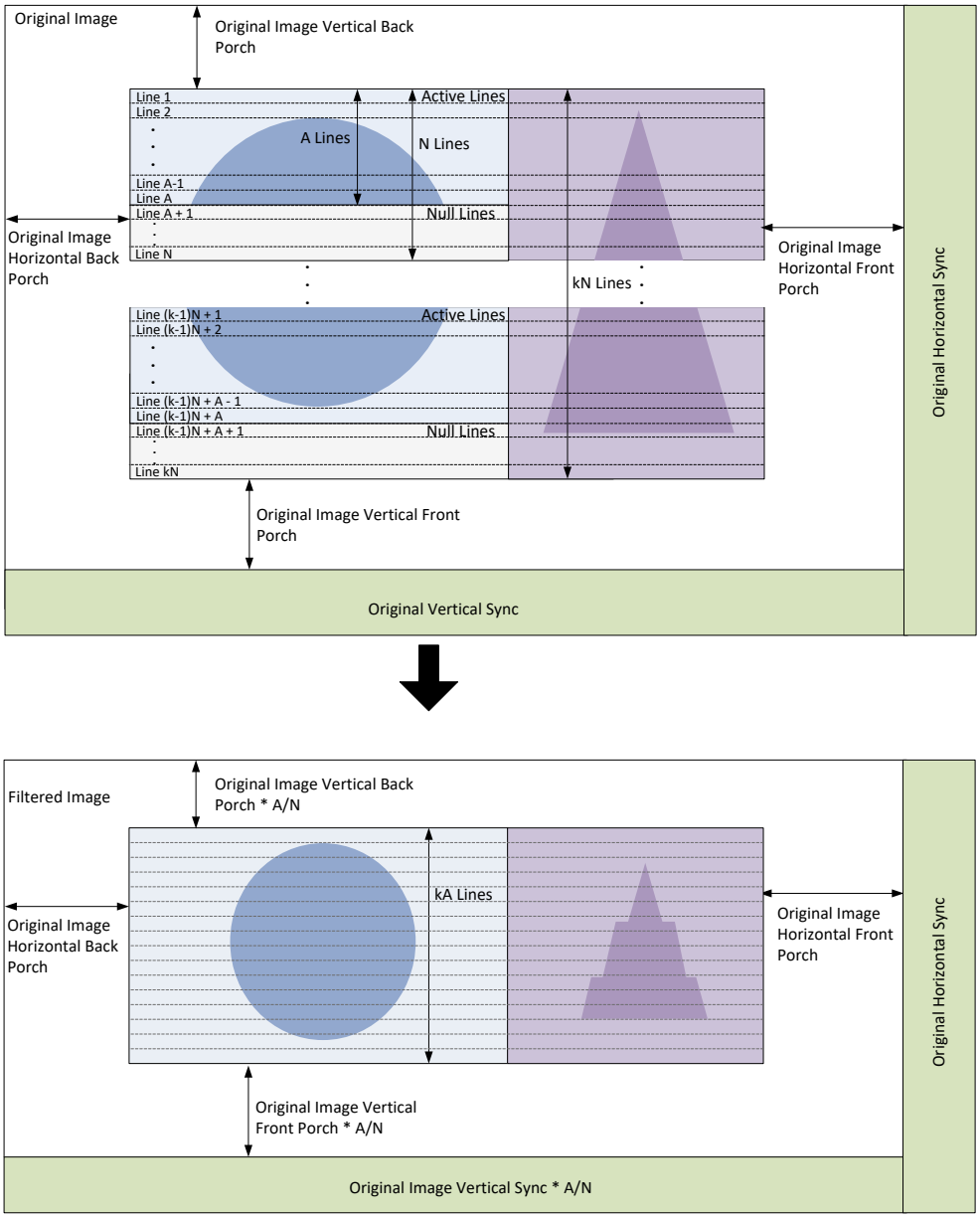


Figure 7-8. Video Filtering

To prevent overflow conditions the following requirements must be satisfied.

- Filtering Ratio = A -((A-1)*A/N)
- Filtering Ratio < 7
- VP Buffer Size > (Filtering Ratio * Horizontal Active)

7.3.4.8 Video Cropping

The video cropping step takes the vertically filtered image and crops image vertically and horizontally. The start and stop positions are measured in pixels based on the filtered image, not the original video frame. Valid positions are 0 to Line Length -1 for horizontal positions and from 0 to Number of Active Lines -1 for vertical positions. Pixels before the start position and after the stop position are not forwarded and replaced with blanking. Any vertical cropping results in additional vertical blanking in the final image. Cropping registers are set for each video processor on Page_12. The horizontal start position is set via CROP_START_X0_VP0 and CROP_START_X1_VPx and the horizontal stop

position is set via CROP_STOP_X0_VPx and CROP_STOP_X1_VPx. The vertical start position is set via CROP_START_Y0_VPx and CROP_START_Y1_VPx and the vertical stop position is set via CROP_STOP_Y0_VPx and CROP_STOP_Y1_VPx. When cropping the second image, the origin of the new image starts at (0,0), not at the CROP_STOP values assigned to the first image.

Table 7-8. Video Cropping Parameters

Enable Cropping	Set X Start Position	Set Y Start Position	Set X Stop Position	Set Y Stop Position
VP_EN_CROP = 1	CROP_START_X[7:0]: 8 LSB of horizontal start position in pixels CROP_START_X[15:8]: 8 MSB of horizontal start position in pixels	CROP_START_Y[7:0]: 8 LSB of vertical start position using the line number CROP_START_Y15:8]: 8 MSB of vertical start position using the line number	CROP_STOP_X[7:0]: 8 LSB of horizontal stop position in pixels CROP_STOP_X[15:8]: 8 MSB of horizontal stop position in pixels	CROP_START_Y[7:0]: 8 LSB of vertical stop position using the line number CROP_START_Y15:8]: 8 MSB of vertical stop position using the line number

7.3.4.9 Video Processor Merge

Two video processors' output can be merged together to make a large image. The two videos that are being merged are required to be the same resolution and blanking. VP0 and VP1 can be combined, VP2 and VP3 can be combined. The video processors can merge images in 2 formats: "Odd/Even Merge" and "Left Right Merge." If VP0 and VP1 are merged, then select VP0 in the LINKx_STREAM_MAPx to output the merged image. If VP2 and VP3 are merged, then select VP2 in the LINKx_STREAM_MAPx to output the merged image. To properly merge the input videos the two input video streams must have a skew of less than 8 pixels.

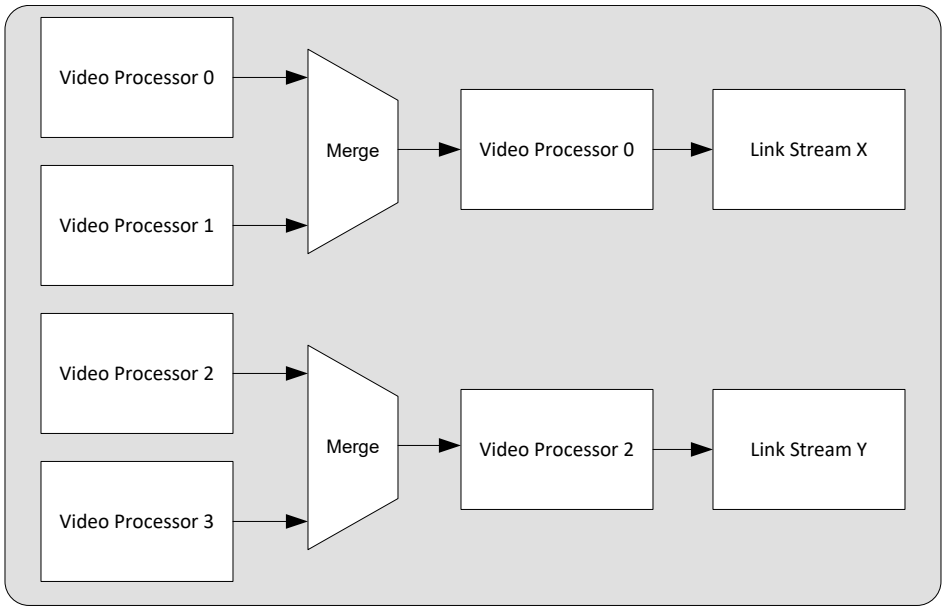


Figure 7-9. Video Processor Merge Block

7.3.4.9.1 Left Right Merge

Left right merge merges two input images using one of the input images as the left side of the final image and the other image as the right side of the final image. To set the video processors to use left right merge set the register VP_DUAL_MERGE_LR_EN to 1 in both of the video processors that are being merged. For the VP0 and VP1 merge, the left image is always in VP0, the right image is always in VP1. For the VP2 and VP3 merge, the left image is always in VP2, and the right image is always in VP3. The Left and Right input video timings must be the same for all video timing parameters. Use the following table to select the proper video timing for the input video and timing for the video processor.

Table 7-9. Left Right Merge Timing Parameters

	Input Video Source 0 and 1	VP0 or VP2 Timing	VP1 or VP3 Timing	Output Timing
Total Horizontal	(Target H Total)/2	Target H Total	Target H Total	Target H Total

Table 7-9. Left Right Merge Timing Parameters (continued)

	Input Video Source 0 and 1	VP0 or VP2 Timing	VP1 or VP3 Timing	Output Timing
Vertical Total	Target V Total	Target V Total	Target V Total	Target V Total
Horizontal Active	(Target H Active)/2	Target H Active	Target H Active	Target H Active
Vertical Active	Target V Active	Target V Active	Target V Active	Target V Active
Horizontal Blanking	(Target H Blanking)/2	Target H Blanking	Target H Blanking	Target H Blanking
Vertical Blanking	Target V Blanking	Target V Blanking	Target V Blanking	Target V Blanking
PCLK	(Target PCLK)/2	Target PCLK	Target PCLK	Target PCLK

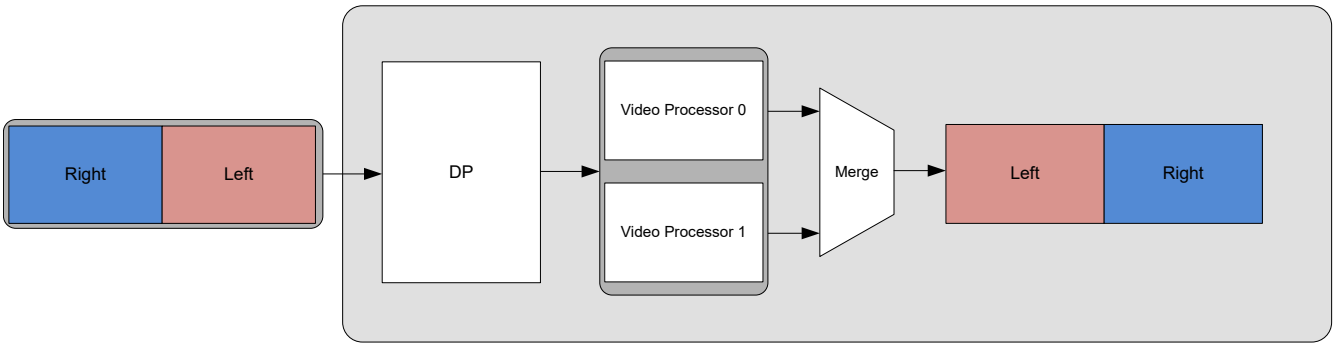


Figure 7-10. Left Right Merge

7.3.4.9.2 Alternating Pixel Merge

Alternating pixel merge merges two input images using one of the input images as the odd (first) horizontal pixels of the output and one image as the even (second) horizontal pixels of the output image. To set the video processors to use alternating pixel merge set the register VP_DUAL_MERGE_ALT_EN to 1 in both of the Video Processors that are being merged. For the VP0 and VP1 merge, the odd image is input to VP0; the even image is input to VP1. For the VP2 and VP3 merge, the odd image is input to VP2; the even image is input to VP3. The odd and even input video timings must be the same for all video timing parameters. Use the following table to select the proper video timing for the input video and timing for the video processor.

Table 7-10. Alternating Pixel Merge Timing Parameters

	Input Video Source 0 and 1	VP0 or VP2 Timing	VP1 or VP3 Timing	Output Timing
Total Horizontal	(Target H Total)/2	(Target H Total)/2	(Target H Total)/2	Target H Total
Vertical Total	Target V Total	Target V Total	Target V Total	Target V Total
Horizontal Active	(Target H Active)/2	(Target H Active)/2	(Target H Active)/2	Target H Active
Vertical Active	Target V Active	Target V Active	Target V Active	Target V Active
Horizontal Blanking	(Target H Blanking)/2	(Target H Blanking)/2	(Target H Blanking)/2	Target H Blanking
Vertical Blanking	Target V Blanking	Target V Blanking	Target V Blanking	Target V Blanking
PCLK	(Target PCLK)/2	Target PCLK	Target PCLK	Target PCLK

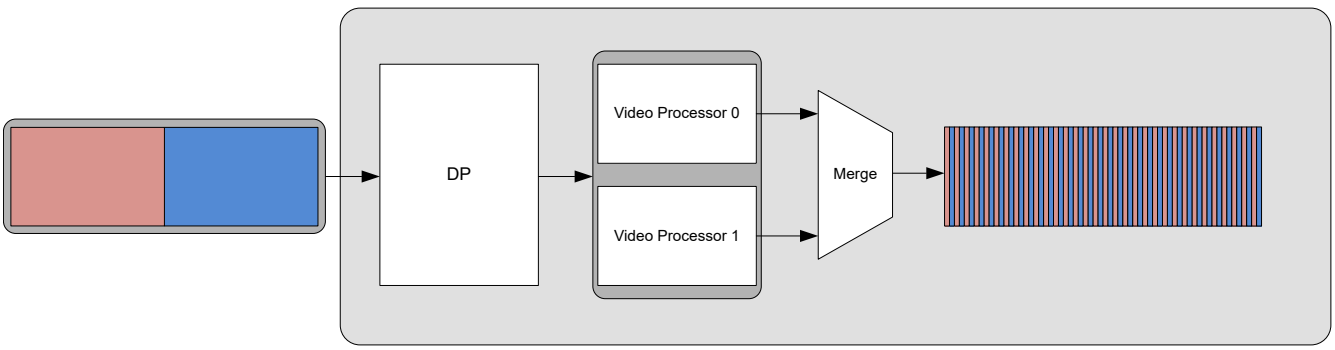


Figure 7-11. Alternating Pixel Merge

7.3.4.9.3 Merged Image Processing

In addition to being mapped directly to an FPD-Link stream the merged stream can also be mapped to the input of the other two video processors. The merged stream can be set as the input to the other two video processors by setting the VP2VP_EN register. This allows merged images to be cropped or filtered before being sent out on the FPD-Link.

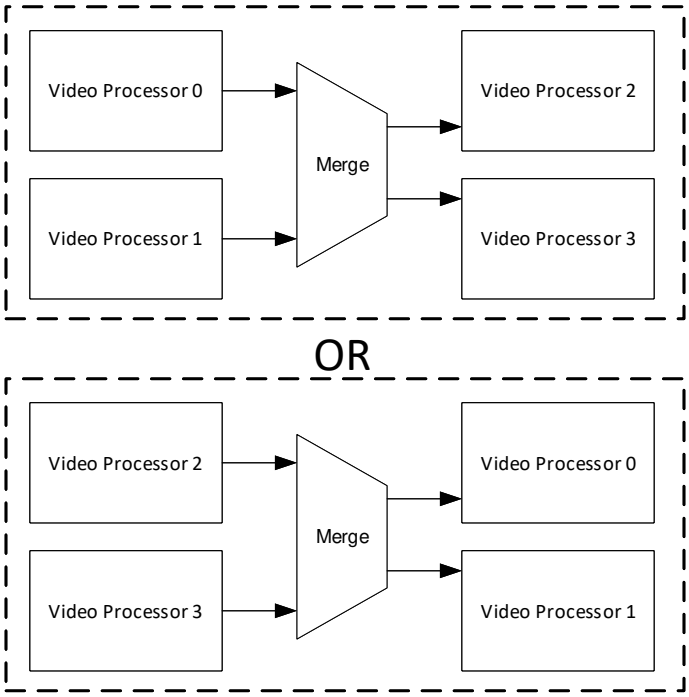


Figure 7-12. Merged Image Forwarding

7.3.5 Dual Serializers Synchronization and Splitting

In Figure 7-13 depicts dual serializers and dual deserializers synchronization configuration. Refer to deserializer datasheet for additional information. The DS90UB983-Q1 is capable of supporting two serializers and two deserializers synchronization configuration using alternate pixel mode. The configuration allows support for higher resolution beyond 8k by stitching four images together to form one large widescreen panorama. In this mode, certain restrictions apply:

Dual serializers synchronization constraints:

- Two serializers must be placed on the same board.
- Two serializers must share a common reference clock.
- Two deserializers must share a common reference clock.
- Two serializers must connect GPIO9 and REFCLK1 pins between two serializers.
- Two deserializers must connect SYNC0 and SYNC1 pins between two deserializers.
- Input images from SoC to the serializers must be synchronized.
- The two input streams from the video source must always track within 50 pixels over the complete frame including any spread spectrum.
- Streams should be synchronized between deserializer outputs within 100 pixels
- All cable lengths are the same.
- The four images are identical resolutions.
- The same SSCG is present on all serializer FPD-Link interfaces.

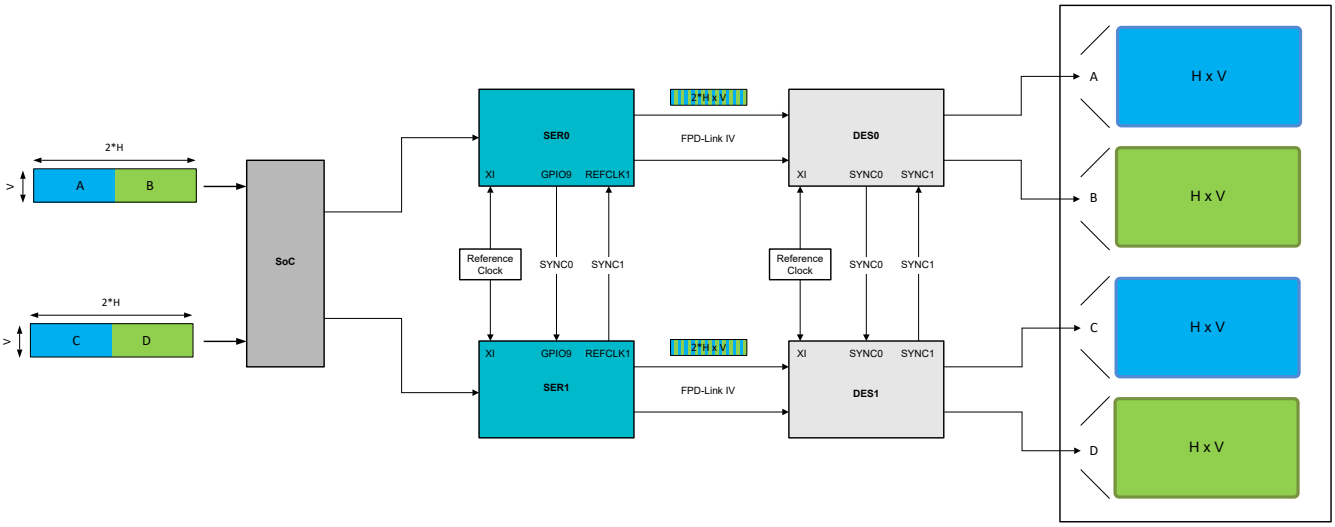


Figure 7-13. Dual Serializer Dual Deserializer Synchronization

7.3.6 FPD-Link Port Register Access

Since the DS90UB983-Q1 contains two downstream ports, some registers are duplicated to allow control and monitoring of the two ports. To facilitate this, the PORT_SEL (0x2D) register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) are available independent of the settings in the TX_PORT_SEL register.

Setting the TX_READ_PORT bit allows reading registers of the selected port. Writes occur to any port for which the TX_WRITE_PORT_x select bit is set, allowing simultaneous writes to both ports if both write bits are set.

7.3.7 FPD-Link Port Polarity Swap

The DS90UB983-Q1 supports inverting the polarity of the positive and negative pins of the FPD-Link ports. The following script can be used to swap the polarity of the pins in FPD-Link IV mode:

```
## ********************************************
## Invert P and N signal for PORT0 and PORT1 in FPD4
## ********************************************
board.WriteI2C(devAddr,0x40,0x04); #Page 1
###Lane 0 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x00)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x01)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x02)
board.WriteI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x08)
reg_value0 = board.ReadI2C(devAddr,0x42)
board.WriteI2C(devAddr,0x42,reg_value0 | 0x80)

###Lane 1 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x20)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x21)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x22)
board.WriteI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x28)
reg_value1 = board.ReadI2C(devAddr,0x42)
board.WriteI2C(devAddr,0x42,reg_value1 | 0x80)
```

The following script can be used to swap the polarity of the pins in FPD-Link III mode:

```
## ******************************************
## Invert P and N signal for PORT0 and PORT1 in FPD3## ******************************************
board.WriteI2C(devAddr,0x40,0x04); #Page 1
###Lane 0 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x00)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x01)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x02)
board.WriteI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x08)
reg_value0 = board.ReadI2C(devAddr,0x42)
board.WriteI2C(devAddr,0x42,reg_value0 | 0x80)

###Lane 1 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x20)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x21)
board.WriteI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x22)
board.WriteI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x28)
reg_value1 = board.ReadI2C(devAddr,0x42)
board.WriteI2C(devAddr,0x42,reg_value1 | 0x80)
```

7.3.8 Power Down (PDB)

The serializer has a PDB input pin to enable or power down the device. This pin can be controlled by an external device or through VDD18, where VDD18 = 1.71 V to 1.89 V. Make sure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, make sure that the pin is driven to 0 V for at least 2 ms before releasing or driving high. In the case where PDB is pulled up to VDD18 directly, a 10-kΩ pull-up resistor and a >10 µF capacitor to ground are required (See Section 9.1).

Toggling PDB low powers down the device and resets all control registers to default. During this time, PDB must be held low for a minimum of 2 ms before going high again.

7.3.9 Internal ADC

The serializer device contains an 8-bit ADC that is used for various functions including line fault detection, temperature sensing, internal voltage sensing and external voltage monitoring. This ADC is configured using indirect register Page_14 in the serializer devices. To enable the ADC set the ADC_MODE (0x0D[7] = 0) on Page_14). Refer to *Diagnostic Features of FPD-Link IV Devices* for more details implementation.

7.3.9.1 ADC Timing Control

The ADC can read the voltage of up to 11 different sources. These sources can be enabled or disabled in register 0x07 or 0x08 on Page_14. By default the ADC reads 5 voltage sources: the thermal sense element, and 4 internal supply voltages. The ADC samples a voltage source for a time period controlled by concatenating 4 bytes of 0x0F, 0x10, 0x11, and 0x11 register to represent the "ADC_SRC_CNTR_x[31:0]". To calculate the frequency at which the ADC updates each voltage source in their register, use the following formula:

$$VOL\_SRC\_FREQ = \frac{25MHz}{\left[ADC\_CLK\_VAL \times SRC\_CNT\_VAL \times \left(\#\_VOL\_SRC\_EN\right)\right]} \quad (20)$$

For example, if "ADC_CTRL_CLK_DIV (0x04[5:4])" is set to 2 and "SRC_CNT_VAL (0x0F,0x10,0x11,0x12)" is set to 13000 and there are 5 voltage sources enabled, then the ADC updates each voltage source at a frequency of 192.3 Hz.

$$192.3Hz = \frac{25MHz}{\left[2 \times 13000 \times (5)\right]} \tag{21}$$

7.3.9.2 Temperature Sensing

The DS90UB983-Q1 uses the ADC and a thermal sense element to measure the junction temperature of the DS90UB983-Q1. The junction temperature is periodically read and stored in the TEMP_FINAL (0x13) register on the ADC control register Page_14. The formula to convert the TEMP_FINAL to Celsius is below. The TEMP_FINAL has a resolution of 2°C.

$$Temperature = (2 \times TEMP\_FINAL) - 273 \tag{22}$$

The DS90UB983-Q1 can also trigger an interrupt when the junction temperature exceeds the value of the TEMP_HIGH (0x33) register or falls below the TEMP_LOW (0x34) register on Page_14. To enable this interrupts status to be displayed on the INTB pin, set bit 3 of the INTERRUPT_CTL (0x51) register on the main page to 1. By default, this interrupt is triggered when internal junction temperatures exceed 140 °C or below -20 degrees C. These thresholds can be changed by writing to the TEMP_HIGH or TEMP_LOW register. The formula to convert between the temperature and the register value is the same as above Equation 22. For more detailed registers setting refer to *Diagnostic Features of FPD-Link IV Devices*.

7.3.9.3 Internal Supply Monitoring

The serializer device uses the ADC to monitor the voltage levels of the 1.8V and 1.15V voltage supplies of the device. The ADC can read the voltages of four different pins of the device. Voltage Sensing below shows the register and pin locations for the four ADC voltage readings. The voltage sensors have a resolution of 2.5% for 1.15V and 1.8V.

For details information on registers setting refer to Page_14 Registers

Table 7-11. Voltage Sensing

Voltage Pin being read	Nominal Voltage	Register name (Address)	Register address (on page_14)	CF (correction factor)
VDD18_FPD pin	1.8V	IV0_FINAL	0x15	3.045
VDD18 pin	1.8V	IV1_FINAL	0x16	3.082
VDD11_P pin	1.15V	IV2_FINAL	0x17	1.844
VDD11_L pin	1.15V	IV3_FINAL	0x18	1.886

- Voltage equation for voltage sense

$$Pin\_Voltage = CF * (1 / 255)* 1.207 * IVx\_FINAL \quad (23)$$

The serializer device can also trigger an interrupt when the voltage supply goes above or below specific voltages. To display this interrupt's status on the INTB pin, set the INTERRUPT_CTL[3] (0x51) register on the main page to 1. The voltage threshold values in Table 7-12 below, are the recommended voltage values and they are +/- 5% of the Nominal Voltage. The upper or lower voltage thresholds can be changed by changing the values of the IVX_HIGH and IVX_LOW registers in the table below:

Table 7-12. Upper Thresholds for Supply Voltages

Supply Pin	Upper Threshold Voltage Register Name	Upper Threshold Voltage Register Offset Address	Upper Threshold Voltage +5% Nominal Voltage (V)	Default Upper Threshold Voltage (V)
VDD18_FPD pin	IV0_HIGH	0x39	1.8881	1.9313
VDD18	IV1_HIGH	0x3C	1.8822	1.9551
VDD11_P	IV2_HIGH	0x3F	1.2045	1.1696
VDD11_L	IV3_HIGH	0x42	1.2048	1.1959

Table 7-13. Lower Thresholds for Supply Voltages

Supply Pin	Lower Threshold Voltage Register Name	Lower Voltage Threshold Register Offset Address	Lower Threshold Voltage -5% Nominal Voltage (V)	Default Lower Threshold Voltage (V)
VDD18_FPD pin	IV0_LOW	0x3A	1.7007	1.7580
VDD18	IV1_LOW	0x3D	1.7071	1.7800
VDD11_P	IV2_LOW	0x40	1.0910	1.0648
VDD11_L	IV3_LOW	0x43	1.0888	1.0888

7.3.9.4 External Voltage Sensing

The ADC on the device can read and monitor the voltages of the GPIO6 and GPIO8 pins. The pins can read voltages from 0.4V to 1.207V. If a higher voltage is to be read, an external voltage divider is required. In order to read the voltage at the GPIO you must enable EXT_VOL0 (0x08[0]) for GPIO6 and EXT_VOL1 (0x08[1]) for GPIO8 on Page_14. Disable the 25KΩ pull down on GPIO6 set REG_GPIO_EN_PULL_LOW_1 (0xC9[6]) on Page_9 to 0. Disable the 25KΩ pull down on GPIO8 set REG_GPIO_EN_PULL_LOW_8 (0xCA[0]) on Page_9 to 0. The ADC voltage can be read in EXT_VOL0_FINAL (0x1B) for GPIO6 and EXT_VOL1_FINAL (0x1C) for GPIO8. The formula to convert the ADC reading to the voltage is in the Equation below. Refer to registers information in Page_14 Registers.

$$GPIOx\_Voltage = \left(\frac{1.207}{255}\right) \times EXT\_VOLx\_FINAL \quad (24)$$

The device can also trigger an interrupt when the voltages on GPIO6 and GPIO8 go above or below specific voltages. To display this interrupt's status on the INTB pin set the INTERRUPT_CTL[3] in (0x51) register on the main page to 1. The registers to set the upper and lower voltages is in the Table Below. To calculate the values for the upper and lower threshold use the above formula to convert from voltage to register value.

Table 7-14. Upper or Lower External Voltage Threshold

Description	Register Name	Register Address (Page_14)
GPIO6 Upper Threshold	EXT_VOL0_HIGH	0x4C
GPIO6 Lower Threshold	EXT_VOL0_LOW	0x4D
GPIO8 Upper Threshold	EXT_VOL1_HIGH	0x4F
GPIO8 Lower Threshold	EXT_VOL1_LOW	0x50

7.3.10 Serial Link Fault Detect

As part of the diagnostics features for the DS90UB983-Q1, the line fault detection circuitry can be used to detect faults with the connection between the serializer and deserializer. This is done by monitoring and sensing the voltage on the cable between the SerDes and transmitting that voltage to a GPIO on either the serializer or deserializer. Refer to the Line-Fault Detection Hardware Implementation section and apps note *Diagnostic Features of FPD-Link IV Devices*, SNLA322 for more details of hardware implementation.

7.3.11 Interrupt Pin (INTB)

The INTB pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions. The global interrupt must be enabled, as well as the individual interrupts of interest, via the INTERRUPT_CTL (0x51) register. The available interrupts are shown in Table 7-15. Video processor interrupts are enabled via the INTR_CTL_VP_VPx indirect access registers (Page_12 0x33, 0x73, 0xB3, and 0xF3). DP Receiver interrupts are enabled via INTR_CTL_DP_RX_PORT indirect access. FPD Transmitter Port interrupts are enabled via INTR_CTL_FPD4_PORTx indirect access registers (Page_9 0x8C, 0x9C), and Page_0 of FPD3_ICR (0xC6) and FPD3_ISR (0xC7). Interrupt statuses are available regardless of whether an interrupt is included in the overall interrupt, including when the corresponding bit in INTERRUPT_CTL is set to 0.

The general procedure for the FPD Transmitter interrupts to be monitored on the INTB pin configuration is as follows in FPD-Link III mode. If there is no active video on the SER input side, register 0x34[6] = 1 must be set on the FPD-Link III deserializer in order to establish LOCK.

1. FPD-Link IV SER - Enable REM_INT as part of the FPD-Link III Transmitter interrupt by setting in Main Page Reg 0xC6[5] = 1, 0xC6[0] = 1
2. FPD-Link IV SER - Enable Global INTB and FPD_TX Interrupts Main Page Reg 0x51[7] = 1, 0x51[1:0] = 0b11
3. Force FPD-Link III deserializer INTB_IN = L
4. Observe FPD-Link IV SER INTB = L
5. Force FPD-Link III deserializer INTB_IN = H
6. Observe FPD-Link IV SER INTB = L (INTB pin still low)
7. Read FPD-Link IV SER Main Page Register 0xC7 to clear interrupt
8. Observe FPD-Link IV SER INTB = H

Table 7-15. Interrupt Statuses

Status	Address	Description
Global Interrupt (GLOBAL_INT)	0x52[7]	Set when any of the enabled interrupts is set.
DP Receiver Interrupt (IS_DP_RX0)	0x52[4]	Set when any of the enabled DP interrupts is set. This interrupt will be cleared upon reading the 0x188 APB register or INTR_STS_DP_RX_PORT Page_9.

Table 7-15. Interrupt Statuses (continued)

Status	Address	Description
Device Interrupts (DEVICE_INT)	0x52[3]	Set when any of the temprature, voltage monitor, line-fault and ESD interrupts is set register 0x87[3:0] and 0x23 - 0x2F in Page_14 addresses for component interrupt status.
Back channel GPIO Interrupt (BC_GPIO_INT)	0x52[2]	Set when any of the back channel GPIO interrupt is set in the register status 0xA6[7:0] and 0xA7[5:0].
FPD Transmitter 1 Interrupt (IS_FPD_TX1)	0x52[1]	Set when any enabled FPD TX Port 1 interrupt is set.
FPD Transmitter 0 Interrupt (IS_FPD_TX0)	0x52[0]	Set when any enabled FPD TX Port 0 interrupt is set.

7.3.12 Remote Interrupt Pin (GPIO4 / REM_INTB)

GPIO4 / REM_INTB is configured as a GPIO pin by default. The remote interrupt function must be enabled manually after startup if required. At device startup this pin must be left floating or pulled to GND. The REM_INTB outputs the interrupt from the INTB_IN deserializer. In Independent mode, REM_INTB can be configured to mirror the INTB_IN signal from either the partnering deserializer connected to Port 0 or Port 1 of the serializer.

The general procedure for configuring the (GPIO4 / REM_INTB) interrupt in FPD-Link III or FPD-Link IV mode is shown in these steps.

1. FPD-Link IV SER - Enable REM_INT as part of the FPD-Link Transmitter interrupt by setting in Main Page Reg 0xC6[5] = 1, 0xC6[0] = 1
2. FPD-Link IV SER - Configure GPIO4 Output[1] and forward REM_INT by writing 0x1B = 0x88 for Port 0 or writing 0x1B = 0x98 for Port 1
3. FPD-Link IV SER - Enable Global INTB and FPD_TX Interrupts Main Page Reg 0x51[7] = 1, 0x51[1:0] = 0b11
4. Force DES INTB_IN = L
5. Observe FPD-Link IV SER REM_INTB = L
6. Force DES INTB_IN = H
7. Observe FPD-Link IV SER REM_INTB = H

7.3.13 Video Processor Interrupt

Video processor interrupts are enabled via the INTR_CTL_VP_VPx indirect access registers (Page_12 0x33, 0x73, 0xB3, and 0xF3). Video processor interrupt statuses can be read in the INTR_STS_VP_VPx indirect access registers (Page_12 0x31, 0x71, 0xB1, and 0xF1). Video processor interrupt statuses can be polled periodically to detect video processor interrupts or a GPIO can be set to output the VP interrupt status to be monitored by a MCU to detect a VP interrupt.

Table 7-16. Video Processor Interrupt Statuses

Status	Address	Description
Video Crop Vertical Error (IS_CROP_VERT_ERR)	INTR_STS_VP_VPx[6]	Indicates that the video frame does not have enough lines for programmed vertical cropping.
Video Crop Horizontal Error (IS_CROP_HOR_ERR)	INTR_STS_VP_VPx[5]	Indicates that the video frame does not have enough pixels in a line for the programmed horizontal cropping.
Timing Generation Data Available Error (IS_TIMING_DATA_ERR)	INTR_STS_VP_VPx[4]	Indicates that the timing generator has detected a line length error or other error that results in no data being available to send from the video buffer during the active horizontal period.
Timing Generation Line Number Error (IS_TIMING_LINE_ERR)	INTR_STS_VP_VPx[3]	This error is reported if the timing generator detects a mismatch between the expected line number and the incoming line number. This can occur during video buffer errors or if the timing generator is not synchronized with the incoming video stream. When this error is reported, video lines are removed from the video buffers.

[1] For expanded functionality, REM_INTB may be mapped to any GPIOx.

Table 7-16. Video Processor Interrupt Statuses (continued)

Status	Address	Description
Timing Generation Active Start Error (IS_TIMING_STRT_ERR)	INTR_STS_VP_VPx[2]	This error is reported if video data is not available when the timing generator indicates the start of the active video period.
Video Buffer Error (IS_VP_VBUF_ERR)	INTR_STS_VP_VPx[1]	Indicates the video buffer has detected an overflow error.
Video Processor Status Changed (IS_VP_STATUS_CHANGE)	INTR_STS_VP_VPx[0]	Indicates the video processor status has changed (any of the other interrupts in INTR_STS_VP_VPx is set or cleared).

7.3.14 FPD Transmitter Interrupt

FPD Transmitter Port interrupts are enabled via INTR_CTL_FPD4_PORTx indirect access registers (Page_9 0x8C and 0x9C) and FPD3_ICR (Page_0 0xC6). The status can be read in registers 0x8D and 0x9D on Page_9, and 0xC7 on Main Page_0.

Table 7-17. FPD Transmitter Interrupt Statuses

Status	Field Enable	Description
Receiver Lock Detected	INTR_STS_FPD4_PORTx[6], FPD3_ICR[6]	Set when the deserializer has indicated it is locked to the incoming data
Remote Interrupt	INTR_STS_FPD4_PORTx[5], FPD_ICR[5]	Indicates the deserializer INTB_IN is LOW (interrupt detected)
Deserializer Interrupt	INTR_STS_FPD4_PORTx[4]	Indicates that the deserializer global interrupt is detected.

7.3.15 ESD Event Interrupt

The device can be configured to trigger an interrupt when the number of ESD events exceeds a given threshold. To enable this interrupt set the DEVICE_INT_EN (0x51[3]) register to 1 and ESD_EVENT_INT_EN (0x61[6]) register to 1. The number of ESD events the device has detected is stored in the ESD_EVENT_COUNTER (0xBC[5:0]) register. The ESD event threshold count in the ESD_EVENT_COUNTER_THRESHOLD (0x61[5:0]) register. To clear the interrupt, first clear the ESD_EVENT_COUNTER (0xBC[5:0]) register by writing a "0" and then a "1" to the ESD_EVENT_COUNTER_ENABLE (0xBC[6]) register, then write a "1" to the ESD_EVENT_INT_STS_CLR (0x61[7]) register.

7.3.16 DP Receiver Interrupt

DP Receiver interrupts are enabled via INTR_CTL_DP_RX_PORT indirect access 0x3E in Page_9. The statuses of these interrupts are shown in INTR_STS_DP_RX_PORT indirect access 0x3F in Page_9. DisplayPort interrupt statuses are available regardless of whether an interrupt is included in the overall DP receiver interrupt, including when the corresponding bit in INTR_CTL_DP_RX_PORT is set to 0.

Table 7-18. DisplayPort Receiver Interrupt Statuses

Status	Address	Description
DP Sink 1 Status Change (IS_DP_SINK1_STS_CHANGE)	INTR_STS_DP_RX_PORT[6]	Indicates that DP stream 1 status change (valid only in MST case)
DP Sink 0 Status Change (IS_DP_SINK0_STS_CHANGE)	INTR_STS_DP_RX_PORT[5]	Indicates that DP stream 0 status change
DP Link Rate Change (IS_DP_LINK_RATE_CHANGE)	INTR_STS_DP_RX_PORT[4]	Indicates that DP Port Link rate change
DP Lane Count Change (IS_DP_LANE_COUNT_CHANGE)	INTR_STS_DP_RX_PORT[3]	Indicates that DP Port Lane count change

Table 7-18. DisplayPort Receiver Interrupt Statuses (continued)

Status	Address	Description
DP Core Interrupt (IS_ANY_DP_RX_CORE_INTR)	INTR_STS_DP_RX_PORT[2]	Indicates that one or more of the DisplayPort core interrupts has been detected.
DP Link Training Done (IS_DP_LINK_TRAINING_DONE)	INTR_STS_DP_RX_PORT[1]	Indicates that the DisplayPort link training is completed
DP Link Lost (IS_DP_LINK_LOST)	INTR_STS_DP_RX_PORT[0]	Indicates that the DisplayPort link is lost

7.3.17 DisplayPort Core Interrupts

The DP core interrupts are masked or unmasked in INTERRUPT_MASK (0x180) and their statuses are shown in INTERRUPT_CAUSE (0x188). By default, all DP core interrupts are masked. When interrupts are masked, their statuses are not shown in INTERRUPT_CAUSE.

Table 7-19. DisplayPort Core Interrupt Statuses

Status	Address	Description
Lane Count Change (LANE_COUNT_CHANGE)	INTERRUPT_CAUSE[21]	Indicates the DPCD register containing the current lane count has changed. This status will be flagged even when the DPCD register value is changed and the lane count is not changed (e.g. an invalid lane count is requested).
Link Rate Change (LINK_RATE_CHANGE)	INTERRUPT_CAUSE[20]	Indicates the DPCD register containing the current link rate has changed. This status will be flagged even when the DPCD register value is changed and the link rate is not changed (e.g. an invalid link rate is requested).
Training Pattern Set (TRAINING_PATTERN_SET)	INTERRUPT_CAUSE[16]	Indicates the DPCD register for the training state has changed.
Link Configuration Change (LINK_CONFIG_CHANGE)	INTERRUPT_CAUSE[11]	Indicates either the DPCD register containing the current link rate or current lane count have changed. This status will be flagged even when the DPCD register value(s) are changed and the link rate or lane count is not changed (e.g. invalid link rate or lane count requested).
Training Complete (TRAINING_COMPLETE)	INTERRUPT_CAUSE[8]	Indicates the training sequence has been complete for the number of enabled lanes. This interrupt is only set after training has been complete for at least 512 microseconds.
Training Lost (TRAINING_LOST)	INTERRUPT_CAUSE[7]	This interrupt is set whenever the receiver has been trained and subsequently loses clock recovery, symbol lock or inter-lane alignment. This interrupt will only occur when training has been lost for at least 512 microseconds. The link training lost interrupt will not be set if the DP TX intentionally changes the lane count or lane rate (indicated by writing to LINK_BW_SET or LANE_COUNT_SET)
Power Down Request (POWER_DOWN)	INTERRUPT_CAUSE[5]	The transmitter has requested a power down event through the power state DPCD register.
Power Up Request (POWER_UP)	INTERRUPT_CAUSE[4]	The transmitter has requested a power up event through the power state DPCD register.
Virtual Sink 1 Interrupt (VIRTUAL_SINK_1_INTERRUPT)	INTERRUPT_CAUSE[1]	Valid only in MST mode. This interrupt is set when a sink specific interrupt has occurred. See the SINK_1_INTERRUPT_CAUSE register for a description of the conditions that can cause an interrupt.
Virtual Sink 0 Interrupt (VIRTUAL_SINK_0_INTERRUPT)	INTERRUPT_CAUSE[0]	In SST mode or MST mode, this interrupt indicates that a sink specific interrupt has occurred. See the SINK_0_INTERRUPT_CAUSE register for a description of the conditions that can cause an interrupt.
InfoFrame Depth (INFOFRAME_DEPTH)	SINK_x_INTERRUPT_CAUSE[5]	Set when the DP core has received the number of InfoFrame packets set in the SEC_INFOFRAME_INTERRUPT_DEPTH register.
Vertical Blanking (VERTICAL_BLANKING)	SINK_x_INTERRUPT_CAUSE[3]	This interrupt is set at the start of the vertical blanking interval as indicated by the VerticalBlanking_Flag in the VB-ID field.
No Video (NO_VIDEO)	SINK_x_INTERRUPT_CAUSE[2]	The receiver has detected the no video flags in the VB-ID field after active video has been received.
Video Detect (VIDEO_DETECT)	SINK_x_INTERRUPT_CAUSE[1]	The receiver has detected the start of active video transmission after the link has previously been in the no video state.

Table 7-19. DisplayPort Core Interrupt Statuses (continued)

Status	Address	Description
Video Made Change (VIDEO_MODE_CHANGE)	SINK_x_INTERRUPT_CAUSE[0]	A change has been detected in the current video mode transmitted on the DisplayPort link as indicated by the MSA fields. The horizontal and vertical resolution parameters are monitored for changes.

7.3.18 FPD-Link IV Built-In Self Test (BIST)

An optional at-speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.18.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer via the BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer stores errors over the forward channel in its registers. The serializer also tracks errors indicated by the CRC fields in each back channel frame. Enabling BIST mode does not cause loss of lock.

See Figure 7-14 for the BIST mode flow diagram.

Step 1: The Serializer is paired with an FPD-Link IV Deserializer, BIST Mode is enabled via the register on the Deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x02[5] be toggled locally on the Serializer (set 0x02[5]=1, then set 0x02[5]=0).

Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link interface to the deserializer. Once the serializer and the deserializer are in BIST mode, the deserializer starts checking the data stream. If an error is detected, it is indicated in the error registers of the deserializer. On the serializer, errors on the back channel are monitored and stored in the BIST_BC_ERROR register (0x0F).

Step 3: BIST is stopped via the deserializer register and the deserializer stops checking the data. The final test result is held in BIST_BC_ERROR and the BIST error register on the deserializer. The BIST duration is user controlled by the duration between enabling BIST mode and disabling BIST mode.

**BIST can only be disabled from the deserilizer. During BIST remote access to the deserilizer from the serializer is disabled.

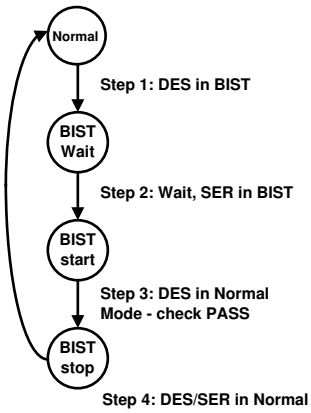


Figure 7-14. BIST Mode Flow Diagram

7.3.18.2 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sending video data and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, etc. and is transmitted over the serial link

to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers.

The back channel data is checked for CRC errors once the serializer locks onto the back channel serial stream, as indicated by link detect status (register bit 0x0C[0]). Back channel errors are stored in the BIST_BC_ERROR register, which is cleared when the serializer enters BIST mode. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.

7.3.19 Auxiliary Buffers and Secondary-Data Packets (SDP)

The Auxiliary Buffer (ABUFF) architecture includes a non-video data path over FPD-Link IV forward channel only. The Auxiliary Buffers are meant to store SDPs (Meta-Data) and audio data. Each buffer can receive data packets from the auxiliary sources, which can then be mapped to one of the 6 streams on each of the two link layers or to either of the two DisplayPort outputs if a DP deserializer is the partner device. On the deserializer, more than one ABUFF can be mapped to a stream on the FPD-Link daisy-chain output.

If an ABUFF is mapped to a stream shared with one of the video buffers (VBUFF), the Link layer (LINK0/1) will fetch the data from ABUFF after the video data has been sent. The data in the ABUFF is sent over the FPD-Link IV link only during the horizontal blanking period of the video stream. Alternatively, an ABUFF could be mapped to a stream that is not mapped to any of the VBUFF. In this case, the auxiliary data is transmitted over the FPD-Link IV along with the video stream but using separate, dedicated timeslots.

There are multiple sources for the ABUFF on the serializer side. The ABUFF destination for the serializers are the 6 streams inside each link layer. An ABUFF to Link Layer mapping muxes/demuxes nodes to/from Link 0 and Link 1 streams based on a per ABUFF register select bit (as part of serializer ABUFF register map). The deserializer has 6 stream destinations for daisy-chain transmitting and for the DS90Ux984-Q1 deserializer, two SDP DP/eDP ports. Audio stream SDPs received on the DS90Ux983-Q1 DP/eDP port are converted to I2S data format prior to being sent across the FPD-Link IV link. The deserializer's I2S controller copies the audio auxiliary data from stream 0 or stream 1 if SDP_TYPE_IN (serializer register 0x81 plus offset) is 0 (audio packets). The partner deserializer can output the I2S audio channels on I2S pins or for eDP/DP deserializers regenerate the audio stream SDP on DP/eDP ports Refer to Application Note SNLA407 *FPD-Link IV Audio* for more details on configuration.

ABUFF sources and destinations for the DS90Ux98x family devices are as follows:

Table 7-20. DS90Ux98x ABUFF Sources and Destinations

Device	ABUFF Sources	ABUFF Destinations
DS90Ux981	Audio, CSI	Link layer 0 or 1 streams
DS90Ux983	Audio, DP	Link layer 0 or 1 streams
DS90Ux984	FPD-Link IV RX	Daisy-chain link layer 0 or 1 streams, DP/eDP ports 0 and 1
DS90Ux988	FPD-Link IV RX	Daisy-chain link layer 0 or 1 streams

Table 7-21. Supported Secondary Data Packets

Packet Type Value	Packet Type	Transmission Timing
0x01	Audio TimeStamp	At least once per video frame
0x02	Audio Stream	During horizontal and vertical blanking period of Main Video stream
0x81	Vendor-Specific	As per Section 6.1 of CTA-861
0x82	Auxiliary Video Information	As per Section 6.4 of CTA-861
0x83	Source Product Description	As per Section 6.5 of CTA-861
0x84	Audio InfoFrame	As per Section 6.6 of CTA-861
0x87	Dynamic Range and Mastering	As per Section 6.9 of CTA-861

DP/eDP Audio Stream packets can not be passed through as SDP over the FPD-Link. This packet type is converted to I2S audio data and transmitted via Data Island Transport or Audio over GPIO modes. DP/eDP Audio Stream packets can be regenerated for output on DS90UB984-Q1 DP/eDP ports 0 and/or 1.

The auxiliary data with respect to blanking time has the following constraint:

1. Highest number of bits to transmit in that time is 567 bits
2. Total horizontal blanking time is minimum of 100 pixels
3. Total vertical blanking lines is minimum of 1 line
4. Any data that needs to be sent at the rate of once per frame can be sent during vertical blanking lines

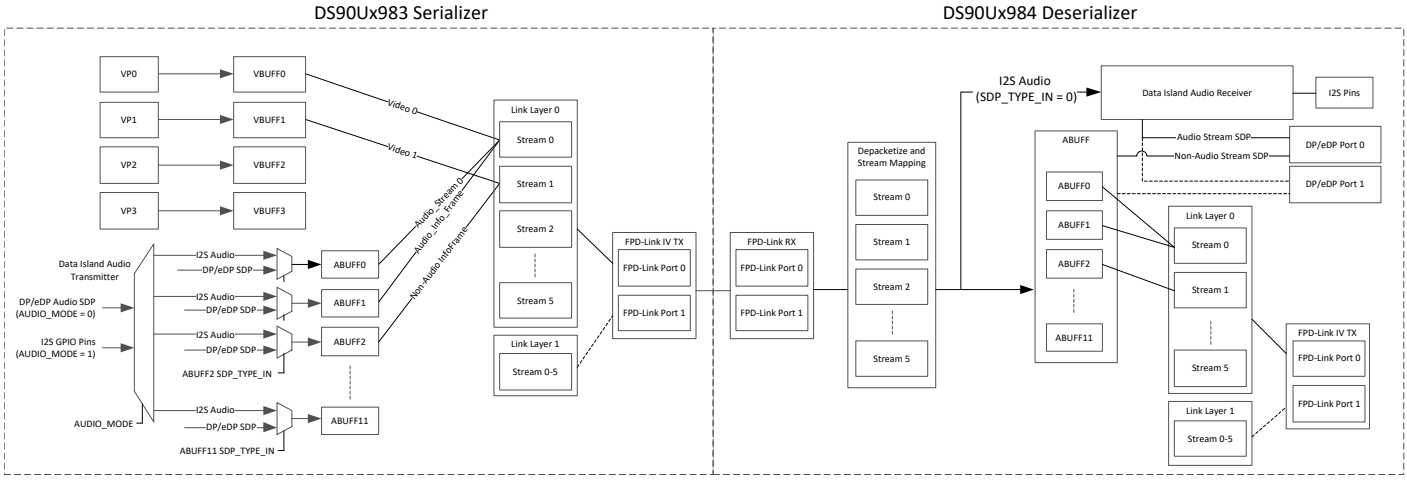


Figure 7-15. Example Auxiliary Buffer Configuration

7.3.19.1 ABUFF Serializer Configuration and Registers

The serializer Auxiliary Buffer registers are on Page_11 registers 0x80 through 0xDF. Each of the 12 ABUFFs have 8 registers assigned containing fields for configuration, mapping, and interrupts; as shown in Table 7-22. For additional information on debug and interrupt configuration, refer to the serializer register map.

Table 7-22. Serializer ABUFF0 Registers

Register	Bits	Field	Description
Page_11 0x80	7	SDP_OFFSET_CRCTN_BYP	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUFF packet 1: Offset correction feature is bypassed"
Page_11 0x80	4:2	SDP_FIFO_RD_THRESH	Buffer threshold reached before reading FIFO
Page_11 0x80	1	ABUFF_TO_PORT_SEL	ABUFF0 Port Select This bit works in conjunction with ABUFF_TO_DEST_SEL. 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer
Page_11 0x80	0	ABUFF_ENABLE	0: ABUFF disabled 1: ABUFF enabled
Page_11 0x81	3:0	SDP_TYPE_IN	Type of SDP: 0: Audio Reserved 2: Audio Info Frame 3: Non-Audio Info Frame 4: MISC 5: Reserved 6: Reserved Reserved

Table 7-22. Serializer ABUFF0 Registers (continued)

Register	Bits	Field	Description
Page_11 0x82	7:5	ABUFF_TO_DEST_SEL	ABUFF0 Destination Select ABUFF_TO_PORT_SEL to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 111: Reserved
Page_11 0x82	4:0	SRC_TO_ABUFF_SEL	Maps ABUFF to ABUFF SRCx

7.3.19.2 ABUFF Deserializer Configuration and Registers

The deserializer auxiliary buffer registers are on Page_17 registers 0x80 through 0xDF. Each of the 12 ABUFFs have 3 registers (ABUFFx_CTL0 through ABUFFx_CTL8) assigned containing fields for configuration, mapping, and interrupts. Table 7-23 shows the primary registers for enabling and mapping ABUFF0. For additional debug and interrupt configuration, refer to the register map.

Table 7-23. Deserializer ABUFF0 Registers

Register	Bits	Field	Description
Page_17 0x80	1	ABUFF_TO_PORT_SEL	ABUFF0 Port Select This bit works in conjunction with ABUFF_TO_DEST_SEL. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer
Page_17 0x80	0	ABUFFx_ENABLE	0: ABUFFx disabled 1: ABUFFx enabled
Page_17 0x82	7:5	ABUFF_TO_DEST_SEL	ABUFF0 Destination Select ABUFF_TO_PORT_SEL to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 111: Reserved

7.3.20 Audio

The serializer I2S pins or other audio interfaces, such as DP, can be sent audio over to the deserializer. For audio pass-through, the audio streams support 32 to 192 kHz sampling rate (32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz), 2 to 8-channels, and 16 to 32 bit word size (all even intervals, e.g. 16, 18, 20, 22, 24, 26, 28, 30, 32). I2S audio is supported from serializer to deserializer but the reverse direction (deserializer to serializer) is not supported.

Many of the serializer and deserializer audio registers are configured in the serializer and sent over the FPD-Link to the deserializer. For DS90Ux983, I2S audio can be received from either DisplayPort audio packets or from I2S pins. Downstream deserializers cannot convert between I2S and TDM. Therefore, converting audio modes must be performed by the serializer.

Refer to Application Note SNLA407 *FPD-Link IV Audio* for more details on implementation.

7.3.20.1 Audio Formats

7.3.20.1.1 Parallel I2S

I2S audio is supported externally through I2S pins (I2S_CLK, I2S_WC, and I2S_Dx) which are shared with GPIO pins. The bit clock (I2S_CLK) supports frequencies between 1 MHz to 12.288 MHz. Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input. Using the I2S_2_TDM feature, up to 8 channels of I2S can be multiplexed together to output a TDM signal. The I2S interface supports a range of I2S sample rates as shown in the table below:

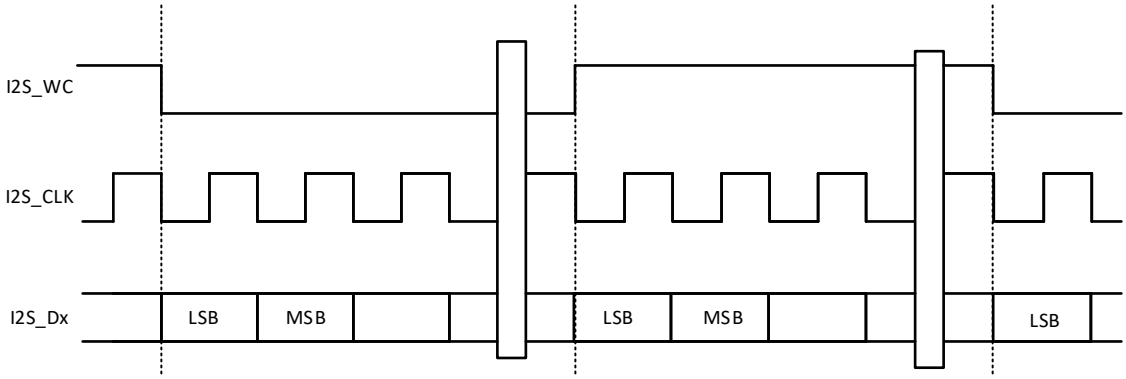


Figure 7-16. I2S Frame Timing Diagram

Table 7-24. I2S Audio Sample Rates Example

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

7.3.20.1.2 TDM Audio Interface

In addition to the I2S audio interface, the serializer also supports TDM format. A number of specifications for TDM format are in common use, and the DS90Ux98x offers flexible support for word length, bit clock, number of channels that can be multiplexed. For example, assume that word clock signal (I2S_WC) period = 256 × bit clock (I2S_CLK) time period. In this case, the DS90Ux98x can multiplex 8 channels with maximum word length of 32 bits each. Using the TDM_2_I2S feature, a TDM input is deconstructed into 8 I2S channels. Figure 7-17 shows the 8 channel TDM with 32-bit word length with 24-bits of data, in a format similar to I2S.

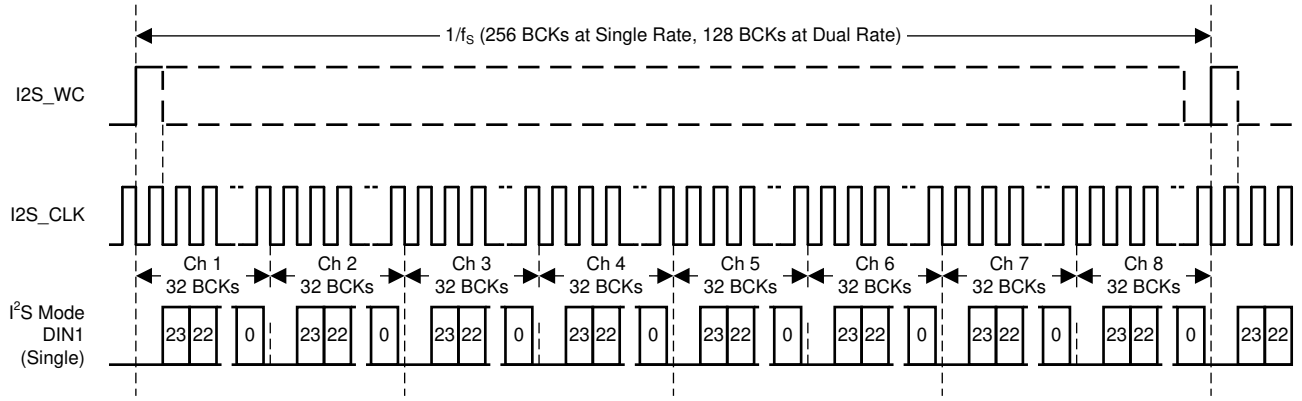


Figure 7-17. TDM Format

7.3.20.1.3 DP/eDP Audio Stream Packets

DS90Ux983 serializer DP/eDP receivers can accept audio over the DisplayPort input. The DP/eDP audio packets are converted to I2S by the serializer by setting AUDIO_MODE field in AUDIO_CFG to 0. Once transmitted to downstream deserializer, the audio data can be output to I2S or sent to DP/eDP port as audio stream packets (SDP). Audio stream packets can be output from DP deserializer DP/eDP output ports, see deserializer datasheet for more information.

7.3.20.1.4 Audio Inputs and Conversion

The serializer audio input can be in parallel I2S format or TDM format. If I2S_2_TDM or TDM_2_I2S is set, audio input is converted and sent to deserializer via FPD-Link III or FPD-Link IV datapath and audio transport configuration per Transport Modes, Splitting, and Forwarding. DS90Ux983 serializers can also support 24-bit DisplayPort audio packet input, as described in DP/eDP Audio Stream Packets. Available registers for TDM configuration and serializer audio format conversion are shown in Table 7-25.

Table 7-25. 98x and 943A Serializer Registers: Audio Formatting and Conversion

Address	Register Name	Field	Description
0x53[7]	AUDIO_CFG	TDM_2_I2S	Enable TDM to parallel I2S audio conversion: When this bit is set, the TDM to parallel I2S conversion is enabled. TDM audio data on the I2S_DA pin will be split onto four I2S data signals. In this mode, the input has to be 8 channel with 32-bit word length.
0x53[6]	AUDIO_CFG	I2S_2_TDM	Enable Parallel I2S to TDM Audio conversion: Setting this bit to a 1 will enable TDM audio conversion for the I2S audio. Parallel I2S data on the I2S pins will be serialized onto a single I2S_DA signal for sending over the serial link. In this mode, the input has to be 16-bit or 32-bit word length and up to 8 channels. Note: the output will be 8 channel TDM but if not all 8 channels are used, the unused channels will be blanked in the output.
0x53[5]	AUDIO_CFG	AUDIO_MODE	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0: DisplayPort 1: I2S audio from I2S pins

Table 7-25. 98x and 943A Serializer Registers: Audio Formatting and Conversion (continued)

Address	Register Name	Field	Description
0x53[3]	AUDIO_CFG	TDM_FS_MODE	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio generator. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0x0 = Active high Frame Sync. 0x1 = Active low Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
0x53[2]	AUDIO_CFG	TDM_DELAY	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0x0 = Data is not delayed from Frame Sync (data is left justified). 0x1 = Data is delayed 1 bit from Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
0x53[1:0]	AUDIO_CFG	TDM_FS_WIDTH	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion 00 = FS is 50/50 duty cycle 01 = FS is one slot/channel wide 1x = FS is 1 clock pulse wide

7.3.20.2 Transport Modes, Splitting, and Forwarding

The serializer or deserializer daisy-chain can send Audio to downstream deserializers via Audio over GPIO and Data Island transport modes. Audio over GPIO and Data Island transport modes can be used in FPD-Link III and FPD-Link IV modes, depending on the capability of the serializer and deserializer. The user must pay attention to the FPD mode, transport mode, and port enabling when configuring Audio registers since some registers only apply to certain transport and FPD-Link modes or ports.

Audio over GPIO transport mode utilizes the in-band forward channel GPIO bit stream to send the I2S clock, word clock, and 4 channels of Audio data to the deserializer. In Audio over GPIO mode, the four GPIO signals are assigned as follows:

- FC_GPIO0 : I2S_CLK
- FC_GPIO1 : I2S_WC
- FC_GPIO2 : I2S_DA
- FC_GPIO3 : I2S_DB

Audio via GPIO only supports 2 or 4-channel audio.

Audio Data Island transport mode utilizes Audio packet data in the video stream channel. This method allows 2, 4, or 8 channels of Audio to be sent.

Refer to Application Note SNLA407 *FPD-Link IV Audio* for more details on implementation.

7.3.20.2.1 FPD-Link IV Audio Transport Modes

In FPD-Link IV mode, the serializer or local deserializer daisy-chain Audio registers in FPD4_DATAPATH_CTL and FPD3_DATAPATH_CTL are configured based on desired transport mode, number of Audio channels, and port configuration. Both I2S_TRANSPORT_SEL and FPD4_I2S_TRANSPORT need to be configured to the same transport mode. I2S_MODE and FPD4_I2SB_FC_EN are set based on the number of Audio channels. I2S_TRANSPORT_SEL, FPD4_I2S_TRANSPORT, and FPD4_I2SB_FC_EN are port specific registers and are used in combination with the PORT_SEL register (0x0E for deserializer daisy-chain and 0x2D for serializer) to select which FPD-Link IV port is configured. I2S transport on FPD-Link Port 0 is enabled by setting

main page register 0x02[1] to 1. I2S transport on FPD-Link Port 1 is enabled by setting main page register 0x02[2] to 1. When enabled, transport mode for each port is set based on the I2S_TRANSPORT_SEL and FPD4_I2S_TRANSPORT.

When transporting Audio via Data Island transport mode with video present, there is a minimum horizontal blanking constraint based the amount of Audio bits accumulated during active video portion of the frame.

AUDIO_FPD_FRAME_CNT * FPD_FRAME_PERIOD < HBLANK_PERIOD (25)

Where

AUDIO_FPD_FRAME_CNT = (AUDIO_BITS_PER_LINE / 128)+2
AUDIO_BITS_PER_LINE = (HTOTAL / PCLK) * (I2S_CLK * 4)
FPD_FRAME_PERIOD (in ns) = 132 / FPD_RATE (in Mbps)
PCLK = Pixel Clock in MHz
HBLANK_PERIOD (in ns) = (HTOTAL - HACTIVE) / PCLK (in MHz)

Where
If I2S: I2S_CLK=SAMPLE_RATE*WORD_SIZE*2
If TDM: I2S_CLK=SAMPLE_RATE*WORD_SIZE*NUMBER_CHANNELS

When operating in Data Island transport mode, the Audio data is transmitted through the auxiliary buffers described in Auxiliary Buffers and Secondary-Data Packets (SDP). By default, ABUFF0 and ABUFF1 are configured for packetized Audio transport. For general use cases, ABUFF0 must be enabled and mapped to Link Layer 0 when Link Layer 0 Audio is desired and ABUFF1 must be enabled and mapped to Link Layer 1 when Link Layer 1 Audio is desired. Audio data can be transmitted without video through any desired stream by mapping ABUFFx to that stream. To extract Audio output from a terminating deserializer, Stream 0 must be enabled and used for ABUFF with audio.

Table 7-26. FPD-Link IV Transmit Audio Configuration

Serializer Configuration Field	Field Name	Description
Main_Page 0x5A[3]	I2S_TRANSPORT_SEL	Enable I2S data as Forward Channel Data Island 0x0 = Enable I2S Data Island Transport 0x1 = Enable I2S Data Forward Channel Frame Transport
Main_Page 0x5A[1:0]	I2S_MODE	I2S Channel Mode 0x0 = 2-channel I2S audio 0x1 = 4-channel I2S audio 0x2 = 5.1- or 7.1-channel surround audio is enabled 0x3 = Reserved Note that I2S Data Island Transport is the only option for surround audio.
Main_Page 0x0D[6]	FPD4_I2SB_FC_EN_Px	If FPD4 Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is per port register.
Main_Page 0x0D[5]	FPD4_I2S_TRANSPORT_Px	In FPD4, this indicates if 0x0 = I2S data over FC_GPIO if bit [4] is set. This bit for port 1 is default set to 0 This is per port register.
Main_Page 0x0D[4]	FPD4_FC_SDP_STREAM_Px	In FPD4, if bit[5] is 0: 0x0 = I2S audio for FPD4 is disabled (default) 0x1 = I2S audio over FC_GPIO enabled. This is a per port register. If bit[5] is 1: 0x0 = I2S over data island through SDP0 stream 0x1 = I2S over data island through SDP1 stream

Table 7-26. FPD-Link IV Transmit Audio Configuration (continued)

Serializer Configuration Field	Field Name	Description
Main_Page 0x02[2:1]	I2S_EN	Enable I2S input and transport 0x1 = Enabled I2S transport through FPD-Link Port 0 0x2 = Enables I2S transport through FPD-Link Port 1
Main_Page 0x05[1:0]	I2S_AUDIO_SPLIT	Split audio for FPD4 Port 0 and Port 1; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.

7.3.20.2.2 FPD-Link III Audio Transport Modes

By default, audio transport in FPD-Link III mode is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames can be disabled from control registers if Audio over GPIO is desired. In this mode, I2S_DA and I2S_DB are transmitted to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer. If connected to a DS90UB926Q-Q1 deserializer, only I2S_DA is transmitted. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[A..D]), can only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer.

To disable Data Island Transport mode and use Audio over GPIO mode instead, set I2S_TRANSPORT_SEL to 1. Set the number of I2S channels in the I2S_MODE (0x5A[1:0]) register.

Table 7-27 shows I2S_MODE and I2S_TRANSPORT_SEL settings for the possible channel count and transport mode combinations for FPD-Link III audio transmitting from serializer or deserializer daisy-chain output. Table 7-28 shows the specific registers used for FPD-Link III audio transport configuration in either Audio over GPIO or Data Island transport modes.

Table 7-27. FPD-Link III TX Audio Example Configurations

I2S Pins	Number of Audio Channels	Transport Mode	I2S_MODE (Main_Page 0x5A[1:0])	I2S_TRANSPORT_SEL (Main_Page 0x5A[3])
1	2	Data Island	0b00	0
1	2	Audio over GPIO	0b00	1
2	4	Data Island	0b01	0
2	4	Audio over GPIO	0b01	1
4	8(1)	Data Island	0b10	0

(1) If only use 6 channels, serializer treats Data Island like an I2S input with blanked data. Two unused channels can be blanked.

Table 7-28. FPD-Link III Transmit Audio Configuration

Serializer Configuration Field	Field Name	Description
Main_Page 0x5A[3]	I2S_TRANSPORT_SEL	Enable I2S data as Forward Channel Data Island 0x0 = Enable I2S Data Island Transport 0x1 = Enable I2S Data Forward Channel Frame Transport
Main_Page 0x5A[1:0]	I2S_MODE	I2S Channel Mode 0x0 = 2-channel I2S audio 0x1 = 4-channel I2S audio 0x2 = 5.1- or 7.1-channel surround audio is enabled 0x3 = Reserved Note that I2S Data Island Transport is the only option for surround audio.
Main_Page 0x0D[6]	FPD4_I2SB_FC_EN_Px	Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is per port register.
Main_Page 0x0D[5]	FPD4_I2S_TRANSPORT_Px	This bit indicates if 0x0 = I2S data over FC_GPIO if bit [4] is set. This bit for port 1 is default set to 0 This is per port register.

Table 7-28. FPD-Link III Transmit Audio Configuration (continued)

Serializer Configuration Field	Field Name	Description
Main_Page 0x0D[4]	FPD4_FC_SDP_STREAM_Px	If bit[5] is 0: 0x0 = I2S audio for FPD4 is disabled. - Default 0x1 = I2S audio over FC_GPIO enabled. This is per port register. If bit[5] is 1: 0 = I2S over data island through SDP0 stream 1 = I2S over data island through SDP1 stream
Main_Page 0x02[2:1]	I2S_EN	Enable I2S input and transport 0x1 = Enabled I2S transport through FPD-Link Port 0 0x2 = Enables I2S transport through FPD-Link Port 1

7.3.21 FPD-Link IV Daisy-Chaining

When the DS90UB983-Q1 is paired with FPD-Link IV deserializers, daisy-chain functionality supported for both FPD-Link IV or FPD-Link III modes drivers. Daisy-chaining allows the user to system to drive multiple displays from one source stream. The FPD-Link IV deserializers can extract 1 or more video stream(s) for export to a local display with remaining video streams forwarded to any downstrean deserializers. With four video processors on the DS90UB983-Q1, up to four display streams can be supported (the last deserializer can be either an FPD-Link IV deserializer or FPD-Link III deserializer). Possible use cases can be seen in the Figure 7-18, Figure 7-19, and Figure 7-20, showing the deserializer configured for 1 video stream output and 2 video stream outputs. More info on daisy-chaining can be found in FPD-Link IV deserializer data sheets.

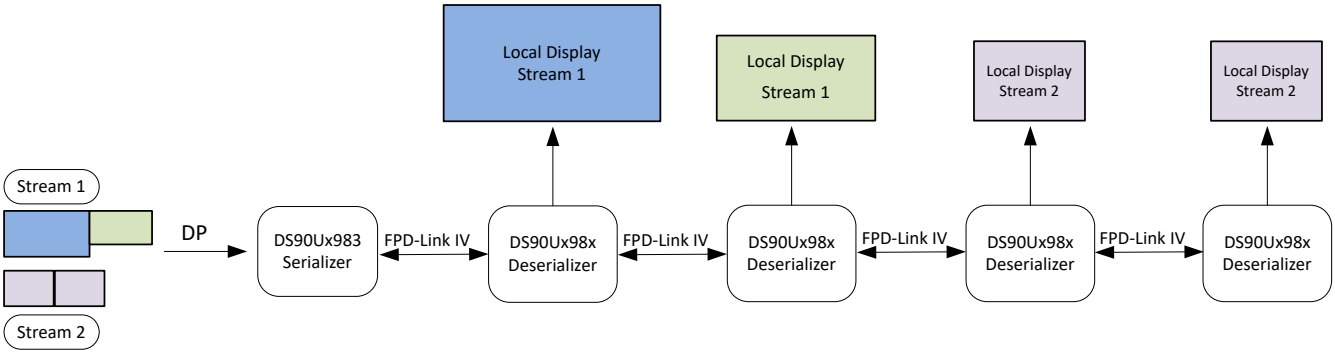


Figure 7-18. Daisy-Chaining Application Example

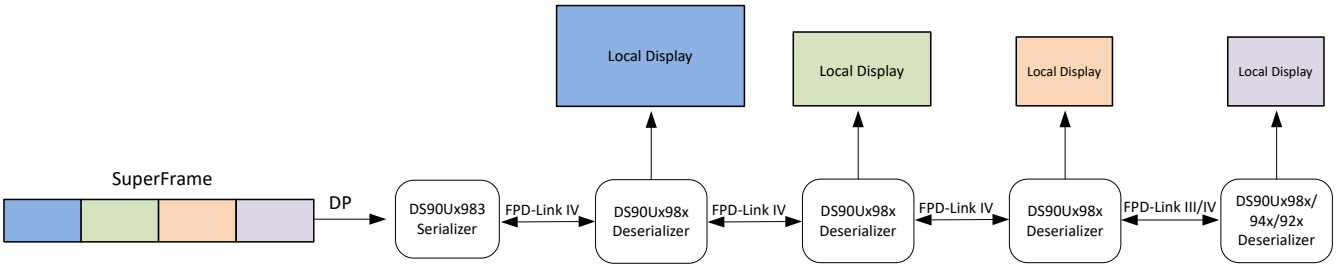


Figure 7-19. SuperFrame Daisy-Chaining Application Example

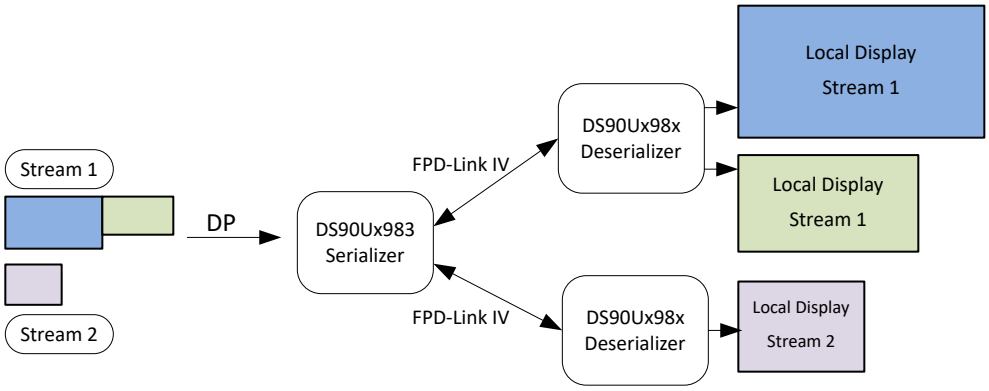


Figure 7-20. Split Daisy-Chaining Application Example

7.3.22 General-Purpose I/O

7.3.22.1 GPIO[0:13] Configuration

In normal operation, GPIO[0:13] can be used as general purpose inputs or outputs. GPIO modes are configured in the GPIOx_PIN_CTL registers (0x17 - 0x24). GPIO[10:13] share pins with the SPI interface in FPD-Link III backward compatibility mode. When using the SPI interface, the SPI configuration will override standard GPIO register configuration. GPIO[2:3] and GPIO[5:8] share pins with the I2S audio interface. When using the I2S interface, I2S configuration settings will override standard GPIO register configuration.

If a GPIO is set to "VP Combined INTERRUPT Status" when a VP interrupt occurs then the GPIO will pulse high for about 40 ns or if set to "Inverted VP Combined INTERRUPT Status" low for about 40 ns. This can be used to detect and count VP interrupts as they occur. The interrupt status can also be read from a register.

Table 7-29. GPIO Configuration

GPIO Output Function	Source	GPIO Output Enable GPIOx_PIN_CTL[7]	GPIOX Output Source Select GPIOx_PIN_CTL[6:4]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[3:0]
GPIOx Output Disabled	X	0	X	X
GPIOx linked to BC_GPIO0	Received from FPD Port 0	1	000	0000
GPIOx linked to BC_GPIO1		1	000	0001
GPIOx linked to BC_GPIO2		1	000	0010
GPIOx linked to BC_GPIO3		1	000	0011
GPIOx linked to BC_GPIO4		1	000	0100
GPIOx linked to BC_GPIO5		1	000	0101
GPIOx linked to BC_GPIO6		1	000	0110
GPIOx linked to BC_GPIO7		1	000	0111
PORT0 REM_INTB		1	000	1000
PORT0 RX_LOCK_DET		1	000	1001
PORT0 FPD3_TX_INTN		1	000	1010
PORT0 FPD3_TX_INT		1	000	1011
PORT0 RX_LOCK_DET Anded with PORT1 RX_LOCK_DET		1	000	1100
Reserved	Reserved	1	000	1101-1111
GPIOx linked to BC_GPIO8	Received from FPD Port 0	1	100	0000
GPIOx linked to BC_GPIO9		1	100	0001
GPIOx linked to BC_GPIO10		1	100	0010
GPIOx linked to BC_GPIO11		1	100	0011
GPIOx linked to BC_GPIO12		1	100	0100
GPIOx linked to BC_GPIO13		1	100	0101
GPIOx linked to BC_GPIO14		1	100	0110
GPIOx linked to BC_GPIO15		1	100	0111
PORT0 REM_INTB		1	100	1000
PORT0 RX_LOCK_DET		1	100	1001
PORT0 FPD3_TX_INTN		1	100	1010
PORT0 FPD3_TX_INT		1	100	1011
Reserved	Reserved	1	100	1100-1111

Table 7-29. GPIO Configuration (continued)

GPIO Output Function	Source	GPIO Output Enable GPIOx_PIN_CTL[7]	GPIOX Output Source Select GPIOx_PIN_CTL[6:4]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[3:0]
GPIOx linked to BC_GPIO0	Received from FPD Port 1	1	001	0000
GPIOx linked to BC_GPIO1		1	001	0001
GPIOx linked to BC_GPIO2		1	001	0010
GPIOx linked to BC_GPIO3		1	001	0011
GPIOx linked to BC_GPIO4		1	001	0100
GPIOx linked to BC_GPIO5		1	001	0101
GPIOx linked to BC_GPIO6		1	001	0110
GPIOx linked to BC_GPIO7		1	001	0111
PORT1 REM_INTB		1	001	1000
RX_LOCK_DET		1	001	1001
FPD3_TX_INTN		1	001	1010
FPD3_TX_INT		1	001	1011
Reserved	Reserved	1	001	1100-1111
GPIOx linked to BC_GPIO8	Received from FPD Port 1	1	101	0000
GPIOx linked to BC_GPIO9		1	101	0001
GPIOx linked to BC_GPIO10		1	101	0010
GPIOx linked to BC_GPIO11		1	101	0011
GPIOx linked to BC_GPIO12		1	101	0100
GPIOx linked to BC_GPIO13		1	101	0101
GPIOx linked to BC_GPIO14		1	101	0110
GPIOx linked to BC_GPIO15		1	101	0111
REM_INTB		1	101	1000
RX_LOCK_DET		1	101	1001
FPD3_TX_INTN		1	101	1010
FPD3_TX_INT		1	101	1011
Reserved	Reserved	1	101	1100-1111

Table 7-29. GPIO Configuration (continued)

GPIO Output Function	Source	GPIO Output Enable GPIOx_PIN_CTL[7]	GPIOX Output Source Select GPIOx_PIN_CTL[6:4]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[3:0]
Fixed output value of 0	NA	1	x10	0000
Fixed output value of 1		1	x10	0001
Inverted INTERRUPT STATUS		1	x10	0010
INTERRUPT STATUS		1	x10	0011
Inverted VP Combined INTERRUPT Status		1	x10	0100
VP Combined INTERRUPT Status		1	x10	0101
Reserved		1	x10	0110-1111

Table 7-30. GPIO Output Functions

GPIO OUTPUT FUNCTION	FUNCTION DESCRIPTION
REM_INTB	INTB_IN signal for the deserializer
RX_LOCK_DET	FPD-LinkLock status from the deserialiazer see "FPD-Link Lock" section
FPD3_TX_INT	FPD-Link III interrupt
FPD3_TX_INTN	Inverted FPD-Link III interrupt
INTERRUPT STATUS	Global Interrupt signal (Inverse of the Interrupt Pin)
Inverted INTERRUPT STATUS	Global Interrupt signal Inverted (mirrors the Interrupt Pin)
VP Combined INTERRUPT Status	The GPIO will be high for about 40ns when a interrupt in the video processor is triggered
Inverted VP Combined INTERRUPT Status	The GPIO will be low for about 40ns when a interrupt in the video processor is triggered

7.3.22.2 Back Channel GPIO Configuration

For Back Channel GPIO operation, 1, 4, 8, or 16 GPIOs can be sent over the back channel frame where the number of Back Channel GPIOs is programmed via GPIO_BC_EN register. When GPIO[0:13] pins are configured to output back channel GPIOs, the effective GPIO frequency will depend on the back channel frequency and configuration, configured by the partner deserializer. Consult the appropriate deserializer datasheet for details on how to configure the back channel frequency. As well, the selected deserializer GPIOs must be configured to be sent on the back channel using the deserializer registers. GPIO0 has the option to enable High-Speed GPIO mode through GPIO_BC_EN register on the serializer and BC_FRAMES is programmed on the paired FPD-Link IV deserializer.

The procedure below is an example configuring the GPIOx information carried from backward compatible DS90Ux94x, and DS90Ux92x deserializer to the DS90UB983-Q1 serializer. Note that the D_GPIO[3:0] of the backward compatible device, such as a DS90Ux94x or DS90Ux92x deserializer requires dual link mode operation. For normal GPIO operation, setting dual link port is not required.

Setting backward compatible for FPD-Link III mode GPIOs:

- Establish a link between the serializer and deserializer.
- Configure the deserializer device to dual port mode operation in register 0x34[1:0] = 0x3.
- Select the desired D_GPIOx pin for example D_GPIO3 in register 0x1F[3:0]= 0x3.
- Apply VDDIO to the D_GPIO3 for the deserializer.
- Configure the serializer DS90UB983-Q1 device for dual port mode in register 0x2D = 0x12.
- Disable the GPIOx input GPIO_IN_EN_HIGH[5:0] in register 0x3E and GPIO_IN_EN_LOW[7:0] in register 0x3F.
- Enable GPIO output GPIOx_PIN_CTL[3:0] in register 0x17 - 0x24. (DGPIOs are always received on port1, if so, port1 needs to be selected from GPIOx_PIN_CTL[6:4])
- Set GPIO output enable GPIOx_PIN_CTL[7] in register 0x17 - 0x24.

Setting back channel for FPD-Link IV mode GPIOs:

- Refer to deserializer 98x devices for register configuration.
- Select the desired GPIOx in the register GPIOx_PIN_CTL[6:4] and GPIOx_PIN_CTL[3:0]

Table 7-31. Back Channel GPIO Configuration

DESCRIPTION	OUTPUT SIGNAL
GPIO_BC_EN	0x0: Four GPIO slots from the Back Channel mapped on local GPIO[3:0] slots 0x1:Eight GPIO slots from the Back Channel mapped on local GPIO[7:0] slots 0x10: Sixteen GPIO slots from the Back Channel mapped on local [GPIO15:0] slots (Only up to fourteen GPIOs mapped is a valid configuration due to the limited number of GPIOs) 0x11: One HS-GPIO0

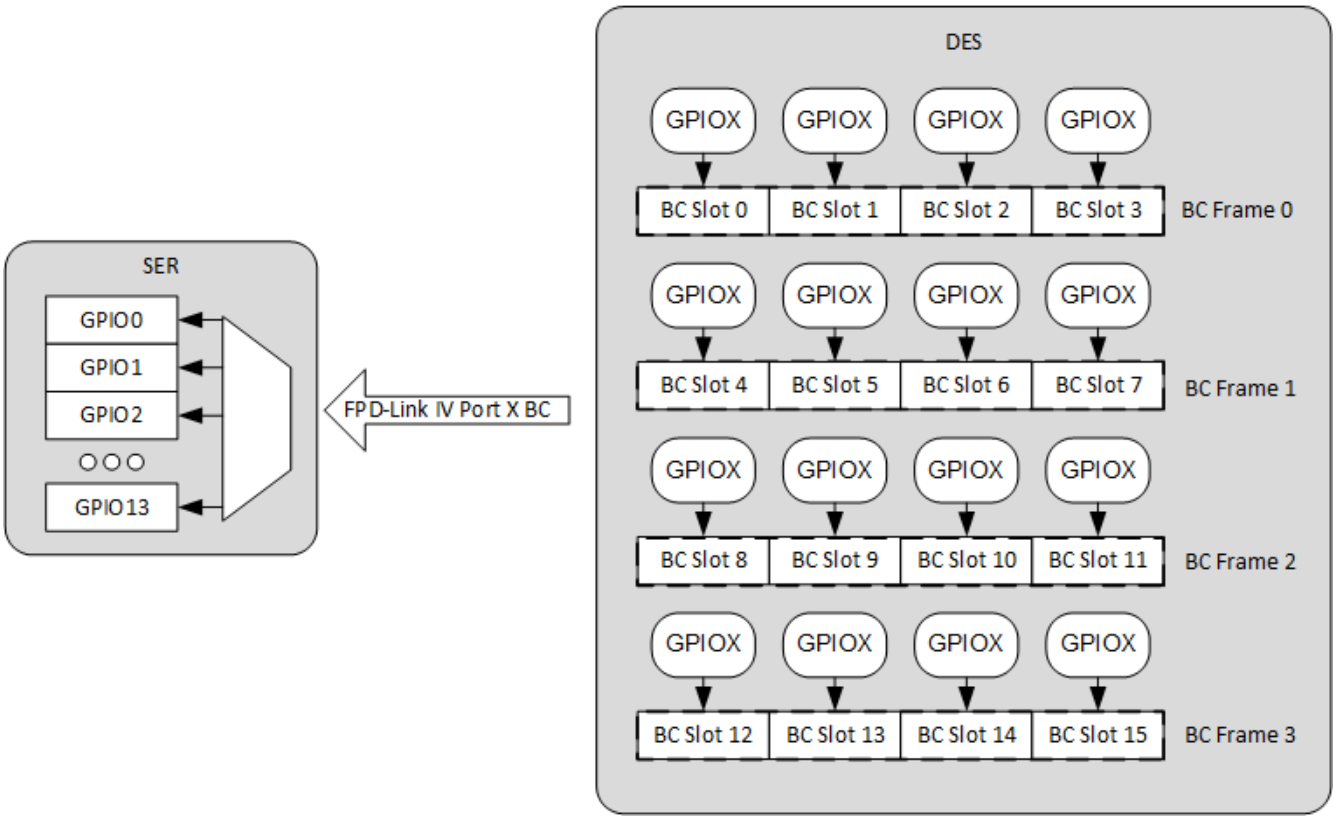


Figure 7-21. Back Channel GPIO

7.3.22.3 Forward Channel GPIO Configuration

The DS90UB983-Q1 can send input data from the GPIO pins across the forward channel to a remote deserializer. In order to do this, the GPIO pin must be programmed for input mode using the GPIO_PIN_CTLx registers. There are four forward channel GPIO signals (FC_GPIOx) per FPD port that can be used to send data from any of the fourteen GPIO pins. All FC_GPIOx signals are sent as part of every other forward channel frame. The same GPIO pin can be connected to multiple forward channel GPIO signals. In addition to sending input data from GPIO pins, fixed values can also be sent on the forward channel GPIO signals. For each port, the following GPIO controls are available through the FC_GPIO_CTL0 (0x15), FC_GPIO_CTL1 (0x16), and FPD4_DATAPATH_CTL (0x0D) registers :

The procedure below is an example configuring the GPIOx information carried from DS90UB983-Q1 serializer to the backward compatible DS90Ux94x, and DS90Ux92x deserializer. Note that the D_GPIO[3:0] of the backward compatible device such as DS90Ux94x, and DS90Ux92x deserializer requires to set dual link mode operation. For normal GPIO operation, setting dual link is not required.

Setting forward channel FPD-Link III mode GPIOs:

- Establish a link between the serializer DS90UB983-Q1 and deserializer 92x and 94x.
- Configure the deserializer device to dual port mode operation in register 0x34[1:0] = 0x3.
- Select the desired D_GPIOx pin, for example D_GPIO3 in register 0x1F[3:0]= 0x5.
- Configure the serializer DS90UB983-Q1 device in dual port mode in register 0x59 = 0x3.
- There are a total of 4 GPIO slots for GPIO mapping. These slots are corresponded to the GPIOx in the deserializer. For example, FC_GPIO slot 3 is programmed to use GPIO3 pin as the source. Enabling the desired GPIOx slot in register FPD4_DATAPATH_CTL[1:0] = 0x3. This will enable four GPIO[3:0] for the deserializer.
- Assign the desired GPIOx for the DS90UB983-Q1 device by configuring the register 0x15 and 0x16. For this example set FC_GPIO_CTL1[7:0] = 0x0 to assign GPIO0 for DS90UB983-Q1.
- Apply 1.8V to GPIO0 of the DS90UB983-Q1 device
- Enable the GPIOx input GPIO_IN_EN_HIGH[5:0] in register 0x3E and GPIO_IN_EN_LOW[7:0] in register 0x3F.
- Disable GPIO output GPIO0_PIN_CTL[7] in register 0x17 - 0x24.

Setting forward channel FPD-Link IV mode GPIOs:

- Establish a link between the serializer DS90UB983-Q1 and deserializer 98x.
- Configure the serializer DS90UB983-Q1 device in dual port mode in register 0x05 FPD4_CFG[5:2].
- Assign the desired GPIOx for the DS90UB983-Q1 device by configuring the register 0x15 and 0x16. For this example set FC_GPIO_CTL1[7:0] = 0x0 to assign GPIO0 for DS90UB983-Q1.
- Apply 1.8V to GPIO0 of the DS90UB983-Q1 device
- Enable the GPIOx input GPIO_IN_EN_HIGH[5:0] in register 0x3E and GPIO_IN_EN_LOW[7:0] in register 0x3F.
- Disable GPIO output GPIO0_PIN_CTL[7] in register 0x17 - 0x24.

Table 7-32. Forward Channel GPIO Configuration

DESCRIPTION	OUTPUT SIGNAL
GPIOEN_FC	GPIOs disabled: GPIOEN_FC = 0x00 One GPIO: GPIOEN_FC = 0x01 Two GPIOs: GPIOEN_FC = 0x02 Four GPIOs: GPIOEN_FC = 0x03
FC_GPIOx	GPIO0: FC_GPIOx_SEL = 0000 GPIO1: FC_GPIOx_SEL = 0001 GPIO2: FC_GPIOx_SEL = 0010 ... GPIO13: FC_GPIOx_SEL = 1101 Constant value of 0: FC_GPIOx_SEL = 1110 Constant value of 1: FC_GPIOx_SEL = 1111

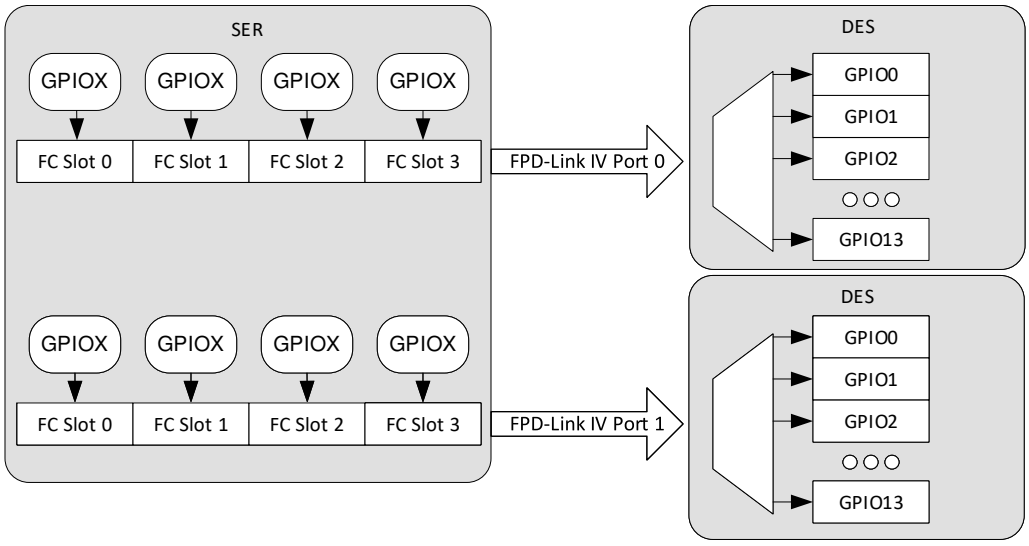


Figure 7-22. Forward Channel GPIO

7.3.23 Internal Pattern Generation

The DS90UB983-Q1 serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. For FPD-Link IV operation, there is one pattern generator per video processor.

7.3.23.1 Pattern Options

The DS90UB983-Q1 serializer pattern generator is capable of generating 20 default patterns for use in basic testing and debugging of panels. Each can be inverted using PGCTL register and the FPD4_PGCTL_VPx registers on Page_12, shown below:

1. Checkerboard (White/Black)
2. White
3. Black
4. Red
5. Green
6. Blue
7. Horizontally Scaled Black to White
8. Horizontally Scaled Black to Red
9. Horizontally Scaled Black to Green
10. Horizontally Scaled Black to Blue
11. Vertically Scaled Black to White
12. Vertically Scaled Black to Red
13. Vertically Scaled Black to Green
14. Vertically Scaled Black to Blue
15. Custom color (or the inversion) configured in PGRS, PGGS, PGBS registers
16. VCOM (Yellow, Cyan, Yellow, Red)
17. Alternate VCOM (Blue, Cyan, Yellow, Red)
18. Custom Color Checkerboard (Custom/Black)
19. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)
20. UNH-IOL MIPI D-PHY Compliance Test Pattern

Due to the quad pixel clock architecture of the FPD-Link IV serializer devices, patterns #6-9 (horizontally scaled patterns) and #19 (color bars) must only be used when the active line length meets a minimum number of pixels based on the configured bits per color. If the minimum horizontal pixel count is not met, then the pattern does not correctly scale to the screen size (ex. less than 8 color bars shown). If the screen size does not meet the minimum number of horizontal pixels, then it is suggested to use one of the other available patterns instead.

Table 7-33. Minimum Pixels Per Line for PATGEN Horizontally Scaled or Color Bar Patterns

PATGEN Bits Per Pixel	Minimum Active Horizontal Pixels
30bpp	4096
24bpp	1024
18bpp	256

7.3.23.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where 8 most significant bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode and 30-bit color mode can be activated from the configuration registers. In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0. In 30-bit mode, 10 most significant bits of the Red, Green, and Blue outputs are enabled.

7.3.23.3 Video Timing

The Pattern Generator uses the video timing settings of the video processor being used to generate the pattern . Set the PATGEN_TSEL field (Page_12 registers 0x29, 0x69, 0xA9, 0xE9) to 0 to use the video processor timing when the video processor timing is used to generate the pattern. The PATEGEN_FREERUN field Page_12 registers 0x28, 0x68, 0xA8, 0xE8) must be set to 1 to operate independently from the incoming video.

7.3.23.4 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

7.3.23.5 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns can be defined in the registers. The patterns can appear in any order in the sequence and can also appear more than once. The pattern sequence can be configured through PGTS0x register found in Pattern Generator Indirect Register Map.

7.3.23.6 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. There is one copy of this register map per each video processor. It can be accessed through the Pattern Generator Indirect Address (PGIA) (0x66 Main Page and 0x2A, 0x6A, 0xAA, and 0xEA on Page_12) and the Pattern Generator Indirect Data (PGID) registers (0x67 Main Page and 0x2B, 0x6B, 0xAB, and 0xEB on Page_12). See Application Note AN-2198.

7.3.24 Backward Compatibility

The DS90UB983-Q1 serializer is backward compatible to DS90Ux94x and DS90Ux92x deserializers. To enable backward capability, set the desired channel to FPD-Link III mode via FPD3_TX_MODE (0x59[2:0]). The FPD-Link III data path can be connected to any of the four video streams from the video processor modules FPD3_STREAM_SEL(0x57) register.

Table 7-34. Backward Compatibility

MODE	DESERIALIZER	PCLK	Forward Channel Rate	Back Channel Rate	Output Format	Typical Resolution Supported
Single Link	DS90UB924	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	10 Mbps	oLDI	900p/720p
	DS90Ux926	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	10 Mbps	RGB	720p
	DS90Ux928	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	10 Mbps	oLDI	720p
	DS90Ux940	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	900p / 720p
	DS90Ux940N	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	900p / 720p
	DS90Ux948	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	900p / 720p
	DS90Ux984 in FPD-Link III Mode	25 MHz ≤ PCLK ≤ 162 MHz	875 Mbps to 5.67 Gbps	5 Mbps 10 Mbps 20 Mbps	DP	1080p
	DS90Ux988 in FPD-Link III Mode	25 MHz ≤ PCLK ≤ 162 MHz	875 Mbps to 5.67 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	1080p
Dual Link	DS90Ux948	50 MHz ≤ PCLK ≤ 192 MHz	1.75 Gbps to 6.72 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	2K (2048x1080) / FHD (1920x1080)
	DS90Ux940	50 MHz ≤ PCLK ≤ 170 MHz	1.75 Gbps to 5.95 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	WUXGA (1920×1200) / FHD (1920x1080)
	DS90Ux940N	50 MHz ≤ PCLK ≤ 170 MHz	1.75 Gbps to 5.95 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	WUXGA (1920×1200) / FHD (1920x1080)
	DS90Ux984 in FPD-Link III Mode	50 MHz ≤ PCLK ≤ 324 MHz	1.75 Gbps to 11.34 Gbps	5 Mbps 10 Mbps 20 Mbps	DP	2K/3K
	DS90Ux988 in FPD-Link III Mode	50 MHz ≤ PCLK ≤ 324 MHz	1.75 Gbps to 11.34 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	2K/3K

The DS90Ux94x deserializer linerates are automatically set based on the PCLK frequency. In the FPD-Link III mode, the PLL must be programmed to generate the correct line rate (dividers, Reference REFCLK select, etc.) and the ENABLE_FPD3_FIFO (0x5B[3]) register must be set to 1.

7.3.24.1 Video Processor Configuration in FPD-Link III Mode

Video filtering, video cropping, and video timing parameters must be configured in the same manner as in FPD-Link IV Mode. However, the PCLK used in FPD-Link III mode is sourced directly from the reference source, not from the forward channel rate so the video processor frequency is set differently. As well, the FPD-Link port configuration is different in FPD-Link III mode vs FPD-Link IV mode. In FPD-Link III mode, only one video stream is assigned to each FPD-Link Port, meaning that a maximum of two video processors can be enabled.

7.3.24.1.1 FPD-Link III Port Configuration

Each FPD-Link III Port can transmit data from one of the four video processors (VP0 to VP3). The FPD3_STREAM_SEL (0x57) register is used to select which video processor the FPD-Link Port transmits. In Independent or Single FPD-Link III modes select the FPD-Link port using PORT_SEL (0x2D) then set the FPD3_STREAM_SEL register to select the video processor for the FPD-Link port. In Dual FPD-Link III the register is not port specific and the setting applies to both ports.

Table 7-35. Video Stream Forwarding

Video Processor	FPD-Link Port
VPx	VP0: FPD3_STREAM_SEL[1:0] = 0x0 VP1: FPD3_STREAM_SEL[1:0] = 0x1 VP2: FPD3_STREAM_SEL[1:0] = 0x2 VP3: FPD3_STREAM_SEL[1:0] = 0x3

7.3.24.1.2 Video Processor Frequency

The video processor clock is a quad-pixel clock generated automatically to be 1/4 of the PCLK corresponding to the selected FPD-Link III line rate. The video processor clock is generated using a phase-locked loop (PLL) with the selected reference clock as the input, as shown in the FPD-Link III PLL section. The reference clock source is selected using either the CH0_FPD3_REFCLK1 or CH1_FPD3_REFCLK1 bits (0x5[6] or 0x5[7]). The VCO's (voltage controlled oscillators) range is 3500 MHz to 7000 MHz. Configuring the PLL requires selecting the input source, setting the N-divider, numerator, denominator, MASH order (either integer or fractional), and the post-divider. After configuring these settings, the PLL must be reset using either the PLL_CH0_RESET or PLL_CH1_RESET bits (0x1[5] or 0x1[4]). The video processor clock is governed by the following equations:

$$\mathrm{VP\_CLK} = \frac{\mathrm{Target\_PCLK}}{4} \tag{26}$$

$$\mathrm{FPD3\_Line\_Rate(MHz)} = \mathrm{Target\_PCLK} \times 35 \tag{27}$$

$$f_{VCO}\left(\mathrm{MHz}\right) = \left(\frac{\mathrm{FPD\_Line\_Rate}}{2}\right) \times \mathrm{P} \tag{28}$$

where

- f_{VCO} is the VCO frequency
- P is the post-divider value (2, 4, 8, or 16)

$$f_{VCO} = f_{REF} \times 2 \times \left[\mathrm{N} + \left(\frac{\mathrm{NUM}}{\mathrm{DEN}}\right)\right] \tag{29}$$

where

- f_{Ref} is the reference frequency, either from the XI or REFCLK1
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206), NUM ≤ DEN
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

7.3.24.1.3 Example FPD-Link III PLL Calculation

1. Start with the desired PCLK frequency and calculate the corresponding FPD-Link III Line Rate (PCLK × 35).
   - EX: PCLK = 95.75 MHz, so FPD-Link III Line Rate = 3351.25 MHz
2. Then consider all potential VCO frequencies (FPD-Link III Line Rate / 2 × P) and find the valid VCO frequencies which fall in the VCO range of 3500-7000MHz
   - EX: Potential VCO frequencies are: 3351.25 / 2 × 2 = 3351.25 MHz, 3351.25 / 2 × 4 = 6702.5 MHz, 3351.25 / 2 × 8 = 13,405 MHz, and 3351.25 / 2 × 16 = 26,810 MHz. Only 6702.5 MHz is a valid VCO frequency. This means that POST_DIV must be programmed to 0x6 (selects a post-divider of 4).
3. Determine the integer portion of the N-divider (integer portion of f_{VCO}/ (2 × f_{Ref})).
   - EX: 6702.5 / (2 × f_{Ref}) = 6702.5 / (2 × 27) = 124.12 so the integer portion is 124. This means that NDIV[7:0] must be programmed to 0x7C and NDIV[15:8] must be programmed to 0x00.

4. Determine the numerator and denominator of the N-divider (fractional portion of f_{VCO}/ (2 × f_{Ref})).
   - EX: 6702.5 / (2 × 27) - 124 = 0.12 $\overline{037}$. A fractional approximation of this is 13/108. Larger denominators are preferred when possible. To find the form of this fraction with the largest possible denominator, find the closest multiple of the denominator to the maximum denominator (16,777,206). Divide the maximum denominator (16,777,206) by the current denominator (108) and round down: 16,777,206 / 108 = 155,344.5 so use the 155,344th multiple of the original fraction. Multiplying our numerator and denominator by this factor gives us our final fraction: 2,019,472 / 16,777,152 [2]

Table 7-36. FPD-Link III Clock Register Configuration

Reference Select	XI: CHx_FPD3_REFCLK1 = 0 REFCLK1: CHx_FPD3_REFCLK1 = 1
N-Divider	NDIV[15:0] = Integer portion of N divider
Numerator	NUM[23:0] = Numerator portion of N divider
Denominator	DEN[23:0] = Denominator portion of N divider
MASH Order	Integer: MASH_ORDER= 0x0 Fractional: MASH_ORDER = 0x2
Post-Divider	2: POST_DIV = 0x5 4: POST_DIV = 0x6 8: POST_DIV = 0x7 16: POST_DIV = 0x4

7.3.24.2 FPD-Link III Modes of Operation

The FPD-Link III transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The following modes are supported:

7.3.24.2.1 FPD-Link III Single Link Operation

Single Link mode transmits the video over a single FPD-Link III to a single receiver. Single link mode supports frequencies up to 96 MHz for 24-bit video when paired with the DS90Ux940, DS90Ux940N, DS90Ux948, or DS90UB924. This mode is compatible with the DS90Ux926 or DS90Ux928 when operating below 85 MHz. When paired with another FPD-Link IV capable device, single link mode supports frequencies up to 162 MHz. If the downstream device is capable, the secondary FPD-Link III link can be used for high-speed control.

In Forced Single mode (set via FPD3_MODE_CTL1 register), the secondary TX Phy and back channel is disabled.

7.3.24.2.2 FPD-Link III Dual Link Operation

In Dual Link mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links. The receiver must be capable of receiving the dual-stream video. Dual link mode is capable of supporting an pixel clock frequency of up to 324 MHz (limited by deserializer capability), with each FPD-Link III TX port running at one-half the frequency. This allows support for full 2K video. The secondary FPD-Link III link could be used for high-speed control.

Dual Link mode can be enabled using the FPD3_MODE_CTL register, as long as both FPD-Link Ports are configured for FPD-Link III mode in both the FPD4_TX_MODE register.

7.3.24.2.3 FPD-Link III Independent Operation

In this mode, the two FPD-Link channels operate as independent single link channels. When switching from independent to dual mode or vice-versa, a soft reset is required to establish the link.

7.3.24.2.4 FPD-Link III Replicate Mode

To use replicate mode, set the FPD-Link III mode to independent and configure two video processors identically with each video processor mapped to a single FPD-Link III channel.

[2] Various methods an be used to find the fractional representation. Free tools to find a fractional representation of a decimal such as this one can simplify this process.

7.3.24.2.5 Setting FPD-Link III Modes

The DS90UB983-Q1 automatically detects the capabilities of downstream links and can resolve whether a single device, dual-capable device, or multiple single link devices are connected.

Modes can be set using the FPD3_MODE_CTL register, as long as the FPD-Link Port is configured for FPD-Link III mode in the FPD4_TX_MODE register.

7.3.24.3 FPD-Link Back Channel Optimizations

When switching to a FPD-Link mode different from the MODE_SEL2 strap setting, the following scripts can be run to optimize the back channel receiver for the intended more.

The following script contains the optimizations for serializers strapped in FPD-Link III mode during start up and later switched to FPD-Link IV :

```
## ********************************************************
## Optimized back channel settings for FPD3 to FPD4 Mode
## ********************************************************
board.WriteI2C(DEV_ADDR,0x40,0x04) #Select Page 1 FPD Port Indirect Page
board.WriteI2C(DEV_ADDR,0x41,0x05) #Setting BC Setting 0 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x06) #Setting BC Setting 1 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x0D) #Setting BC Setting 2 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x34)
board.WriteI2C(DEV_ADDR,0x41,0x0E) #Setting BC Setting 3 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x53)
board.WriteI2C(DEV_ADDR,0x41,0x25) #Setting BC Setting 0 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x26) #Setting BC Setting 1 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x2D) #Setting BC Setting 2 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x34)
board.WriteI2C(DEV_ADDR,0x41,0x2E) #Setting BC Setting 3 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x53)
```

The following script contains the optimizations for serializers strapped in FPD-Link IV mode during start up and later switched to FPD-Link III :

```
## ********************************************************
## Optimized back channel settings for FPD4 to FPD3 Mode
## ********************************************************
board.WriteI2C(DEV_ADDR,0x40,0x04) #Select Page 1 FPD Port Indirect Page
board.WriteI2C(DEV_ADDR,0x41,0x05) #Setting BC Setting 0 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x06) #Setting BC Setting 1 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0xFF)
board.WriteI2C(DEV_ADDR,0x41,0x0D) #Setting BC Setting 2 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x0E) #Setting BC Setting 3 for Port 0
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x25) #Setting BC Setting 0 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x26) #Setting BC Setting 1 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0xFF)
board.WriteI2C(DEV_ADDR,0x41,0x2D) #Setting BC Setting 2 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x2E) #Setting BC Setting 3 for Port 1
board.WriteI2C(DEV_ADDR,0x42,0x70)
```

7.3.24.4 SPI Communication (Pass-Through Mode)

In backward compatible mode, the SPI Control Channel utilizes the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available, Forward Channel and Reverse Channel modes. In Forward Channel mode, the SPI Controller is located at the Serializer, such that the direction of sending SPI data is in the same direction as the video data. In Reverse Channel mode, the SPI Controller is located at the Deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI Control Channel can operate in a high speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the peripheral to the controller on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies as the POCI pin can be ignored by the controller.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

Note: SPI cannot be used to access Serializer / Deserializer registers.

7.3.24.4.1 SPI Mode Configuration

SPI is configured over I^2C using the High-Speed Control Channel Configuration Mode (HSCC_MODE) field found in register 0x10 and 0x11. The bits must be configured for either High-Speed, Forward Channel SPI mode (110) or High-Speed, Reverse Channel SPI mode (111).

7.3.24.4.2 Forward Channel SPI Operation

In Forward Channel SPI operation, the SPI controller located on the Serializer generates the SPI Clock (SCK), Peripheral IN Controller OUT data (PICO), and active low Chip Select (CS). The serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SCK, PICO, and CS are each sent on data bits in the forward channel frame. At the Deserializer, the SPI signals are regenerated using the pixel clock. In order to preserve setup and hold time, the Deserializer will hold PICO data while the SCK signal is high. In addition, it delays SCK by one pixel clock relative to the PICO data, increasing setup by one pixel clock.

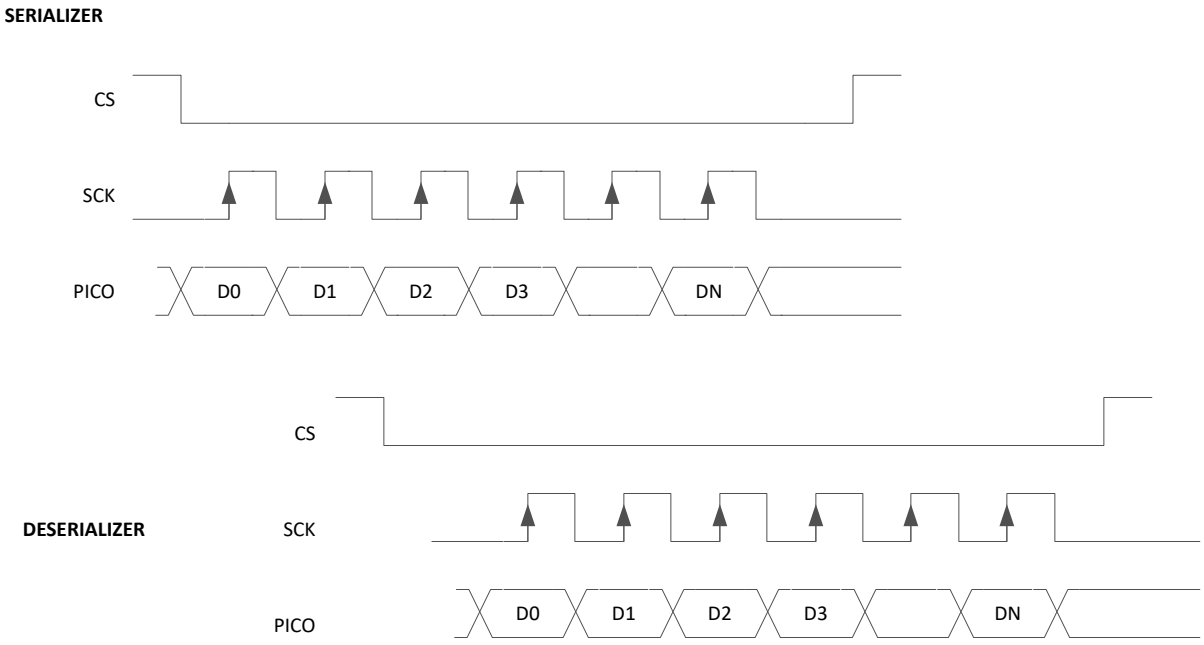


Figure 7-23. Forward Channel SPI Write

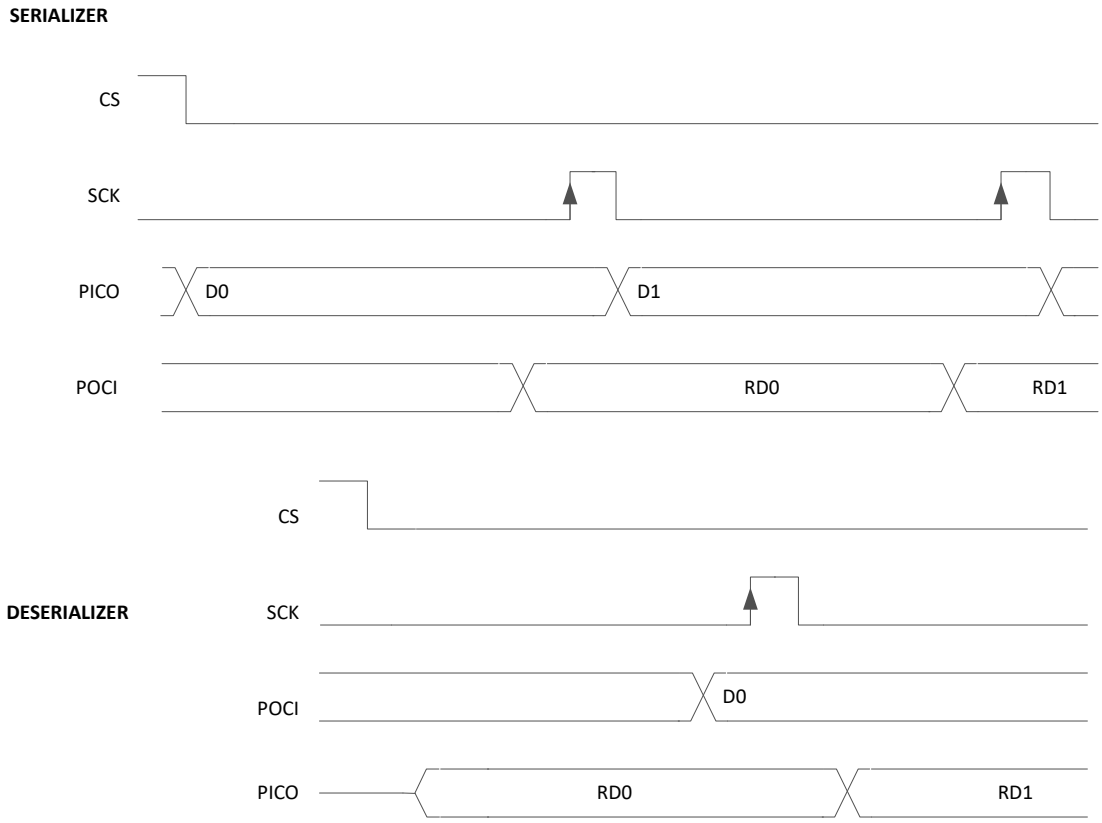


Figure 7-24. Forward Channel SPI Read

7.3.24.4.3 Reverse Channel SPI Operation

In Reverse Channel SPI operation, the deserializer samples the Chip Select (CS), SPI clock (SCK) into the internal oscillator clock domain. In addition, upon detection of the active SPI clock edge, the deserializer samples the SPI data (PICO). The SPI data samples are stored in a buffer to be passed to the Serializer over the back channel. The deserializer sends SPI information in a back channel frame to the Serializer. In each back channel frame, the deserializer sends an indication of the Chip Select value. The Chip Select must be inactive (high) for at least one back-channel frame period to ensure propagation to the Serializer.

Because data is delivered in separate back channel frames and buffered, the data can be regenerated in bursts. The following figure shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the CS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

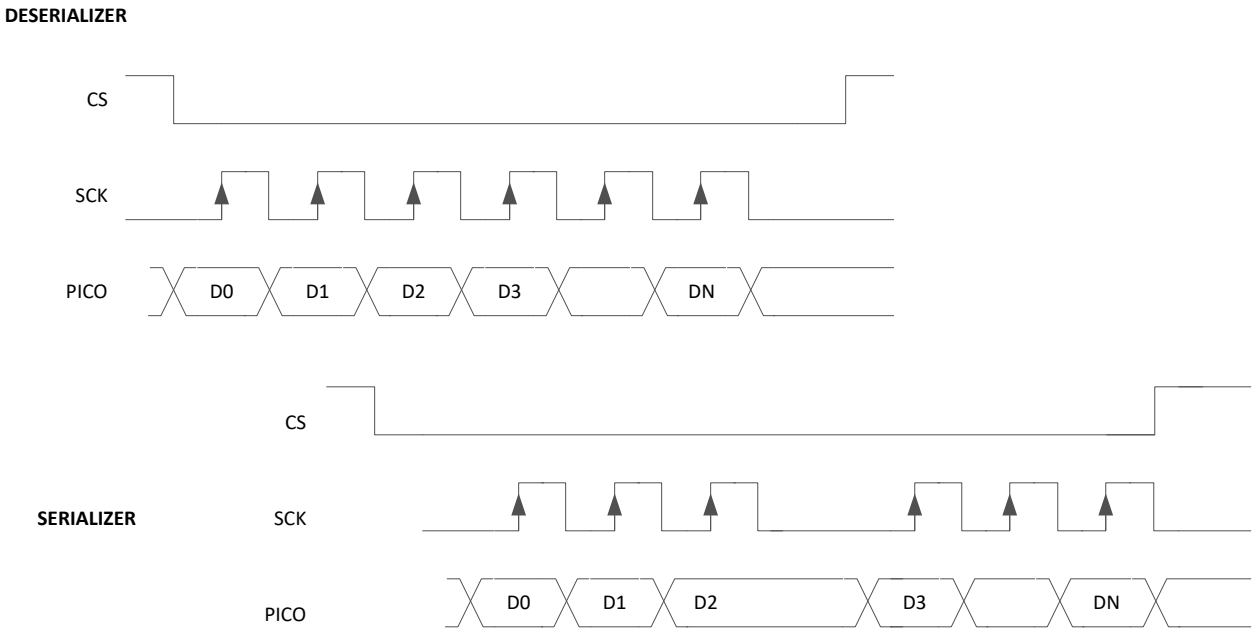


Figure 7-25. Reverse Channel SPI Write

For Reverse Channel SPI reads, the SPI controller must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in Forward channel mode. Note that at most one data/clock sample will be sent per back channel frame.

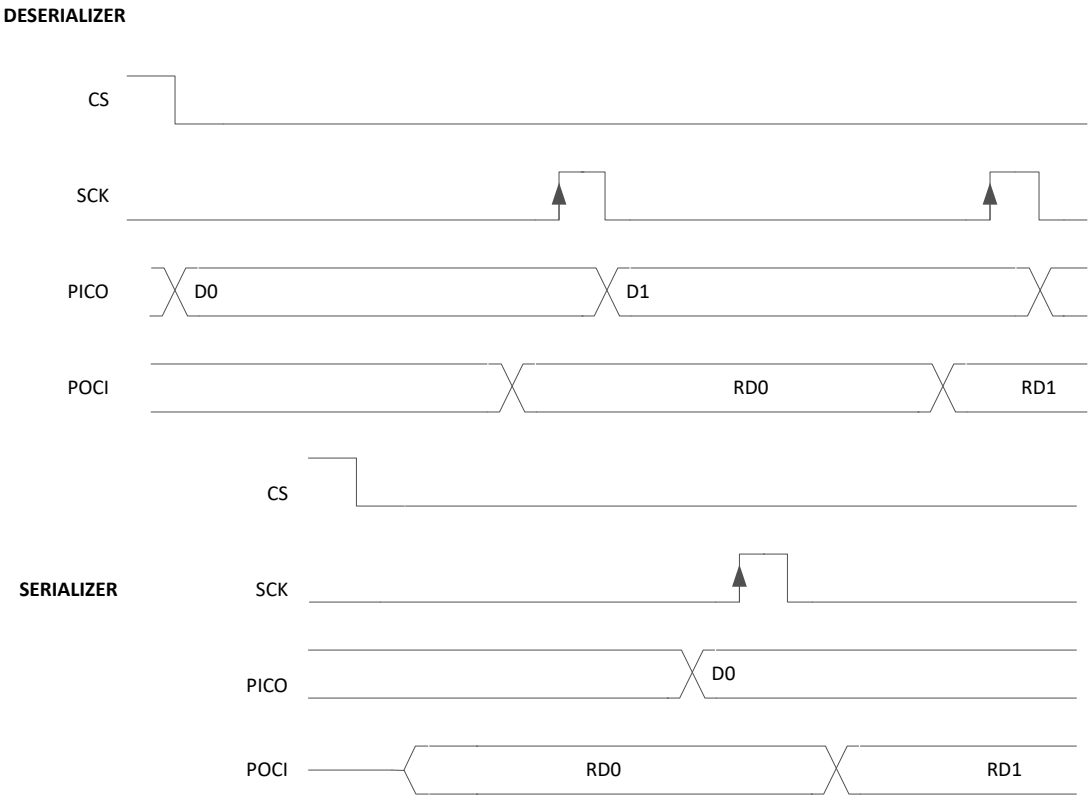


Figure 7-26. Reverse Channel SPI Read

For both Reverse Channel SPI writes and reads, the CS signal must be deasserted for at least one back channel frame period.

Table 7-37. SPI CS Deassertion Requirement

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

7.3.24.5 FPD-Link III I2S Audio

Refer to Parallel I2S in audio section for detail information.

7.3.24.6 FPD-Link III I2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames can be disabled from control registers if Forward Channel Frame Transport of I2S data is desired. In this mode, only I2S_DA is transmitted to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer. If connected to a DS90UB926Q-Q1 deserializer, I2S_DA and I2S_DB are transmitted. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[A..D]), can only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer.

7.3.24.7 FPD-Link III Pattern Generation

In backwards compatible mode the pattern generator is set in the video processor pattern generation registers like in FPD-Link IV. Depending upon the FPD-Link III mode there are some additional constraints:

1. Single Lane Mode: Only a single video processor is enabled and mapped to the appropriate FPD-Link port. Video output only on single lane.
2. Independent Mode: Two video processors are enabled and each of these video processors is mapped to a single FPD-Link port.
3. Dual Lane Mode: One video processor is enabled and mapped to FPD-Link Port 0. The video output is on both FPD-Link lanes.

7.3.24.7.1 Video Processor Pattern Generation

This method of pattern generation is the same as that used with FPD-Link IV pattern generation, in which the pattern generation configuration is done via the pattern generation registers on the Video Processor Register Page (Page_12) and the indirect access pattern generator registers.

7.3.24.7.2 FPD-Link Port Pattern Generation

This is the method of pattern generation used by previous FPD-Link III devices such as DS90Ux94x devices. In this method, the indirect access pattern generator registers will be used as well as registers 0x64-0x65 on the main page. This mode can use external timing and for proper operation PATGEN_TSEL must be programmed to 0. For detailed information on how to configure the patterns, refer to Application Note SNLA132.

7.3.24.8 FPD-Link III Built-In Self Test (BIST)

An optional at-speed FPD-Link III Built-In Self Test (BIST) feature supports testing of the high speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.24.8.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test can select the internal Oscillator clock (OSC) frequency. The user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See Figure 7-27 for the BIST mode flow diagram.

Step 1: The Serializer is paired with an FPD-Link III Deserializer, BIST Mode is enabled via the BISTEN pin or through register on the Deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x02[5] be toggled locally on the Serializer (set 0x02[5]=1, then set 0x02[5]=0). The desired clock source is selected through the deserializer BISTC pin, or through register on the Deserializer.

Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: The link returns to normal operation after the deserializer BISTEN pin is low. Figure 7-28 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they can be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

**BIST can only be disabled from the deserilizer. During BIST remote access to the deserilizer from the serializer is disabled.

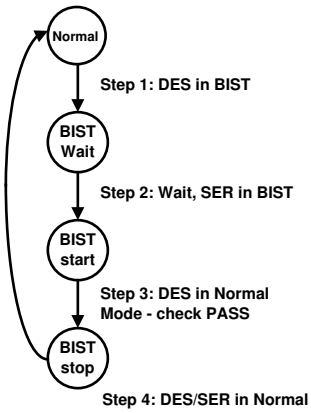


Figure 7-27. BIST Mode Flow Diagram

7.3.24.8.2 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, etc. and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0]). CRC errors are recorded in an 8-bit register in the

deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.

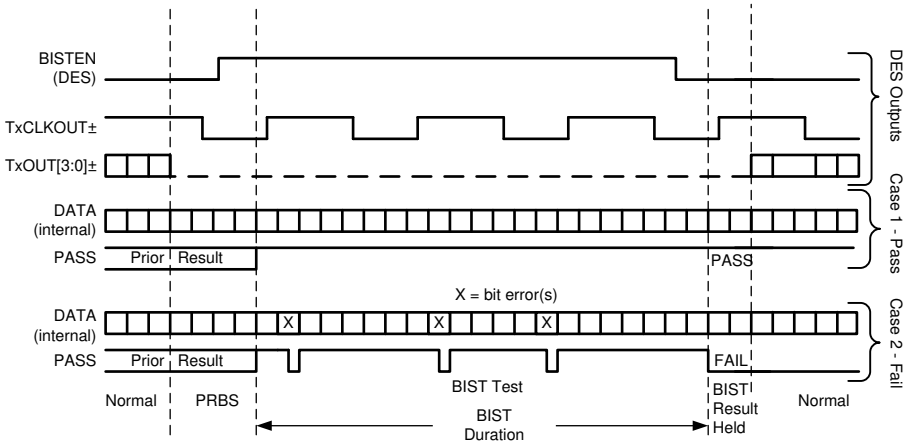


Figure 7-28. BIST Waveforms with OLDI Deserializer

7.4 Device Functional Modes

7.4.1 Mode Select Configuration Settings (MODE_SEL[0:2])

The MODE_SEL[0:2] is used to latch into the register location during power-up. The configuration of the device may be done via the MODE_SEL[0:2] input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[0:2] inputs. The 3-bit MODE_SEL strapped values can be read from TX_MODE_STS register at address 0x27[6:4] and 0x27[2:0] for MODE_SEL1 and MODE_SEL0 respectively. Changing the MODE_SEL strap settings requires PDB to be toggled. All settings strapped by MODE_SELx can be adjusted via I^2C access after power up to configure a different mode or PCLK rate.

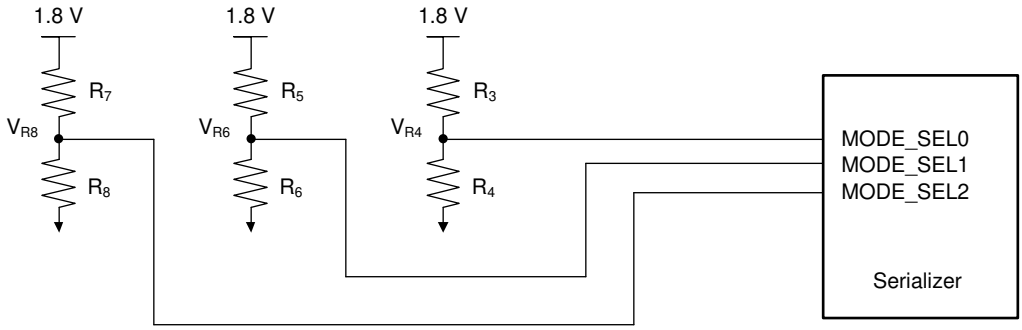


Figure 7-29. MODE_SEL[0:2] Connection Diagram

Table 7-38. MODE_SEL[0:2] Settings Selection

MODE SELECTION	MODE	FUNCTION
MODE_SEL0	FPD Mode	FPD-Link IV protocol
		Backward compatible FPD-Link III
	FPD4 Rates	13.5Gbps, 10.8Gbps, 6.75Gbps, 3.375Gbps
	FPD3 Rates	0.875Gbps (25 MHz PCLK), 2.975Gbps (85 MHz PCLK)
	Dual/Independent	Dual
		Independent

Table 7-38. MODE_SEL[0:2] Settings Selection (continued)

MODE SELECTION	MODE	FUNCTION
MODE_SEL1	SST/MST	SST
		MST
	DP/eDP	DP
		eDP
	HPD	3.3V
		1.8V
MODE_SEL2	FPD Mode	MODE_SEL0 Option Set0
		MODE_SEL0 Option Set1

MODE_SEL2 is used to strap two sets of MODE_SEL0 for options of FPD-Link modes and FPD-Link rates.

Table 7-39. Configuration Select (MODE_SEL2)

Mode #	Ratio Min (V)	Ratio Typical (V)	Ratio Max (V)	TARGET V_{R8} (V)	SUGGESTED RESISTOR PULL-UP R7 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R8 kΩ (1% tol)	FPD4 or FPD3
1	0	0	0.35	V_{IL}	OPEN	Any value less than 100	FPD4 (default)
2	0.65	0.913	1.05	V_{IH}	Any value less than 100	OPEN	FPD3

MODE_SEL0 is the strap pin for FPD mode interface (FPD-Link IV vs FPD-Link III) and FPD Dual/Independent mode. A proper strapping can ensure lock in FPD-Link mode during power-up.

Table 7-40. Configuration Select (MODE_SEL0) when (MODE_SEL2 = 0)

Mode #	Ratio Min (V)	Ratio Typical (V)	Ratio Max (V)	TARGET V_{R4} (V)	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD-Link Rate (Gbps)	TX FPD-Link Mode
1	0	0	0.115	0	OPEN	40.2	10.8	FPD4 Dual
2	0.172	0.211	0.244	0.380	95.3	25.5	10.8	FPD4 Independent
3	0.291	0.325	0.362	0.585	22.1	10.7	13.5	FPD4 Dual
4	0.408	0.441	0.464	0.794	28.0	22.1	13.5	FPD4 Independent
5	0.528	0.556	0.575	1.001	15.0	18.7	6.75	FPD4 Dual
6	0.640	0.673	0.684	1.211	14.3	29.4	6.75	FPD4 Independent
7	0.761	0.790	0.813	1.422	21.5	80.6	3.375	FPD4 Independent
8	0.874	0.926	1.0	1.667	10.0	97.6	2.975 (85 MHz)	FPD3 Independent

Table 7-41. Configuration Select (MODE_SEL0) when (MODE_SEL2 = 1)

Mode #	Ratio Min (V)	Ratio Typical (V)	Ratio Max (V)	TARGET V_{R4} (V)	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD-Link Rate (Gbps)	TX FPD-Link Mode
1	0	0	0.115	0	OPEN	40.2	0.875 (25 MHz)	FPD3 Dual
2	0.172	0.211	0.244	0.380	95.3	25.5	0.875 (25 MHz)	FPD3 Independent

Table 7-41. Configuration Select (MODE_SEL0) when (MODE_SEL2 = 1) (continued)

Mode #	Ratio Min (V)	Ratio Typical (V)	Ratio Max (V)	TARGET V_{R4} (V)	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD-Link Rate (Gbps)	TX FPD-Link Mode
3	0.291	0.325	0.362	0.585	22.1	10.7	0.875 (25 MHz)	FPD3 Single, TX0
4	0.408	0.441	0.464	0.794	28.0	22.1	0.875 (25 MHz)	FPD3 Single, TX1
5	0.528	0.556	0.575	1.001	15.0	18.7	2.975 (85 MHz)	FPD3 Dual
6	0.640	0.673	0.684	1.211	14.3	29.4	2.975 (85 MHz) FPD3 Port 0, FPD4 6.75 Port 1	FPD3 Port 0, FPD 4 Port 1
7	0.761	0.790	0.813	1.422	21.5	80.6	2.975 (85 MHz)	FPD3 Single, TX0
8	0.874	0.926	1.0	1.667	10.0	97.6	2.975 (85 MHz)	FPD3 Single, TX1

MODE_SEL1 is used to strap in combination of video interface specific settings, select multi-stream transport support, and HPD voltage.

Table 7-42. Configuration Select (MODE_SEL1)

Mode #	Ratio Min (V)	Ratio Typical (V)	Ratio Max (V)	TARGET V_{R6} (V)	SUGGESTED RESISTOR PULL-UP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R6 kΩ (1% tol)	HPD (V)	SST/MST	DP/eDP
1	0	0	0.115	0	OPEN	40.2	3.3	SST	DP
2	0.172	0.211	0.244	0.380	95.3	25.5	3.3	MST	DP
3	0.291	0.325	0.362	0.585	22.1	10.7	1.8	SST	DP
4	0.408	0.441	0.464	0.794	28.0	22.1	1.8	MST	DP
5	0.528	0.556	0.575	1.001	15.0	18.7	3.3	SST	eDP
6	0.640	0.673	0.684	1.211	14.3	29.4	3.3	MST	eDP
7	0.761	0.790	0.813	1.422	21.5	80.6	1.8	SST	eDP
8	0.874	0.926	1.0	1.667	10.0	97.6	1.8	MST	eDP

The strapped values can be viewed and/or modified in the following locations:

- FPD-Link Mode: Latched to register 0x5[5:2]
- FPD-Link III Mode: Latched to register 0x59[2:0]

Changing the FPD-Link Mode will also cause the PLL settings to be changed, which will be reflected in Page 2: FPD PLL registers.

7.4.2 FPD-Link IV Modes of Operation

The FPD-Link IV transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The FPD-Link Port mode is set via the FPD_TX_MODE[5:2] register. See Backward Compatibility modes. The following modes are supported in FPD-Link IV mode:

7.4.2.1 Single Link Operation

Single Link mode transmits the video over FPD-Link Port 0 to a single receiver. To enter FPD-Link IV single mode, set FPD4_TX_MODE[5:2] = 0xB or 0xE for FPD4 Port0 and FPD4 Port1 respectively.

7.4.2.2 Independent Link Operation

Independent Link mode transmits video over two FPD-Link ports, which each FPD-Link port being sent to a single receiver. Independent mode is configured by setting the register to FPD_TX_MODE[5:2] = 0xF. When the

FPD_TX_MODE is changed from independent to dual mode or vice-versa, a soft reset requires to change the mode, and the link is established correctly.

7.4.2.3 Dual Link Operation

In Dual Link mode, the FPD-Link IV TX splits a single video stream and sends alternating pixels on two downstream links. The receiver must be capable of receiving the dual-stream video. Dual link mode is supports a total line rate of 27 Gbps over dual FPD-Link channels or 13.5 Gbps over single FPD-Link channel. Bidirectional control channels functions such as GPIOs and I^2C transfer are handled independently on Port 0 and Port 1, as in independent mode. Independent mode is configured by setting the register to FPD4_TX_MODE[5:2] = 0xA.

7.5 Programming

7.5.1 I^2C Serial Control Bus

7.5.1.1 I^2C Device Address

The DS90UB983-Q1 implements three I^2C-compatible serial control buses. The I^2C is for local device configuration and incorporates a Bidirectional Control Channel (BCC) that allows communication across the FPD-Link cable with remote deserializers as well as remote I^2C target devices. The DS90UB983-Q1 implements three I^2C compatible targets and three I^2C controller (sends I^2C commands on all three I^2C ports) capable of operation with Standard, Fast, Fast-plus and High Speed. This allows for remote I^2C operation up to 1 MHz and local I^2C operation up to 3.4 MHz. The 3.4 MHz communication is not supported when all three I^2C ports operate I^2C transaction simultaneously. In high-speed mode accessing to the local registers can only support up to two ports.

For accesses to local registers, the I^2C targets operate without stretching the clock. Accesses to remote devices over the Bidirectional Control Channel results in clock stretching to allow for response time across the link. The DS90UB983-Q1 can also act as I^2C Controller for regenerating Bidirectional Control Channel accesses originating from the remote devices across FPD-Link.

The primary device address is set via a resistor divider (R1 and R2 — see Figure 7-30 below) connected to the IDx pin. Each of the three I^2C ports has a dedicated target address. By default, the target address of I^2C target 0 is set to the primary I^2C address corresponding to the IDx pin. I^2C target 0 is the primary I^2C address (7-bit form) plus one and I^2C target 1 is the primary I^2C address (7-bit form) plus two, and I^2C target 2 is the primary I^2C address (7-bit form) plus three. For instance, if the primary I^2C address is set to 0x18, I^2C target 0 has a target address of 0x18, I^2C target 1 has a target address of 0x1A, and and I^2C target 2 has a target address of 0x1C. These addresses can be overwritten using the DEV_ID register, which has three copies, one for each I^2C target.

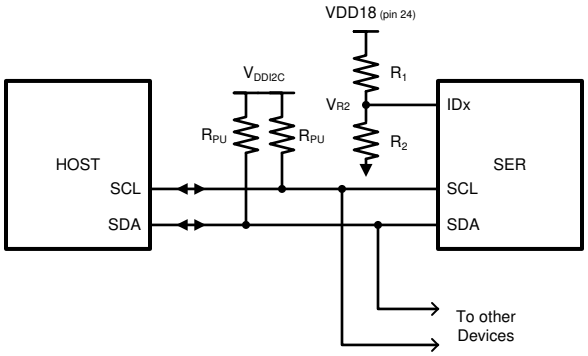


Figure 7-30. I^2C Connection

The IDx pin configures the control interface to one of four possible device addresses. A pull-up resistor and a pull-down resistor can be used to set the appropriate voltage on the IDx input pin. See below.

Table 7-43. Serial Control Bus Addresses For IDx

MODE #	RATIO TYPICAL	VR2 (V); VDD = 1.8	I²C Voltage Level	SUGGESTED RESISTOR PULL-UP R1 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R2 kΩ (1% tol)	7-BIT ADDRESS I²C Target 0	8-BIT ADDRESS I²C Target 0	8-BIT ADDRESS I²C Target 1	8-BIT ADDRESS I²C Target 2
1	0	0	1.8	OPEN	10.0	0x0C	0x18	0x1A	0x1C
2	0.213	0.384	1.8	42.2	11.5	0x10	0x20	0x22	0x24
3	0.327	0.589	1.8	29.4	14.3	0x14	0x28	0x2A	0x2C
4	0.441	0.793	1.8	28.7	22.6	0x18	0x30	0x32	0x34
5	0.551	0.999	3.3	15	18.7	0x0C	0x18	0x1A	0x1C
6	0.671	1.208	3.3	13.7	28	0x10	0x20	0x22	0x24
7	0.787	1.417	3.3	16.2	60.4	0x14	0x28	0x2A	0x2C
8	1	1.8	3.3	10.0	OPEN	0x18	0x30	0x32	0x34

7.5.1.2 I²C Bus Operation

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD18} or V_{DD33}. The pull-up resistor value can be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low. Refer to "*I2C Bus Pullup Resistor Calculation*, SLVA689" to determine the pull-up resistor value for the SCL and SDA rise time.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions Low while SCL is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 7-31

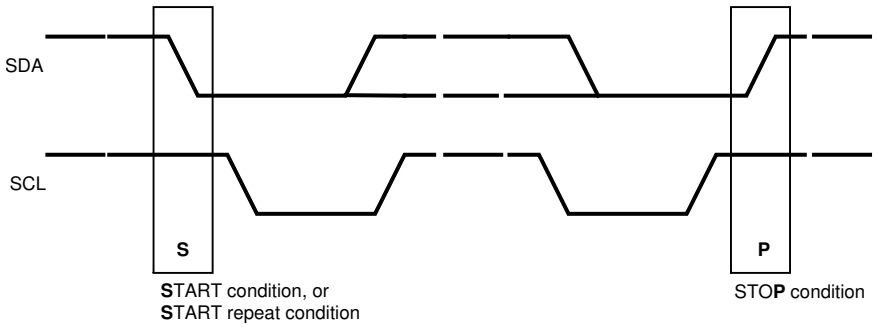


Figure 7-31. Start And Stop Conditions

To communicate with an I²C target, the host controller sends the target address and listens for a response from the target. This response is referred to as an acknowledge bit (ACK). If a target on the bus is addressed correctly, the controller Acknowledges (ACKs) by driving the SDA bus low. If the address doesn't match a device's target address, the controller Not-acknowledges (NACKs) by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the controller is writing data, the target ACKs after every data byte is successfully received. When the controller is reading data, the controller ACKs after every data byte is received to let the target know the controller wants to receive another data byte. When the controller wants to stop reading, the controller NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition.

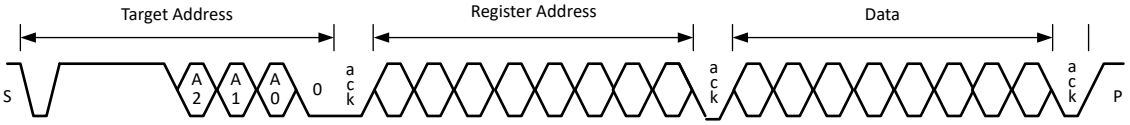


Figure 7-32. Serial Control Bus — Write

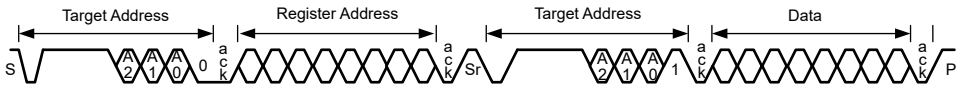


Figure 7-33. Serial Control Bus — Read

The I²C controller located at the serializer must support I²C clock stretching. For more information on I²C interface requirements and throughput considerations, please refer to TI Application Note SNLA131.

The serializer includes several different mechanisms to prevent I²C bus hangs:

- I²C Bus Arbitrator
- I²C Bus Timeout
- BCC Watchdog Timer

The I²C bus arbitrator function is designed to prevent one I²C target device of the SER holding the other I²C targets from accessing the BCC. An example of this timeout is when an I²C target's CLK is held by the controller during a transfer between Device address and Offset address phase or between Offset address phase and a repeated start phase for a long period of time. The timer starts after the SER I²C target receives a START command, and expires after the timeout period set by ARB_TIMEOUT (register 0x3[6:5]) if the SER I²C target does not receive a STOP command. When the ARB_TIMEOUT occurs, a STOP signal is internally generated by the SER and sent to the DES through the BCC. The arbiter to access BCC is now free to be used by the other I²C targets of the SER. The STOP signal is passed on the remote DES I²C bus. The I²C bus arbitrator can be disabled by setting ARB_TIMEOUT_DISABLE = 1 in register 0x3[7]. The I²C bus arbitrator can be safely disabled without consequence if the system implementation does not utilize more than one I²C bus on the SER device or if the system has provisions put in place to make sure that I²C transactions from multiple controllers on the SER side do not attempt to simultaneously communicate using multiple I²C target devices of the SER.

The I²C bus timeout function is designed to make sure that the local I²C bus is free in the case where the SER is configured to act as a proxy I²C controller on the bus (if an I²C controller on the remote DES side initiates a command to access a device attached to the local SER I²C bus through the BCC). The I²C bus timer starts when the SER proxy I²C controller has started a command, and expires after either 1 second or 50us (based on the setting of I2C_BUS_TIMER_SPEEDUP in register 0x3[1]) if no toggling of SDA is detected while SCL is HIGH. When the timeout occurs, the SER internally generates a NACK signal and sends to the remote DES through the BCC to free the DES I²C bus. The I²C bus timeout feature can be disabled by setting I2C_BUS_TIMER_DISABLE = 1 in register 0x3[0]. The I²C bus timer must not be disabled if the system implementation is configured to use the proxy I²C controller functionality of the SER (when a remote controller device attached to the DES I²C bus needs to access a target I²C device on the SER I²C bus through the BCC). The I2C_BUS_TIMER_SPEEDUP function can be used to reduce the timeout period of the I²C controller on the DES side if that controller needs to access a remote target on the SER side more quickly after initial power up of the FPD-Link.

The BCC watchdog timer is designed to prevent the local SER I²C bus from stretching the I²C CLK beyond an acceptable time period. This timeout can potentially happen when trying to access a remote DES or remote I²C target attached to the remote DES. The timer starts after the SER receives a START command from the local I²C target. The timer expires after the timeout period set by BCC_WATCHDOG_TIMER (register 0x29[7:1]) if the SER does not receive a response from the remote deserializer through the BCC. When the timeout happens, a NACK is sent to the local I²C controller attached to the SER. The BCC watchdog timeout can be disabled by setting BCC_WDOG_DIS = 1 in register 0x29[0], however disabling the BCC watchdog timer under any typical system configuration is not recommended, as the lack of a timeout can lock the I²C bus if any transaction is issued over the BCC when the FPD-Link is not yet LOCKed, or if there is an error in the BCC I²C transaction.

7.5.2 Bidirectional Control

The Bidirectional Control Channel (BCC) is compatible with I²C devices, allowing local I²C target access to device registers as well as bidirectional I²C operation across the link to the deserializer and attached devices. I²C access must not be attempted across the link when TX Port Lock status is Low.

7.5.3 I²C Target Operation

The DS90UB983-Q1 implements three I²C-compatible targets capable of operation compliant to the Standard, Fast, and Fast-plus modes of operation allowing I²C operation at up to 1 MHz clock frequencies (up to 3.4 MHz for local bus access). Local I²C transactions to access DS90UB983-Q1 registers can be conducted 2 ms after power supplies are stable and PDB is brought high. For accesses to local registers, the I²C target operates without stretching the clock (except when multiple I²C targets are being used to access the DS90UB983-Q1 registers simultaneously). Make sure that control registers for indirect access registers (e.g. 0x40-0x42) are not being accessed simultaneously by multiple I²C controllers. In cases where multiple I²C controllers attempt to access the same DS90UB983-Q1 register at the same time, priority is given to I²C Port 0, Port 1, followed by Port 2, and lastly I²C commands sent over the back channel.

A spurious one-byte I²C read or write transaction with a random address can be observed on the local bus when a downstream deserializer is reset, powered-on/off, hot-plugged, or connected/disconnected. On the serializer or deserializer, remote downstream I²C transactions can be disabled to prohibit the potential I²C transactions from being acknowledged. On the serializer, set main page register I2C_CTRL_CHAIN_CTL2 (0x3A) to 0x88 to disable I²C transactions from a remote controller. On the deserializer, set main page register TX_I2C_CONTROLLER_DISABLE (0x08[5]) to disable I²C transactions originating from a downstream controller.

7.5.4 Remote Target Operation

The Bidirectional Control Channel provides a mechanism to read or write I²C registers in remote devices over the FPD-Link interface. The I²C Controller located at the deserializer must support I²C clock stretching. Accesses to serializers or remote target devices over the Bidirectional Control Channel results in clock stretching to allow for response time across the link. The DS90UB983-Q1 acts as an I²C target on the local bus, forwards read and write requests to the remote device, and returns the response from the remote device to the local I²C bus. To allow for the propagation and regeneration of the I²C transaction at the remote device, the DS90UB983-Q1 stretches the I²C clock while waiting for the remote response.

To communicate with a remote target device, a routing mechanism is used to send BCC commands from a source to destination based on system topology. The serializer or deserializer that is connected to the host controller must control the BCC routing. If the DS90UB983-Q1 is not connected to the host controller, consult the appropriate serializer or deserializer data sheet for details on how to configure bidirectional channel communication routing. To enable remote target operation, register 0x07 [3] must be set to enable I²C pass through mode for each I²C Bus. For example, to configure I²C Port 0 to communicate with remote devices, I²C Port 0, register 0x07[3] must be set by an I²C controller attached to port 0 and to configure I²C Port 1 to communicate with remote devices, I²C Port 1, register 0x07[3] must be set by an I²C controller attached to Port 1. If the DS90UB983-Q1 is connected to host controller, registers TARGET_ALIAS_x(0x70 - 0x77), TARGET_ALIAS_x(0x78 - 0x7F), and TARGET_DEST_x(0x88 - 0x8F) are grouped together to control the direction, routing port, source and destination of bidirectional communication. Each I²C port has a copy of TARGET_ALIAS_x(0x70 - 0x77), TARGET_ALIAS_x(0x78 - 0x7F), and TARGET_DEST_x(0x88 - 0x8F) registers. A description of these registers are listed in Table 7-44.

Table 7-44. Bidirectional Channel Communication Over Daisy-Chain Registers

Register Name	Bits	Bits Name	Description
TARGET_ID_x	7:1	TARGET_IDx	7-bit Remote target Device ID x Configures the physical I²C address of the remote I²C target device attached to the remote deserializer. If an I²C transaction is addressed to the target Alias ID x, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the deserializer.
	0	RESERVED	Reserved

Table 7-44. Bidirectional Channel Communication Over Daisy-Chain Registers (continued)

Register Name	Bits	Bits Name	Description
TARGET_ALIAS_x	7:1	TARGET_ALIAS_IDx	7-bit Remote target Device Alias ID x Configures the decoder for detecting transactions designated for an I^2C target device attached to the remote deserializer. The transaction is remapped to the address specified in the target ID x register. A value of 0 in this field disables access to the remote I^2C target.
	0	LCL_PORTSEL_IDx	In a remote I^2C transaction, this bit directs the transaction to either take Port 0 or Port 1 of the local FPD-Link to hop to the next device.
TARGET_DEST_x	7:5	DEST_ADDR	Destination port selection See Table 7-45
	4	FIRST_DC_PSEL	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
	3	MID_DC_PSEL	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
	2	FINAL_DC_PSEL	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
	1:0	REMAINING_DEPTH	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth

TARGET_ID_x controls the BCC message routing directions. When this bit is set to 0, BCC messages are routed to downstream devices. Set to one has no effect.

TARGET_ALIAS_x controls the BCC message routing ports. When this bit is set to 1, BCC messages are routed through either RX port 1 or daisy-chain TX port 1 depending on TARGET_ID_x[0] settings. When this bit is set to 0, BCC messages are routed through either RX port 0 or daisy-chain TX port 0 depending on TARGET_ID_x[0] settings.

TARGET_DEST_x controls the destination port selections (bit 2:0), depth 1 port selection (bit 3), depth 2 port selection (bit 4), depth 3 port selection (bit 5), and remaining depth (bit 7:6). Available destination port selections are listed in Table 7-45.

Table 7-45. Destination Port Selections

TARGET_DEST_x[7:5]	DS90UB983-Q1 Serializer	DS90Ux98x Deserializer(1)
000	I^2C Port 0	I^2C Port 0
001	I^2C Port 1	I^2C Port 1
010	I^2C Port 2	Reserved
011-111	Reserved	Reserved

(1) Refer to corresponding DS90Ux98x data sheet.

Daisy-chain operation supports a maximum of three daisy-chain devices. Depths 1, 2 , and 3 port selection bit controls the forwarding port selection of the corresponding daisy-chain device.

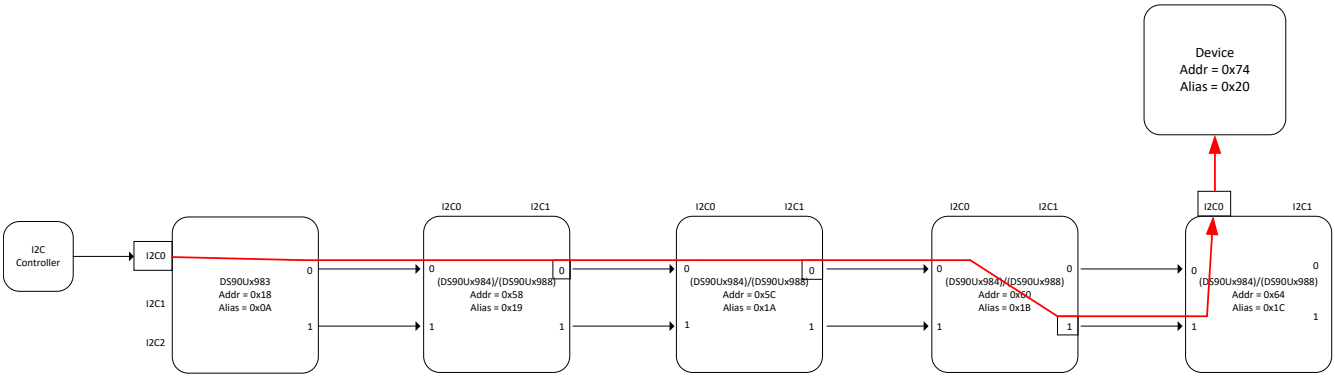


Figure 7-34. Daisy-Chain Communication Example #1

Table 7-46. Daisy-Chain Communication Example #1

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111010	0x74
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0010000	0x20
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	000	0x07
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	1	
	1:0	REMAINING_DEPTH[1:0]	11	

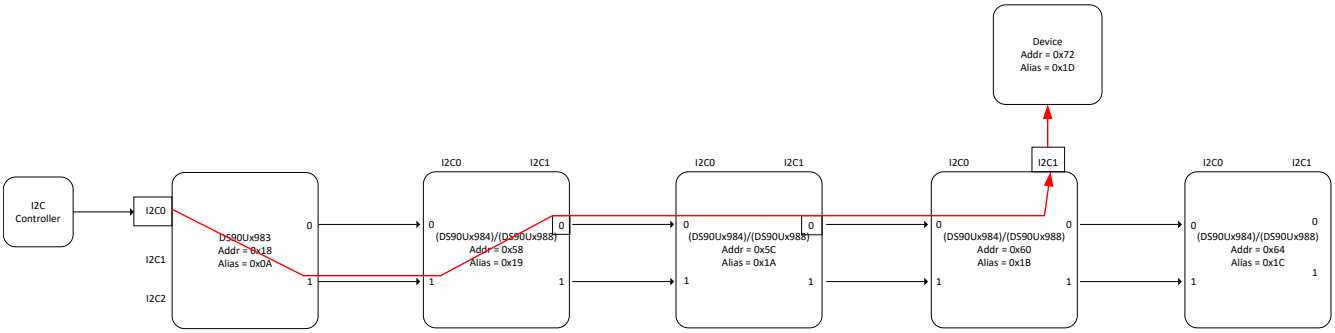


Figure 7-35. Daisy-Chain Communication Example #2

Table 7-47. Daisy-Chain Communication Example #2

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111 001	0x72
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0001110	0x1D
	0	LCL_PORTSEL_ID0	1	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	001	0x22
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

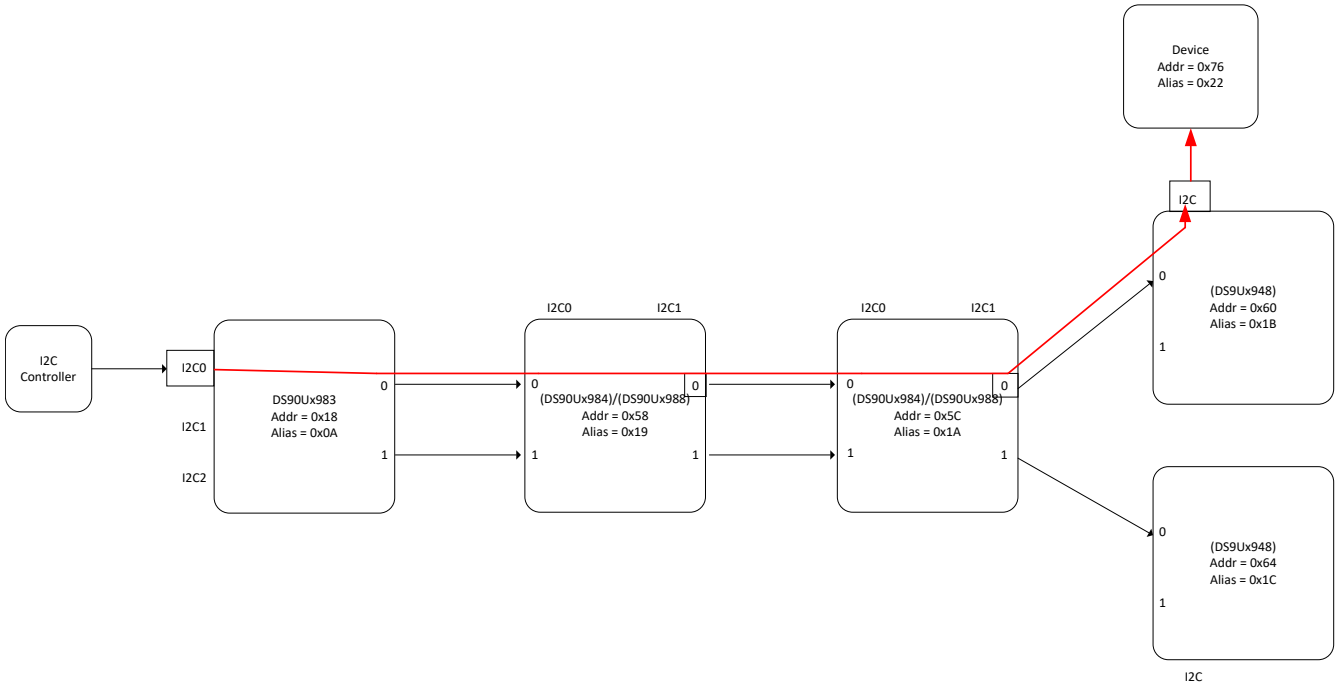


Figure 7-36. Daisy-Chain Communication Example #3

Table 7-48. Daisy-Chain Communication Example #3

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111 011	0x76
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0010001	0x22
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	000	0x02
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

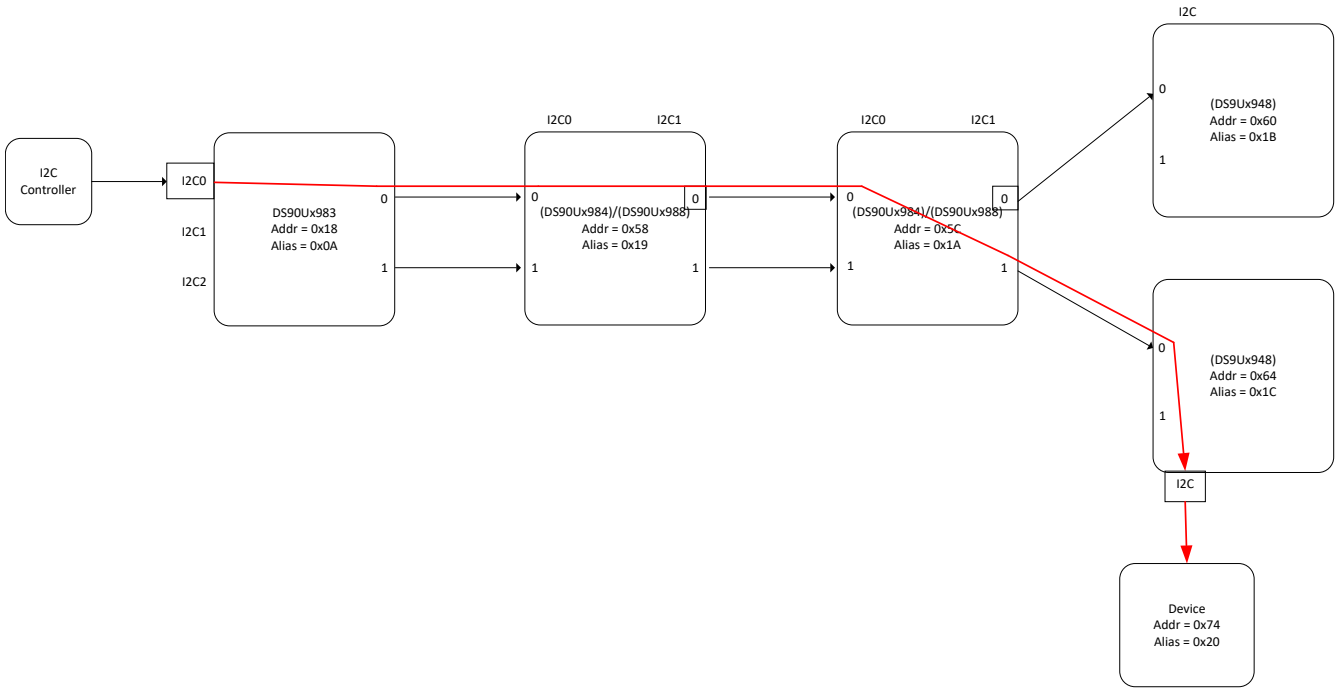


Figure 7-37. Daisy-Chain Communication Example #4

Table 7-49. Daisy-Chain Communication Example #2

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111 010	0x74
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0010000	0x20
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	000	0x06
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	1	
	1:0	REMAINING_DEPTH[1:0]	10	

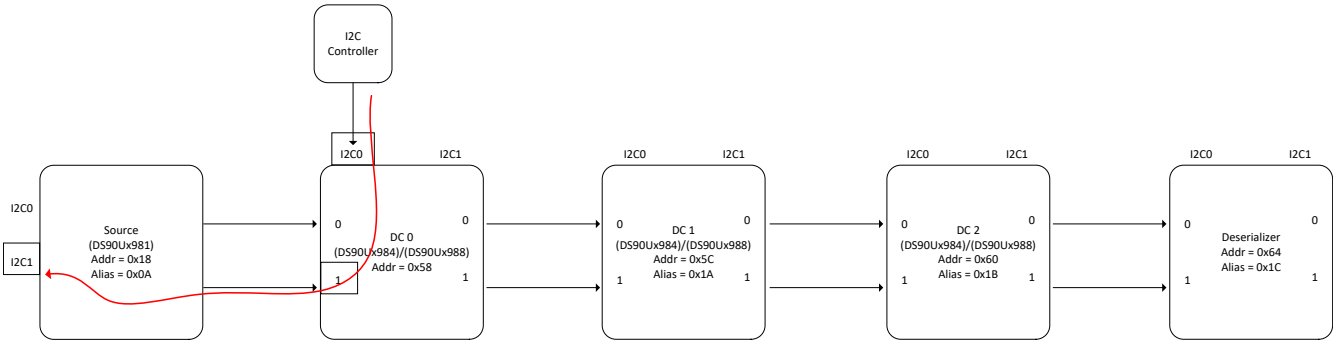


Figure 7-38. BCC Communication Upstream Example

Table 7-50. BCC Communication Upstream Example

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0001 1000	0x18
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0000101	0x0B
	0	LCL_PORTSEL_ID0	1	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	001	0x20
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	0	

Daisy-chain operation supports a maximum of three daisy-chain devices plus one additional deserializer. Depths 1, 2, and 3 port selection bit controls the forwarding port selection of the corresponding daisy-chain device.

7.5.4.1 Remote Target Addressing

Various system use cases require multiple devices with the same fixed I^2C target address to be remotely accessible from the same I^2C bus at the serializer. The DS90UB983-Q1 provides target ID virtual addressing to differentiate target target addresses when connecting two or more remote devices. Eight pairs of Target Alias and Target ID registers are allocated for each I^2C target in registers 0x70 through 0x7F. The alias registers allow programming virtual addresses which the host controller uses to access remote devices. The Target ID register provides the actual target address for the device on the remote I^2C bus. Because eight pairs of registers are available for each I^2C target (total of 24 pairs), multiple devices can be directly accessible remotely without the need for reprogramming. Multiple aliases can be assigned to the same Target ID as well.

7.5.5 Multi-Controller Arbitration Support

The Bidirectional Control Channel implements I^2C compatible bus arbitration in the proxy I^2C controller implementation. When sending a data bit, each I^2C controller senses the value on the SDA line. If the controller is sending a logic 1 but senses a logic 0, the controller has lost arbitration. The controller stops driving SDA, retrying the transaction when the bus becomes idle. Thus, multiple I^2C controllers can be implemented in the system.

If the system does require controller-target operation in both directions across the BCC, some method of communication must be used to make sure only one direction of operation occurs at any time. The communication method can include using available read/write registers in one of the devices to allow controllers to communicate with each other to pass control between the two controllers.

7.5.6 I²C Restrictions on Multi-Controller Operation

The I²C specification does not provide for arbitration between controllers under certain conditions. The system must make sure the following conditions cannot occur to prevent undefined conditions on the I²C bus:

- One controller generates a repeated Start while another controller is sending a data bit.
- One controller generates a Stop while another controller is sending a data bit.
- One controller generates a repeated Start while another controller sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I²C target.

7.5.7 Multi-Controller Access to Device Registers

When using the latest generation of FPD-Link devices, main page registers can be accessed simultaneously from both local and remote I²C controllers. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I²C targets is still allowed in only one direction at a time.

7.5.8 Indirect Register Page Access Through Alternative Device Address

Alternatively to using the indirect register access registers (0x40, 0x41, 0x42) the indirect register pages can be accessed and modified by using an alternative I²C address. To set the I²C address set register IND_REG_I2C_IDX (0xF9, 0xFB, 0xFD, 0xFF), to set the indirect register page set IND_REG_I2C_CTLx (0xF8, 0xFA, 0xFC, 0xFE). All of these I²C addresses can then be accessed from local I²C controllers attached to the device. For remote I²C access using the direct access option, only IND_REG_ID0 can be mapped one page at a time.

An I²C controller on the deserializer can only use the I²C address IND_REG_I2C_ID0 (0xF9) to access the corresponding indirect register page that is set in register IND_REG_I2C_CTL0(0xF8).

7.5.9 Unique ID

Each device is programmed with a Unique ID that is burnt into devices at Wafer level. Unique ID with a 12 bytes customer readable value indicating wafer lot and position of each IC inside a wafer. Combination of UniqueIDs can be read and maintained by customer in a database or in a Hash table. Each system can be identified by the UniqueID programmed into the devices. Authenticity of the overall system can be established at the powerup/initialization or periodically by checking the UniqueID.

A Unique ID is programmed into each device and can be read using I^2C reads. To read the Unique ID, set the APB_SELECT (0x48[7:3]) register to DIE ID (00011) then set registers APB_ADRx (0x49 and 0x4A) to the Unique ID register being read, then read the APB_DATA0 register. There are 12 Unique ID registers, each of the registers contain 8 bits of the total unique ID. The table below lists the Unique ID APB registers addresses.

Table 7-51. Unique ID Registers

APB register	APB address (APB_ADR0 = APB address[0:7], APB_ADR1 = APB address[8:15])
UNIQUE_ID_0	0x0000
UNIQUE_ID_1	0x0001
UNIQUE_ID_2	0x0002
UNIQUE_ID_3	0x0003
UNIQUE_ID_4	0x0004
UNIQUE_ID_5	0x0005
UNIQUE_ID_6	0x0006
UNIQUE_ID_7	0x0007
UNIQUE_ID_8	0x0008
UNIQUE_ID_9	0x0009
UNIQUE_ID_10	0x000A
UNIQUE_ID_11	0x000B

7.5.10 FPD-Link Lock

The deserializer's PLL locks onto the FPD-Link signal sent out of the DS90UB983-Q1 and constantly send the lock status to the DS90UB983-Q1 across the back channel. The DS90UB983-Q1 displays this lock status in the RX_LOCK_DET (0x0C[6]) register. If the forward channel signal or back channel signal are disrupted then the DS90UB983-Q1 indicates a loss of lock. If the deserializer is locked onto the forward channel signal and the back channel signal is disrupted then the DS90UB983-Q1 indicates a loss of lock.

7.5.11 ESD Event Counter

The ESD event counter tracks the number of ESD events experienced by the device. These ESD events are counted when the integrated ESD structure is activated. The ESD event counter is enabled by default and must be cleared to 0 on power up by writing a 0 and then a 1 to the ESD_EVENT_COUNTER_ENABLE (0xBC[6]) as power supply transients can cause the ESD event counter to increment. The number of ESD events can be read in the ESD_EVENT_COUNTER (0xBC[5:0]) register. There is no ESD dead-time built into the counter, which means that even with a single pulse event more than one ESD event can be logged. The ESD event counter can not count ESD events on the FPD-Link lines themselves because the external CMC's and ESD protection can prevent the device's ESD structure from triggering. The ESD_EVENT_COUNTER (0xBC[5:0]) register does not clear when the device is reset through registers or through the PDB pin. To clear the ESD_EVENT_COUNTER (0xBC[5:0]) register to 0 set the ESD_EVENT_COUNTER_ENABLE (0xBC[6]) register to 0 then 1.

7.6 Register Maps

The DS90UB983-Q1 implements the following register blocks, accessible via I^2C including over the bidirectional control channel:

- Shared Registers
- FPD-Link TX Port Registers (separate register block for each of the TX ports)

- I²C Port Registers (separate register block for each of the I²C ports)

Table 7-52. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP		
0x00	I²C Port Registers	I2C Target 0	I2C Target 1	I2C Target 2
0x01-0x06	Digital Shared Registers	Shared		
0x07-0x08	I²C Port Registers	I2C Target 0	I2C Target 1	I2C Target 2
0x09-0x16	Digital TX Port Registers	FPD TX Port 0 *R: 0x2D[5:4]=00*	FPD TX Port 1 *R: 0x2D[5:4]=01*	
0x17-0x2C	Digital Shared Registers			
0x2D	I²C Port Registers	I2C Target 0	I2C Target 1	I2C Target 2
0x2E-0x56	Digital Shared Registers	Shared		
0x57-0x6F	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1	
0x70-0x7F	I²C Port Registers	I2C Target 0	I2C Target 1	I2C Target 2
0x80-0xA3	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1	
0xA4-0xBF	Digital Shared Registers	Shared		
0xC0-0xFF	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1	

7.6.1 Page 0: UB MainPage Registers

Table 7-53 lists the memory-mapped registers for the Page 0: UB MainPage registers. All register offset addresses not listed in Table 7-53 should be considered as reserved locations and the register contents should not be modified.

Table 7-53. PAGE 0: UB MAINPAGE Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG2	GENERAL_CFG2	Go
0x3	I2C_CONTROLLER_CFG	I2C_CONTROLLER_CFG	Go
0x5	FPD4_CFG	FPD4_CFG	Go
0x6	GENERAL_STS2	GENERAL_STS2	Go
0x7	GENERAL_CFG	GENERAL_CFG	Go
0x8	DES_ID	DES_ID	Go
0x9	BC_DUTY_CYC	BC_DUTY_CYC	Go
0xA	CRC_ERROR0	CRC_ERROR0	Go
0xB	CRC_ERROR1	CRC_ERROR1	Go
0xC	GENERAL_STS	GENERAL_STS	Go
0xD	FPD4_DATAPATH_CTL	FPD4_DATAPATH_CTL	Go
0xE	FPD4_DATAPATH_CTL2	FPD4_DATAPATH_CTL2	Go
0xF	BIST_BC_ERRORS	BIST_BC_ERRORS	Go
0x10	FPD3_DES_CAP1	FPD3_DES_CAP1	Go
0x11	FPD3_DES_CAP2	FPD3_DES_CAP2	Go
0x12	FPD4_REMOTE_PAR_CAP1	FPD4_REMOTE_PAR_CAP1	Go
0x13	FPD4_REMOTE_PAR_CAP2	FPD4_REMOTE_PAR_CAP2	Go
0x14	TX_BIST_CTL	TX_BIST_CTL	Go
0x15	FC_GPIO_CTL0	FC_GPIO_CTL0	Go
0x16	FC_GPIO_CTL1	FC_GPIO_CTL1	Go
0x17	GPIO0_PIN_CTL	GPIO0_PIN_CTL	Go
0x18	GPIO1_PIN_CTL	GPIO1_PIN_CTL	Go
0x19	GPIO2_PIN_CTL	GPIO2_PIN_CTL	Go
0x1A	GPIO3_PIN_CTL	GPIO3_PIN_CTL	Go
0x1B	GPIO4_PIN_CTL	GPIO4_PIN_CTL	Go
0x1C	GPIO5_PIN_CTL	GPIO5_PIN_CTL	Go
0x1D	GPIO6_PIN_CTL	GPIO6_PIN_CTL	Go
0x1E	GPIO7_PIN_CTL	GPIO7_PIN_CTL	Go
0x1F	GPIO8_PIN_CTL	GPIO8_PIN_CTL	Go
0x20	GPIO9_PIN_CTL	GPIO9_PIN_CTL	Go
0x21	GPIO10_PIN_CTL	GPIO10_PIN_CTL	Go
0x22	GPIO11_PIN_CTL	GPIO11_PIN_CTL	Go
0x23	GPIO12_PIN_CTL	GPIO12_PIN_CTL	Go
0x24	GPIO13_PIN_CTL	GPIO13_PIN_CTL	Go
0x25	GPI_PIN_STS1	GPI_PIN_STS1	Go
0x26	GPI_PIN_STS2	GPI_PIN_STS2	Go
0x27	TX_MODE_STS	TX_MODE_STS	Go
0x28	GPIO_EN_BC	GPIO_EN_BC	Go
0x29	BCC_WDOG_CTL	BCC_WDOG_CTL	Go

Table 7-53. PAGE 0: UB MAINPAGE Registers (continued)

Address	Acronym	Register Name	Section
0x2A	I2C_CONTROL	I2C_CONTROL	Go
0x2B	SCL_HIGH_TIME	SCL_HIGH_TIME	Go
0x2C	SCL_LOW_TIME	SCL_LOW_TIME	Go
0x2D	TX_PORT_SEL	TX_PORT_SEL	Go
0x2E	LINK_DET_CTL	LINK_DET_CTL	Go
0x2F	IO_CTL	IO_CTL	Go
0x30	DEVICE_REV_ID	DEVICE_REV_ID	Go
0x31	PLL_REFCLK_FREQ	PLL_REFCLK_FREQ	Go
0x32	XO_REFCLK_FREQ	XO_REFCLK_FREQ	Go
0x38	I2C_CTRL_CHAIN_CTL1	I2C_CTRL_CHAIN_CTL1	Go
0x39	I2C_CTRL_CHAIN_CTL2	I2C_CTRL_CHAIN_CTL2	Go
0x3A	I2C_CTRL_CHAIN_CTL3	I2C_CTRL_CHAIN_CTL3	Go
0x3C	MAILBOX_3C	MAILBOX_3C	Go
0x3D	MAILBOX_3D	MAILBOX_3D	Go
0x3E	GPIO_IN_EN_HIGH	GPIO_IN_EN_HIGH	Go
0x3F	GPIO_IN_EN_LOW	GPIO_IN_EN_LOW	Go
0x40	IND_ACC_CTL	IND_ACC_CTL	Go
0x41	IND_ACC_ADDR	IND_ACC_ADDR	Go
0x42	IND_ACC_DATA	IND_ACC_DATA	Go
0x43	VP_CONFIG_REG	VP_CONFIG_REG	Go
0x44	VP_ENABLE_REG	VP_ENABLE_REG	Go
0x46	VP_GLOBAL_ISR	VP_GLOBAL_ISR	Go
0x47	BCC_CONFIG	BCC_CONFIG	Go
0x48	APB_CTL	APB_CTL	Go
0x49	APB_ADR0	APB_ADR0	Go
0x4A	APB_ADR1	APB_ADR1	Go
0x4B	APB_DATA0	APB_DATA0	Go
0x4C	APB_DATA1	APB_DATA1	Go
0x4D	APB_DATA2	APB_DATA2	Go
0x4E	APB_DATA3	APB_DATA3	Go
0x51	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x52	INTERRUPT_STS	INTERRUPT_STS	Go
0x53	AUDIO_CFG	AUDIO_CFG	Go
0x54	SPI_TIMING1	SPI_TIMING1	Go
0x55	SPI_TIMING2	SPI_TIMING2	Go
0x56	SPI_CONFIG	SPI_CONFIG	Go
0x57	FPD3_STREAM_SEL	FPD3_STREAM_SEL	Go
0x58	FPD3_DUAL_STS	FPD3_DUAL_STS	Go
0x59	FPD3_MODE_CTL	FPD3_MODE_CTL	Go
0x5A	FPD3_DATAPATH_CTL	FPD3_DATAPATH_CTL	Go
0x5B	FPD3_FIFO_CFG	FPD3_FIFO_CFG	Go
0x5C	FPD3_FIFO_STS	FPD3_FIFO_STS	Go
0x61	ESD_EVENT_INT_CONTROL	ESD_EVENT_INT_CONTROL	Go
0x62	FC_POWERDOWN_CTL	FC_POWERDOWN_CTL	Go
0x63	BC_POWERDOWN_CTL	BC_POWERDOWN_CTL	Go

Table 7-53. PAGE 0: UB MAINPAGE Registers (continued)

Address	Acronym	Register Name	Section
0x6A	BC_DOWNSAMPLING_CFG	BC_DOWNSAMPLING_CFG	Go
0x6B	ENH_BC_STS	ENH_BC_STS	Go
0x6D	BCC_STATUS	BCC_STATUS	Go
0x6E	BC_CONFIG	BC_CONFIG	Go
0x6F	FC_BCC_TEST	FC_BCC_TEST	Go
0x70	TARGET_ID_0	TARGET_ID_0	Go
0x71	TARGET_ID_1	TARGET_ID_1	Go
0x72	TARGET_ID_2	TARGET_ID_2	Go
0x73	TARGET_ID_3	TARGET_ID_3	Go
0x74	TARGET_ID_4	TARGET_ID_4	Go
0x75	TARGET_ID_5	TARGET_ID_5	Go
0x76	TARGET_ID_6	TARGET_ID_6	Go
0x77	TARGET_ID_7	TARGET_ID_7	Go
0x78	TARGET_ALIAS_0	TARGET_ALIAS_0	Go
0x79	TARGET_ALIAS_1	TARGET_ALIAS_1	Go
0x7A	TARGET_ALIAS_2	TARGET_ALIAS_2	Go
0x7B	TARGET_ALIAS_3	TARGET_ALIAS_3	Go
0x7C	TARGET_ALIAS_4	TARGET_ALIAS_4	Go
0x7D	TARGET_ALIAS_5	TARGET_ALIAS_5	Go
0x7E	TARGET_ALIAS_6	TARGET_ALIAS_6	Go
0x7F	TARGET_ALIAS_7	TARGET_ALIAS_7	Go
0x87	LOCAL_INT_STS	LOCAL_INT_STS	Go
0x88	TARGET_DEST_0	TARGET_DEST_0	Go
0x89	TARGET_DEST_1	TARGET_DEST_1	Go
0x8A	TARGET_DEST_2	TARGET_DEST_2	Go
0x8B	TARGET_DEST_3	TARGET_DEST_3	Go
0x8C	TARGET_DEST_4	TARGET_DEST_4	Go
0x8D	TARGET_DEST_5	TARGET_DEST_5	Go
0x8E	TARGET_DEST_6	TARGET_DEST_6	Go
0x8F	TARGET_DEST_7	TARGET_DEST_7	Go
0xA0	RX_BCAPS	RX_BCAPS	Go
0xA3	KSV_FIFO	KSV_FIFO	Go
0xA4	GPIO_INT_CTL0	GPIO_INT_CTL0	Go
0xA5	GPIO_INT_CTL1	GPIO_INT_CTL1	Go
0xA6	GPIO_INT_STS0	GPIO_INT_STS0	Go
0xA7	GPIO_INT_STS1	GPIO_INT_STS1	Go
0xBC	FPD_TX_ESD_EVENT_CNTR	FPD_TX_ESD_EVENT_CNTR	Go
0xBF	DUAL_VIDSYNC	DUAL_VIDSYNC	Go
0xC6	FPD3_ICR	FPD3_ICR	Go
0xC7	FPD3_ISR	FPD3_ISR	Go
0xE2	LINK_CFG_ALIAS	LINK_CFG_ALIAS	Go
0xE4	FPD3_STS_ALIAS	FPD3_STS_ALIAS	Go
0xE6	FPD3_ICR_ALIAS	FPD3_ICR_ALIAS	Go
0xE7	FPD3_ISR_ALIAS	FPD3_ISR_ALIAS	Go
0xF0	TX_ID0	TX_ID0	Go

Table 7-53. PAGE 0: UB MAINPAGE Registers (continued)

Address	Acronym	Register Name	Section
0xF1	TX_ID1	TX_ID1	Go
0xF2	TX_ID2	TX_ID2	Go
0xF3	TX_ID3	TX_ID3	Go
0xF4	TX_ID4	TX_ID4	Go
0xF5	TX_ID5	TX_ID5	Go
0xF6	TX_ID6	TX_ID6	Go
0xF8	IND_REG_I2C_CTL0	IND_REG_I2C_CTL0	Go
0xF9	IND_REG_I2C_ID0	IND_REG_I2C_ID0	Go
0xFA	IND_REG_I2C_CTL1	IND_REG_I2C_CTL1	Go
0xFB	IND_REG_I2C_ID1	IND_REG_I2C_ID1	Go
0xFC	IND_REG_I2C_CTL2	IND_REG_I2C_CTL2	Go
0xFD	IND_REG_I2C_ID2	IND_REG_I2C_ID2	Go
0xFE	IND_REG_I2C_CTL3	IND_REG_I2C_CTL3	Go
0xFF	IND_REG_I2C_ID3	IND_REG_I2C_ID3	Go

Complex bit access types are encoded to fit into small table cells. Table 7-54 shows the codes that are used for access types in this section.

Table 7-54. Page 0: UB MainPage Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
RW	R W	Read Write
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WCOR	W COR	Write
WStrap	W Strap	Write Default value loaded from bootstrap pin after reset.
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 I2C_DEVICE_ID Register (Address = 0x0) [Reset = 0x00]

I2C_DEVICE_ID is shown in Table 7-55.

Return to the Summary Table.

Table 7-55. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	DEVICE_ID	R/WStrap	0x0	7-bit I2C address of Serializer for the primary I2C port Defaults to address configured by the IDx strap pin. Each I2C target derives its DEVICE_ID from the value written to this register. Note that serializer has 3 targets I2C target 0 = DEVICE_ID (primary I2C address) I2C target 1 = DEVICE_ID + 1 I2C target 2 = DEVICE_ID + 2 To change the device ID, set I2C_DEVICE_ID[0] to 1 and then write to this register at the I2C device address you want to change.
0	SER_ID	R/W	0x0	0x0 = Device ID is based on the value strapped from the IDx pin 0x1 = Register I2C Device ID overrides value strapped from the IDx pin

7.6.1.2 RESET_CTL Register (Address = 0x1) [Reset = 0x00]

RESET_CTL is shown in Table 7-56.

Return to the Summary Table.

Table 7-56. RESET_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DPRX_RESET	RH/W1S	0x0	DPRX (SM + PLL) reset When this bit set, any configurations applied to the APB registers will be reset.
5	PLL_CH01_RESET	RH/W1S	0x0	Channel 0 and 1 PLL only reset 0x5B[3] will need to be re-asserted by toggling from low to high if a soft reset or PLL reset is performed in FPD-Link III mode. This will ensure to reset the FIFO in FPD-Link III datapath.
4	PLL_CH23_RESET	RH/W1S	0x0	Channel 2 and 3 PLL only reset 0x5B[3] will need to be re-asserted by toggling from low to high if a soft reset or PLL reset is performed in FPD-Link III mode. This will ensure to reset the FIFO in FPD-Link III datapath.
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	DIGITAL_RESET_ALL	RH/W1S	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 0x0 = Normal operation 0x1 = Reset
0	DIGITAL_RESET_NOREGS	RH/W1S	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. Any configurations applied to the APB registers will be reset. 0x5B[3] will need to be re-asserted by toggling from low to high if a soft reset or PLL reset is performed in FPD-Link III mode. This will ensure to reset the FIFO in FPD-Link III datapath. 0x0 = Normal operation 0x1 = Reset

7.6.1.3 GENERAL_CFG2 Register (Address = 0x2) [Reset = 0xD0]

GENERAL_CFG2 is shown in Table 7-57.

Return to the Summary Table.

Table 7-57. GENERAL_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALFRATE_MODE_CH1	R	0x1	FPD half/full rate mode for FPD-Link III or FPD-Link IV lane 1 By default, this register is Read-Only status indicating the current rate setting, based on the FPD mode of operation as follows: 0x0 = Full-rate, if device configured to 3.375Gbps through mode strap in FPD-Link IV NRZ mode. 0x1 = Half-rate, if device is configured for FPD-Link III mode, or FPD-Link IV NRZ mode (13.5, 12.528, 10.8, 6.75 Gbps). If the FPD_RATE_OVERRIDE bit in the register is set to 1, this register becomes Read-Write and will control the half-rate mode setting for digital logic.
6	HALFRATE_MODE_CH0	R	0x1	FPD half/full rate mode for FPD-Link III or FPD-Link IV lane 0 By default, this register is Read-Only status indicating the current rate setting, based on the FPD mode of operation as follows: 0x0 = Full-rate, if device configured to 3.375Gbps through mode strap in FPD-Link IV NRZ mode. 0x1 = Half-rate, if device is configured for FPD-Link III mode, or FPD-Link IV NRZ mode (13.5, 12.528, 10.8, 6.75 Gbps). If the FPD_RATE_OVERRIDE bit in the register is set to 1, this register becomes Read-Write and will control the half-rate mode setting for digital logic.
5	CRC_ERROR_RESET	R/W	0x0	Clear CRC Error Counters. This bit is NOT self-clearing. 0x0 = Normal operation 0x1 = Clear counters
4	DPRX_EN	R/W	0x1	Enables DPRX Port0
3	EXT_DP_eDP_CTRL	R/WStrap	0x0	Enable external I2C control for DisplayPort/eDP initialization sequence. Loaded from MODE_SEL0 pin at powerup.
2:1	I2S_EN	R/W	0x0	Enable I2S for FPD-Link IV through GPIO or data island method depending upon per port REG 0x5A[3] selection.
0	FPD_RATE_OVERRIDE	R/W	0x0	FPD Rate Override Control 0x0 = FPD Half-rate/Full-rate setting is based on configured operational mode. 0x1 = FPD Half-rate/Full-rate setting is based on override controls.

7.6.1.4 I2C_CONTROLLER_CFG Register (Address = 0x3) [Reset = 0x60]

I2C_CONTROLLER_CFG is shown in Table 7-58.

Return to the Summary Table.

Table 7-58. I2C_CONTROLLER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ARB_TIMEOUT_DISABLE	R/W	0x0	By default, ARB_TIMEOUT values are effective. This bit provides an overide to disable timeout in case it is needed.
6:5	ARB_TIMEOUT	R/W	0x3	This is for I2C Daisy Chain Arbiter timeout. Defaul is set to highest timeout = 0x3. 0x0 = 80us 0x1 = 160us 0x2 = 320us 0x3 = 2.4ms
4:3	SDA_OUT_DELAY	R/W	0x0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 0x0 = 200ns 0x1 = 240ns 0x2 = 280ns 0x3 = 320ns Actual delays may be larger dependent on system capacitances and signal rise/fall times.

Table 7-58. I2C_CONTROLLER_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOCAL_WRITE_DIS	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C controller attached to the Deserializer. Setting this bit does not affect remote access to I2C targets at the Serializer.
1	I2C_BUS_TIMER_SPEED UP	R/W	0x0	Speed up I2C Bus Watchdog Timer 0x0 = Watchdog Timer expires after approximately 1 second. 0x1 = Watchdog Timer expires after approximately 50 microseconds
0	I2C_BUS_TIMER_DISAB LE	R/W	0x0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL.

7.6.1.5 FPD4_CFG Register (Address = 0x5) [Reset = 0x28]

FPD4_CFG is shown in Table 7-59.

Return to the Summary Table.

Table 7-59. FPD4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_FPD3_REFCLK1	R/W	0x0	Use reference 1 (25MHz) for CH1 FPD-Link III instead of reference 0 (27MHz)
6	CH0_FPD3_REFCLK1	R/W	0x0	Use reference 1 (25MHz) for CH0 FPD-Link III instead of reference 0 (27MHz)
5:2	FPD4_TX_MODE	R/WStrap	0xA	FPD-Link IV TX Mode: This register controls the operating mode of the FPD-Link IV Transmit function. 0x0 = FPD-Link III Port 0, FPD-Link III Port 1 FPD-Link III mode selected by 0x59) 0x3 = FPD-Link IV Port 0, FPD-Link III Port 1 (set 0x59 to forced single Port 1) 0xA = FPD-Link IV Dual 0xB = Forced Single FPD-Link IV Port0 (Port 1 disabled) 0xC = FPD-Link III Port 0, FPD-Link IV Port 1 (set 0x59 to forced single Port 0) 0xE = Forced Single FPD-Link IV Port1 (Port 0 disabled) 0xF = FPD-Link IV Independent
1	I2S_AUDIO_SPLIT_P1	R/W	0x0	Split audio for FPD-Link IV Port0; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.
0	I2S_AUDIO_SPLIT_P0	R/W	0x0	Split audio for FPD-Link IV Port1; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.

7.6.1.6 GENERAL_STS2 Register (Address = 0x6) [Reset = 0x38]

GENERAL_STS2 is shown in Table 7-60.

Return to the Summary Table.

Table 7-60. GENERAL_STS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 7-60. GENERAL_STS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	DEV	R	0x1	0x0 = DS90UH983 0x1 = DS90UB983
4	XO_REFCLK_VALID	R	0x1	PLL REFCLK valid for XO pin.
3	PLL_REFCLK_VALID	R	0x1	PLL REFCLK valid for REFCLK1 pin.
2:0	RESERVED	R	0x0	Reserved

7.6.1.7 GENERAL_CFG Register (Address = 0x7) [Reset = 0x80]

GENERAL_CFG is shown in Table 7-61.

Return to the Summary Table.

Table 7-61. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_CRC_CHECKER_ENABLE	R/W	0x1	CRC Checker Enable 0x0 = Disable 0x1 = Enable The TX_PORT_SEL register controls which FPD port is selected for this register bit.
6	RESERVED	R	0x0	Reserved
5	TX_AUTO_ACK	R/W	0x0	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Target, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. Each I2C Target maintains it's own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x0 = Disable 0x1 = Enable
4	I2C_PASS_ALL	R/W	0x0	Each I2C target maintains it's own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x0 = Enable Forward Control Channel pass-through only of I2C accesses to I2C Target IDs matching either the remote Deserializer Target ID or the remote Target ID. Each I2C target maintains it's own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x1 = Enable Forward Control Channel pass-through of all I2C accesses to I2C Target IDs that do not match the Serializer I2C Target ID.
3	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through Mode Each I2C target maintains it's own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x0 = Pass-Through Disabled 0x1 = Pass-Through Enabled
2	RESERVED	R/W	0x0	Reserved
1	SST_MST_MODE_STRAP	R	0x0	MST function: 0 = SST Mode 1 = MST Mode
0	MODE_SEL2_STRAP	R	0x0	Setting the FPD-Link III or IV mode. 0x0 = Enable FPD-Link IV mode 0x1 = Enable FPD-Link III mode

7.6.1.8 DES_ID Register (Address = 0x8) [Reset = 0x00]

DES_ID is shown in Table 7-62.

Return to the Summary Table.

Table 7-62. DES_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	DES_DEV_ID	R/W	0x0	7-bit Deserializer Device ID Configures the I2C Target ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates the Deserializer Device ID for the Deserializer attached to Port 1
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Deserializer Device ID Prevent auto-loading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. If PORT1_SEL is set, this bit controls DES_DEV_ID.

7.6.1.9 BC_DUTY_CYC Register (Address = 0x9) [Reset = 0x7E]

BC_DUTY_CYC is shown in Table 7-63.

Return to the Summary Table.

If PORT1_SEL is set, this register indicates Port1 Back Channel Duty Cycle

Table 7-63. BC_DUTY_CYC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BC_DUTY_CYCLE	R	0x7E	Back Channel Duty Cycle measurement (per port): This register provides a measurement of the back channel duty cycle for the selected FPD-Link III port. The measurement is between 0 and 255 where 0x80 indicates a 50% duty cycle signal. To determine % duty cycle from the measurement, use the following equation: Duty Cycle (%) = BC_DUTY_CYCLE * 100 / 256

7.6.1.10 CRC_ERROR0 Register (Address = 0xA) [Reset = 0x00]

CRC_ERROR0 is shown in Table 7-64.

Return to the Summary Table.

If PORT1_SEL is set, this register indicates Port1 Status

Table 7-64. CRC_ERROR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_ERROR_7_0	R	0x0	Number of Back Channel CRC errors – 8 least significant bits. This register is cleared using the CRC ERROR RESET in register 0x04.

7.6.1.11 CRC_ERROR1 Register (Address = 0xB) [Reset = 0x00]

CRC_ERROR1 is shown in Table 7-65.

Return to the Summary Table.

If PORT1_SEL is set, this register indicates Port1 Status

Table 7-65. CRC_ERROR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_ERROR_15_8	R	0x0	Number of Back Channel CRC errors – 8 most significant bits. This register is cleared using the CRC ERROR RESET in register 0x04.

7.6.1.12 GENERAL_STS Register (Address = 0xC) [Reset = 0x00]

GENERAL_STS is shown in Table 7-66.

Return to the Summary Table.

If PORT1_SEL is set, this register indicates Port1 Status

Table 7-66. GENERAL_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RX_LOCK_DET	R	0x0	RX Lock detect for selected port: This bit indicates current Receiver Lock Detect status for the selected port. This value is returned as part of the back channel information from the Deserializer.
5	RESERVED	R	0x0	Reserved
4	LINK_LOST	R	0x0	Link Lost Flag for selected port: This bit indicates that loss of link has been detected. This register bit will stay high until cleared using the CRC ERROR RESET in register 0x02[5].
3	BIST_CRC_ERROR	R	0x0	CRC error during BIST communication with Deserializer. This bit is cleared upon restart of BIST or assertion of CRC ERROR RESET in register 0x02[5].
2	RESERVED	R	0x0	Reserved
1	BC_CRC_ERROR	R	0x0	Back channel error detect for selected port: Back channel CRC error during communication with Deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x02[5].
0	LINK_DETECT	R	0x0	Link Detect status for selected port: 0x0 = Cable link not detected 0x1 = Cable link detected

7.6.1.13 FPD4_DATAPATH_CTL Register (Address = 0xD) [Reset = 0x00]

FPD4_DATAPATH_CTL is shown in Table 7-67.

Return to the Summary Table.

Datapath Control Register 1
The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

Table 7-67. FPD4_DATAPATH_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	GPIOEN_FC	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs for the selected port 0x0 = GPIOs disabled 0x1 = One GPIO 0x2 = Two GPIOs 0x3 = Four GPIOs

7.6.1.14 FPD4_DATAPATH_CTL2 Register (Address = 0xE) [Reset = 0x00]

FPD4_DATAPATH_CTL2 is shown in Table 7-68.

Return to the Summary Table.

Datapath Control Register 2
The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

Table 7-68. FPD4_DATAPATH_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	FC_ECC_BCC_ONLY	R/W	0x0	Forward Channel ECC on I2C only If ECC operation is enabled, this bit indicates if ECC is enabled for the I2C bit only.
2	FC_ECC_GPIO	R/W	0x0	Forward Channel ECC on GPIO bit If ECC operation is enabled, this bit indicates if ECC is included for the GPIO bit which is encoded as part of CSI[0].
1:0	FC_ECC	R/W	0x0	Forward Channel ECC Operation 0x0 = No ECC present 0x1 = 6-bit ECC 0x2 = 7-bit ECC 0x3 = 8-bit ECC

7.6.1.15 BIST_BC_ERRORS Register (Address = 0xF) [Reset = 0x00]

BIST_BC_ERRORS is shown in Table 7-69.

Return to the Summary Table.

Table 7-69. BIST_BC_ERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BIST_BC_ERROR_COUNT	R	0x0	BIST Back Channel CRC Error Counter This register is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04. If PORT1_SEL is set, this register indicates port 1 status

7.6.1.16 FPD3_DES_CAP1 Register (Address = 0x10) [Reset = 0x00]

FPD3_DES_CAP1 is shown in Table 7-70.

Return to the Summary Table.

FPD-Link III Deserializer Capabilities Register 1
This register contains the lower bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

Table 7-70. FPD3_DES_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FREEZE_FPD3_DES_CAP	R/W	0x0	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Back Channel. The Capabilities will be frozen at the values written in registers 0x10 and 0x11.

Table 7-70. FPD3_DES_CAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	HSCC_MODE_0	R/W	0x0	High-Speed Control Channel bit 0 Lowest bit of the 3-bit HSCC indication. The other 2 bits are contained in Deserializer Capabilities 2. This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	DUAL_LINK_CAP	R/W	0x0	Dual link Capabilities Indicates if the Deserializer is capable of dual link operation. This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
2	DUAL_CHANNEL	R/W	0x0	Dual Channel 0/1 Indication In a dual-link capable device, indicates if this is the primary or secondary channel. 0x0 = Primary channel (channel 0) 0x1 = Secondary channel (channel 1) This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
1	VID_24B_HD_AUD	R/W	0x0	Deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
0	DES_CAP_FC_GPIO	R/W	0x0	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.

7.6.1.17 FPD3_DES_CAP2 Register (Address = 0x11) [Reset = 0x00]

FPD3_DES_CAP2 is shown in Table 7-71.

Return to the Summary Table.

FPD-Link III Deserializer Capabilities Register 2
This register contains the upper bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

Table 7-71. FPD3_DES_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	FC_BCC_CRC6	R/W	0x0	Enable Forward Channel CRC6 for BCC frames Enable enhanced CRC and start sequence for forward channel signaling of the Bidirectional Control Channel
2	RESERVED	R	0x0	Reserved

Table 7-71. FPD3_DES_CAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	HSCC_MODE_2_1	R/W	0x0	High-Speed Control Channel bit 0 Upper 2-bit of total 3-bit HSCC indication. The lowest bit is contained in Deserializer Capabilities 1. 0x0 = Normal back channel frame, GPIO mode 0x1 = High Speed GPIO mode, 1 GPIO 0x2 = High Speed GPIO mode, 2 GPIOs 0x3 = High Speed GPIO mode: 4 GPIOs 0x4 = Reserved 0x5 = Reserved 0x6 = High Speed, Forward Channel SPI mode 0x7 = High Speed, Reverse Channel SPI mode In Single Link devices, only Normal back channel frame modes (0x0) are supported.

7.6.1.18 FPD4_REMOTE_PAR_CAP1 Register (Address = 0x12) [Reset = 0x00]

FPD4_REMOTE_PAR_CAP1 is shown in Table 7-72.

Return to the Summary Table.

FPD-Link IV Partner Capabilities Register 1
This register contains the lower bits of the Partner Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

Table 7-72. FPD4_REMOTE_PAR_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FREEZE_FPD4_DES_CAP	R/W	0x0	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Back Channel. The Capabilities will be frozen at the values written in registers 0x12 and 0x13.
6	RESERVED	R	0x0	Reserved
5	BIST_EN	R/W	0x0	Link BIST Enable This bit is used in conjunction with capable de-serializers to enable link BIST.
4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

7.6.1.19 FPD4_REMOTE_PAR_CAP2 Register (Address = 0x13) [Reset = 0x00]

FPD4_REMOTE_PAR_CAP2 is shown in Table 7-73.

Return to the Summary Table.

Table 7-73. FPD4_REMOTE_PAR_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FPD4_REMOTE_PAR_CAP2	R/W	0x0	FPD-Link IV Deserializer Capabilities Register 2 This register contains the upper bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

7.6.1.20 TX_BIST_CTL Register (Address = 0x14) [Reset = 0x00]

TX_BIST_CTL is shown in Table 7-74.

Return to the Summary Table.

BIST and DOPL mode control register

Table 7-74. TX_BIST_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	BISTEN_NO_RESET	R/W	0x0	Enable BIST mode with FPD PLL reset
2:1	RESERVED	R	0x0	Reserved
0	BIST_EN	R/W	0x0	BIST Control 0x0 = Disabled 0x1 = Enabled This bit is used in conjunction with capable serializers to enable link BIST.

7.6.1.21 FC_GPIO_CTL0 Register (Address = 0x15) [Reset = 0x10]

FC_GPIO_CTL0 is shown in Table 7-75.

Return to the Summary Table.

Forward channel GPIO Control Register 0

Table 7-75. FC_GPIO_CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	FC_GPIO1_SEL	R/W	0x1	Forward channel GPIO1 Select: Determines the data sent on GPIO1 for the selected port forward channel. 0x0 - 0xD = Pin GPIOx 0xE = Constant value of 0 0xF = Constant value of 1 TX Port 0 Default = 0x1 TX Port 1 Default = 0xB
3:0	FC_GPIO0_SEL	R/W	0x0	Forward channel GPIO0 Select: Determines the data sent on GPIO0 for the selected port forward channel. 0x0 - 0xD = Pin GPIOx 0xE = Constant value of 0 0xF = Constant value of 1 TX Port 0 Default = 0x0 TX Port 1 Default = 0xA

7.6.1.22 FC_GPIO_CTL1 Register (Address = 0x16) [Reset = 0x32]

FC_GPIO_CTL1 is shown in Table 7-76.

Return to the Summary Table.

Forward channel GPIO Control Register 1

Table 7-76. FC_GPIO_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	FC_GPIO3_SEL	R/W	0x3	Forward channel GPIO3 Select: Determines the data sent on GPIO3 for the selected port forward channel. 0x0 - 0xD = Pin GPIOx 0xE = Constant value of 0 0xF = Constant value of 1 TX Port 0 Default = 0x3 TX Port 1 Default = 0xD

Table 7-76. FC_GPIO_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	FC_GPIO2_SEL	R/W	0x2	Forward channel GPIO2 Select: Determines the data sent on GPIO2 for the selected port forward channel. 0x0 - 0xD = Pin GPIOx 0xE = Constant value of 0 0xF = Constant value of 1 TX Port 0 Default = 0x2 TX Port 1 Default = 0xC

7.6.1.23 GPIO0_PIN_CTL Register (Address = 0x17) [Reset = 0x00]

GPIO0_PIN_CTL is shown in Table 7-77.

Return to the Summary Table.

Table 7-77. GPIO0_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO0_OUTPUT_EN	R/W	0x0	GPIO0 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-77. GPIO0_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO0_OUT_SEL	R/W	0x0	GPIO0 Output Select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO0_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO0_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO0_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO0_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-77. GPIO0_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.24 GPIO1_PIN_CTL Register (Address = 0x18) [Reset = 0x00]

GPIO1_PIN_CTL is shown in Table 7-78.

Return to the Summary Table.

Table 7-78. GPIO1_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_OUTPUT_EN	R/W	0x0	GPIO1 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-78. GPIO1_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO1_OUT_SEL	R/W	0x0	GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO1_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO1_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO1_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO1_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-78. GPIO1_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.25 GPIO2_PIN_CTL Register (Address = 0x19) [Reset = 0x00]

GPIO2_PIN_CTL is shown in Table 7-79.

Return to the Summary Table.

Table 7-79. GPIO2_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO2_OUTPUT_EN	R/W	0x0	GPIO2 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-79. GPIO2_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO2_OUT_SEL	R/W	0x0	GPIO2 Output Select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO2_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO2_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO2_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO2_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-79. GPIO2_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.26 GPIO3_PIN_CTL Register (Address = 0x1A) [Reset = 0x00]

GPIO3_PIN_CTL is shown in Table 7-80.

Return to the Summary Table.

Table 7-80. GPIO3_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO3_OUTPUT_EN	R/W	0x0	GPIO3 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select Selects output source for GPIO3 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-80. GPIO3_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO3_OUT_SEL	R/W	0x0	GPIO3 Output Select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO3_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO3_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO3_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO3_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-80. GPIO3_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.27 GPIO4_PIN_CTL Register (Address = 0x1B) [Reset = 0x08]

GPIO4_PIN_CTL is shown in Table 7-81.

Return to the Summary Table.

Table 7-81. GPIO4_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO4_OUTPUT_EN	R/W	0x0	GPIO4 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO4_OUT_SRC	R/W	0x0	GPIO4 Output Source Select Selects output source for GPIO4 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-81. GPIO4_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO4_OUT_SEL	R/W	0x8	GPIO4 Output Select Determines the output data for the selected source. If GPIO4_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO4_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO4_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO4_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO4_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-81. GPIO4_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.28 GPIO5_PIN_CTL Register (Address = 0x1C) [Reset = 0x00]

GPIO5_PIN_CTL is shown in Table 7-82.

Return to the Summary Table.

Table 7-82. GPIO5_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO5_OUTPUT_EN	R/W	0x0	GPIO5 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO5_OUT_SRC	R/W	0x0	GPIO5 Output Source Select Selects output source for GPIO5 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-82. GPIO5_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO5_OUT_SEL	R/W	0x0	GPIO5 Output Select Determines the output data for the selected source. If GPIO5_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO5_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO5_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO5_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO5_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-82. GPIO5_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.29 GPIO6_PIN_CTL Register (Address = 0x1D) [Reset = 0x00]

GPIO6_PIN_CTL is shown in Table 7-83.

Return to the Summary Table.

Table 7-83. GPIO6_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO6_OUTPUT_EN	R/W	0x0	GPIO6 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO6_OUT_SRC	R/W	0x0	GPIO6 Output Source Select Selects output source for GPIO6 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-83. GPIO6_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO6_OUT_SEL	R/W	0x0	GPIO6 Output Select Determines the output data for the selected source. If GPIO6_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO6_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO6_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO6_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO6_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-83. GPIO6_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.30 GPIO7_PIN_CTL Register (Address = 0x1E) [Reset = 0x00]

GPIO7_PIN_CTL is shown in Table 7-84.

Return to the Summary Table.

Table 7-84. GPIO7_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO7_OUTPUT_EN	R/W	0x0	GPIO7 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO7_OUT_SRC	R/W	0x0	GPIO7 Output Source Select Selects output source for GPIO7 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-84. GPIO7_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO7_OUT_SEL	R/W	0x0	GPIO7 Output Select Determines the output data for the selected source. If GPIO7_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO7_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO7_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO7_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO7_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-84. GPIO7_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.31 GPIO8_PIN_CTL Register (Address = 0x1F) [Reset = 0x00]

GPIO8_PIN_CTL is shown in Table 7-85.

Return to the Summary Table.

Table 7-85. GPIO8_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_OUTPUT_EN	R/W	0x0	GPIO8 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO8_OUT_SRC	R/W	0x0	GPIO8 Output Source Select Selects output source for GPIO8 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-85. GPIO8_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO8_OUT_SEL	R/W	0x0	GPIO8 Output Select Determines the output data for the selected source. If GPIO8_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO8_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO8_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO8_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO8_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-85. GPIO8_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.32 GPIO9_PIN_CTL Register (Address = 0x20) [Reset = 0x00]

GPIO9_PIN_CTL is shown in Table 7-86.

Return to the Summary Table.

Table 7-86. GPIO9_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO9_OUTPUT_EN	R/W	0x0	GPIO9 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO9_OUT_SRC	R/W	0x0	GPIO9 Output Source Select Selects output source for GPIO9 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-86. GPIO9_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO9_OUT_SEL	R/W	0x0	GPIO9 Output Select Determines the output data for the selected source. If GPIO9_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO9_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO9_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO9_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO9_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-86. GPIO9_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.33 GPIO10_PIN_CTL Register (Address = 0x21) [Reset = 0x00]

GPIO10_PIN_CTL is shown in Table 7-87.

Return to the Summary Table.

Table 7-87. GPIO10_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO10_OUTPUT_EN	R/W	0x0	GPIO10 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO10_OUT_SRC	R/W	0x0	GPIO10 Output Source Select Selects output source for GPIO10 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-87. GPIO10_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO10_OUT_SEL	R/W	0x0	GPIO10 Output Select Determines the output data for the selected source. If GPIO10_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO10_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO10_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO10_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO10_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-87. GPIO10_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.34 GPIO11_PIN_CTL Register (Address = 0x22) [Reset = 0x00]

GPIO11_PIN_CTL is shown in Table 7-88.

Return to the Summary Table.

Table 7-88. GPIO11_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO11_OUTPUT_EN	R/W	0x0	GPIO11 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO11_OUT_SRC	R/W	0x0	GPIO11 Output Source Select Selects output source for GPIO11 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-88. GPIO11_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO11_OUT_SEL	R/W	0x0	GPIO11 Output Select Determines the output data for the selected source. If GPIO11_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO11_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO11_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO11_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO11_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-88. GPIO11_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.35 GPIO12_PIN_CTL Register (Address = 0x23) [Reset = 0x00]

GPIO12_PIN_CTL is shown in Table 7-89.

Return to the Summary Table.

Table 7-89. GPIO12_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO12_OUTPUT_EN	R/W	0x0	GPIO12 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO12_OUT_SRC	R/W	0x0	GPIO12 Output Source Select Selects output source for GPIO12 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-89. GPIO12_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO12_OUT_SEL	R/W	0x0	GPIO12 Output Select Determines the output data for the selected source. If GPIO12_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO12_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO12_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO12_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO12_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-89. GPIO12_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.36 GPIO13_PIN_CTL Register (Address = 0x24) [Reset = 0x00]

GPIO13_PIN_CTL is shown in Table 7-90.

Return to the Summary Table.

Table 7-90. GPIO13_PIN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO13_OUTPUT_EN	R/W	0x0	GPIO13 Output Enable 0x0 = Disabled 0x1 = Enabled
6:4	GPIO13_OUT_SRC	R/W	0x0	GPIO13 Output Source Select Selects output source for GPIO13 data: 000b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 0 100b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 0 001b = Select lower 8bits of Back channel GPIO and FPD-Link port status from port 1 101b = Select upper 8bits of Back channel GPIO and FPD-Link port status from port 1 x10b = Device Status x11b = Reserved For more information on what can be selected with each setting of this registers, see description for GPIO0_OUT_SEL.

Table 7-90. GPIO13_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO13_OUT_SEL	R/W	0x0	GPIO13 Output Select Determines the output data for the selected source. If GPIO13_OUT_SRC is set to 000b, the following selections apply: 0000b = Received PORT0 BC_GPIO0 0001b = Received PORT0 BC_GPIO1 0010b = Received PORT0 BC_GPIO2 0011b = Received PORT0 BC_GPIO3 0100b = Received PORT0 BC_GPIO4 0101b = Received PORT0 BC_GPIO5 0110b = Received PORT0 BC_GPIO6 0111b = Received PORT0 BC_GPIO7 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100b = AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET) 1101 - 1111b = Reserved If GPIO13_OUT_SRC is set to 100b, the following selections apply: 0000b = Received PORT0 BC_GPIO8 0001b = Received PORT0 BC_GPIO9 0010b = Received PORT0 BC_GPIO10 0011b = Received PORT0 BC_GPIO11 0100b = Received PORT0 BC_GPIO12 0101b = Received PORT0 BC_GPIO13 0110b = Received PORT0 BC_GPIO14 0111b = Received PORT0 BC_GPIO15 1000b = PORT0 RX_INTN 1001b = PORT0 RX_LOCK_DET 1010b = PORT0 FPD3_TX_INTN 1011b = PORT0 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO13_OUT_SRC is set to 001b, the following selections apply: 0000b = Received PORT1 BC_GPIO0 0001b = Received PORT1 BC_GPIO1 0010b = Received PORT1 BC_GPIO2 0011b = Received PORT1 BC_GPIO3 0100b = Received PORT1 BC_GPIO4 0101b = Received PORT1 BC_GPIO5 0110b = Received PORT1 BC_GPIO6 0111b = Received PORT1 BC_GPIO7 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO13_OUT_SRC is set to 101b, the following selections apply: 0000b = Received PORT1 BC_GPIO8 0001b = Received PORT1 BC_GPIO9 0010b = Received PORT1 BC_GPIO10 0011b = Received PORT1 BC_GPIO11 0100b = Received PORT1 BC_GPIO12 0101b = Received PORT1 BC_GPIO13 0110b = Received PORT1 BC_GPIO14 0111b = Received PORT1 BC_GPIO15 1000b = PORT1 RX_INTN 1001b = PORT1 RX_LOCK_DET 1010b = PORT1 FPD3_TX_INTN 1011b = PORT1 FPD3_TX_INT 1100 - 1111b = Reserved If GPIO13_OUT_SRC is set to x10b (Device Status), the following selections apply: 0000b = Fixed output value of 0 0001b = Fixed output value of 1 0010b = Inverted INTERRUPT STATUS 0011b = INTERRUPT STATUS 0100b = Inverted VP Combined INTERRUPT Status

Table 7-90. GPIO13_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101b = VP Combined INTERRUPT Status 0110 - 1111b = Reserved

7.6.1.37 GPI_PIN_STS1 Register (Address = 0x25) [Reset = 0x00]

GPI_PIN_STS1 is shown in Table 7-91.

Return to the Summary Table.

Table 7-91. GPI_PIN_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GPIO_PIN_STS_7_0	R	0x0	Read status value set on the GPIO pins 7:0

7.6.1.38 GPI_PIN_STS2 Register (Address = 0x26) [Reset = 0x00]

GPI_PIN_STS2 is shown in Table 7-92.

Return to the Summary Table.

Table 7-92. GPI_PIN_STS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	GPIO_PIN_STS_13_8	R	0x0	Read status value set on the GPIO pins 13:8

7.6.1.39 TX_MODE_STS Register (Address = 0x27) [Reset = 0x88]

TX_MODE_STS is shown in Table 7-93.

Return to the Summary Table.

Table 7-93. TX_MODE_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MODE_SEL1_DONE	R	0x1	Indicates MODE_SEL1 value has stabilized and been latched
6:4	MODE_SEL1_DECODE	R/WStrap	0x0	Returns the 3-bit decode of the MODE_SEL1 pin
3	MODE_SEL0_DONE	R	0x1	Indicates MODE_SEL0 value has stabilized and been latched
2:0	MODE_SEL0_DECODE	R/WStrap	0x0	Returns the 3-bit decode of the MODE_SEL0 pin

7.6.1.40 GPIO_EN_BC Register (Address = 0x28) [Reset = 0x02]

GPIO_EN_BC is shown in Table 7-94.

Return to the Summary Table.

Table 7-94. GPIO_EN_BC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved

Table 7-94. GPIO_EN_BC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	GPIO_BC_EN	R/W	0x2	Indicates how many GPIOs are carried through FPD-Link IV back-channel. When 0x0 = four GPIOs mapped on local GPIO[3:0], where every back-channel frames always provides 4 GPIOs. When 0x1 = Eight GPIOs mapped on local GPIOs. Where Idle frame with K28.5 and K28.3 carries GPIO[3:0] and K28.1 and K28.2 provides GPIO[7:4]. i.e. every alternate back-channel frames provide GPIO[3:0] and GPIO[7:4] When 0x2 = 16 GPIOs mapped on local GPIOs, (with Max valid GPIOs are only 13), where Idle frame with K28.5 =GPIO[3:0], K28.1 =GPIO[7:4], K28.3 =GPIO[11:8] and K28.2 =GPIO[15:12]. i.e. every fourth frame updates given GPIO frame status. When 0x3 = back channel receives one HS GPIO. Each back channel frame contains four samples for single GPIO. HS GPIO is always on GPIO[0] from back-channel module, one for each FPD-Link IV port

7.6.1.41 BCC_WDOG_CTL Register (Address = 0x29) [Reset = 0x1FC]

BCC_WDOG_CTL is shown in Table 7-95.

Return to the Summary Table.

Table 7-95. BCC_WDOG_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	BCC_WATCHDOG_TIMER	R/W	0x7E	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WDOG_DIS	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 0x0 = Enables BCC Watchdog Timer operation 0x1 = Disables BCC Watchdog Timer operation

7.6.1.42 I2C_CONTROL Register (Address = 0x2A) [Reset = 0x1E]

I2C_CONTROL is shown in Table 7-96.

Return to the Summary Table.

Table 7-96. I2C_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	SDA_HOLD_TIME	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

7.6.1.43 SCL_HIGH_TIME Register (Address = 0x2B) [Reset = 0x7F]

SCL_HIGH_TIME is shown in Table 7-97.

Return to the Summary Table.

Table 7-97. SCL_HIGH_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_SCL_HIGH	R/W	0x7F	I2C Controller SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the controller on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional oscillator clock periods. Min_delay = 38.0952ns * (TX_SCL_HIGH + 5)

7.6.1.44 SCL_LOW_TIME Register (Address = 0x2C) [Reset = 0x7F]

SCL_LOW_TIME is shown in Table 7-98.

Return to the Summary Table.

Table 7-98. SCL_LOW_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_SCL_LOW	R/W	0x7F	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay = 38.0952ns * (TX_SCL_LOW + 5)

7.6.1.45 TX_PORT_SEL Register (Address = 0x2D) [Reset = 0x01]

TX_PORT_SEL is shown in Table 7-99.

Return to the Summary Table.

FPD TX Port page Select
Select TX port register page for reading and writing port specific registers. The register provides separate controls for read selection and for write selection. The 2-bit TX_READ_PORT field provides for reading values from a single port. The 4-bit TX_WRITE_PORT field provides individual enables for each port, allowing simultaneous writes to any of the four FPD-Link III Receive port register blocks.
A separate copy of the TX_PORT_SEL register is maintained for each possible function that may access the registers, preventing conflict between the possible sources of register access.

Table 7-99. TX_PORT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PHYS_PORT_NUM	R	0x0	Physical port number. This field provides the physical port connection when reading from a remote device via the Bidirectional Control Channel or through local I2C interface. When accessed via local I2C interfaces, the value returned is the I2C port connection. When accessed via Bidirectional Control Channel, the value returned is the port number of the received port connection. Main Page = 0: 0x0 = Target0/Controller0 0x1 = Target1/Controller1 0x2 = Target2 0x3 = DPAux

Table 7-99. TX_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	TX_READ_PORT	R/W	0x0	Select TX port for register read. This field selects one of the two TX port register blocks for readback. This applies to all paged FPD-Link III/FPD-Link IV Transmitter port registers. 0x0 = Port 0 registers 0x1 = Port 1 registers When access via local I2C interfaces, the default settings depends upon the interface as shown in the default value column.Since there are only 2 physical FPD TX ports, values of 2 and 3 do not provide access to FPD TX port registers. Settings of 2 and 3 will return values for DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or Controller rather than per FPD port. Main Page = 0: 0x0 = Target0/Controller0 0x1 = Target1/Controller1 0x2 = Target2/Controller2 0x3 = DPAux
3	TX_WRITE_PORT_3	R/W	0x0	Write enable for DPAux Controller/Target registers. Setting this bit will allow writing DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or Controller rather than per FPD port. 0x0 = write disables 0x1 = write enables. Main page = 0: Target0/Controller0 = 0 Target1/Controller1 = 0 Target2/Controller2 = 0 DPAux = 1
2	TX_WRITE_PORT_2	R/W	0x0	Write enable for Target2/Controller2 registers. Setting this bit will allow writing DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or Controller rather than per FPD port. DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or Controller rather than per FPD port. DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or Controller rather than per FPD port. 0x0 = write disables 0x1 = write enables. Main page = 0 Target0/Controller0 = 0 Target1/Controller1 = 0 Target2/Controller2 = 1 DPAux = 0
1	TX_WRITE_PORT_1	R/W	0x0	Write enable for TX port 1 registers. This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to all paged FPD-Link III/FPD-Link IV transmitter port registers. 0x0 = write disables 0x1 = write enables. Main page = 0: Target0/Controller0 = 0 Target1/Controller1 = 1 Target2/Controller2 = 0 DPAux = 0

Table 7-99. TX_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_WRITE_PORT_0	R/W	0x1	Write enable for TX port 0 registers. This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to all paged FPD-Link III/FPD-Link IV transmitter port registers. 0x0 = write disables 0x1 = write enables. Main page = 0 Target0/Controller0 = 1 Target1/Controller1 = 0 Target2/Controller2 = 0 DPAux = 0

7.6.1.46 LINK_DET_CTL Register (Address = 0x2E) [Reset = 0x00]

LINK_DET_CTL is shown in Table 7-100.

Return to the Summary Table.

Table 7-100. LINK_DET_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	LINK_DETECT_TIMER	R/W	0x0	Bidirectional Control Channel Link Detect Timer This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 0x0 = 162,000µs 0x1 = 325,000µs 0x2 = 650,000µs 0x3 = 1,300µs 0x4 = 10.25µs 0x5 = 20.5µs 0x6 = 41µs 0x7 = 82µs

7.6.1.47 IO_CTL Register (Address = 0x2F) [Reset = 0x89]

IO_CTL is shown in Table 7-101.

Return to the Summary Table.

Table 7-101. IO_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_SEL3P3V	R/WStrap	0x1	I2C select 0x0 = 1.8V 0x1 = 3.3V Strapped from the IDx pin during power-up
6	RESERVED	R/W	0x0	Reserved
5:4	RESERVED	R/W	0x0	Reserved
3:0	RESERVED	R/W	0x9	Reserved

7.6.1.48 DEVICE_REV_ID Register (Address = 0x30) [Reset = 0x52]

DEVICE_REV_ID is shown in Table 7-102.

Return to the Summary Table.

Table 7-102. DEVICE_REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	REV_ID	R	0x5	Revision ID 0x5 = Production (Top marking A0)
3:0	RESERVED	R	0x2	Reserved

7.6.1.49 PLL_REFCLK_FREQ Register (Address = 0x31) [Reset = 0x1A]

PLL_REFCLK_FREQ is shown in Table 7-103.

Return to the Summary Table.

Table 7-103. PLL_REFCLK_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL_REFCLK_FREQ	R	0x1A	PLL refclk detection frequency for REFCLK1 pin.

7.6.1.50 XO_REFCLK_FREQ Register (Address = 0x32) [Reset = 0x1A]

XO_REFCLK_FREQ is shown in Table 7-104.

Return to the Summary Table.

Table 7-104. XO_REFCLK_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	XO_REFCLK_FREQ	R	0x1A	XO refclk detection frequency for XO pin.

7.6.1.51 I2C_CTRL_CHAIN_CTL1 Register (Address = 0x38) [Reset = 0x21]

I2C_CTRL_CHAIN_CTL1 is shown in Table 7-105.

Return to the Summary Table.

Table 7-105. I2C_CTRL_CHAIN_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	I2C_TARGET1_CONN	R/W	0x2	I2C Target 1 Connection Controls which I2C port is connected to I2C Target 1 Allowed values: 0x0 = No connection 0x1 = Connect primary I2C port (SDA0/SCL0) 0x2 = Connect second I2C port (SDA1/SCL1) 0x4 = Connect third I2C port (SDA2/SCL2)
3	RESERVED	R	0x0	Reserved
2:0	I2C_TARGET0_CONN	R/W	0x1	I2C Target 0 Connection Controls which I2C port is connected to I2C Target 0 Allowed values: 0x0 = No connection 0x1 = Connect primary I2C port (SDA0/SCL0) 0x2 = Connect second I2C port (SDA1/SCL1) 0x4 = Connect third I2C port (SDA2/SCL2)

7.6.1.52 I2C_CTRL_CHAIN_CTL2 Register (Address = 0x39) [Reset = 0x04]

I2C_CTRL_CHAIN_CTL2 is shown in Table 7-106.

Return to the Summary Table.

Table 7-106. I2C_CTRL_CHAIN_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	I2C_TARGET2_CONN	R/W	0x4	I2C Target 2 Connection Controls which I2C port is connected to I2C Target 2 Allowed values: 0x0 = No connection 0x1 = Connect primary I2C port (SDA0/SCL0) 0x2 = Connect second I2C port (SDA1/SCL1) 0x4 = Connect third I2C port (SDA2/SCL2)

7.6.1.53 I2C_CTRL_CHAIN_CTL3 Register (Address = 0x3A) [Reset = 0x00]

I2C_CTRL_CHAIN_CTL3 is shown in Table 7-107.

Return to the Summary Table.

Table 7-107. I2C_CTRL_CHAIN_CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_CONTROLLER1	R/W	0x0	Disable remote controller from FPD link port 1
6:4	RESERVED	R	0x0	Reserved
3	DIS_CONTROLLER0	R/W	0x0	Disable remote controller from fPD link port 0
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.6.1.54 MAILBOX_3C Register (Address = 0x3C) [Reset = 0x00]

MAILBOX_3C is shown in Table 7-108.

Return to the Summary Table.

Table 7-108. MAILBOX_3C Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MAILBOX_3C	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

7.6.1.55 MAILBOX_3D Register (Address = 0x3D) [Reset = 0x00]

MAILBOX_3D is shown in Table 7-109.

Return to the Summary Table.

Table 7-109. MAILBOX_3D Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MAILBOX_3D	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

7.6.1.56 GPIO_IN_EN_HIGH Register (Address = 0x3E) [Reset = 0xFF]

GPIO_IN_EN_HIGH is shown in Table 7-110.

Return to the Summary Table.

Table 7-110. GPIO_IN_EN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x1	Reserved
6	RESERVED	R	0x1	Reserved
5	GPIO13_INPUT_EN	R/W	0x1	GPIO13 Input Enable 0x0 = Disabled 0x1 = Enabled
4	GPIO12_INPUT_EN	R/W	0x1	GPIO12 Input Enable 0x0 = Disabled 0x1 = Enabled
3	GPIO11_INPUT_EN	R/W	0x1	GPIO11 Input Enable 0x0 = Disabled 0x1 = Enabled
2	GPIO10_INPUT_EN	R/W	0x1	GPIO10 Input Enable 0x0 = Disabled 0x1 = Enabled
1	GPIO9_INPUT_EN	R/W	0x1	GPIO9 Input Enable 0x0 = Disabled 0x1 = Enabled
0	GPIO8_INPUT_EN	R/W	0x1	GPIO8 Input Enable 0x0 = Disabled 0x1 = Enabled

7.6.1.57 GPIO_IN_EN_LOW Register (Address = 0x3F) [Reset = 0xFF]

GPIO_IN_EN_LOW is shown in Table 7-111.

Return to the Summary Table.

Table 7-111. GPIO_IN_EN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO7_INPUT_EN	R/W	0x1	GPIO7 Input Enable 0x0 = Disabled 0x1 = Enabled
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable 0x0 = Disabled 0x1 = Enabled
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable 0x0 = Disabled 0x1 = Enabled
4	GPIO4_INPUT_EN	R/W	0x1	GPIO4 Input Enable 0x0 = Disabled 0x1 = Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0x0 = Disabled 0x1 = Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0x0 = Disabled 0x1 = Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0x0 = Disabled 0x1 = Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0x0 = Disabled 0x1 = Enabled

7.6.1.58 IND_ACC_CTL Register (Address = 0x40) [Reset = 0x00]

IND_ACC_CTL is shown in Table 7-112.

Return to the Summary Table.

Table 7-112. IND_ACC_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:2	IND_ACC_SEL	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0x0 = Disabled 0x1 = FPD Ports 0-1 registers including broadcast write 0x2 = FPD PLL 0-1 registers including broadcast write 0x3 = Reserved 0x4 = DisplayPort lanes 0-1 registers 0x5 = DisplayPort lanes 2-3 registers 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = DFT/DP PLL Common Registers 0xA = Reserved 0xB = TX Link Layer Registers 0xC = Video Processor 0/1/2/3 Registers 0xD = Reserved 0xE = SAR ADC Registers 0xF = Reserved
1	IND_ACC_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1. For auto-increment on reads, the IND_ACC_READ bit should also be set.
0	IND_ACC_READ	R/W	0x0	Indirect Access Register Read: Typically, this bit should be set to 1 when reading indirect access registers. It should be set to 0 when writing to indirect access registers. For access to page 1 registers, setting this bit allows Clear-on-read of status registers. If this bit is set to 0, the status registers may be read, but will not be cleared on read. For access to analog registers that require prefetch, setting this allows generation of a read strobe to the analog block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register.

7.6.1.59 IND_ACC_ADDR Register (Address = 0x41) [Reset = 0x00]

IND_ACC_ADDR is shown in Table 7-113.

Return to the Summary Table.

Table 7-113. IND_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IND_ACC_ADDR	R/W	0x0	Indirect Access Register Offset: This regiser contains the 8-bit register offset for the indirect access.

7.6.1.60 IND_ACC_DATA Register (Address = 0x42) [Reset = 0x00]

IND_ACC_DATA is shown in Table 7-114.

Return to the Summary Table.

Table 7-114. IND_ACC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IND_ACC_DATA	R/W	0x0	Indirect Access Register Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register

7.6.1.61 VP_CONFIG_REG Register (Address = 0x43) [Reset = 0x01]

VP_CONFIG_REG is shown in Table 7-115.

Return to the Summary Table.

Video Processor Global Configuration Register

Table 7-115. VP_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	VP2VP_OL_EN	R/W	0x0	0x1 = Allows the overlap feature on VP0 and VP1 Using the Merged Output of VP2 and VP3 0x2 = Allows the overlap feature on VP2 and VP3 Using the Merged Output of VP0 and VP1
3	RESERVED	R	0x0	Reserved
2:0	NUM_VID_STREAMS	R/W	0x1	Number of Video Processors meant to be used. This field controls the memory allocation, in pixels, to the VPs (VP0:VP1:VP2:VP3) 0x0 = 16K:0:0:0 0x1 = 16K:16K:0:0 0x2 = 16K:8K:8K:0 0x3 = 8K:8K:8K:8K

7.6.1.62 VP_ENABLE_REG Register (Address = 0x44) [Reset = 0x00]

VP_ENABLE_REG is shown in Table 7-116.

Return to the Summary Table.

Video Processor Enable Register

Table 7-116. VP_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	VP3_ENABLE	R/W	0x0	Enable Video Processor 3 Additional control and status for VP3 are starting at register 0xC0 of Indirect Register page 12
2	VP2_ENABLE	R/W	0x0	Enable Video Processor 2 Additional control and status for VP2 are starting at register 0x80 of Indirect Register page 12
1	VP1_ENABLE	R/W	0x0	Enable Video Processor 1 Additional control and status for VP1 are starting at register 0x40 of Indirect Register page 12
0	VP0_ENABLE	R/W	0x0	Enable Video Processor 0 Additional control and status for VP0 are starting at register 0x00 of Indirect Register page 12

7.6.1.63 VP_GLOBAL_ISR Register (Address = 0x46) [Reset = 0x00]

VP_GLOBAL_ISR is shown in Table 7-117.

Return to the Summary Table.

Video Processor Global Interrupt Status Register
Summary of interrupt status from all video processors

Table 7-117. VP_GLOBAL_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	VP3_INTERRUPT	R	0x0	Video Processor Interrupt for Video Processor 3 Indicates if any of the bits in the VP_ISR_3 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
2	VP2_INTERRUPT	R	0x0	Video Processor Interrupt for Video Processor 2 Indicates if any of the bits in the VP_ISR_2 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP1_INTERRUPT	R	0x0	Video Processor Interrupt for Video Processor 1 Indicates if any of the bits in the VP_ISR_1 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
0	VP0_INTERRUPT	R	0x0	Video Processor Interrupt for Video Processor 0 Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.

7.6.1.64 BCC_CONFIG Register (Address = 0x47) [Reset = 0x00]

BCC_CONFIG is shown in Table 7-118.

Return to the Summary Table.

Table 7-118. BCC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	I2C_Controller_Disable	R/W	0x0	This bit will disable the remote reads and writes from the I2C controller. I2C controller writes and reads to the local registers will still work, but no remote writes and reads 0x0 = I2C controller remote read/write is enabled 0x1 = I2C controller remote read/writes is disabled
4	BCC_TERM_ON_ERR	R/W	0x0	Terminate Control Channel transactions on CRC Error detection During control channel operations, if a CRC Error occurs, it is unlikely to affect control channel operation. Setting this bit will allow more conservative operation that terminates any active Control Channel operation if an error is detected in the back channel. 0x0 = Don't terminate BCC transactions on CRC Errors 0x1 = Terminate BCC transactions on CRC Errors This bit will have no effect if Enhanced Error checking is disabled (BCC_EN_ENH_ERROR set to 0).
3	RESERVED	R	0x0	Reserved
2	BCC_ACK_REMOTE_READ	R/W	0x0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Serializer to generate an internal acknowlege to the beginning of a remote I2C target read. This allows additional error detection at the Deserializer. This bit should not be set when operating with Deserializers that do not support Enhanced Error Checking. 0x0 = Disable 0x1 = Enable

Table 7-118. BCC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BCC_EN_DATA_CHK	R/W	0x0	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, If an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit should not be set when operating with Deserializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. 0x0 = Disable returned data error detection 0x1 = Enable returned data error detection
0	BCC_EN_ENH_ERROR	R/W	0x0	Enable Enhanced Error checking in Bidirection Control Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0x0 = Disable Enhanced Error checking 0x1 = Enable Enhanced Error checking

7.6.1.65 APB_CTL Register (Address = 0x48) [Reset = 0x00]

APB_CTL is shown in Table 7-119.

Return to the Summary Table.

APB Control Register

Table 7-119. APB_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	APB_SELECT	R/W	0x0	APB Select: Selects target for register access: 0x0 = DisplayPort RX 0 APB registers 0x1 = Reserved 0x2 = Configuration Data (read only) 0x3 = Die ID (read only) 0x4 - 0xF = Reserved
2	APB_AUTO_INC	R/W	0x0	APB Auto Increment: Enables auto-increment mode. Upon completion of an APB read or write, the APB address will automatically be incremented by0x1
1	APB_READ	RH/W1S	0x0	Start APB Read: Setting this bit to a 1 will begin an APB read. Read data will be available in the APB_DATA0 register. The APB_ADR0 register should be programmed prior to setting this bit. This bit will be cleared when the read is complete.
0	APB_ENABLE	R/W	0x0	APB Interface Enable: Set to a 1 to enable the APB interface. The APB_SELECT bits indicate what device is selected.

7.6.1.66 APB_ADR0 Register (Address = 0x49) [Reset = 0x00]

APB_ADR0 is shown in Table 7-120.

Return to the Summary Table.

APB Address Register 0

Table 7-120. APB_ADR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APB_ADR0	R/W	0x0	APB Address byte 0 (LSB)

7.6.1.67 APB_ADR1 Register (Address = 0x4A) [Reset = 0x00]

APB_ADR1 is shown in Table 7-121.

Return to the Summary Table.

APB Address Register 1

Table 7-121. APB_ADR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APB_ADR1	R/W	0x0	APB Address byte 1 (MSB)

7.6.1.68 APB_DATA0 Register (Address = 0x4B) [Reset = 0x00]

APB_DATA0 is shown in Table 7-122.

Return to the Summary Table.

APB Data Register 0

Table 7-122. APB_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APB_DATA0	R/W	0x0	Byte 0 (LSB) of the APB Interface Data

7.6.1.69 APB_DATA1 Register (Address = 0x4C) [Reset = 0x00]

APB_DATA1 is shown in Table 7-123.

Return to the Summary Table.

APB Data Register 1

Table 7-123. APB_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APB_DATA1	R/W	0x0	Byte 1 of the APB Interface Data

7.6.1.70 APB_DATA2 Register (Address = 0x4D) [Reset = 0x00]

APB_DATA2 is shown in Table 7-124.

Return to the Summary Table.

APB Data Register 2

Table 7-124. APB_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APB_DATA2	R/W	0x0	Byte 2 of the APB Interface Data

7.6.1.71 APB_DATA3 Register (Address = 0x4E) [Reset = 0x00]

APB_DATA3 is shown in Table 7-125.

Return to the Summary Table.

APB Data Register 3

Table 7-125. APB_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APB_DATA3	R/W	0x0	Byte 3 (MSB) of the APB Interface Data

7.6.1.72 INTERRUPT_CTL Register (Address = 0x51) [Reset = 0x00]

INTERRUPT_CTL is shown in Table 7-126.

Return to the Summary Table.

Table 7-126. INTERRUPT_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INTB_PIN_EN	R/W	0x0	Global Interrupt Enable
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	IE_DP_RX0	R/W	0x0	DP Receiver Interrupt Enable interrupt from the DisplayPort Receiver
3	DEVICE_INT_EN	R/W	0x0	Enable local interrupts. ESD event counter, TEMP sensor, Voltage sensor, line fault. Check status reg 0x87
2	REMOTE_INT_EN	R/W	0x0	Enable remote interrupts. Remote interrupts are captured in REG 0xA6 and 0xA7.
1	IE_FPD_TX1	R/W	0x0	FPD TX Port 1 Interrupt Enable interrupt from FPD TX Port 1
0	IE_FPD_TX0	R/W	0x0	FPD TX Port 0 Interrupt Enable interrupt from FPD TX Port 0

7.6.1.73 INTERRUPT_STS Register (Address = 0x52) [Reset = 0x00]

INTERRUPT_STS is shown in Table 7-127.

Return to the Summary Table.

Table 7-127. INTERRUPT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL_INT	R	0x0	Global Interrupt Enable. Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INTB_PIN_EN bit in the INTERRUPT_CTL register. Bsically OR's the STS bits in this register only if corresponding IE* bit is set in INERRUPT_CTL register
6	RESERVED	R	0x0	Reserved
5	IS_DP_RX1	R	0x0	Reserved
4	IS_DP_RX0	R	0x0	DP Receiver Interrupt An interrupt has occurred for the DisplayPort Receiver. This interrupt will be cleared upon reading the APB 0x188 register.
3	DEVICE_INT	R	0x0	Local device interrupts. This bit set when any of the temprature, voltage monitor, line-fault and ESD interrupts is set register 0x87[3:0].
2	REMOTE_INT	R	0x0	Remote GPIOs interrupts. This bit set when any of the Back channel GPIO's Interrupt is high in the register status 0xA6[7:0] and 0xA7[5:0].
1	IS_FPD_TX1	R	0x0	FPD-Link III TX Port 1 Interrupt An interrupt has occurred for FPD TX Port 1 either in FPD-Link III or FPD-Link IV datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are FPD-Link III_PORT_STS1, FPD-Link IV_PORT_STS1.
0	IS_FPD_TX0	R	0x0	FPD-Link III TX Port 0 Interrupt An interrupt has occurred for FPD TX Port 0 either in FPD-Link III or FPD-Link IV datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are FPD-Link III_PORT_STS0, FPD-Link IV_PORT_STS0

7.6.1.74 AUDIO_CFG Register (Address = 0x53) [Reset = 0x22]

AUDIO_CFG is shown in Table 7-128.

Return to the Summary Table.

Table 7-128. AUDIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TDM_2_PARALLEL	R/W	0x0	Enable TDM to parallel I2S audio conversion: When this bit is set, the TDM to parallel I2S conversion is enabled. TDM audio data on the I2S_DA pin will be split onto four I2S data signals.
6	PARALLEL_2_TDM	R/W	0x0	Enable Parallel to TDM Audio conversion: Setting this bit to a 1 will enable TDM audio conversion for the I2S audio. Parallel I2S data on the I2S pins will be serialized onto a single I2S_DA signal for sending over the serial link.
5	AUDIO_MODE	R/W	0x1	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0x0 = Undefined 0x1 = I2S audio from I2S pins
4	RESERVED	R/W	0x0	Reserved
3	TDM_FS_MODE	R/W	0x0	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio generator. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0x0 = Active high Frame Sync 0x1 = Active low Frame Sync (similar to I2S word select) This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
2	TDM_DELAY	R/W	0x0	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0x0 = Data is not delayed from Frame Sync (data is left justified) 0x1 = Data is delayed 1 bit from Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
1:0	TDM_FS_WIDTH	R/W	0x2	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion 00b = FS is 50/50 duty cycle 01b = FS is one slot/channel wide 1xb = FS is 1 clock pulse wide

7.6.1.75 SPI_TIMING1 Register (Address = 0x54) [Reset = 0x22]

SPI_TIMING1 is shown in Table 7-129.

Return to the Summary Table.

Table 7-129. SPI_TIMING1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SPI_HOLD	R/W	0x2	SPI Data Hold from SPI clock: FPD-Link III only These bits set the minimum hold time for SPI data following the SPI clock sampling edge. In addition, this also sets the minimum active pulse width for the SPI output clock. Hold = (SPI_HOLD + 1) * 40ns For example, default setting of 2 will result in 120ns data hold time.

Table 7-129. SPI_TIMING1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SPI_SETUP	R/W	0x2	SPI Data Setup to SPI Clock: FPD-Link III only These bits set the minimum setup time for SPI data to the SPI clock active edge. In addition, this also sets the minimum inactive width for the SPI output clock. Hold = (SPI_SETUP + 1) * 40ns For example, default setting of 2 will result in 120ns data setup time.

7.6.1.76 SPI_TIMING2 Register (Address = 0x55) [Reset = 0x02]

SPI_TIMING2 is shown in Table 7-130.

Return to the Summary Table.

Table 7-130. SPI_TIMING2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SPI_CS_SETUP	R/W	0x2	SPI Target Select Setup: FPD-Link III only This field controls the delay from assertion of the Target Select low to initial data timing. Delays are in units of 40ns. Delay = (SPI_CS_SETUP + 1) * 40ns

7.6.1.77 SPI_CONFIG Register (Address = 0x56) [Reset = 0x00]

SPI_CONFIG is shown in Table 7-131.

Return to the Summary Table.

Table 7-131. SPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_CTRL_OVER	R	0x0	SPI Controller Overflow Detection: FPD-Link III only This flag is set if the SPI Controller detects an overflow condition. This occurs if the SPI Controller is unable to regenerate the remote SPI data at a fast enough rate to keep up with data arriving from the remote Deserializer. If this condition occurs, it suggests the SPI_SETUP and SPI_HOLD times should be set to smaller values. This flag is cleared by setting the SPI_CLR_OVER bit in this register.
6:3	RESERVED	R	0x0	Reserved
2	SPI_CLR_OVER	R/W	0x0	Clear SPI Controller Overflow Flag: FPD-Link III only Setting this bit to 1 will clear the SPI Controller Overflow Detection flag (SPI_CTRL_OVER). This bit is not self-clearing and must be set back to 0.
1	SPI_CPHA	R	0x0	SPI Clock Phase setting: FPD-Link III only Determines which phase of the SPI clock is used for sampling data. 0x0 = Data sampled on leading (first) clock edge 0x1 = Data sampled on trailing (second) clock edge This bit is read-only, with a value of 0. The serializer does not support CPHA of 1.
0	SPI_CPOL	R/W	0x0	SPI Clock Polarity setting: FPD-Link III only Determines the base (inactive) value of the SPI clock. 0x0 = base value of the clock is 0 0x1 = base value of the clock is 1 This bit affects both capture and propagation of SPI signals.

7.6.1.78 FPD3_STREAM_SEL Register (Address = 0x57) [Reset = 0x00]

FPD3_STREAM_SEL is shown in Table 7-132.

Return to the Summary Table.

FPD-LINK III Video Stream Select

Table 7-132. FPD3_STREAM_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	FPD3_STREAM	R/W	0x0	FPD-Link III Stream Selects the video processor stream to connect to the selected FPD-Link III transmitter 0x0 = TX Port 0 0x1 = TX Port 1

7.6.1.79 FPD3_DUAL_STS Register (Address = 0x58) [Reset = 0x00]

FPD3_DUAL_STS is shown in Table 7-133.

Return to the Summary Table.

FPD-LINK III Status. This register shows status for the selected FPD-Link III.

Table 7-133. FPD3_DUAL_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FPD3_LINK_RDY	R	0x0	FPD-Link III Link ready: This bit indicates that the FPD-Link III link has detected a valid downstream connection and determined capabilities for the downstream link.
6	FPD3_TX_STS	R	0x0	FPD-Link III Transmit status: This bit indicates that the FPD-Link III Transmitter is active and the receiver is locked to the transmit clock. It is only asserted once a valid input has been detected, and the FPD-Link III Transmit connection has entered the correct mode (i.e. Single vs Dual mode)..
5:4	FPD3_PORT_STS	R	0x0	FPD-Link III Port Status: If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 0x0 = Dual FPD-Link III Transmitter mode 0x1 = Single FPD-Link III Transmit on port 0 0x2 = Single FPD-Link III Transmit on port 1 0x3 = FPD-Link III Transmit on both ports (Replicate or Splitter mode)
3:0	RESERVED	R	0x0	Reserved

7.6.1.80 FPD3_MODE_CTL Register (Address = 0x59) [Reset = 0x00]

FPD3_MODE_CTL is shown in Table 7-134.

Return to the Summary Table.

FPD-LINK III Mode Control.

Table 7-134. FPD3_MODE_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DUAL_ALIGN_DE	R/W	0x0	Dual Align on DE: In dual-link mode, if this bit is set to a 1, the odd/even data will be sent on the primary/secondary links respectively, based on the assertion of DE. If this bit is set to a 0, data will be sent on alternating links without regard to odd/even pixel position.

Table 7-134. FPD3_MODE_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DISABLE_DUAL_SWAP	R/W	0x0	Disable Dual Swap: Prevents automatic correction of swapped Dual link connection. Setting this bit allows writes to the DUAL_SWAP control in the DUAL_CTL1 register
4	DUAL_SWAP	R/W	0x0	Dual Swap Control: Indicates current status of the Dual Swap control. If automatic correction of Dual Swap is disabled via the DISABLE_DUAL_SWAP control, this bit may be modified by software.
3	FORCE_LINK_RDY	R/W	0x0	Force Link Ready: Forces link ready indication, bypassing back channel link detection. To enable desired operation, it may be necessary to force the Deserializer capabilites registers (DES_CAP1 and DES_CAP2) for each port.
2:0	FPD3_TX_MODE	R/WStrap	0x0	FPD-Link III TX Mode: This register controls the operating mode of the FPD-Link III Transmit function. 0x0 = Reserved 0x1 = Forced Single Port 0 FPD-Link III Transmitter mode 0x2 = Forced Single Port 1 FPD-Link III Transmitter mode 0x3 = Forced Dual FPD-Link III Transmitter mode 0x4 = Reserved 0x5 = Forced Independent FPD-Link III mode 0x6 = Reserved 0x7 = Forced Splitter Mode (half of video stream on each port) Default value is set by the MODE_SEL0 pin

7.6.1.81 FPD3_DATAPATH_CTL Register (Address = 0x5A) [Reset = 0x02]

FPD3_DATAPATH_CTL is shown in Table 7-135.

Return to the Summary Table.

FPD-LINK III Datapath Control. This configures the selected FPD-Link III.

Table 7-135. FPD3_DATAPATH_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	DE_POLARITY	R/W	0x0	FPD-Link III only This bit indicates the polarity of the DE (Data Enable) signal. 0x0 = DE is positive (active high, idle low) 0x1 = DE is inverted (active low, idle high)
4	RESERVED	R/W	0x0	Reserved
3	I2S_TRANSPORT_SEL	R/W	0x0	FPD-Link III only 0x0 = Enable I2S Data Island Transport 0x1 = Enable I2S Data Forward Channel Frame Transport
2	VIDEO_18B_EN	R/W	0x0	FPD-Link III only 18-bit Video Select 0x0 = Select 24-bit video mode 0x1 = Select 18-bit video mode

Table 7-135. FPD3_DATAPATH_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	I2S_MODE	R/W	0x2	FPD-Link III only I2S Channel Mode 0x0 = 2-channel I2S audio 0x1 = 4-channel I2S audio 0x2 = 5.1- or 7.1-channel surround audio is enabled 0x3 = Reserved Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

7.6.1.82 FPD3_FIFO_CFG Register (Address = 0x5B) [Reset = 0x23]

FPD3_FIFO_CFG is shown in Table 7-136.

Return to the Summary Table.

Table 7-136. FPD3_FIFO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	FPD3_ALIGN_ERR_THR	R/W	0x2	FPD-Link III Channel Alignment Error Threshold This field configures the threshold for flagging an error in FPD-Link III channel alignment. If the FPD-Link III Channel Alignment (FPD3_CHAN_ALIGN) magnitude is greater than this value, an error will be flagged in FPD3_CHAN_ALIGN_ERR.
3	ENABLE_FPD3_FIFO	R/W	0x0	Enable 35- to 40-bit FIFO This bit enables the 35- to 40-bit FIFOs.
2:0	FPD3_FIFO_DRAIN	R/W	0x3	Drain threshold for 35- to 40-bit FIFOs in 40-bit words This field configures the number of 40-bit words available in the 35-bit to 40-bit FIFO at which to start draining the FIFO. Valid values are 0-3; values above 3 will likely cause FIFO overruns. A value of 7 is invalid.

7.6.1.83 FPD3_FIFO_STS Register (Address = 0x5C) [Reset = 0x00]

FPD3_FIFO_STS is shown in Table 7-137.

Return to the Summary Table.

Table 7-137. FPD3_FIFO_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	FPD3_CHAN_ALIGN_ERR	RC	0x0	FPD-Link III Channel Alignment Error This bit indicates an error in alignment between the two FPD-Link III channels.
3:0	RESERVED	RC	0x0	Reserved

7.6.1.84 ESD_EVENT_INT_CONTROL Register (Address = 0x61) [Reset = 0x00]

ESD_EVENT_INT_CONTROL is shown in Table 7-138.

Return to the Summary Table.

Table 7-138. ESD_EVENT_INT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ESD_EVENT_INT_STS_CLR	R/W	0x0	When set upon read, this bit indicates ESD Event counter > ESD Event counter threshould When programmed to 1, clears the ESD_EVENT_INT

Table 7-138. ESD_EVENT_INT_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ESD_EVENT_INT_EN	R/W	0x0	ESD Event Interrupt enable bit
5:0	ESD_EVENT_COUNTER_THRESHOLD	R/W	0x0	ESD Event Counter Threshold

7.6.1.85 FC_POWERDOWN_CTL Register (Address = 0x62) [Reset = 0x00]

FC_POWERDOWN_CTL is shown in Table 7-139.

Return to the Summary Table.

Table 7-139. FC_POWERDOWN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	PD_FCTX	R/W	0x0	Override Value for powering down the FC transmitter
2	PD_FCTX_OV	R/W	0x0	Override enable for powering down the FC transmitter
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

7.6.1.86 BC_POWERDOWN_CTL Register (Address = 0x63) [Reset = 0x00]

BC_POWERDOWN_CTL is shown in Table 7-140.

Return to the Summary Table.

Table 7-140. BC_POWERDOWN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PD_BCRX	R/W	0x0	Override Value for powering down the BC receiver
4	RESERVED	R/W	0x0	Reserved
3	RSTB_BC	R/W	0x0	Override Value for resetting the BC
2	RESERVED	R/W	0x0	Reserved
1	RSTB_BC_EARLY	R/W	0x0	Override Value for resetting the BC early signal
0	RESERVED	R/W	0x0	Reserved

7.6.1.87 BC_DOWNSAMPLING_CFG Register (Address = 0x6A) [Reset = 0x0A]

BC_DOWNSAMPLING_CFG is shown in Table 7-141.

Return to the Summary Table.

Table 7-141. BC_DOWNSAMPLING_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BC_DOWNSAMPLING_RATE	R/WStrap	0x0	Back channel down sampling rate 0x0 = downsampling rate 1 (10.8/6.75/3.375 Gbps IVI Strap) 0x1 = downsampling rate 2 (13.5/12.528 Gbps IVI Strap)
5	RESERVED	R/W	0x0	Reserved
4:0	RESERVED	R/W	0xA	Reserved

7.6.1.88 ENH_BC_STS Register (Address = 0x6B) [Reset = 0x00]

ENH_BC_STS is shown in Table 7-142.

Return to the Summary Table.

BCC Status Register
This register provides error status for the Bidirectional Control Channel.

Table 7-142. ENH_BC_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	ALIGN_ERR_P3	R	0x0	Align Error Flag When ENH_BC_CHK_EN is set in ENH_BC_CHK register, then this bit will show the status the alignment error flag, This occurs if a valid K 28.5 code occurs in a different byte than expected,
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	VALID_K_CODE_ERR_P3	R	0x0	Valid K Code Error Flag When ENH_BC_CHK_EN is set in ENH_BC_CHK register, then this bit will show the status of valid K code errors. This occurs when the K code is valid but not the K28.5 code that is expected.

7.6.1.89 BCC_STATUS Register (Address = 0x6D) [Reset = 0x00]

BCC_STATUS is shown in Table 7-143.

Return to the Summary Table.

Table 7-143. BCC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	BCC_CONTROLLER_ERR_P3	RC	0x0	BCC Controller Error This flag indicates a back channel CRC error or loss of back channel Lock occurred while waiting for a response from the Deserializer while the BCC I2C Controller is active. This flag is cleared on read of this register.
3	BCC_CONTROLLER_TO_P3	RC	0x0	BCC Target Timeout Error This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the Deserializer while the BCC I2C Controller is active. This flag is cleared on read of this register.
2	BCC_TARGET_ERR_P3	RC	0x0	BCC Target Error This flag indicates a back channel CRC error or loss of back channel Lock occurred while waiting for a response from the Deserializer while the BCC I2C Target is active. This flag is cleared on read of this register.
1	BCC_TARGET_TO_P3	RC	0x0	BCC Target Timeout Error This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the Deserializer while the BCC I2C Target is active. This flag is cleared on read of this register.
0	BCC_RESP_ERR_P3	RC	0x0	This flag indicates an error has been detected in response to a command on the Bidirectional Control Channel. When the Serializer sends a control channel frame, the Deserializer should return the 8-bit data field in the subsequent response. The Serializer checks the returned data for errors, and will set this flag if an error is detected. This flag is cleared on read of this register .

7.6.1.90 BC_CONFIG Register (Address = 0x6E) [Reset = 0x86]

BC_CONFIG is shown in Table 7-144.

Return to the Summary Table.

Table 7-144. BC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2:0	BC_CONFIG	R/WStrap	0x6	0x0 = 13.5/12.528/6.75/3.375 Gbps IVI Strap 0x6 = 10.8 Gbps IVI Strap

7.6.1.91 FC_BCC_TEST Register (Address = 0x6F) [Reset = 0x00]

FC_BCC_TEST is shown in Table 7-145.

Return to the Summary Table.

Forward Channel BCC Test Register
This register allows forcing error conditions on the Forward Channel BCC interface. This allows system testing of error handling.

Table 7-145. FC_BCC_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	FORCE_BCC_ERROR_P3	RH/W1S	0x0	Force an error on forward channel BCC frame Setting the FORCE_BCC_ERROR bit will cause an error to be forced on a forward channel BCC frame. The BCC_ERROR_SEL and BCC_FRAME_SEL fields in this register determine the type of error to be forced and which frame will include the error. This bit is self-clearing and will always return 0.
5:3	BCC_ERROR_SEL_P3	R/W	0x0	BCC Error Select The BCC Error Select determines which type of error is forced on a forward channel BCC frame. 0x0 = No error 0x1 = Force CRC Error 0x2 = Force Sequence Error (skips one sequence number) 0x3 = Drop BCC Frame (results in sequence error at Deserializer) 0x4 = Force error on Data field (random bit 1 through 7) 0x5 = Force error on Data field, bit 0 (RW bit if during Start command) 0x6 - 0x7 = Reserved
2:0	BCC_FRAME_SEL_P3	R/W	0x0	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

7.6.1.92 TARGET_ID_0 Register (Address = 0x70) [Reset = 0x00]

TARGET_ID_0 is shown in Table 7-146.

Return to the Summary Table.

Remove Target ID register 0

Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-146. TARGET_ID_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.93 TARGET_ID_1 Register (Address = 0x71) [Reset = 0x00]

TARGET_ID_1 is shown in Table 7-147.

Return to the Summary Table.

Remove Target ID register 1
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-147. TARGET_ID_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.94 TARGET_ID_2 Register (Address = 0x72) [Reset = 0x00]

TARGET_ID_2 is shown in Table 7-148.

Return to the Summary Table.

Remove Target ID register 2
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-148. TARGET_ID_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.95 TARGET_ID_3 Register (Address = 0x73) [Reset = 0x00]

TARGET_ID_3 is shown in Table 7-149.

Return to the Summary Table.

Remove Target ID register 3

Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-149. TARGET_ID_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.96 TARGET_ID_4 Register (Address = 0x74) [Reset = 0x00]

TARGET_ID_4 is shown in Table 7-150.

Return to the Summary Table.

Remove Target ID register 4
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-150. TARGET_ID_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID4	R/W	0x0	7-bit Remote Target Device ID 4 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.97 TARGET_ID_5 Register (Address = 0x75) [Reset = 0x00]

TARGET_ID_5 is shown in Table 7-151.

Return to the Summary Table.

Remove Target ID register 5
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-151. TARGET_ID_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.98 TARGET_ID_6 Register (Address = 0x76) [Reset = 0x00]

TARGET_ID_6 is shown in Table 7-152.

Return to the Summary Table.

Remove Target ID register 6

Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-152. TARGET_ID_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.99 TARGET_ID_7 Register (Address = 0x77) [Reset = 0x00]

TARGET_ID_7 is shown in Table 7-153.

Return to the Summary Table.

Remove Target ID register 7
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-153. TARGET_ID_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R/W	0x0	Reserved

7.6.1.100 TARGET_ALIAS_0 Register (Address = 0x78) [Reset = 0x00]

TARGET_ALIAS_0 is shown in Table 7-154.

Return to the Summary Table.

Remove Target Alias register 0
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-154. TARGET_ALIAS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID0	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

7.6.1.101 TARGET_ALIAS_1 Register (Address = 0x79) [Reset = 0x00]

TARGET_ALIAS_1 is shown in Table 7-155.

Return to the Summary Table.

Remove Target Alias register 1
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-155. TARGET_ALIAS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID1	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID1.

7.6.1.102 TARGET_ALIAS_2 Register (Address = 0x7A) [Reset = 0x00]

TARGET_ALIAS_2 is shown in Table 7-156.

Return to the Summary Table.

Remove Target Alias register 2
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-156. TARGET_ALIAS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID2	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID2

7.6.1.103 TARGET_ALIAS_3 Register (Address = 0x7B) [Reset = 0x00]

TARGET_ALIAS_3 is shown in Table 7-157.

Return to the Summary Table.

Remove Target Alias register 3
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-157. TARGET_ALIAS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.

Table 7-157. TARGET_ALIAS_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LCL_PORTSEL_ID3	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID3.

7.6.1.104 TARGET_ALIAS_4 Register (Address = 0x7C) [Reset = 0x00]

TARGET_ALIAS_4 is shown in Table 7-158.

Return to the Summary Table.

Remove Target Alias register 4
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-158. TARGET_ALIAS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID4	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID4.

7.6.1.105 TARGET_ALIAS_5 Register (Address = 0x7D) [Reset = 0x00]

TARGET_ALIAS_5 is shown in Table 7-159.

Return to the Summary Table.

Remove Target Alias register 5
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-159. TARGET_ALIAS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID5	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID5.

7.6.1.106 TARGET_ALIAS_6 Register (Address = 0x7E) [Reset = 0x00]

TARGET_ALIAS_6 is shown in Table 7-160.

Return to the Summary Table.

Remove Target Alias register 6
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-160. TARGET_ALIAS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID6	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID6.

7.6.1.107 TARGET_ALIAS_7 Register (Address = 0x7F) [Reset = 0x00]

TARGET_ALIAS_7 is shown in Table 7-161.

Return to the Summary Table.

Remove Target Alias register 7
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-161. TARGET_ALIAS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	TARGET_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID7	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID7.

7.6.1.108 LOCAL_INT_STS Register (Address = 0x87) [Reset = 0x00]

LOCAL_INT_STS is shown in Table 7-162.

Return to the Summary Table.

Table 7-162. LOCAL_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	INTERRUPT_TEMP	R	0x0	Interrupt status for temperature sensor
2	INTERRUPT_VOLT	R	0x0	Interrupt status for voltage monitor
1	INTERRUPT_LINE_FAULT	R	0x0	Interrupt status for line fault
0	INTERRUPT_ESD_EVENT	R	0x0	Interrupt status for ESD event

7.6.1.109 TARGET_DEST_0 Register (Address = 0x88) [Reset = 0x00]

TARGET_DEST_0 is shown in Table 7-163.

Return to the Summary Table.

Remove Target Destination register 0

Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-163. TARGET_DEST_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.110 TARGET_DEST_1 Register (Address = 0x89) [Reset = 0x00]

TARGET_DEST_1 is shown in Table 7-164.

Return to the Summary Table.

Remove Target Destination register 1
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-164. TARGET_DEST_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.111 TARGET_DEST_2 Register (Address = 0x8A) [Reset = 0x00]

TARGET_DEST_2 is shown in Table 7-165.

Return to the Summary Table.

Remove Target Destination register 2
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-165. TARGET_DEST_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.112 TARGET_DEST_3 Register (Address = 0x8B) [Reset = 0x00]

TARGET_DEST_3 is shown in Table 7-166.

Return to the Summary Table.

Remove Target Destination register 3
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-166. TARGET_DEST_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1

Table 7-166. TARGET_DEST_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.113 TARGET_DEST_4 Register (Address = 0x8C) [Reset = 0x00]

TARGET_DEST_4 is shown in Table 7-167.

Return to the Summary Table.

Remove Target Destination register 4
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-167. TARGET_DEST_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.114 TARGET_DEST_5 Register (Address = 0x8D) [Reset = 0x00]

TARGET_DEST_5 is shown in Table 7-168.

Return to the Summary Table.

Remove Target Destination register 5
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-168. TARGET_DEST_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1

Table 7-168. TARGET_DEST_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.115 TARGET_DEST_6 Register (Address = 0x8E) [Reset = 0x00]

TARGET_DEST_6 is shown in Table 7-169.

Return to the Summary Table.

Remove Target Destination register 6
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-169. TARGET_DEST_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.116 TARGET_DEST_7 Register (Address = 0x8F) [Reset = 0x00]

TARGET_DEST_7 is shown in Table 7-170.

Return to the Summary Table.

Remove Target Destination register 7
Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 7-170. TARGET_DEST_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEST_ADDR		0x0	Destination port selection
4	FIRST_DC_PSEL		0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
3	MID_DC_PSEL		0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
2	FINAL_DC_PSEL		0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0x0 = BCC commands route through Port 0 0x1 = BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 0x0 = 0 remaining depth 0x1 = 1 remaining depth 0x2 = 2 remaining depth 0x3 = 3 remaining depth

7.6.1.117 RX_BCAPS Register (Address = 0xA0) [Reset = 0x00]

RX_BCAPS is shown in Table 7-171.

Return to the Summary Table.

Table 7-171. RX_BCAPS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.6.1.118 KSV_FIFO Register (Address = 0xA3) [Reset = 0x00]

KSV_FIFO is shown in Table 7-172.

Return to the Summary Table.

Table 7-172. KSV_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	KSV_FIFO_DWNSTRM_RCVR	R	0x0	Each read of the KSV FIFO returns one byte of the KSV FIFO list composed by the downstream Receiver.

7.6.1.119 GPIO_INT_CTL0 Register (Address = 0xA4) [Reset = 0x00]

GPIO_INT_CTL0 is shown in Table 7-173.

Return to the Summary Table.

Table 7-173. GPIO_INT_CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GPIO_INT_CTL0	R/W	0x0	Enable Interrupt from GPIO [7:0]. The interrupts are based on BC GPIO slots.

7.6.1.120 GPIO_INT_CTL1 Register (Address = 0xA5) [Reset = 0x00]

GPIO_INT_CTL1 is shown in Table 7-174.

Return to the Summary Table.

Table 7-174. GPIO_INT_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5:0	GPIO_INT_CTL1	R/W	0x0	Enable Interrupt from GPIO [15:8]. The interrupts are based on BC GPIO slots. (GPIO[15:14] are reserved.)

7.6.1.121 GPIO_INT_STS0 Register (Address = 0xA6) [Reset = 0x00]

GPIO_INT_STS0 is shown in Table 7-175.

Return to the Summary Table.

Table 7-175. GPIO_INT_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GPIO_INT_STS0	RW/WCOR	0x0	Interrupt Status from GPIO [7:0] Interrupt bit is asserted by rising edge of GPIO bit and Clear-on-Read.

7.6.1.122 GPIO_INT_STS1 Register (Address = 0xA7) [Reset = 0x00]

GPIO_INT_STS1 is shown in Table 7-176.

Return to the Summary Table.

Table 7-176. GPIO_INT_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	RW/WCOR	0x0	Reserved
5:0	GPIO_INT_STS1	RW/WCOR	0x0	Interrupt Status from GPIO [15:8] Interrupt bit is asserted by rising edge of GPIO bit and Clear-on-Read. (GPIO[15:14] are reserved)

7.6.1.123 FPD_TX_ESD_EVENT_CNTR Register (Address = 0xBC) [Reset = 0x3F]

FPD_TX_ESD_EVENT_CNTR is shown in Table 7-177.

Return to the Summary Table.

Table 7-177. FPD_TX_ESD_EVENT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	

Table 7-177. FPD_TX_ESD_EVENT_CNTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	ESD_EVENT_COUNTER	R	0x3F	ESD Event Counter Displays the number of ESD events that have occurred ESD Event Counter Enable At power up this register should be disabled and re-enabled to clear the effects of power supply transients Writing a 0 to this register will clear the ESD_EVENT_COUNTER register to 0.

7.6.1.124 DUAL_VIDSYNC Register (Address = 0xBF) [Reset = 0x00]

DUAL_VIDSYNC is shown in Table 7-178.

Return to the Summary Table.

Table 7-178. DUAL_VIDSYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	DUAL_VIDSYNC_SLV	R/W	0x0	This device is a target in dual video sync mode: 1-target, 0- controller
0	DUAL_VIDSYNC_MODE	R/W	0x0	Video sync mode between dual SER/dual channels: 1- enabled, 0- disabled

7.6.1.125 FPD3_ICR Register (Address = 0xC6) [Reset = 0x00]

FPD3_ICR is shown in Table 7-179.

Return to the Summary Table.

Table 7-179. FPD3_ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	IE_RXDET_INT	R/W	0x0	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If LINK_CFG[3] (RX_DET_SEL) is set to a 1, the interrupt will wait for Receiver Lock Detect.
5	IE_RX_REM_INT	R/W	0x0	Interrupt on Receiver interrupt: Enables interrupt on indication from the downstream receiver. Allows propagation of interrupts from downstream devices.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

7.6.1.126 FPD3_ISR Register (Address = 0xC7) [Reset = 0x00]

FPD3_ISR is shown in Table 7-180.

Return to the Summary Table.

Table 7-180. FPD3_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 7-180. FPD3_ISR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	IS_RXDET_INT	R	0x0	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If If LINK_CFG[3] (RX_DET_SEL) is set to a 1, the interrupt will wait for Receiver Lock Detect.
5	IS_RX_REM_INT	R	0x0	Interrupt on Receiver interrupt: Receiver has indicated an interrupt request from down-stream device.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	INT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated.

7.6.1.127 LINK_CFG_ALIAS Register (Address = 0xE2) [Reset = 0x82]

LINK_CFG_ALIAS is shown in Table 7-181.

Return to the Summary Table.

Table 7-181. LINK_CFG_ALIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LINK_CFG	R	0x82	Read-only alias of LINK_CFG register

7.6.1.128 FPD3_STS_ALIAS Register (Address = 0xE4) [Reset = 0x40]

FPD3_STS_ALIAS is shown in Table 7-182.

Return to the Summary Table.

Table 7-182. FPD3_STS_ALIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FPD3_STS	R	0x40	Read-only alias of FPD3_STS register

7.6.1.129 FPD3_ICR_ALIAS Register (Address = 0xE6) [Reset = 0x00]

FPD3_ICR_ALIAS is shown in Table 7-183.

Return to the Summary Table.

Table 7-183. FPD3_ICR_ALIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FPD3_ICR	R	0x0	Read-only alias of FPD3_ICR register

7.6.1.130 FPD3_ISR_ALIAS Register (Address = 0xE7) [Reset = 0x00]

FPD3_ISR_ALIAS is shown in Table 7-184.

Return to the Summary Table.

Table 7-184. FPD3_ISR_ALIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FPD3_ISR	R	0x0	Read-only alias of FPD3_ISR register

7.6.1.131 TX_ID0 Register (Address = 0xF0) [Reset = 0x5F]

TX_ID0 is shown in Table 7-185.

Return to the Summary Table.

Table 7-185. TX_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID0	R	0x5F	TX_ID0: First byte ID code, '_ '

7.6.1.132 TX_ID1 Register (Address = 0xF1) [Reset = 0x55]

TX_ID1 is shown in Table 7-186.

Return to the Summary Table.

Table 7-186. TX_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID1	R	0x55	TX_ID1: 2nd byte of ID code, 'U '

7.6.1.133 TX_ID2 Register (Address = 0xF2) [Reset = 0x48]

TX_ID2 is shown in Table 7-187.

Return to the Summary Table.

Table 7-187. TX_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID2	R	0x48	TX_ID2: 3rd byte of ID code. Value will be either 'B ' or 'H '. 'H ' indicates an HDCP capable device. UB = 0x42 UH = 0x48

7.6.1.134 TX_ID3 Register (Address = 0xF3) [Reset = 0x39]

TX_ID3 is shown in Table 7-188.

Return to the Summary Table.

Table 7-188. TX_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID3	R	0x39	TX_ID3: 4th byte of ID code, '9 '

7.6.1.135 TX_ID4 Register (Address = 0xF4) [Reset = 0x38]

TX_ID4 is shown in Table 7-189.

Return to the Summary Table.

Table 7-189. TX_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID4	R	0x38	TX_ID4: 5th byte of ID code, '8'

7.6.1.136 TX_ID5 Register (Address = 0xF5) [Reset = 0x33]

TX_ID5 is shown in Table 7-190.

Return to the Summary Table.

Table 7-190. TX_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID5	R	0x33	TX_ID5: 6th byte of ID code, '3'

7.6.1.137 TX_ID6 Register (Address = 0xF6) [Reset = 0x30]

TX_ID6 is shown in Table 7-191.

Return to the Summary Table.

Table 7-191. TX_ID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_ID6	R	0x30	TX_ID6: 7th byte of ID code, '0'

7.6.1.138 IND_REG_I2C_CTL0 Register (Address = 0xF8) [Reset = 0x00]

IND_REG_I2C_CTL0 is shown in Table 7-192.

Return to the Summary Table.

Table 7-192. IND_REG_I2C_CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	IND_ACC_SEL0	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0x0 = Disabled 0x1 = FPD Ports 0-1 registers including broadcast write 0x2 = FPD PLL 0-1 registers including broadcast write 0x3 = Reserved 0x4 = DisplayPort lanes 0-1 registers 0x5 = DisplayPort lanes 2-3 registers 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = DFT/DP PLL Common Registers 0xA = Reserved 0xB = TX Link Layer Registers 0xC = Video Processor 0/1/2/3 Registers 0xD = Reserved 0xE = SAR ADC Registers 0xF = Reserved NOTE: This register acts the same way as the TX_PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.

7.6.1.139 IND_REG_I2C_ID0 Register (Address = 0xF9) [Reset = 0x00]

IND_REG_I2C_ID0 is shown in Table 7-193.

Return to the Summary Table.

Table 7-193. IND_REG_I2C_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	IND_I2C_ID0	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL0; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

7.6.1.140 IND_REG_I2C_CTL1 Register (Address = 0xFA) [Reset = 0x00]

IND_REG_I2C_CTL1 is shown in Table 7-194.

Return to the Summary Table.

Table 7-194. IND_REG_I2C_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	IND_ACC_SEL1	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0x0 = Disabled 0x1 = FPD Ports 0-1 registers including broadcast write 0x2 = FPD PLL 0-1 registers including broadcast write 0x3 = Reserved 0x4 = DisplayPort lanes 0-1 registers 0x5 = DisplayPort lanes 2-3 registers 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = DFT/DP PLL Common Registers 0xA = Reserved 0xB = TX Link Layer Registers 0xC = Video Processor 0/1/2/3 Registers 0xD = Reserved 0xE = SAR ADC Registers 0xF = Reserved NOTE: This register acts the same way as the TX_PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.

7.6.1.141 IND_REG_I2C_ID1 Register (Address = 0xFB) [Reset = 0x00]

IND_REG_I2C_ID1 is shown in Table 7-195.

Return to the Summary Table.

Table 7-195. IND_REG_I2C_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	IND_I2C_ID1	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL1; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

7.6.1.142 IND_REG_I2C_CTL2 Register (Address = 0xFC) [Reset = 0x00]

IND_REG_I2C_CTL2 is shown in Table 7-196.

Return to the Summary Table.

Table 7-196. IND_REG_I2C_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	IND_ACC_SEL2	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0x0 = Disabled 0x1 = FPD Ports 0-1 registers including broadcast write 0x2 = FPD PLL 0-1 registers including broadcast write 0x3 = Reserved 0x4 = DisplayPort lanes 0-1 registers 0x5 = DisplayPort lanes 2-3 registers 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = DFT/DP PLL Common Registers 0xA = Reserved 0xB = TX Link Layer Registers 0xC = Video Processor 0/1/2/3 Registers 0xD = Reserved 0xE = SAR ADC Registers 0xF = Reserved NOTE: This register acts the same way as the TX_PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.

7.6.1.143 IND_REG_I2C_ID2 Register (Address = 0xFD) [Reset = 0x00]

IND_REG_I2C_ID2 is shown in Table 7-197.

Return to the Summary Table.

Table 7-197. IND_REG_I2C_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	IND_I2C_ID2	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL2; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

7.6.1.144 IND_REG_I2C_CTL3 Register (Address = 0xFE) [Reset = 0x00]

IND_REG_I2C_CTL3 is shown in Table 7-198.

Return to the Summary Table.

Table 7-198. IND_REG_I2C_CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 7-198. IND_REG_I2C_CTL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	IND_ACC_SEL3	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0x0 = Disabled 0x1 = FPD Ports 0-1 registers including broadcast write 0x2 = FPD PLL 0-1 registers including broadcast write 0x3 = Reserved 0x4 = DisplayPort lanes 0-1 registers 0x5 = DisplayPort lanes 2-3 registers 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = DFT/DP PLL Common Registers 0xA = Reserved 0xB = TX Link Layer Registers 0xC = Video Processor 0/1/2/3 Registers 0xD = Reserved 0xE = SAR ADC Registers 0xF = Reserved NOTE: This register acts the same way as the TX_PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.

7.6.1.145 IND_REG_I2C_ID3 Register (Address = 0xFF) [Reset = 0x00]

IND_REG_I2C_ID3 is shown in Table 7-199.

Return to the Summary Table.

Table 7-199. IND_REG_I2C_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	IND_I2C_ID3	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL3; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

7.6.2 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map (Table 7-200). Register access is provided via an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0x40-0x42 in the Main Page_0 register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:
1. Write to the IND_ACC_CTL (0x40) register to select the desired register block
2. Write to the IND_ACC_ADDR (0x41) register to set the register offset
3. Write the data value to the IND_ACC_DATA (0x42) register

If auto-increment is set in the IND_ACC_CTL register, repeating Step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:
1. Write to the IND_ACC_CTL (0x40) register to select the desired register block
2. Write to the IND_ACC_ADDR (0x41) register to set the register offset
3. Read from the IND_ACC_DATA (0x42) register

If auto-increment is set in the IND_ACC_CTL register, repeating Step 3 will read additional data bytes from subsequent register offset locations.

Table 7-200. Indirect Register Map Description

IA SELECT 0x40[5:2]	PAGE/BLOCK	INDIRECT REGISTERS	DESCRIPTION
0000	0	Reserved	Reserved
0001	1	Page 1: FPD Port Swap (Section 7.6.2.1)	FPD-Link Port Control Registers
0010	2	Page 2: FPD PLL (Section 7.6.2.2)	FPD-Link PLL Control Registers
0011	3	Reserved	Reserved
0100	4	Page 4: DP Lane 0 and Lane 1 (Section 7.6.2.3)	DP Controls for lane 0 & 1 Registers
0101	5	Page 5: DP Lane 2 and Lane 3 (Section 7.6.2.4)	DP Controls for lane 2 & 3 Registers
0110	6	Reserved	Reserved
0111	7	Reserved	Reserved
1000	8	Reserved	Reserved
1001	9	Page 9: DP/FPD Interrupts (Section 7.6.2.5)	DP/FPD Interrupts Registers
1010	10	Reserved	Reserved
1011	11	Page 11: TX Link Layer (Section 7.6.2.6)	Transmitter Link Layer and ABUFF Registers
1100	12	Page 12: Video Processor (Section 7.6.2.7)	Video Processor Registers
1101	13	Reserved	Reserved
1110	14	Page 14: SAR ADC Control (Section 7.6.2.8)	Temperature, Line Fault, and Voltage Sensor Control Registers

7.6.2.1 Page 1: FPD Port Swap Registers

Table 7-201 lists the memory-mapped registers for the Page 1: FPD Port Swap registers. All register offset addresses not listed in Table 7-201 should be considered as reserved locations and the register contents should not be modified.

Table 7-201. PAGE 1: FPD PORT SWAP Registers

Address	Acronym	Register Name	Section
0x0	INVERT_POLARTIY_PORT0_CTL0	INVERT_POLARTIY_PORT0_CTL0	Go
0x1	INVERT_POLARTIY_PORT0_CTL1	INVERT_POLARTIY_PORT0_CTL1	Go
0x2	INVERT_POLARTIY_PORT0_CTL2	INVERT_POLARTIY_PORT0_CTL2	Go
0x20	INVERT_POLARTIY_PORT1_CTL0	INVERT_POLARTIY_PORT1_CTL0	Go
0x21	INVERT_POLARTIY_PORT1_CTL1	INVERT_POLARTIY_PORT1_CTL1	Go
0x22	INVERT_POLARTIY_PORT1_CTL2	INVERT_POLARTIY_PORT1_CTL2	Go

Complex bit access types are encoded to fit into small table cells. Table 7-202 shows the codes that are used for access types in this section.

Table 7-202. Page 1: FPD Port Swap Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.1.1 INVERT_POLARTIY_PORT0_CTL0 Register (Address = 0x0) [Default = 0x00]

INVERT_POLARTIY_PORT0_CTL0 is shown in Table 7-203.

Return to the Summary Table.

Table 7-203. INVERT_POLARTIY_PORT0_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY_PORT0_CTL0	R/W	0x0	Invert polarity PORT0 for Control 0 0x0 = Normal operation 0x1 = Inverted polarity

7.6.2.1.2 INVERT_POLARTIY_PORT0_CTL1 Register (Address = 0x1) [Default = 0x00]

INVERT_POLARTIY_PORT0_CTL1 is shown in Table 7-204.

Return to the Summary Table.

Table 7-204. INVERT_POLARTIY_PORT0_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY_PORT0_CTL1	R/W	0x0	Invert polarity PORT0 for Control 1 0x0 = Normal operation 0x1 = Inverted polarity

7.6.2.1.3 INVERT_POLARTIY_PORT0_CTL2 Register (Address = 0x2) [Default = 0x00]

INVERT_POLARTIY_PORT0_CTL2 is shown in Table 7-205.

Return to the Summary Table.

Table 7-205. INVERT_POLARTIY_PORT0_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1:0	INVERT_POLARTIY_PORT0_CTL2	R/W	0x0	Invert polarity PORT0 for Control 2 0x0 = Normal operation 0x1 = Inverted polarity

7.6.2.1.4 INVERT_POLARTIY_PORT1_CTL0 Register (Address = 0x20) [Default = 0x00]

INVERT_POLARTIY_PORT1_CTL0 is shown in Table 7-206.

Return to the Summary Table.

Table 7-206. INVERT_POLARTIY_PORT1_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY_PORT1_CTL0	R/W	0x0	Invert polarity PORT1 for Control 0 0x0 = Normal operation 0x1 = Inverted polarity

7.6.2.1.5 INVERT_POLARTIY_PORT1_CTL1 Register (Address = 0x21) [Default = 0x00]

INVERT_POLARTIY_PORT1_CTL1 is shown in Table 7-207.

Return to the Summary Table.

Table 7-207. INVERT_POLARTIY_PORT1_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY_PORT1_CTL1	R/W	0x0	Invert polarity PORT1 for Control 1 0x0 = Normal operation 0x1 = Inverted polarity

7.6.2.1.6 INVERT_POLARTIY_PORT1_CTL2 Register (Address = 0x22) [Default = 0x00]

INVERT_POLARTIY_PORT1_CTL2 is shown in Table 7-208.

Return to the Summary Table.

Table 7-208. INVERT_POLARTIY_PORT1_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1:0	INVERT_POLARTIY_PORT1_CTL2	R/W	0x0	Invert polarity PORT1 for Control 1 0x0 = Normal operation 0x1 = Inverted polarity

7.6.2.2 Page 2: FPD PLL Registers

Table 7-209 lists the memory-mapped registers for the Page 2: FPD PLL registers. All register offset addresses not listed in Table 7-209 should be considered as reserved locations and the register contents should not be modified.

Table 7-209. PAGE 2: FPD PLL Registers

Address	Acronym	Register Name	Section
0x0	PLL_LOST_STATUS_CH0	PLL_LOST_STATUS_CH0	Go
0x4	MASH_ORDER_CH0	MASH_ORDER_CH0	Go
0x5	NDIV_7:0_CH0	NDIV_7:0_CH0	Go
0x6	NDIV_15:8_CH0	NDIV_15:8_CH0	Go
0x7	PLL_LOCK_STATUS_CH0	PLL_LOCK_STATUS_CH0	Go
0xE	VCO_CH0	VCO_CH0	Go
0x13	PDIV_CH0	PDIV_CH0	Go
0x14	SSCG_CTRL1_CH0	SSCG_CTRL1_CH0	Go
0x15	SSCG_CTRL2_CH0	SSCG_CTRL2_CH0	Go
0x16	SSCG_CTRL3_CH0	SSCG_CTRL3_CH0	Go
0x17	SSCG_CTRL4_CH0	SSCG_CTRL4_CH0	Go
0x18	DEN_7:0_CH0	DEN_7:0_CH0	Go
0x19	DEN_15:8_CH0	DEN_15:8_CH0	Go
0x1A	DEN_23:16_CH0	DEN_23:16_CH0	Go
0x1E	NUM_7:0_CH0	NUM_7:0_CH0	Go
0x1F	NUM_15:8_CH0	NUM_15:8_CH0	Go
0x20	NUM_23:16_CH0	NUM_23:16_CH0	Go
0x40	PLL_LOST_STATUS_CH1	PLL_LOST_STATUS_CH1	Go
0x44	MASH_ORDER_CH1	MASH_ORDER_CH1	Go
0x45	NDIV_7:0_CH1	NDIV_7:0_CH1	Go
0x46	NDIV_15:8_CH1	NDIV_15:8_CH1	Go
0x47	PLL_LOCK_STATUS_CH1	PLL_LOCK_STATUS_CH1	Go
0x4E	VCO_CH1	VCO_CH1	Go
0x53	PDIV_CH1	PDIV_CH1	Go
0x54	SSCG_CTL1_CH1	SSCG_CTL1_CH1	Go
0x55	SSCG_CTL2_CH1	SSCG_CTL2_CH1	Go
0x56	SSCG_CTL3_CH1	SSCG_CTL3_CH1	Go
0x57	SSCG_CTL4_CH1	SSCG_CTL4_CH1	Go
0x58	DEN_7:0_CH1	DEN_7:0_CH1	Go
0x59	DEN_15:8_CH1	DEN_15:8_CH1	Go
0x5A	DEN_23:16_CH1	DEN_23:16_CH1	Go
0x5E	NUM_7:0_CH1	NUM_7:0_CH1	Go
0x5F	NUM_15:8_CH1	NUM_15:8_CH1	Go
0x60	NUM_23:16_CH1	NUM_23:16_CH1	Go

Complex bit access types are encoded to fit into small table cells. Table 7-210 shows the codes that are used for access types in this section.

Table 7-210. Page 2: FPD PLL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 7-210. Page 2: FPD PLL Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
WStrap	W Strap	Write Default value loaded from bootstrap pin after reset.
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.2.1 PLL_LOST_STATUS_CH0 Register (Address = 0x0) [Default = 0x01]

PLL_LOST_STATUS_CH0 is shown in Table 7-211.

Return to the Summary Table.

Table 7-211. PLL_LOST_STATUS_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_LOCK_LOST		0x0	checks to see if pll_lock has been lost, clears after read
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

7.6.2.2.2 MASH_ORDER_CH0 Register (Address = 0x4) [Default = 0x01]

MASH_ORDER_CH0 is shown in Table 7-212.

Return to the Summary Table.

Table 7-212. MASH_ORDER_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	MASH_ORDER	R/WStrap	0x0	Sets MASH order 0x0 = Integer 0x2 = Fractional Default value is set by the MODE_SEL0 pin For FPD3 modes, defaults to fractional (010) For FPD4 modes, defaults to integer (000)
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

7.6.2.2.3 NDIV_7:0_CH0 Register (Address = 0x5) [Default = 0x64]

NDIV_7:0_CH0 is shown in Table 7-213.

Return to the Summary Table.

DEFAULT_05

Table 7-213. NDIV_7:0_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NDIV[7:0]	R/WStrap	0x64	N Divider 8-LSB for FPD-Link Port 0. 0x0 = NDIV = 1 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x6E (NDIV = 110) For FPD4 modes, default = 0x7D (NDIV = 125)

7.6.2.2.4 NDIV_15:8_CH0 Register (Address = 0x6) [Default = 0x00]

NDIV_15:8_CH0 is shown in Table 7-214.

Return to the Summary Table.

DEFAULT_06

Table 7-214. NDIV_15:8_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NDIV[15:8]	R/WStrap	0x0	N Divider 8-MSB for FPD-Link Port 0. Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x00 (NDIV = 110) For FPD4 modes, default = 0x00 (NDIV = 125)

7.6.2.2.5 PLL_LOCK_STATUS_CH0 Register (Address = 0x7) [Default = 0x01]

PLL_LOCK_STATUS_CH0 is shown in Table 7-215.

Return to the Summary Table.

Table 7-215. PLL_LOCK_STATUS_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	PLL_LOCK	R	0x1	PLL_LOCK status

7.6.2.2.6 VCO_CH0 Register (Address = 0xE) [Default = 0x93]

VCO_CH0 is shown in Table 7-216.

Return to the Summary Table.

Table 7-216. VCO_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6:4	RESERVED	R/W	0x1	Reserved
3:2	VCO_SEL	R/WStrap	0x0	Lock VCO selection 0x0 = VCO1 0x1 = VCO2 0x2 = VCO3 0x3 = VCO4 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x0 (VCO1) For FPD4 modes, default = 0x1 (VCO2)

Table 7-216. VCO_CH0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	RESERVED	R/W	0x3	Reserved

7.6.2.2.7 PDIV_CH0 Register (Address = 0x13) [Default = 0x80]

PDIV_CH0 is shown in Table 7-217.

Return to the Summary Table.

Table 7-217. PDIV_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	AUTO_VCO_SEL_EN	R/W	0x1	VCO auto selection, instead of programming which vco manually
6:4	VCO_POST_DIV_SEL	R/WStrap	0x0	VCO post divider 0x0 = /1 (FPD-Link IV only) 0x1 = /2 (FPD-Link IV only) 0x2 = /4 (FPD-Link IV only) 0x3 = /8 (FPD-Link IV only) 0x4 = /16 (FPD-Link III only) 0x5 = /2 (FPD-Link III only) 0x6 = /4 (FPD-Link III only) 0x7 = /8 (FPD-Link III only) Default value is set by the MODE_SEL0 pin FPD-Link III default = 110 (/4) FPD-Link IV default = 000 (/1)
3:0	RESERVED	R/W	0x0	Reserved

7.6.2.2.8 SSCG_CTRL1_CH0 Register (Address = 0x14) [Default = 0x80]

SSCG_CTRL1_CH0 is shown in Table 7-218.

Return to the Summary Table.

Table 7-218. SSCG_CTRL1_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SSCG_MODE_SPREAD	R/W	0x1	SSCG mode spread selection 0x0 = down-spread ramp 0x1 = center-spread ramp
6:0	RAMPX_INC[6:0]	R/W	0x0	Increment per step that will be added to the ramp [6:0] for SSCG

7.6.2.2.9 SSCG_CTRL2_CH0 Register (Address = 0x15) [Default = 0x00]

SSCG_CTRL2_CH0 is shown in Table 7-219.

Return to the Summary Table.

Table 7-219. SSCG_CTRL2_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_INC[14:7]	R/W	0x0	Increment per step that will be added to the ramp [14:7] for SSCG

7.6.2.2.10 SSCG_CTRL3_CH0 Register (Address = 0x16) [Default = 0x00]

SSCG_CTRL3_CH0 is shown in Table 7-220.

Return to the Summary Table.

Table 7-220. SSCG_CTRL3_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_STOP[7:0]	R/W	0x0	number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

7.6.2.2.11 SSCG_CTRL4_CH0 Register (Address = 0x17) [Default = 0x00]

SSCG_CTRL4_CH0 is shown in Table 7-221.

Return to the Summary Table.

Table 7-221. SSCG_CTRL4_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	SSCG_EN	R/W	0x0	enable spread spectrum clock generation
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	RAMPX_STOP[9:8]	R/W	0x0	number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

7.6.2.2.12 DEN_7:0_CH0 Register (Address = 0x18) [Default = 0xF6]

DEN_7:0_CH0 is shown in Table 7-222.

Return to the Summary Table.

Table 7-222. DEN_7:0_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH[7:0]	R/W	0xF6	Bits 7:0 of denominator of fractional N-divider for FPD-Link Port 0.

7.6.2.2.13 DEN_15:8_CH0 Register (Address = 0x19) [Default = 0xFF]

DEN_15:8_CH0 is shown in Table 7-223.

Return to the Summary Table.

Table 7-223. DEN_15:8_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH[15:8]	R/W	0xFF	Bits 15:8 of denominator of fractional N-divider for FPD-Link Port 0.

7.6.2.2.14 DEN_23:16_CH0 Register (Address = 0x1A) [Default = 0xFF]

DEN_23:16_CH0 is shown in Table 7-224.

Return to the Summary Table.

Table 7-224. DEN_23:16_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH[23:16]	R/W	0xFF	Bits 23:16 of denominator of fractional N-divider for FPD-Link Port 0.

7.6.2.2.15 NUM_7:0_CH0 Register (Address = 0x1E) [Default = 0x00]

NUM_7:0_CH0 is shown in Table 7-225.

Return to the Summary Table.

Table 7-225. NUM_7:0_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH[7:0]	R/WStrap	0x0	Bits 7:0 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x4A (NUM = 3106890) For FPD4 modes, default = 0

7.6.2.2.16 NUM_15:8_CH0 Register (Address = 0x1F) [Default = 0x00]

NUM_15:8_CH0 is shown in Table 7-226.

Return to the Summary Table.

Table 7-226. NUM_15:8_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH[15:8]	R/WStrap	0x0	Bits 15:8 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x68 (NUM = 3106890) For FPD4 modes, default = 0

7.6.2.2.17 NUM_23:16_CH0 Register (Address = 0x20) [Default = 0x00]

NUM_23:16_CH0 is shown in Table 7-227.

Return to the Summary Table.

Table 7-227. NUM_23:16_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH[23:16]	R/WStrap	0x0	Bits 23:16 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x2F (NUM = 3106890) For FPD4 modes, default = 0

7.6.2.2.18 PLL_LOST_STATUS_CH1 Register (Address = 0x40) [Default = 0x01]

PLL_LOST_STATUS_CH1 is shown in Table 7-228.

Return to the Summary Table.

Table 7-228. PLL_LOST_STATUS_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_LOCK_LOST		0x0	checks to see if pll_lock has been lost, clears after read
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

7.6.2.2.19 MASH_ORDER_CH1 Register (Address = 0x44) [Default = 0x01]

MASH_ORDER_CH1 is shown in Table 7-229.

Return to the Summary Table.

Table 7-229. MASH_ORDER_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	MASH_ORDER	R/WStrap	0x0	bits to program MASH order Mode values 3'h7: adas_mode ? 3'h2:3'h2 Default: adas_mode ? 3'h2:3'h0
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

7.6.2.2.20 NDIV_7:0_CH1 Register (Address = 0x45) [Default = 0x64]

NDIV_7:0_CH1 is shown in Table 7-230.

Return to the Summary Table.

DEFAULT_05

Table 7-230. NDIV_7:0_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT[7:0]	R/WStrap	0x64	Ncount's Divider values Default value is set by the MODE_SEL0 pin For FPD3 modes, default NCOUNT = 110 For FPD4 modes, default NCOUNT = 125

7.6.2.2.21 NDIV_15:8_CH1 Register (Address = 0x46) [Default = 0x00]

NDIV_15:8_CH1 is shown in Table 7-231.

Return to the Summary Table.

DEFAULT_06

Table 7-231. NDIV_15:8_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT[15:8]	R/WStrap	0x0	Ncount's Divider values Default value is set by the MODE_SEL0 pin For FPD3 modes, default NCOUNT = 124 For FPD4 modes, default NCOUNT = 125

7.6.2.2.22 PLL_LOCK_STATUS_CH1 Register (Address = 0x47) [Default = 0x01]

PLL_LOCK_STATUS_CH1 is shown in Table 7-232.

Return to the Summary Table.

Table 7-232. PLL_LOCK_STATUS_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved

Table 7-232. PLL_LOCK_STATUS_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	PLL_LOCK	R	0x1	PLL_LOCK status

7.6.2.2.23 VCO_CH1 Register (Address = 0x4E) [Default = 0x93]

VCO_CH1 is shown in Table 7-233.

Return to the Summary Table.

Table 7-233. VCO_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6:4	RESERVED	R/W	0x1	Reserved
3:2	VCO_N_ACTIVE	R/WStrap	0x0	Lock VCO selection 0x0 = VCO1 0x1 = VCO2 0x2 = VCO3 0x3 = VCO4 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x0 (VCO1) For FPD4 modes, default = 0x1 (VCO2)
1:0	RESERVED	R/W	0x3	Reserved

7.6.2.2.24 PDIV_CH1 Register (Address = 0x53) [Default = 0x80]

PDIV_CH1 is shown in Table 7-234.

Return to the Summary Table.

Table 7-234. PDIV_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	AUTO_VCO_SEL_EN	R/W	0x1	vco auto selection, instead of programming which vco manually
6:4	VCO_POST_DIV_SEL	R/WStrap	0x0	VCO post divider 0x0 = /1 (FPD-Link IV only) 0x1 = /2 (FPD-Link IV only) 0x2 = /4 (FPD-Link IV only) 0x3 = /8 (FPD-Link IV only) 0x4 = /16 (FPD-Link III only) 0x5 = /2 (FPD-Link III only) 0x6 = /4 (FPD-Link III only) 0x7 = /8 (FPD-Link III only) Default value is set by the MODE_SEL0 pin FPD-Link III default = 110 (/4) FPD-Link IV default = 000 (/1)
3:0	RESERVED	R/W	0x0	Reserved

7.6.2.2.25 SSCG_CTL1_CH1 Register (Address = 0x54) [Default = 0x80]

SSCG_CTL1_CH1 is shown in Table 7-235.

Return to the Summary Table.

Table 7-235. SSCG_CTL1_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SSCG_CTR_SPRD	R/W	0x1	SSCG mode spread selection 0x0 = down-spread ramp 0x1 = center-spread ramp
6:0	RAMPX_INC[6:0]	R/W	0x0	Increment per step that will be added to the ramp [6:0] for SSCG

7.6.2.2.26 SSCG_CTL2_CH1 Register (Address = 0x55) [Default = 0x00]

SSCG_CTL2_CH1 is shown in Table 7-236.

Return to the Summary Table.

Table 7-236. SSCG_CTL2_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_INC[14:7]	R/W	0x0	Increment per step that will be added to the ramp [14:7] for SSCG

7.6.2.2.27 SSCG_CTL3_CH1 Register (Address = 0x56) [Default = 0x00]

SSCG_CTL3_CH1 is shown in Table 7-237.

Return to the Summary Table.

Table 7-237. SSCG_CTL3_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_STOP[7:0]	R/W	0x0	number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

7.6.2.2.28 SSCG_CTL4_CH1 Register (Address = 0x57) [Default = 0x00]

SSCG_CTL4_CH1 is shown in Table 7-238.

Return to the Summary Table.

Table 7-238. SSCG_CTL4_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	SSCG_EN	R/W	0x0	enable spread spectrum clock generation
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	RAMPX_STOP[9:8]	R/W	0x0	number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

7.6.2.2.29 DEN_7:0_CH1 Register (Address = 0x58) [Default = 0xF6]

DEN_7:0_CH1 is shown in Table 7-239.

Return to the Summary Table.

DEFAULT_18

Table 7-239. DEN_7:0_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH[7:0]	R/W	0xF6	Bits 7:0 of denominator of fractional N-divider for FPD-Link Port 0.

7.6.2.2.30 DEN_15:8_CH1 Register (Address = 0x59) [Default = 0xFF]

DEN_15:8_CH1 is shown in Table 7-240.

Return to the Summary Table.

Table 7-240. DEN_15:8_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH[15:8]	R/W	0xFF	Bits 15:8 of denominator of fractional N-divider for FPD-Link Port 0.

7.6.2.2.31 DEN_23:16_CH1 Register (Address = 0x5A) [Default = 0xFF]

DEN_23:16_CH1 is shown in Table 7-241.

Return to the Summary Table.

Table 7-241. DEN_23:16_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH[23:16]	R/W	0xFF	Bits 23:16 of denominator of fractional N-divider for FPD-Link Port 0.

7.6.2.2.32 NUM_7:0_CH1 Register (Address = 0x5E) [Default = 0x00]

NUM_7:0_CH1 is shown in Table 7-242.

Return to the Summary Table.

Table 7-242. NUM_7:0_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH[7:0]	R/WStrap	0x0	Bits 7:0 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x4A (NUM = 3106890) For FPD4 modes, default = 0

7.6.2.2.33 NUM_15:8_CH1 Register (Address = 0x5F) [Default = 0x00]

NUM_15:8_CH1 is shown in Table 7-243.

Return to the Summary Table.

Table 7-243. NUM_15:8_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH[15:8]	R/WStrap	0x0	Bits 15:8 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x4A (NUM = 3106890) For FPD4 modes, default = 0

7.6.2.2.34 NUM_23:16_CH1 Register (Address = 0x60) [Default = 0x00]

NUM_23:16_CH1 is shown in Table 7-244.

Return to the Summary Table.

Table 7-244. NUM_23:16_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH[23:16]	R/WStrap	0x0	Bits 23:16 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default = 0x4A (NUM = 3106890) For FPD4 modes, default = 0

7.6.2.3 Page 4: DP LN0 LN1 Registers

Table 7-245 lists the memory-mapped registers for the Page 4: DP LN0 LN1 registers. All register offset addresses not listed in Table 7-245 should be considered as reserved locations and the register contents should not be modified.

Table 7-245. PAGE 4: DP LN0 LN1 Registers

Address	Acronym	Register Name	Section
0x29	DP_LN0_POL_29	DP_LN0_POL_29	Go
0xA9	DP_LN1_POL_A9	DP_LN1_POL_A9	Go

Complex bit access types are encoded to fit into small table cells. Table 7-246 shows the codes that are used for access types in this section.

Table 7-246. Page 4: DP LN0 LN1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.3.1 DP_LN0_POL_29 Register (Address = 0x29) [Default = 0x01]

DP_LN0_POL_29 is shown in Table 7-247.

Return to the Summary Table.

Table 7-247. DP_LN0_POL_29 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	SW_LANE0_POL	R/W	0x1	Inverts the lane data polarity when set to 1

7.6.2.3.2 DP_LN1_POL_A9 Register (Address = 0xA9) [Default = 0x00]

DP_LN1_POL_A9 is shown in Table 7-248.

Return to the Summary Table.

Table 7-248. DP_LN1_POL_A9 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

Table 7-248. DP_LN1_POL_A9 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	SW_LANE1_POL	R/W	0x0	Inverts the lane data polarity when set to 1

7.6.2.4 Page 5: DP LN2 LN3 Registers

Table 7-249 lists the memory-mapped registers for the Page 5: DP LN2 LN3 registers. All register offset addresses not listed in Table 7-249 should be considered as reserved locations and the register contents should not be modified.

Table 7-249. PAGE 5: DP LN2 LN3 Registers

Address	Acronym	Register Name	Section
0x29	DP_LN2_POL_29	DP_LN2_POL_29	Go
0xA9	DP_LN3_POL_A9	DP_LN3_POL_A9	Go

Complex bit access types are encoded to fit into small table cells. Table 7-250 shows the codes that are used for access types in this section.

Table 7-250. Page 5: DP LN2 LN3 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.4.1 DP_LN2_POL_29 Register (Address = 0x29) [Default = 0x01]

DP_LN2_POL_29 is shown in Table 7-251.

Return to the Summary Table.

Table 7-251. DP_LN2_POL_29 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	SW_LANE2_POL	R/W	0x1	Inverts the lane data polarity when set to 1

7.6.2.4.2 DP_LN3_POL_A9 Register (Address = 0xA9) [Default = 0x00]

DP_LN3_POL_A9 is shown in Table 7-252.

Return to the Summary Table.

Table 7-252. DP_LN3_POL_A9 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

Table 7-252. DP_LN3_POL_A9 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	SW_LANE3_POL	R/W	0x0	Inverts the lane data polarity when set to 1

7.6.2.5 Page 9: DP DFT Registers

Table 7-253 lists the memory-mapped registers for the Page 9: DP DFT registers. All register offset addresses not listed in Table 7-253 should be considered as reserved locations and the register contents should not be modified.

Table 7-253. PAGE 9: DP DFT Registers

Address	Acronym	Register Name	Section
0x1	HPD_OVERRIDE_EN	HPD_OVERRIDE_EN	Go
0x3E	INTR_CTL_DP_RX_PORT	INTR_CTL_DP_RX_PORT	Go
0x3F	INTR_STS_DP_RX_PORT	INTR_STS_DP_RX_PORT	Go
0x88	ALARM_BC_EN_PORT0	ALARM_BC_EN_PORT0	Go
0x8C	INTR_CTL_FPD4_PORT0	INTR_CTL_FPD4_PORT0	Go
0x8D	INTR_STS_FPD4_PORT0	INTR_STS_FPD4_PORT0	Go
0x98	ALARM_BC_EN_PORT1	ALARM_BC_EN_PORT1	Go
0x9C	INTR_CTL_FPD4_PORT1	INTR_CTL_FPD4_PORT1	Go
0x9D	INTR_STS_FPD4_PORT1	INTR_STS_FPD4_PORT1	Go
0xC9	REG_GPIO_EN_PULL_LOW_1	REG_GPIO_EN_PULL_LOW_1	Go
0xCA	REG_GPIO_EN_PULL_LOW_2	REG_GPIO_EN_PULL_LOW_2	Go

Complex bit access types are encoded to fit into small table cells. Table 7-254 shows the codes that are used for access types in this section.

Table 7-254. Page 9: DP DFT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.5.1 HPD_OVERRIDE_EN Register (Address = 0x1) [Default = 0x50]

HPD_OVERRIDE_EN is shown in Table 7-255.

Return to the Summary Table.

Table 7-255. HPD_OVERRIDE_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x1	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x1	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	REG_DPX_HPD_0V_EN	R/W	0x0	Enable HPD override
0	REG_DPX_HPD_0V	R/W	0x0	HPD enable value

7.6.2.5.2 INTR_CTL_DP_RX_PORT Register (Address = 0x3E) [Default = 0x00]

INTR_CTL_DP_RX_PORT is shown in Table 7-256.

Return to the Summary Table.

Table 7-256. INTR_CTL_DP_RX_PORT Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_DP_SINK1_STS_CHANGE	R/W	0x0	Enables Interrupt on DP stream 1 status change (valid only in MST case)
5	IE_DP_SINK0_STS_CHANGE	R/W	0x0	Enables Interrupt on DP stream 0 status change
4	IE_DP_LINK_RATE_CHANGE	R/W	0x0	Enables Interrupt on DP Port Link rate change
3	IE_DP_LANE_COUNT_CHANGE	R/W	0x0	Enables Interrupt on DP Port Lane count change
2	IE_ANY_DP_RX_CORE_INTR	R/W	0x0	Enables Interrupt on Any DP Core Interrupt
1	IE_DP_LINK_TRAINING_DONE	R/W	0x0	Enables Interrupt on DP Port Link training Done
0	IE_DP_LINK_LOST	R/W	0x0	Enables Interrupt on DP Port Link Lost

7.6.2.5.3 INTR_STS_DP_RX_PORT Register (Address = 0x3F) [Default = 0x00]

INTR_STS_DP_RX_PORT is shown in Table 7-257.

Return to the Summary Table.

Table 7-257. INTR_STS_DP_RX_PORT Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_DP_SINK1_STS_CHANGE		0x0	Interrupt Status on DP stream 1 status change (valid only in MST case)
5	IS_DP_SINK0_STS_CHANGE		0x0	Interrupt Status on DP stream 0 status change
4	IS_DP_LINK_RATE_CHANGE		0x0	Interrupt Status on DP Port Link rate change
3	IS_DP_LANE_COUNT_CHANGE		0x0	Interrupt Status on DP Port Lane count change
2	IS_ANY_DP_RX_CORE_INTR		0x0	Interrupt Status on Any DP Core Interrupt
1	IS_DP_LINK_TRAINING_DONE		0x0	Interrupt Status on DP Port Link training Done
0	IS_DP_LINK_LOST		0x0	Interrupt Status on DP Port Link Lost

7.6.2.5.4 ALARM_BC_EN_PORT0 Register (Address = 0x88) [Default = 0x00]

ALARM_BC_EN_PORT0 is shown in Table 7-258.

Return to the Summary Table.

Table 7-258. ALARM_BC_EN_PORT0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	BCC_TARGET_TO_ERROR_EN	R/W	0x0	Enable BCC_TARGET_TO_ERROR alarm

Table 7-258. ALARM_BC_EN_PORT0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	BCC_TARGET_ERROR_EN	R/W	0x0	Enable BCC_TARGET_ERROR alarm
4	BCC_MSTR_TO_ERROR_EN	R/W	0x0	Enable BC BCC_MSTR_TO_ERR alarm
3	BCC_MSTR_ERROR_EN	R/W	0x0	Enable BCC_MSTR_ERROR alarm
2	BCC_DATA_ERROR_EN	R/W	0x0	Enable BCC_DATA_ERROR alarm
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm

7.6.2.5.5 INTR_CTL_FPD4_PORT0 Register (Address = 0x8C) [Default = 0x00]

INTR_CTL_FPD4_PORT0 is shown in Table 7-259.

Return to the Summary Table.

Table 7-259. INTR_CTL_FPD4_PORT0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_RX_LOCK_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Detect
5	IE_RX_REM_INT	R/W	0x0	Enables Interrupt on Remote Receiver interrupt
4	IE_DES_INT	R/W	0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IE_RX_LOCK_LOST_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

7.6.2.5.6 INTR_STS_FPD4_PORT0 Register (Address = 0x8D) [Default = 0x00]

INTR_STS_FPD4_PORT0 is shown in Table 7-260.

Return to the Summary Table.

Table 7-260. INTR_STS_FPD4_PORT0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_RX_LOCK_DET_INT		0x0	Interrupt on Receiver Lock Detect
5	IS_RX_REM_INT		0x0	Interrupt on Remote Receiver interrupt
4	IS_DES_INT		0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IS_RX_LOCK_LOST_DET_INT		0x0	Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

7.6.2.5.7 ALARM_BC_EN_PORT1 Register (Address = 0x98) [Default = 0x00]

ALARM_BC_EN_PORT1 is shown in Table 7-261.

Return to the Summary Table.

Table 7-261. ALARM_BC_EN_PORT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	BCC_TARGET_TO_ERROR_EN	R/W	0x0	Enable BCC_TARGET_TO_ERROR alarm
5	BCC_TARGET_ERROR_EN	R/W	0x0	Enable BCC_TARGET_ERROR alarm
4	BCC_MSTR_TO_ERROR_EN	R/W	0x0	Enable BC BCC_MSTR_TO_ERR alarm
3	BCC_MSTR_ERROR_EN	R/W	0x0	Enable BCC_MSTR_ERROR alarm
2	BCC_DATA_ERROR_EN	R/W	0x0	Enable BCC_DATA_ERROR alarm
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm

7.6.2.5.8 INTR_CTL_FPD4_PORT1 Register (Address = 0x9C) [Default = 0x00]

INTR_CTL_FPD4_PORT1 is shown in Table 7-262.

Return to the Summary Table.

Table 7-262. INTR_CTL_FPD4_PORT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_RX_LOCK_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Detect
5	IE_RX_REM_INT	R/W	0x0	Enables Interrupt on Remote Receiver interrupt
4	IE_DES_INT	R/W	0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IE_RX_LOCK_LOST_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

7.6.2.5.9 INTR_STS_FPD4_PORT1 Register (Address = 0x9D) [Default = 0x48]

INTR_STS_FPD4_PORT1 is shown in Table 7-263.

Return to the Summary Table.

Table 7-263. INTR_STS_FPD4_PORT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_RX_LOCK_DET_INT		0x1	Interrupt on Receiver Lock Detect
5	IS_RX_REM_INT		0x0	Interrupt on Remote Receiver interrupt
4	IS_DES_INT		0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IS_RX_LOCK_LOST_DET_INT		0x1	Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

7.6.2.5.10 REG_GPIO_EN_PULL_LOW_1 Register (Address = 0xC9) [Default = 0xFF]

REG_GPIO_EN_PULL_LOW_1 is shown in Table 7-264.

Return to the Summary Table.

Table 7-264. REG_GPIO_EN_PULL_LOW_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GPIO_EN_PULL_LOW_7_0	R/W	0xFF	GPIO Enable internal pull down resistors for GPIO 0-7 1 = Pull down enabled 0 = Pull down disabled

7.6.2.5.11 REG_GPIO_EN_PULL_LOW_2 Register (Address = 0xCA) [Default = 0x3F]

REG_GPIO_EN_PULL_LOW_2 is shown in Table 7-265.

Return to the Summary Table.

Table 7-265. REG_GPIO_EN_PULL_LOW_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	GPIO_EN_PULL_LOW_13_8	R/W	0x3F	GPIO Enable internal pull down resistors for GPIO 8-13 1 = Pull down enabled 0 = Pull down disabled

7.6.2.6 Page 11: TX Link Layer Registers

Table 7-266 lists the memory-mapped registers for the Page 11: TX Link Layer registers. All register offset addresses not listed in Table 7-266 should be considered as reserved locations and the register contents should not be modified.

Table 7-266. PAGE 11: TX LINK LAYER Registers

Address	Acronym	Register Name	Section
0x0	LINK_LAYER_CTL	LINK_LAYER_CTL	Go
0x1	LINK0_STREAM_EN	LINK0_STREAM_EN	Go
0x2	LINK0_MAP_REG0	LINK0_MAP_REG0	Go
0x3	LINK0_MAP_REG1	LINK0_MAP_REG1	Go
0x4	LINK0_MAP_REG2	LINK0_MAP_REG2	Go
0x6	LINK0_SLOT_REQ0	LINK0_SLOT_REQ0	Go
0x7	LINK0_SLOT_REQ1	LINK0_SLOT_REQ1	Go
0x8	LINK0_SLOT_REQ2	LINK0_SLOT_REQ2	Go
0x9	LINK0_SLOT_REQ3	LINK0_SLOT_REQ3	Go
0xA	LINK0_SLOT_REQ4	LINK0_SLOT_REQ4	Go
0xB	LINK0_SLOT_REQ5	LINK0_SLOT_REQ5	Go
0xE	LINK0_CONFIG	LINK0_CONFIG	Go
0x11	LINK1_STREAM_EN	LINK1_STREAM_EN	Go
0x12	LINK1_MAP_REG0	LINK1_MAP_REG0	Go
0x13	LINK1_MAP_REG1	LINK1_MAP_REG1	Go
0x14	LINK1_MAP_REG2	LINK1_MAP_REG2	Go
0x16	LINK1_SLOT_REQ0	LINK1_SLOT_REQ0	Go
0x17	LINK1_SLOT_REQ1	LINK1_SLOT_REQ1	Go
0x18	LINK1_SLOT_REQ2	LINK1_SLOT_REQ2	Go
0x19	LINK1_SLOT_REQ3	LINK1_SLOT_REQ3	Go
0x1A	LINK1_SLOT_REQ4	LINK1_SLOT_REQ4	Go
0x1B	LINK1_SLOT_REQ5	LINK1_SLOT_REQ5	Go
0x1E	LINK1_CONFIG	LINK1_CONFIG	Go
0x20	VP_WIDTH0	VP_WIDTH0	Go
0x22	PKT_FIFO_OVRFLW_STS	PKT_FIFO_OVRFLW_STS	Go
0x23	PKT_FIFO_OVRFLW_CLR	PKT_FIFO_OVRFLW_CLR	Go
0x24	CORRUPT_PKT_CRC	CORRUPT_PKT_CRC	Go
0x25	LINK_ECC_TEST0	LINK_ECC_TEST0	Go
0x26	LINK_ECC_TEST1	LINK_ECC_TEST1	Go
0x27	LINK_ECC_TEST2	LINK_ECC_TEST2	Go
0x80	ABUFF0_CTL0	ABUFF0_CTL0	Go
0x81	ABUFF0_CTL1	ABUFF0_CTL1	Go
0x82	ABUFF0_CTL2	ABUFF0_CTL2	Go
0x86	ABUFF0_CTL6	ABUFF0_CTL6	Go
0x88	ABUFF1_CTL0	ABUFF1_CTL0	Go
0x89	ABUFF1_CTL1	ABUFF1_CTL1	Go
0x8A	ABUFF1_CTL2	ABUFF1_CTL2	Go
0x8E	ABUFF1_CTL6	ABUFF1_CTL6	Go
0x90	ABUFF2_CTL0	ABUFF2_CTL0	Go
0x91	ABUFF2_CTL1	ABUFF2_CTL1	Go
0x92	ABUFF2_CTL2	ABUFF2_CTL2	Go

Table 7-266. PAGE 11: TX LINK LAYER Registers (continued)

Address	Acronym	Register Name	Section
0xA8	ABUFF5_CTL0	ABUFF5_CTL0	Go
0xA9	ABUFF5_CTL1	ABUFF5_CTL1	Go
0xAA	ABUFF5_CTL2	ABUFF5_CTL2	Go
0xAD	ABUFF5_CTL5	ABUFF5_CTL5	Go
0xAE	ABUFF5_CTL6	ABUFF5_CTL6	Go
0xB0	ABUFF6_CTL0	ABUFF6_CTL0	Go
0xB1	ABUFF6_CTL1	ABUFF6_CTL1	Go
0xB2	ABUFF6_CTL2	ABUFF6_CTL2	Go
0xB8	ABUFF7_CTL0	ABUFF7_CTL0	Go
0xB9	ABUFF7_CTL1	ABUFF7_CTL1	Go
0xBA	ABUFF7_CTL2	ABUFF7_CTL2	Go
0xBE	ABUFF7_CTL6	ABUFF7_CTL6	Go
0xC0	ABUFF8_CTL0	ABUFF8_CTL0	Go
0xC1	ABUFF8_CTL1	ABUFF8_CTL1	Go
0xC2	ABUFF8_CTL2	ABUFF8_CTL2	Go
0xC8	ABUFF9_CTL0	ABUFF9_CTL0	Go
0xC9	ABUFF9_CTL1	ABUFF9_CTL1	Go
0xCA	ABUFF9_CTL2	ABUFF9_CTL2	Go
0xCE	ABUFF9_CTL6	ABUFF9_CTL6	Go
0xD0	ABUFF10_CTL0	ABUFF10_CTL0	Go
0xD1	ABUFF10_CTL1	ABUFF10_CTL1	Go
0xD2	ABUFF10_CTL2	ABUFF10_CTL2	Go
0xD6	ABUFF10_CTL6	ABUFF10_CTL6	Go
0xD8	ABUFF11_CTL0	ABUFF11_CTL0	Go
0xD9	ABUFF11_CTL1	ABUFF11_CTL1	Go
0xDA	ABUFF11_CTL2	ABUFF11_CTL2	Go
0xDE	ABUFF11_CTL6	ABUFF11_CTL6	Go

Complex bit access types are encoded to fit into small table cells. Table 7-267 shows the codes that are used for access types in this section.

Table 7-267. Page 11: TX Link Layer Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1SS	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.6.1 LINK_LAYER_CTL Register (Address = 0x0) [Default = 0x00]

LINK_LAYER_CTL is shown in Table 7-268.

Return to the Summary Table.

Table 7-268. LINK_LAYER_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	EN_NEW_TSLOT1	RH/W1SS	0x0	Enable New Time-slot assignments for Link Layer 1 Setting this bit to a 1 will enable the device to begin using the new time-slot information programmed inot the LINK1_SLOT_REQ registers. This register bit will be cleared once the new time-slot information has been enabled
2	LINK_LAYER_1_EN	R/W	0x0	Link Layer enable for Link Layer 1 0x0 = all Link Layer 1 video streams disabled 0x1 = Video Streams with LINK1_STREAM_EN bits set will be enabled
1	EN_NEW_TSLOT0	RH/W1SS	0x0	Enable New Time-slot assignments for Link Layer 0 Setting this bit to a 1 will enable the device to begin using the new time-slot information programmed inot the LINKx_SLOT_REQ registers. This register bit will be cleared once the new time-slot information has been enabled
0	LINK_LAYER_0_EN	R/W	0x0	Link Layer enable for Link Layer 0 0x0 = all Link Layer 0 video streams disabled 0x1 = Video Streams with LINK0_STREAM_EN bits set will be enabled

7.6.2.6.2 LINK0_STREAM_EN Register (Address = 0x1) [Default = 0x00]

LINK0_STREAM_EN is shown in Table 7-269.

Return to the Summary Table.

Table 7-269. LINK0_STREAM_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LINK0_STREAM_EN5	R/W	0x0	Link Layer 0 Stream Enable 5 Setting this bit will enable the Link Layer processing for the associated Video Stream.
4	LINK0_STREAM_EN4	R/W	0x0	Link Layer 0 Stream Enable 4 Setting this bit will enable the Link Layer processing for the associated Video Stream.
3	LINK0_STREAM_EN3	R/W	0x0	Link Layer 0 Stream Enable 3 Setting this bit will enable the Link Layer processing for the associated Video Stream.
2	LINK0_STREAM_EN2	R/W	0x0	Link Layer 0 Stream Enable 2 Setting this bit will enable the Link Layer processing for the associated Video Stream.
1	LINK0_STREAM_EN1	R/W	0x0	Link Layer 0 Stream Enable 1 Setting this bit will enable the Link Layer processing for the associated Video Stream.
0	LINK0_STREAM_EN0	R/W	0x0	Link Layer 0 Stream Enable 0 Setting this bit will enable the Link Layer processing for the associated Video Stream.

7.6.2.6.3 LINK0_MAP_REG0 Register (Address = 0x2) [Default = 0x10]

LINK0_MAP_REG0 is shown in Table 7-270.

Return to the Summary Table.

Table 7-270. LINK0_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK0_STREAM_MAP1	R/W	0x1	Link Layer Stream 1 Map Selects the Video Processor for assignment to Video Stream 1. Value may be in the range of 0-5. If the LINK0_STREAM_EN[1] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK0_STREAM_MAP0	R/W	0x0	Link Layer Stream 0 Map Selects the Video Processor for assignment to Video Stream 0. Value may be in the range of 0-5. If the LINK0_STREAM_EN[0] is set to 0, this value will be ignored.

7.6.2.6.4 LINK0_MAP_REG1 Register (Address = 0x3) [Default = 0x32]

LINK0_MAP_REG1 is shown in Table 7-271.

Return to the Summary Table.

Table 7-271. LINK0_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK0_STREAM_MAP3	R/W	0x3	Link Layer Stream 3 Map Selects the Video Processor for assignment to Video Stream 3. Value may be in the range of 0-5. If the LINK0_STREAM_EN[3] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK0_STREAM_MAP2	R/W	0x2	Link Layer Stream 2 Map Selects the Video Processor for assignment to Video Stream 2. Value may be in the range of 0-5. If the LINK0_STREAM_EN[2] is set to 0, this value will be ignored.

7.6.2.6.5 LINK0_MAP_REG2 Register (Address = 0x4) [Default = 0x00]

LINK0_MAP_REG2 is shown in Table 7-272.

Return to the Summary Table.

Table 7-272. LINK0_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK0_STREAM_MAP5	R/W	0x0	Link Layer Stream 5 Map Selects the Video Processor for assignment to Video Stream 5. Value may be in the range of 0-5. If the LINK0_STREAM_EN[3] is set to 5, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK0_STREAM_MAP4	R/W	0x0	Link Layer Stream 4 Map Selects the Video Processor for assignment to Video Stream 4. Value may be in the range of 0-5. If the LINK0_STREAM_EN[2] is set to 4, this value will be ignored.

7.6.2.6.6 LINK0_SLOT_REQ0 Register (Address = 0x6) [Default = 0x00]

LINK0_SLOT_REQ0 is shown in Table 7-273.

Return to the Summary Table.

Table 7-273. LINK0_SLOT_REQ0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ0	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 0. The total number of LINK0 slots should add up to 65. If less than 65 are assigned, the extra slots will be assigned to stream 0.

7.6.2.6.7 LINK0_SLOT_REQ1 Register (Address = 0x7) [Default = 0x00]

LINK0_SLOT_REQ1 is shown in Table 7-274.

Return to the Summary Table.

Table 7-274. LINK0_SLOT_REQ1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ1	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 1.

7.6.2.6.8 LINK0_SLOT_REQ2 Register (Address = 0x8) [Default = 0x00]

LINK0_SLOT_REQ2 is shown in Table 7-275.

Return to the Summary Table.

Table 7-275. LINK0_SLOT_REQ2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ2	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 2.

7.6.2.6.9 LINK0_SLOT_REQ3 Register (Address = 0x9) [Default = 0x00]

LINK0_SLOT_REQ3 is shown in Table 7-276.

Return to the Summary Table.

Table 7-276. LINK0_SLOT_REQ3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ3	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 3.

7.6.2.6.10 LINK0_SLOT_REQ4 Register (Address = 0xA) [Default = 0x00]

LINK0_SLOT_REQ4 is shown in Table 7-277.

Return to the Summary Table.

Table 7-277. LINK0_SLOT_REQ4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ4	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 4.

7.6.2.6.11 LINK0_SLOT_REQ5 Register (Address = 0xB) [Default = 0x00]

LINK0_SLOT_REQ5 is shown in Table 7-278.

Return to the Summary Table.

Table 7-278. LINK0_SLOT_REQ5 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ5	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 5.

7.6.2.6.12 LINK0_CONFIG Register (Address = 0xE) [Default = 0x00]

LINK0_CONFIG is shown in Table 7-279.

Return to the Summary Table.

Table 7-279. LINK0_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	LINK0_POL_OV	R/W	0x0	Link polarity override for PORT0
0	LINK0_EVENT_MODE_EN	R/W	0x0	Link Layer 0 Event Mode enable This bit controls how the link layer sends HSync/VSync information. 0: Send HSync/VSync pulses with active period matching incoming video 1: Send a single cycle event to indicate HSync and VSync

7.6.2.6.13 LINK1_STREAM_EN Register (Address = 0x11) [Default = 0x00]

LINK1_STREAM_EN is shown in Table 7-280.

Return to the Summary Table.

Table 7-280. LINK1_STREAM_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LINK1_STREAM_EN5	R/W	0x0	Link Layer 1 Stream Enable 5 Setting this bit will enable the Link Layer processing for the associated Video Stream.
4	LINK1_STREAM_EN4	R/W	0x0	Link Layer 1 Stream Enable 4 Setting this bit will enable the Link Layer processing for the associated Video Stream.
3	LINK1_STREAM_EN3	R/W	0x0	Link Layer 1 Stream Enable 3 Setting this bit will enable the Link Layer processing for the associated Video Stream.
2	LINK1_STREAM_EN2	R/W	0x0	Link Layer 1 Stream Enable 2 Setting this bit will enable the Link Layer processing for the associated Video Stream.

Table 7-280. LINK1_STREAM_EN Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	LINK1_STREAM_EN1	R/W	0x0	Link Layer 1 Stream Enable 1 Setting this bit will enable the Link Layer processing for the associated Video Stream.
0	LINK1_STREAM_EN0	R/W	0x0	Link Layer 1 Stream Enable 0 Setting this bit will enable the Link Layer processing for the associated Video Stream.

7.6.2.6.14 LINK1_MAP_REG0 Register (Address = 0x12) [Default = 0x00]

LINK1_MAP_REG0 is shown in Table 7-281.

Return to the Summary Table.

Table 7-281. LINK1_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP1	R/W	0x0	Link Layer Stream 1 Map Selects the Video Processor for assignment to Video Stream 1. Value may be in the range of 0-5. If the LINK1_STREAM_EN[1] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK1_STREAM_MAP0	R/W	0x0	Link Layer Stream 0 Map Selects the Video Processor for assignment to Video Stream 0. Value may be in the range of 0-5. If the LINK1_STREAM_EN[0] is set to 0, this value will be ignored.

7.6.2.6.15 LINK1_MAP_REG1 Register (Address = 0x13) [Default = 0x00]

LINK1_MAP_REG1 is shown in Table 7-282.

Return to the Summary Table.

Table 7-282. LINK1_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP3	R/W	0x0	Link Layer Stream 3 Map Selects the Video Processor for assignment to Video Stream 3. Value may be in the range of 0-5. If the LINK1_STREAM_EN[3] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK1_STREAM_MAP2	R/W	0x0	Link Layer Stream 2 Map Selects the Video Processor for assignment to Video Stream 2. Value may be in the range of 0-5. If the LINK1_STREAM_EN[2] is set to 0, this value will be ignored.

7.6.2.6.16 LINK1_MAP_REG2 Register (Address = 0x14) [Default = 0x00]

LINK1_MAP_REG2 is shown in Table 7-283.

Return to the Summary Table.

Table 7-283. LINK1_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

Table 7-283. LINK1_MAP_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:4	LINK1_STREAM_MAP5	R/W	0x0	Link Layer Stream 5 Map Selects the Video Processor for assignment to Video Stream 5. Value may be in the range of 0-5. If the LINK1_STREAM_EN[3] is set to 5, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK1_STREAM_MAP4	R/W	0x0	Link Layer Stream 4 Map Selects the Video Processor for assignment to Video Stream 4. Value may be in the range of 0-5. If the LINK1_STREAM_EN[2] is set to 4, this value will be ignored.

7.6.2.6.17 LINK1_SLOT_REQ0 Register (Address = 0x16) [Default = 0x00]

LINK1_SLOT_REQ0 is shown in Table 7-284.

Return to the Summary Table.

Table 7-284. LINK1_SLOT_REQ0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ0	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 0. The total number of LINK1 slots should add up to 65. If less than 65 are assigned, the extra slots will be assigned to stream 0.

7.6.2.6.18 LINK1_SLOT_REQ1 Register (Address = 0x17) [Default = 0x00]

LINK1_SLOT_REQ1 is shown in Table 7-285.

Return to the Summary Table.

Table 7-285. LINK1_SLOT_REQ1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ1	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 1.

7.6.2.6.19 LINK1_SLOT_REQ2 Register (Address = 0x18) [Default = 0x00]

LINK1_SLOT_REQ2 is shown in Table 7-286.

Return to the Summary Table.

Table 7-286. LINK1_SLOT_REQ2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ2	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 2.

7.6.2.6.20 LINK1_SLOT_REQ3 Register (Address = 0x19) [Default = 0x00]

LINK1_SLOT_REQ3 is shown in Table 7-287.

Return to the Summary Table.

Table 7-287. LINK1_SLOT_REQ3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ3	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 3.

7.6.2.6.21 LINK1_SLOT_REQ4 Register (Address = 0x1A) [Default = 0x00]

LINK1_SLOT_REQ4 is shown in Table 7-288.

Return to the Summary Table.

Table 7-288. LINK1_SLOT_REQ4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ4	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 4.

7.6.2.6.22 LINK1_SLOT_REQ5 Register (Address = 0x1B) [Default = 0x00]

LINK1_SLOT_REQ5 is shown in Table 7-289.

Return to the Summary Table.

Table 7-289. LINK1_SLOT_REQ5 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ5	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 5.

7.6.2.6.23 LINK1_CONFIG Register (Address = 0x1E) [Default = 0x00]

LINK1_CONFIG is shown in Table 7-290.

Return to the Summary Table.

Table 7-290. LINK1_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	LINK1_POL_OV	R/W	0x0	Link polarity override for PORT1
0	LINK1_EVENT_MODE_EN	R/W	0x0	Link Layer 1 Event Mode enable This bit controls how the link layer sends HSync/VSync information. 0: Send HSync/VSync pulses with active period matching incoming video 1: Send a single cycle event to indicate HSync and VSync

7.6.2.6.24 VP_WIDTH0 Register (Address = 0x20) [Default = 0x55]

VP_WIDTH0 is shown in Table 7-291.

Return to the Summary Table.

Table 7-291. VP_WIDTH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	VP3_WIDTH	R/W	0x1	Pixel Width for Video Processor 3 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved
5:4	VP2_WIDTH	R/W	0x1	Pixel Width for Video Processor 2 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved
3:2	VP1_WIDTH	R/W	0x1	Pixel Width for Video Processor 1 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved
1:0	VP0_WIDTH	R/W	0x1	Pixel Width for Video Processor 0 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved

7.6.2.6.25 PKT_FIFO_OVRFLW_STS Register (Address = 0x22) [Default = 0x00]

PKT_FIFO_OVRFLW_STS is shown in Table 7-292.

Return to the Summary Table.

Table 7-292. PKT_FIFO_OVRFLW_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PKT_FIFO_OVRFLW_STS	R	0x0	Packet FIFO overflow status for each video processor. Bits [3:0] are valid. A buffer can overflow if the fill rate (VPx quad pclk) is much faster than the drain rate (link layer slot assignment BW for the stream assigned to VPx).

7.6.2.6.26 PKT_FIFO_OVRFLW_CLR Register (Address = 0x23) [Default = 0x00]

PKT_FIFO_OVRFLW_CLR is shown in Table 7-293.

Return to the Summary Table.

Table 7-293. PKT_FIFO_OVRFLW_CLR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PKT_FIFO_OVRFLW_CLR	R/W	0x0	Clear packet FIFO overflow status for each

7.6.2.6.27 CORRUPT_PKT_CRC Register (Address = 0x24) [Default = 0x00]

CORRUPT_PKT_CRC is shown in Table 7-294.

Return to the Summary Table.

Table 7-294. CORRUPT_PKT_CRC Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	CORRUPT_PKT_CRC	R/W	0x0	Corrupt Stream CRC Set bit to 1 to corrupt the CRC for each video stream data packet. CRC will be corrupted on each packet until this register is cleared.

7.6.2.6.28 LINK_ECC_TEST0 Register (Address = 0x25) [Default = 0x00]

LINK_ECC_TEST0 is shown in Table 7-295.

Return to the Summary Table.

Table 7-295. LINK_ECC_TEST0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FORCE_ECC_STREAM_EN	R/W	0x0	Enable Stream filter matching for forcing errors If this bit is set to 0, the FORCE_ECC_STREAM control will be ignored and errors will be forced on all active video streams If this bit is set to 1, the FORCE_ECC_STREAM field will be used to only force errors on the selected stream.
5	FORCE_ECC_TYPE_EN	R/W	0x0	Enable Type Field matching for forcing errors If this bit is set to 0, the type field will be ignored and errors will be forced on any Control frame If this bit is set to 1, the FORCE_ECC_TYPE field will be used to only force errors on control frames that match that type field.
4	FORCE_ECC_2BIT_SEL	R/W	0x0	Force Errors Number of bits control Indicates the number of bits which will have errors forced in the control field 0: 1-bit error 1: 2-bit error
3:2	FORCE_ECC_ERR_FIELD_SEL	R/W	0x0	Force Errors field select Control frames include 3 or 4 copies of the control information. This control allows forcing errors on 1 to all 4 control frame fields: 0: Force error on 1 field only 1: Force error on 2 fields 2: Force error on 3 fields 3: Force error on all control fields
1	FORCE_1_CTL_ECC_ERR	R/W	0x0	Force Errors on a single ECC Control Frame Set bit to 1 to force an error on a single Forward Channel control frame which match requirements in the LINK_ECC_TEST register settings.
0	FORCE_CTL_ECC_ERR	R/W	0x0	Force Continuous Errors on ECC Control Frames Set bit to 1 to force errors on Forward Channel control frames which match requirements in the LINK_ECC_TEST register settings.

7.6.2.6.29 LINK_ECC_TEST1 Register (Address = 0x26) [Default = 0x08]

LINK_ECC_TEST1 is shown in Table 7-296.

Return to the Summary Table.

Table 7-296. LINK_ECC_TEST1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	FORCE_ECC_LINK1_SELECT	R/W	0x0	Select Link Layer 1 Set bit to 1 to force errors on Link 1
3	FORCE_ECC_LINK0_SELECT	R/W	0x1	Select Link Layer 0 Set bit to 1 to force errors on Link 0
2:0	FORCE_ECC_STREAM	R/W	0x0	Force ECC Stream control If FORCE_ECC_STREAM_EN is set, errors will be forced only on the selected stream.

7.6.2.6.30 LINK_ECC_TEST2 Register (Address = 0x27) [Default = 0x00]

LINK_ECC_TEST2 is shown in Table 7-297.

Return to the Summary Table.

Table 7-297. LINK_ECC_TEST2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FORCE_ECC_TYPE	R/W	0x0	Force ECC Type field If FORCE_ECC_TYPE_EN is set, errors will be force on control frames with a Type field that matches this programmed value.

7.6.2.6.31 ABUFF0_CTL0 Register (Address = 0x80) [Default = 0x01]

ABUFF0_CTL0 is shown in Table 7-298.

Return to the Summary Table.

Table 7-298. ABUFF0_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x1	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.32 ABUFF0_CTL1 Register (Address = 0x81) [Default = 0x00]

ABUFF0_CTL1 is shown in Table 7-299.

Return to the Summary Table.

Table 7-299. ABUFF0_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

Table 7-299. ABUFF0_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.33 ABUFF0_CTL2 Register (Address = 0x82) [Default = 0x00]

ABUFF0_CTL2 is shown in Table 7-300.

Return to the Summary Table.

Table 7-300. ABUFF0_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x0	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.34 ABUFF0_CTL6 Register (Address = 0x86) [Default = 0x00]

ABUFF0_CTL6 is shown in Table 7-301.

Return to the Summary Table.

Table 7-301. ABUFF0_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF		0x0	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x0	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.6.35 ABUFF1_CTL0 Register (Address = 0x88) [Default = 0x01]

ABUFF1_CTL0 is shown in Table 7-302.

Return to the Summary Table.

Table 7-302. ABUFF1_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x1	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.36 ABUFF1_CTL1 Register (Address = 0x89) [Default = 0x00]

ABUFF1_CTL1 is shown in Table 7-303.

Return to the Summary Table.

Table 7-303. ABUFF1_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.37 ABUFF1_CTL2 Register (Address = 0x8A) [Default = 0x01]

ABUFF1_CTL2 is shown in Table 7-304.

Return to the Summary Table.

Table 7-304. ABUFF1_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x1	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.38 ABUFF1_CTL6 Register (Address = 0x8E) [Default = 0x0F]

ABUFF1_CTL6 is shown in Table 7-305.

Return to the Summary Table.

Table 7-305. ABUFF1_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x3	Reserved
1	STS_ABUFF_OF		0x1	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x1	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.6.39 ABUFF2_CTL0 Register (Address = 0x90) [Default = 0x00]

ABUFF2_CTL0 is shown in Table 7-306.

Return to the Summary Table.

Table 7-306. ABUFF2_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.40 ABUFF2_CTL1 Register (Address = 0x91) [Default = 0x00]

ABUFF2_CTL1 is shown in Table 7-307.

Return to the Summary Table.

Table 7-307. ABUFF2_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.41 ABUFF2_CTL2 Register (Address = 0x92) [Default = 0x02]

ABUFF2_CTL2 is shown in Table 7-308.

Return to the Summary Table.

Table 7-308. ABUFF2_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x2	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.42 ABUFF5_CTL0 Register (Address = 0xA8) [Default = 0x00]

ABUFF5_CTL0 is shown in Table 7-309.

Return to the Summary Table.

Table 7-309. ABUFF5_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.43 ABUFF5_CTL1 Register (Address = 0xA9) [Default = 0x00]

ABUFF5_CTL1 is shown in Table 7-310.

Return to the Summary Table.

Table 7-310. ABUFF5_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.44 ABUFF5_CTL2 Register (Address = 0xAA) [Default = 0x05]

ABUFF5_CTL2 is shown in Table 7-311.

Return to the Summary Table.

Table 7-311. ABUFF5_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x5	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.45 ABUFF5_CTL5 Register (Address = 0xAD) [Default = 0x06]

ABUFF5_CTL5 is shown in Table 7-312.

Return to the Summary Table.

Table 7-312. ABUFF5_CTL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RESERVED	R	0x6	Reserved

7.6.2.6.46 ABUFF5_CTL6 Register (Address = 0xAE) [Default = 0x00]

ABUFF5_CTL6 is shown in Table 7-313.

Return to the Summary Table.

Table 7-313. ABUFF5_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF		0x0	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x0	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.6.47 ABUFF6_CTL0 Register (Address = 0xB0) [Default = 0x00]

ABUFF6_CTL0 is shown in Table 7-314.

Return to the Summary Table.

Table 7-314. ABUFF6_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.48 ABUFF6_CTL1 Register (Address = 0xB1) [Default = 0x00]

ABUFF6_CTL1 is shown in Table 7-315.

Return to the Summary Table.

Table 7-315. ABUFF6_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.49 ABUFF6_CTL2 Register (Address = 0xB2) [Default = 0x06]

ABUFF6_CTL2 is shown in Table 7-316.

Return to the Summary Table.

Table 7-316. ABUFF6_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x6	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.50 ABUFF7_CTL0 Register (Address = 0xB8) [Default = 0x00]

ABUFF7_CTL0 is shown in Table 7-317.

Return to the Summary Table.

Table 7-317. ABUFF7_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.51 ABUFF7_CTL1 Register (Address = 0xB9) [Default = 0x00]

ABUFF7_CTL1 is shown in Table 7-318.

Return to the Summary Table.

Table 7-318. ABUFF7_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.52 ABUFF7_CTL2 Register (Address = 0xBA) [Default = 0x07]

ABUFF7_CTL2 is shown in Table 7-319.

Return to the Summary Table.

Table 7-319. ABUFF7_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5

Table 7-319. ABUFF7_CTL2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:0	SRC_TO_ABUFF_SEL	R/W	0x7	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.53 ABUFF7_CTL6 Register (Address = 0xBE) [Default = 0x00]

ABUFF7_CTL6 is shown in Table 7-320.

Return to the Summary Table.

Table 7-320. ABUFF7_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF		0x0	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x0	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.6.54 ABUFF8_CTL0 Register (Address = 0xC0) [Default = 0x00]

ABUFF8_CTL0 is shown in Table 7-321.

Return to the Summary Table.

Table 7-321. ABUFF8_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.55 ABUFF8_CTL1 Register (Address = 0xC1) [Default = 0x00]

ABUFF8_CTL1 is shown in Table 7-322.

Return to the Summary Table.

Table 7-322. ABUFF8_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

Table 7-322. ABUFF8_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.56 ABUFF8_CTL2 Register (Address = 0xC2) [Default = 0x08]

ABUFF8_CTL2 is shown in Table 7-323.

Return to the Summary Table.

Table 7-323. ABUFF8_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x8	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.57 ABUFF9_CTL0 Register (Address = 0xC8) [Default = 0x00]

ABUFF9_CTL0 is shown in Table 7-324.

Return to the Summary Table.

Table 7-324. ABUFF9_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.58 ABUFF9_CTL1 Register (Address = 0xC9) [Default = 0x00]

ABUFF9_CTL1 is shown in Table 7-325.

Return to the Summary Table.

Table 7-325. ABUFF9_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.59 ABUFF9_CTL2 Register (Address = 0xCA) [Default = 0x09]

ABUFF9_CTL2 is shown in Table 7-326.

Return to the Summary Table.

Table 7-326. ABUFF9_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x9	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.60 ABUFF9_CTL6 Register (Address = 0xCE) [Default = 0x00]

ABUFF9_CTL6 is shown in Table 7-327.

Return to the Summary Table.

Table 7-327. ABUFF9_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF		0x0	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x0	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.6.61 ABUFF10_CTL0 Register (Address = 0xD0) [Default = 0x00]

ABUFF10_CTL0 is shown in Table 7-328.

Return to the Summary Table.

Table 7-328. ABUFF10_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.62 ABUFF10_CTL1 Register (Address = 0xD1) [Default = 0x00]

ABUFF10_CTL1 is shown in Table 7-329.

Return to the Summary Table.

Table 7-329. ABUFF10_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.63 ABUFF10_CTL2 Register (Address = 0xD2) [Default = 0x0A]

ABUFF10_CTL2 is shown in Table 7-330.

Return to the Summary Table.

Table 7-330. ABUFF10_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0xA	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.64 ABUFF10_CTL6 Register (Address = 0xD6) [Default = 0x00]

ABUFF10_CTL6 is shown in Table 7-331.

Return to the Summary Table.

Table 7-331. ABUFF10_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF		0x0	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x0	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.6.65 ABUFF11_CTL0 Register (Address = 0xD8) [Default = 0x00]

ABUFF11_CTL0 is shown in Table 7-332.

Return to the Summary Table.

Table 7-332. ABUFF11_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0x0 = Maps to Link Layer of Port 0 0x1 = Maps to Link Layer of Port 1
0	SDP_ENABLE	R/W	0x0	0x0 = Disable ABUFF block 0x1 = Activates the ABUFF block

7.6.2.6.66 ABUFF11_CTL1 Register (Address = 0xD9) [Default = 0x00]

ABUFF11_CTL1 is shown in Table 7-333.

Return to the Summary Table.

Table 7-333. ABUFF11_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	Type of SDP: 0x0 = Audio 0x1 = Reserved 0x2 = Audio Info Frame 0x3 = Non Audio Info Frame 0x4 = MISC 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.2.6.67 ABUFF11_CTL2 Register (Address = 0xDA) [Default = 0x0B]

ABUFF11_CTL2 is shown in Table 7-334.

Return to the Summary Table.

Table 7-334. ABUFF11_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to: 0x0 = Stream 0 0x1 = Stream 1 0x2 = Stream 2 0x3 = Stream 3 0x4 = Stream 4 0x5 = Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0xB	Source of ABUFF data for FPD-Link IV Data Island audio only. 0x0 = SRCx to ABUFF SRC0 0x1 = SRCx to ABUFF SRC1 0x2 = SRCx to ABUFF SRC2 0x3 = SRCx to ABUFF SRC3 0x4 = SRCx to ABUFF SRC4 0x5 = SRCx to ABUFF SRC5 0x6 = SRCx to ABUFF SRC6 0x7 = SRCx to ABUFF SRC7 0x8 = SRCx to ABUFF SRC8 0x9 = SRCx to ABUFF SRC9 0x10 = SRCx to ABUFF SRC10

7.6.2.6.68 ABUFF11_CTL6 Register (Address = 0xDE) [Default = 0x00]

ABUFF11_CTL6 is shown in Table 7-335.

Return to the Summary Table.

Table 7-335. ABUFF11_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF		0x0	0x0 = No overflow 0x1 = ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED		0x0	0x0 = No packets drop 0x1 = ABUFF packets were dropped

7.6.2.7 Page 12: Video Processor Registers

Table 7-336 lists the memory-mapped registers for the Page 12: Video Processor registers. All register offset addresses not listed in Table 7-336 should be considered as reserved locations and the register contents should not be modified.

Table 7-336. PAGE 12: VIDEO PROCESSOR Registers

Address	Acronym	Register Name	Section
0x0	VID_PROC_CTL_VP0	VID_PROC_CTL_VP0	Go
0x1	VID_PROC_CFG_VP0	VID_PROC_CFG_VP0	Go
0x2	DP_H_ACTIVE0_VP0	DP_H_ACTIVE0_VP0	Go
0x3	DP_H_ACTIVE1_VP0	DP_H_ACTIVE1_VP0	Go
0x6	VFILTER_A_VP0	VFILTER_A_VP0	Go
0x7	VFILTER_N_VP0	VFILTER_N_VP0	Go
0x8	CROP_START_X0_VP0	CROP_START_X0_VP0	Go
0x9	CROP_START_X1_VP0	CROP_START_X1_VP0	Go
0xA	CROP_START_Y0_VP0	CROP_START_Y0_VP0	Go
0xB	CROP_START_Y1_VP0	CROP_START_Y1_VP0	Go
0xC	CROP_STOP_X0_VP0	CROP_STOP_X0_VP0	Go
0xD	CROP_STOP_X1_VP0	CROP_STOP_X1_VP0	Go
0xE	CROP_STOP_Y0_VP0	CROP_STOP_Y0_VP0	Go
0xF	CROP_STOP_Y1_VP0	CROP_STOP_Y1_VP0	Go
0x10	VID_H_ACTIVE0_VP0	VID_H_ACTIVE0_VP0	Go
0x11	VID_H_ACTIVE1_VP0	VID_H_ACTIVE1_VP0	Go
0x12	VID_H_BACK0_VP0	VID_H_BACK0_VP0	Go
0x13	VID_H_BACK1_VP0	VID_H_BACK1_VP0	Go
0x14	VID_H_WIDTH0_VP0	VID_H_WIDTH0_VP0	Go
0x15	VID_H_WIDTH1_VP0	VID_H_WIDTH1_VP0	Go
0x16	VID_H_TOTAL0_VP0	VID_H_TOTAL0_VP0	Go
0x17	VID_H_TOTAL1_VP0	VID_H_TOTAL1_VP0	Go
0x18	VID_V_ACTIVE0_VP0	VID_V_ACTIVE0_VP0	Go
0x19	VID_V_ACTIVE1_VP0	VID_V_ACTIVE1_VP0	Go
0x1A	VID_V_BACK0_VP0	VID_V_BACK0_VP0	Go
0x1B	VID_V_BACK1_VP0	VID_V_BACK1_VP0	Go
0x1C	VID_V_WIDTH0_VP0	VID_V_WIDTH0_VP0	Go
0x1D	VID_V_WIDTH1_VP0	VID_V_WIDTH1_VP0	Go
0x1E	VID_V_FRONT0_VP0	VID_V_FRONT0_VP0	Go
0x1F	VID_V_FRONT1_VP0	VID_V_FRONT1_VP0	Go
0x20	GEN_LATE_THRESH_VP0	GEN_LATE_THRESH_VP0	Go
0x21	GEN_EARLY_THRESH_VP0	GEN_EARLY_THRESH_VP0	Go
0x22	GEN_START_DELAY_VP0	GEN_START_DELAY_VP0	Go
0x23	PCLK_GEN_M_0_VP0	PCLK_GEN_M_0_VP0	Go
0x24	PCLK_GEN_M_1_VP0	PCLK_GEN_M_1_VP0	Go
0x25	PCLK_GEN_N_VP0	PCLK_GEN_N_VP0	Go
0x26	MAX_M_ADJUST_VP0	MAX_M_ADJUST_VP0	Go
0x27	VID_PROC_CFG2_VP0	VID_PROC_CFG2_VP0	Go
0x28	FPD4_PGCTL_VP0	FPD4_PGCTL_VP0	Go
0x29	FPD4_PGCFG_VP0	FPD4_PGCFG_VP0	Go
0x2A	FPD4_PGIA_VP0	FPD4_PGIA_VP0	Go

Table 7-336. PAGE 12: VIDEO PROCESSOR Registers (continued)

Address	Acronym	Register Name	Section
0x2B	FPD4_PGID_VP0	FPD4_PGID_VP0	Go
0x2C	FPD4_PGDBG_VP0	FPD4_PGDBG_VP0	Go
0x2D	FPD4_PGTSTDAT_VP0	FPD4_PGTSTDAT_VP0	Go
0x30	VP_STS_VP0	VP_STS_VP0	Go
0x31	INTR_STS_VP_VP0	INTR_STS_VP_VP0	Go
0x33	INTR_CTL_VP_VP0	INTR_CTL_VP_VP0	Go
0x35	MEAS_H_TOTAL0_VP0	MEAS_H_TOTAL0_VP0	Go
0x36	MEAS_H_TOTAL1_VP0	MEAS_H_TOTAL1_VP0	Go
0x40	VID_PROC_CTL_VP1	VID_PROC_CTL_VP1	Go
0x41	VID_PROC_CFG_VP1	VID_PROC_CFG_VP1	Go
0x42	DP_H_ACTIVE0_VP1	DP_H_ACTIVE0_VP1	Go
0x43	DP_H_ACTIVE1_VP1	DP_H_ACTIVE1_VP1	Go
0x46	VFILTER_A_VP1	VFILTER_A_VP1	Go
0x47	VFILTER_N_VP1	VFILTER_N_VP1	Go
0x48	CROP_START_X0_VP1	CROP_START_X0_VP1	Go
0x49	CROP_START_X1_VP1	CROP_START_X1_VP1	Go
0x4A	CROP_START_Y0_VP1	CROP_START_Y0_VP1	Go
0x4B	CROP_START_Y1_VP1	CROP_START_Y1_VP1	Go
0x4C	CROP_STOP_X0_VP1	CROP_STOP_X0_VP1	Go
0x4D	CROP_STOP_X1_VP1	CROP_STOP_X1_VP1	Go
0x4E	CROP_STOP_Y0_VP1	CROP_STOP_Y0_VP1	Go
0x4F	CROP_STOP_Y1_VP1	CROP_STOP_Y1_VP1	Go
0x50	VID_H_ACTIVE0_VP1	VID_H_ACTIVE0_VP1	Go
0x51	VID_H_ACTIVE1_VP1	VID_H_ACTIVE1_VP1	Go
0x52	VID_H_BACK0_VP1	VID_H_BACK0_VP1	Go
0x53	VID_H_BACK1_VP1	VID_H_BACK1_VP1	Go
0x54	VID_H_WIDTH0_VP1	VID_H_WIDTH0_VP1	Go
0x55	VID_H_WIDTH1_VP1	VID_H_WIDTH1_VP1	Go
0x56	VID_H_TOTAL0_VP1	VID_H_TOTAL0_VP1	Go
0x57	VID_H_TOTAL1_VP1	VID_H_TOTAL1_VP1	Go
0x58	VID_V_ACTIVE0_VP1	VID_V_ACTIVE0_VP1	Go
0x59	VID_V_ACTIVE1_VP1	VID_V_ACTIVE1_VP1	Go
0x5A	VID_V_BACK0_VP1	VID_V_BACK0_VP1	Go
0x5B	VID_V_BACK1_VP1	VID_V_BACK1_VP1	Go
0x5C	VID_V_WIDTH0_VP1	VID_V_WIDTH0_VP1	Go
0x5D	VID_V_WIDTH1_VP1	VID_V_WIDTH1_VP1	Go
0x5E	VID_V_FRONT0_VP1	VID_V_FRONT0_VP1	Go
0x5F	VID_V_FRONT1_VP1	VID_V_FRONT1_VP1	Go
0x60	GEN_LATE_THRESH_VP1	GEN_LATE_THRESH_VP1	Go
0x61	GEN_EARLY_THRESH_VP1	GEN_EARLY_THRESH_VP1	Go
0x62	GEN_START_DELAY_VP1	GEN_START_DELAY_VP1	Go
0x63	PCLK_GEN_M_0_VP1	PCLK_GEN_M_0_VP1	Go
0x64	PCLK_GEN_M_1_VP1	PCLK_GEN_M_1_VP1	Go
0x65	PCLK_GEN_N_VP1	PCLK_GEN_N_VP1	Go
0x66	MAX_M_ADJUST_VP1	MAX_M_ADJUST_VP1	Go

Table 7-336. PAGE 12: VIDEO PROCESSOR Registers (continued)

Address	Acronym	Register Name	Section
0x67	VID_PROC_CFG2_VP1	VID_PROC_CFG2_VP1	Go
0x68	FPD4_PGCTL_VP1	FPD4_PGCTL_VP1	Go
0x69	FPD4_PGCFG_VP1	FPD4_PGCFG_VP1	Go
0x6A	FPD4_PGIA_VP1	FPD4_PGIA_VP1	Go
0x6B	FPD4_PGID_VP1	FPD4_PGID_VP1	Go
0x6C	FPD4_PGDBG_VP1	FPD4_PGDBG_VP1	Go
0x6D	FPD4_PGTSTDAT_VP1	FPD4_PGTSTDAT_VP1	Go
0x70	VP_STS_VP1	VP_STS_VP1	Go
0x71	INTR_STS_VP_VP1	INTR_STS_VP_VP1	Go
0x73	INTR_CTL_VP_VP1	INTR_CTL_VP_VP1	Go
0x75	MEAS_H_TOTAL0_VP1	MEAS_H_TOTAL0_VP1	Go
0x76	MEAS_H_TOTAL1_VP1	MEAS_H_TOTAL1_VP1	Go
0x80	VID_PROC_CTL_VP2	VID_PROC_CTL_VP2	Go
0x81	VID_PROC_CFG_VP2	VID_PROC_CFG_VP2	Go
0x82	DP_H_ACTIVE0_VP2	DP_H_ACTIVE0_VP2	Go
0x83	DP_H_ACTIVE1_VP2	DP_H_ACTIVE1_VP2	Go
0x86	VFILTER_A_VP2	VFILTER_A_VP2	Go
0x87	VFILTER_N_VP2	VFILTER_N_VP2	Go
0x88	CROP_START_X0_VP2	CROP_START_X0_VP2	Go
0x89	CROP_START_X1_VP2	CROP_START_X1_VP2	Go
0x8A	CROP_START_Y0_VP2	CROP_START_Y0_VP2	Go
0x8B	CROP_START_Y1_VP2	CROP_START_Y1_VP2	Go
0x8C	CROP_STOP_X0_VP2	CROP_STOP_X0_VP2	Go
0x8D	CROP_STOP_X1_VP2	CROP_STOP_X1_VP2	Go
0x8E	CROP_STOP_Y0_VP2	CROP_STOP_Y0_VP2	Go
0x8F	CROP_STOP_Y1_VP2	CROP_STOP_Y1_VP2	Go
0x90	VID_H_ACTIVE0_VP2	VID_H_ACTIVE0_VP2	Go
0x91	VID_H_ACTIVE1_VP2	VID_H_ACTIVE1_VP2	Go
0x92	VID_H_BACK0_VP2	VID_H_BACK0_VP2	Go
0x93	VID_H_BACK1_VP2	VID_H_BACK1_VP2	Go
0x94	VID_H_WIDTH0_VP2	VID_H_WIDTH0_VP2	Go
0x95	VID_H_WIDTH1_VP2	VID_H_WIDTH1_VP2	Go
0x96	VID_H_TOTAL0_VP2	VID_H_TOTAL0_VP2	Go
0x97	VID_H_TOTAL1_VP2	VID_H_TOTAL1_VP2	Go
0x98	VID_V_ACTIVE0_VP2	VID_V_ACTIVE0_VP2	Go
0x99	VID_V_ACTIVE1_VP2	VID_V_ACTIVE1_VP2	Go
0x9A	VID_V_BACK0_VP2	VID_V_BACK0_VP2	Go
0x9B	VID_V_BACK1_VP2	VID_V_BACK1_VP2	Go
0x9C	VID_V_WIDTH0_VP2	VID_V_WIDTH0_VP2	Go
0x9D	VID_V_WIDTH1_VP2	VID_V_WIDTH1_VP2	Go
0x9E	VID_V_FRONT0_VP2	VID_V_FRONT0_VP2	Go
0x9F	VID_V_FRONT1_VP2	VID_V_FRONT1_VP2	Go
0xA0	GEN_LATE_THRESH_VP2	GEN_LATE_THRESH_VP2	Go
0xA1	GEN_EARLY_THRESH_VP2	GEN_EARLY_THRESH_VP2	Go
0xA2	GEN_START_DELAY_VP2	GEN_START_DELAY_VP2	Go

Table 7-336. PAGE 12: VIDEO PROCESSOR Registers (continued)

Address	Acronym	Register Name	Section
0xA3	PCLK_GEN_M_0_VP2	PCLK_GEN_M_0_VP2	Go
0xA4	PCLK_GEN_M_1_VP2	PCLK_GEN_M_1_VP2	Go
0xA5	PCLK_GEN_N_VP2	PCLK_GEN_N_VP2	Go
0xA6	MAX_M_ADJUST_VP2	MAX_M_ADJUST_VP2	Go
0xA7	VID_PROC_CFG2_VP2	VID_PROC_CFG2_VP2	Go
0xA8	FPD4_PGCTL_VP2	FPD4_PGCTL_VP2	Go
0xA9	FPD4_PGCFG_VP2	FPD4_PGCFG_VP2	Go
0xAA	FPD4_PGIA_VP2	FPD4_PGIA_VP2	Go
0xAB	FPD4_PGID_VP2	FPD4_PGID_VP2	Go
0xAC	FPD4_PGDBG_VP2	FPD4_PGDBG_VP2	Go
0xAD	FPD4_PGTSTDAT_VP2	FPD4_PGTSTDAT_VP2	Go
0xB0	VP_STS_VP2	VP_STS_VP2	Go
0xB1	INTR_STS_VP_VP2	INTR_STS_VP_VP2	Go
0xB3	INTR_CTL_VP_VP2	INTR_CTL_VP_VP2	Go
0xB5	MEAS_H_TOTAL0_VP2	MEAS_H_TOTAL0_VP2	Go
0xB6	MEAS_H_TOTAL1_VP2	MEAS_H_TOTAL1_VP2	Go
0xC0	VID_PROC_CTL_VP3	VID_PROC_CTL_VP3	Go
0xC1	VID_PROC_CFG_VP3	VID_PROC_CFG_VP3	Go
0xC2	DP_H_ACTIVE0_VP3	DP_H_ACTIVE0_VP3	Go
0xC3	DP_H_ACTIVE1_VP3	DP_H_ACTIVE1_VP3	Go
0xC6	VFILTER_A_VP3	VFILTER_A_VP3	Go
0xC7	VFILTER_N_VP3	VFILTER_N_VP3	Go
0xC8	CROP_START_X0_VP3	CROP_START_X0_VP3	Go
0xC9	CROP_START_X1_VP3	CROP_START_X1_VP3	Go
0xCA	CROP_START_Y0_VP3	CROP_START_Y0_VP3	Go
0xCB	CROP_START_Y1_VP3	CROP_START_Y1_VP3	Go
0xCC	CROP_STOP_X0_VP3	CROP_STOP_X0_VP3	Go
0xCD	CROP_STOP_X1_VP3	CROP_STOP_X1_VP3	Go
0xCE	CROP_STOP_Y0_VP3	CROP_STOP_Y0_VP3	Go
0xCF	CROP_STOP_Y1_VP3	CROP_STOP_Y1_VP3	Go
0xD0	VID_H_ACTIVE0_VP3	VID_H_ACTIVE0_VP3	Go
0xD1	VID_H_ACTIVE1_VP3	VID_H_ACTIVE1_VP3	Go
0xD2	VID_H_BACK0_VP3	VID_H_BACK0_VP3	Go
0xD3	VID_H_BACK1_VP3	VID_H_BACK1_VP3	Go
0xD4	VID_H_WIDTH0_VP3	VID_H_WIDTH0_VP3	Go
0xD5	VID_H_WIDTH1_VP3	VID_H_WIDTH1_VP3	Go
0xD6	VID_H_TOTAL0_VP3	VID_H_TOTAL0_VP3	Go
0xD7	VID_H_TOTAL1_VP3	VID_H_TOTAL1_VP3	Go
0xD8	VID_V_ACTIVE0_VP3	VID_V_ACTIVE0_VP3	Go
0xD9	VID_V_ACTIVE1_VP3	VID_V_ACTIVE1_VP3	Go
0xDA	VID_V_BACK0_VP3	VID_V_BACK0_VP3	Go
0xDB	VID_V_BACK1_VP3	VID_V_BACK1_VP3	Go
0xDC	VID_V_WIDTH0_VP3	VID_V_WIDTH0_VP3	Go
0xDD	VID_V_WIDTH1_VP3	VID_V_WIDTH1_VP3	Go
0xDE	VID_V_FRONT0_VP3	VID_V_FRONT0_VP3	Go

Table 7-336. PAGE 12: VIDEO PROCESSOR Registers (continued)

Address	Acronym	Register Name	Section
0xDF	VID_V_FRONT1_VP3	VID_V_FRONT1_VP3	Go
0xE0	GEN_LATE_THRESH_VP3	GEN_LATE_THRESH_VP3	Go
0xE1	GEN_EARLY_THRESH_VP3	GEN_EARLY_THRESH_VP3	Go
0xE2	GEN_START_DELAY_VP3	GEN_START_DELAY_VP3	Go
0xE3	PCLK_GEN_M_0_VP3	PCLK_GEN_M_0_VP3	Go
0xE4	PCLK_GEN_M_1_VP3	PCLK_GEN_M_1_VP3	Go
0xE5	PCLK_GEN_N_VP3	PCLK_GEN_N_VP3	Go
0xE6	MAX_M_ADJUST_VP3	MAX_M_ADJUST_VP3	Go
0xE7	VID_PROC_CFG2_VP3	VID_PROC_CFG2_VP3	Go
0xE8	FPD4_PGCTL_VP3	FPD4_PGCTL_VP3	Go
0xE9	FPD4_PGCFG_VP3	FPD4_PGCFG_VP3	Go
0xEA	FPD4_PGIA_VP3	FPD4_PGIA_VP3	Go
0xEB	FPD4_PGID_VP3	FPD4_PGID_VP3	Go
0xEC	FPD4_PGDBG_VP3	FPD4_PGDBG_VP3	Go
0xED	FPD4_PGTSTDAT_VP3	FPD4_PGTSTDAT_VP3	Go
0xF0	VP_STS_VP3	VP_STS_VP3	Go
0xF1	INTR_STS_VP_VP3	INTR_STS_VP_VP3	Go
0xF3	INTR_CTL_VP_VP3	INTR_CTL_VP_VP3	Go
0xF5	MEAS_H_TOTAL0_VP3	MEAS_H_TOTAL0_VP3	Go
0xF6	MEAS_H_TOTAL1_VP3	MEAS_H_TOTAL1_VP3	Go

Complex bit access types are encoded to fit into small table cells. Table 7-337 shows the codes that are used for access types in this section.

Table 7-337. Page 12: Video Processor Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.7.1 VID_PROC_CTL_VP0 Register (Address = 0x0) [Default = 0x00]

VID_PROC_CTL_VP0 is shown in Table 7-338.

Return to the Summary Table.

Table 7-338. VID_PROC_CTL_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved

Table 7-338. VID_PROC_CTL_VP0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition,Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

7.6.2.7.2 VID_PROC_CFG_VP0 Register (Address = 0x1) [Default = 0xA8]

VID_PROC_CFG_VP0 is shown in Table 7-339.

Return to the Summary Table.

Table 7-339. VID_PROC_CFG_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1 = Ignore Line Number 0 = Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1 = Wait for first video line, adding delay in the horizontal back porch period 0 = Generate extra horizontal lines of blanking while waiting

Table 7-339. VID_PROC_CFG_VP0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x0	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor. Note: The DP Receiver only provides two streams, so only settings of 0 and 1 are valid.

7.6.2.7.3 DP_H_ACTIVE0_VP0 Register (Address = 0x2) [Default = 0x00]

DP_H_ACTIVE0_VP0 is shown in Table 7-340.

Return to the Summary Table.

Table 7-340. DP_H_ACTIVE0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[7:0]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.4 DP_H_ACTIVE1_VP0 Register (Address = 0x3) [Default = 0x00]

DP_H_ACTIVE1_VP0 is shown in Table 7-341.

Return to the Summary Table.

Table 7-341. DP_H_ACTIVE1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[15:8]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.5 VFILTER_A_VP0 Register (Address = 0x6) [Default = 0x01]

VFILTER_A_VP0 is shown in Table 7-342.

Return to the Summary Table.

Table 7-342. VFILTER_A_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A = 1 and VFILTER_N =2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

7.6.2.7.6 VFILTER_N_VP0 Register (Address = 0x7) [Default = 0x01]

VFILTER_N_VP0 is shown in Table 7-343.

Return to the Summary Table.

Table 7-343. VFILTER_N_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

7.6.2.7.7 CROP_START_X0_VP0 Register (Address = 0x8) [Default = 0x00]

CROP_START_X0_VP0 is shown in Table 7-344.

Return to the Summary Table.

Table 7-344. CROP_START_X0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.8 CROP_START_X1_VP0 Register (Address = 0x9) [Default = 0x00]

CROP_START_X1_VP0 is shown in Table 7-345.

Return to the Summary Table.

Table 7-345. CROP_START_X1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.9 CROP_START_Y0_VP0 Register (Address = 0xA) [Default = 0x00]

CROP_START_Y0_VP0 is shown in Table 7-346.

Return to the Summary Table.

Table 7-346. CROP_START_Y0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.10 CROP_START_Y1_VP0 Register (Address = 0xB) [Default = 0x00]

CROP_START_Y1_VP0 is shown in Table 7-347.

Return to the Summary Table.

Table 7-347. CROP_START_Y1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.11 CROP_STOP_X0_VP0 Register (Address = 0xC) [Default = 0x00]

CROP_STOP_X0_VP0 is shown in Table 7-348.

Return to the Summary Table.

Table 7-348. CROP_STOP_X0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.12 CROP_STOP_X1_VP0 Register (Address = 0xD) [Default = 0x00]

CROP_STOP_X1_VP0 is shown in Table 7-349.

Return to the Summary Table.

Table 7-349. CROP_STOP_X1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.13 CROP_STOP_Y0_VP0 Register (Address = 0xE) [Default = 0x00]

CROP_STOP_Y0_VP0 is shown in Table 7-350.

Return to the Summary Table.

Table 7-350. CROP_STOP_Y0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.14 CROP_STOP_Y1_VP0 Register (Address = 0xF) [Default = 0x00]

CROP_STOP_Y1_VP0 is shown in Table 7-351.

Return to the Summary Table.

Table 7-351. CROP_STOP_Y1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.15 VID_H_ACTIVE0_VP0 Register (Address = 0x10) [Default = 0x00]

VID_H_ACTIVE0_VP0 is shown in Table 7-352.

Return to the Summary Table.

Table 7-352. VID_H_ACTIVE0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.16 VID_H_ACTIVE1_VP0 Register (Address = 0x11) [Default = 0x00]

VID_H_ACTIVE1_VP0 is shown in Table 7-353.

Return to the Summary Table.

Table 7-353. VID_H_ACTIVE1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.17 VID_H_BACK0_VP0 Register (Address = 0x12) [Default = 0x00]

VID_H_BACK0_VP0 is shown in Table 7-354.

Return to the Summary Table.

Table 7-354. VID_H_BACK0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.18 VID_H_BACK1_VP0 Register (Address = 0x13) [Default = 0x00]

VID_H_BACK1_VP0 is shown in Table 7-355.

Return to the Summary Table.

Table 7-355. VID_H_BACK1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.19 VID_H_WIDTH0_VP0 Register (Address = 0x14) [Default = 0x00]

VID_H_WIDTH0_VP0 is shown in Table 7-356.

Return to the Summary Table.

Table 7-356. VID_H_WIDTH0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.20 VID_H_WIDTH1_VP0 Register (Address = 0x15) [Default = 0x00]

VID_H_WIDTH1_VP0 is shown in Table 7-357.

Return to the Summary Table.

Table 7-357. VID_H_WIDTH1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.21 VID_H_TOTAL0_VP0 Register (Address = 0x16) [Default = 0x00]

VID_H_TOTAL0_VP0 is shown in Table 7-358.

Return to the Summary Table.

Table 7-358. VID_H_TOTAL0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.22 VID_H_TOTAL1_VP0 Register (Address = 0x17) [Default = 0x00]

VID_H_TOTAL1_VP0 is shown in Table 7-359.

Return to the Summary Table.

Table 7-359. VID_H_TOTAL1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.23 VID_V_ACTIVE0_VP0 Register (Address = 0x18) [Default = 0x00]

VID_V_ACTIVE0_VP0 is shown in Table 7-360.

Return to the Summary Table.

Table 7-360. VID_V_ACTIVE0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.24 VID_V_ACTIVE1_VP0 Register (Address = 0x19) [Default = 0x00]

VID_V_ACTIVE1_VP0 is shown in Table 7-361.

Return to the Summary Table.

Table 7-361. VID_V_ACTIVE1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.25 VID_V_BACK0_VP0 Register (Address = 0x1A) [Default = 0x00]

VID_V_BACK0_VP0 is shown in Table 7-362.

Return to the Summary Table.

Table 7-362. VID_V_BACK0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.26 VID_V_BACK1_VP0 Register (Address = 0x1B) [Default = 0x00]

VID_V_BACK1_VP0 is shown in Table 7-363.

Return to the Summary Table.

Table 7-363. VID_V_BACK1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.27 VID_V_WIDTH0_VP0 Register (Address = 0x1C) [Default = 0x00]

VID_V_WIDTH0_VP0 is shown in Table 7-364.

Return to the Summary Table.

Table 7-364. VID_V_WIDTH0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.28 VID_V_WIDTH1_VP0 Register (Address = 0x1D) [Default = 0x00]

VID_V_WIDTH1_VP0 is shown in Table 7-365.

Return to the Summary Table.

Table 7-365. VID_V_WIDTH1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.29 VID_V_FRONT0_VP0 Register (Address = 0x1E) [Default = 0x00]

VID_V_FRONT0_VP0 is shown in Table 7-366.

Return to the Summary Table.

Table 7-366. VID_V_FRONT0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.30 VID_V_FRONT1_VP0 Register (Address = 0x1F) [Default = 0x00]

VID_V_FRONT1_VP0 is shown in Table 7-367.

Return to the Summary Table.

Table 7-367. VID_V_FRONT1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.31 GEN_LATE_THRESH_VP0 Register (Address = 0x20) [Default = 0x00]

GEN_LATE_THRESH_VP0 is shown in Table 7-368.

Return to the Summary Table.

Table 7-368. GEN_LATE_THRESH_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.32 GEN_EARLY_THRESH_VP0 Register (Address = 0x21) [Default = 0x00]

GEN_EARLY_THRESH_VP0 is shown in Table 7-369.

Return to the Summary Table.

Table 7-369. GEN_EARLY_THRESH_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.33 GEN_START_DELAY_VP0 Register (Address = 0x22) [Default = 0x10]

GEN_START_DELAY_VP0 is shown in Table 7-370.

Return to the Summary Table.

Table 7-370. GEN_START_DELAY_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

7.6.2.7.34 PCLK_GEN_M_0_VP0 Register (Address = 0x23) [Default = 0x00]

PCLK_GEN_M_0_VP0 is shown in Table 7-371.

Return to the Summary Table.

Table 7-371. PCLK_GEN_M_0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0} Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.35 PCLK_GEN_M_1_VP0 Register (Address = 0x24) [Default = 0x10]

PCLK_GEN_M_1_VP0 is shown in Table 7-372.

Return to the Summary Table.

Table 7-372. PCLK_GEN_M_1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.36 PCLK_GEN_N_VP0 Register (Address = 0x25) [Default = 0x0F]

PCLK_GEN_N_VP0 is shown in Table 7-373.

Return to the Summary Table.

Table 7-373. PCLK_GEN_N_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{PCLK\_GEN\_M}$. The default setting for this register chooses an N value of 2^{15} or 32,768.

7.6.2.7.37 MAX_M_ADJUST_VP0 Register (Address = 0x26) [Default = 0x08]

MAX_M_ADJUST_VP0 is shown in Table 7-374.

Return to the Summary Table.

Table 7-374. MAX_M_ADJUST_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

7.6.2.7.38 VID_PROC_CFG2_VP0 Register (Address = 0x27) [Default = 0x00]

VID_PROC_CFG2_VP0 is shown in Table 7-375.

Return to the Summary Table.

Video Processor Configuration Register 2

Table 7-375. VID_PROC_CFG2_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (meaasured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

Table 7-375. VID_PROC_CFG2_VP0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

7.6.2.7.39 FPD4_PGCTL_VP0 Register (Address = 0x28) [Default = 0x08]

FPD4_PGCTL_VP0 is shown in Table 7-376.

Return to the Summary Table.

Table 7-376. FPD4_PGCTL_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: Checkerboard (White/Black) 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom/Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

Table 7-376. FPD4_PGCTL_VP0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	When PATGEN_LEGACY_ENB = 0, Pattern generator, pattern checker and forwarding enable encoding: 00: Disable pattern generator and pattern checker 01: Enable pattern generator 10: Enable pattern checker, do not forward patterns on to the RX datapath 11: Enable pattern checker, forward patterns on to the RX datapath When PAT_ENC_EN = 2 'b10 or PAT_ENC_EN = 2 'b11, the local pattern generator is still enabled internally for comparison with incoming video stream When PAT_ENC_EN = 2 'b11, the local pattern generator 's patterns are forwarded, not the incoming video stream When PATGEN_LEGACY_ENB = 1, PAT_ENC_EN[1]: 1: Enable pattern checker 0: Disable pattern checker PAT_ENC_EN[0]: 1: Enable pattern generator 0: Disable pattern generator Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]

7.6.2.7.40 FPD4_PGCFG_VP0 Register (Address = 0x29) [Default = 0x08]

FPD4_PGCFG_VP0 is shown in Table 7-377.

Return to the Summary Table.

Table 7-377. FPD4_PGCFG_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

Table 7-377. FPD4_PGCFG_VP0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

7.6.2.7.41 FPD4_PGIA_VP0 Register (Address = 0x2A) [Default = 0x00]

FPD4_PGIA_VP0 is shown in Table 7-378.

Return to the Summary Table.

Table 7-378. FPD4_PGIA_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

7.6.2.7.42 FPD4_PGID_VP0 Register (Address = 0x2B) [Default = 0x00]

FPD4_PGID_VP0 is shown in Table 7-379.

Return to the Summary Table.

Table 7-379. FPD4_PGID_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

7.6.2.7.43 FPD4_PGDBG_VP0 Register (Address = 0x2C) [Default = 0x00]

FPD4_PGDBG_VP0 is shown in Table 7-380.

Return to the Summary Table.

Table 7-380. FPD4_PGDBG_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	PATGEN_DBG_SEL	R/W	0x0	Test Mux Select: This field selects the signals to be brought out on the test output bus as well as read in the PGTSTDAT register. See the Debug Monitor section of the Pattern Generator DDS for details.
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN_RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.

Table 7-380. FPD4_PGDBG_VP0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	PATGEN_DBG_FREERUN	R/W	0x0	Test Mux Freerun: Enables continuous output of test mux data. If set to 0, data will be sampled and held following setting of the PATGEN_DBG_SAMPLE register bit. Freerun operation is most useful for viewing on external pins. Sample/Hold is most useful for reading through the PGTSTDAT register.
0	PATGEN_DBG_SAMPLE	RH/W1S	0x0	Test Mux Sample/Hold: Enables sampling of the test mux data within its source clock domain. Guarantees valid data readback through the PGTSTDAT register. This bit is self-clearing.

7.6.2.7.44 FPD4_PGTSTDAT_VP0 Register (Address = 0x2D) [Default = 0x00]

FPD4_PGTSTDAT_VP0 is shown in Table 7-381.

Return to the Summary Table.

Table 7-381. FPD4_PGTSTDAT_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	PATGEN_TST_DATA	R	0x0	Test Data: This field contains the Debug Monitor output. See the Debug Monitor section of the Pattern Generator DDS for details.

7.6.2.7.45 VP_STS_VP0 Register (Address = 0x30) [Default = 0x00]

VP_STS_VP0 is shown in Table 7-382.

Return to the Summary Table.

Video Processor Status Register

Table 7-382. VP_STS_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved: Reads return 0, writes are ignored.
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

7.6.2.7.46 INTR_STS_VP_VP0 Register (Address = 0x31) [Default = 0x00]

INTR_STS_VP_VP0 is shown in Table 7-383.

Return to the Summary Table.

Video Interrupt Status Register
The bits in this register will be set on occurrence of the associated event. If the corresponding interrupt mask register is set, an Interrupt will be generated for the event. The interrupt status bits will be cleared on a read of this register.

Table 7-383. INTR_STS_VP_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR		0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR		0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.
4	IS_TIMING_DATA_ERR		0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR		0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR		0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR		0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

7.6.2.7.47 INTR_CTL_VP_VP0 Register (Address = 0x33) [Default = 0x00]

INTR_CTL_VP_VP0 is shown in Table 7-384.

Return to the Summary Table.

Video Interrupt Control Register
The bits in this register enable interrupts for the associated bits in the Interrupt Status register.

Table 7-384. INTR_CTL_VP_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

7.6.2.7.48 MEAS_H_TOTAL0_VP0 Register (Address = 0x35) [Default = 0x00]

MEAS_H_TOTAL0_VP0 is shown in Table 7-385.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-385. MEAS_H_TOTAL0_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.49 MEAS_H_TOTAL1_VP0 Register (Address = 0x36) [Default = 0x00]

MEAS_H_TOTAL1_VP0 is shown in Table 7-386.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-386. MEAS_H_TOTAL1_VP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.50 VID_PROC_CTL_VP1 Register (Address = 0x40) [Default = 0x00]

VID_PROC_CTL_VP1 is shown in Table 7-387.

Return to the Summary Table.

Video Processor Control Register

Table 7-387. VID_PROC_CTL_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.

Table 7-387. VID_PROC_CTL_VP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition,Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

7.6.2.7.51 VID_PROC_CFG_VP1 Register (Address = 0x41) [Default = 0xA9]

VID_PROC_CFG_VP1 is shown in Table 7-388.

Return to the Summary Table.

Video Processor Configuration Register

Table 7-388. VID_PROC_CFG_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1: Ignore Line Number 0: Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra horizontal lines of blanking while waiting
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x1	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor. Note: The DP Receiver only provides two streams, so only settings of 0 and 1 are valid.

7.6.2.7.52 DP_H_ACTIVE0_VP1 Register (Address = 0x42) [Default = 0x00]

DP_H_ACTIVE0_VP1 is shown in Table 7-389.

Return to the Summary Table.

Table 7-389. DP_H_ACTIVE0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[7:0]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.53 DP_H_ACTIVE1_VP1 Register (Address = 0x43) [Default = 0x00]

DP_H_ACTIVE1_VP1 is shown in Table 7-390.

Return to the Summary Table.

Table 7-390. DP_H_ACTIVE1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[15:8]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.54 VFILTER_A_VP1 Register (Address = 0x46) [Default = 0x01]

VFILTER_A_VP1 is shown in Table 7-391.

Return to the Summary Table.

Vertical Filter A Register

Table 7-391. VFILTER_A_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A = 1 and VFILTER_N =2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

7.6.2.7.55 VFILTER_N_VP1 Register (Address = 0x47) [Default = 0x01]

VFILTER_N_VP1 is shown in Table 7-392.

Return to the Summary Table.

Vertical Filter B Register

Table 7-392. VFILTER_N_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

7.6.2.7.56 CROP_START_X0_VP1 Register (Address = 0x48) [Default = 0x00]

CROP_START_X0_VP1 is shown in Table 7-393.

Return to the Summary Table.

Crop Start X1 Register

Table 7-393. CROP_START_X0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.57 CROP_START_X1_VP1 Register (Address = 0x49) [Default = 0x00]

CROP_START_X1_VP1 is shown in Table 7-394.

Return to the Summary Table.

Crop Start X1 Register

Table 7-394. CROP_START_X1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.58 CROP_START_Y0_VP1 Register (Address = 0x4A) [Default = 0x00]

CROP_START_Y0_VP1 is shown in Table 7-395.

Return to the Summary Table.

Crop Start Y0 Register

Table 7-395. CROP_START_Y0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.59 CROP_START_Y1_VP1 Register (Address = 0x4B) [Default = 0x00]

CROP_START_Y1_VP1 is shown in Table 7-396.

Return to the Summary Table.

Crop Start Y1 Register

Table 7-396. CROP_START_Y1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.60 CROP_STOP_X0_VP1 Register (Address = 0x4C) [Default = 0x00]

CROP_STOP_X0_VP1 is shown in Table 7-397.

Return to the Summary Table.

Crop Stop X0 Register

Table 7-397. CROP_STOP_X0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.61 CROP_STOP_X1_VP1 Register (Address = 0x4D) [Default = 0x00]

CROP_STOP_X1_VP1 is shown in Table 7-398.

Return to the Summary Table.

Crop Stop X1 Register

Table 7-398. CROP_STOP_X1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.62 CROP_STOP_Y0_VP1 Register (Address = 0x4E) [Default = 0x00]

CROP_STOP_Y0_VP1 is shown in Table 7-399.

Return to the Summary Table.

Crop Stop Y0 Register

Table 7-399. CROP_STOP_Y0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.63 CROP_STOP_Y1_VP1 Register (Address = 0x4F) [Default = 0x00]

CROP_STOP_Y1_VP1 is shown in Table 7-400.

Return to the Summary Table.

Crop Stop Y1 Register

Table 7-400. CROP_STOP_Y1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.64 VID_H_ACTIVE0_VP1 Register (Address = 0x50) [Default = 0x00]

VID_H_ACTIVE0_VP1 is shown in Table 7-401.

Return to the Summary Table.

Table 7-401. VID_H_ACTIVE0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.65 VID_H_ACTIVE1_VP1 Register (Address = 0x51) [Default = 0x00]

VID_H_ACTIVE1_VP1 is shown in Table 7-402.

Return to the Summary Table.

Table 7-402. VID_H_ACTIVE1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.66 VID_H_BACK0_VP1 Register (Address = 0x52) [Default = 0x00]

VID_H_BACK0_VP1 is shown in Table 7-403.

Return to the Summary Table.

Table 7-403. VID_H_BACK0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.67 VID_H_BACK1_VP1 Register (Address = 0x53) [Default = 0x00]

VID_H_BACK1_VP1 is shown in Table 7-404.

Return to the Summary Table.

Table 7-404. VID_H_BACK1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.68 VID_H_WIDTH0_VP1 Register (Address = 0x54) [Default = 0x00]

VID_H_WIDTH0_VP1 is shown in Table 7-405.

Return to the Summary Table.

Table 7-405. VID_H_WIDTH0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.69 VID_H_WIDTH1_VP1 Register (Address = 0x55) [Default = 0x00]

VID_H_WIDTH1_VP1 is shown in Table 7-406.

Return to the Summary Table.

Table 7-406. VID_H_WIDTH1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.70 VID_H_TOTAL0_VP1 Register (Address = 0x56) [Default = 0x00]

VID_H_TOTAL0_VP1 is shown in Table 7-407.

Return to the Summary Table.

Table 7-407. VID_H_TOTAL0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.71 VID_H_TOTAL1_VP1 Register (Address = 0x57) [Default = 0x00]

VID_H_TOTAL1_VP1 is shown in Table 7-408.

Return to the Summary Table.

Table 7-408. VID_H_TOTAL1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.72 VID_V_ACTIVE0_VP1 Register (Address = 0x58) [Default = 0x00]

VID_V_ACTIVE0_VP1 is shown in Table 7-409.

Return to the Summary Table.

Table 7-409. VID_V_ACTIVE0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.73 VID_V_ACTIVE1_VP1 Register (Address = 0x59) [Default = 0x00]

VID_V_ACTIVE1_VP1 is shown in Table 7-410.

Return to the Summary Table.

Table 7-410. VID_V_ACTIVE1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.74 VID_V_BACK0_VP1 Register (Address = 0x5A) [Default = 0x00]

VID_V_BACK0_VP1 is shown in Table 7-411.

Return to the Summary Table.

Table 7-411. VID_V_BACK0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.75 VID_V_BACK1_VP1 Register (Address = 0x5B) [Default = 0x00]

VID_V_BACK1_VP1 is shown in Table 7-412.

Return to the Summary Table.

Table 7-412. VID_V_BACK1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.76 VID_V_WIDTH0_VP1 Register (Address = 0x5C) [Default = 0x00]

VID_V_WIDTH0_VP1 is shown in Table 7-413.

Return to the Summary Table.

Table 7-413. VID_V_WIDTH0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.77 VID_V_WIDTH1_VP1 Register (Address = 0x5D) [Default = 0x00]

VID_V_WIDTH1_VP1 is shown in Table 7-414.

Return to the Summary Table.

Table 7-414. VID_V_WIDTH1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.78 VID_V_FRONT0_VP1 Register (Address = 0x5E) [Default = 0x00]

VID_V_FRONT0_VP1 is shown in Table 7-415.

Return to the Summary Table.

Table 7-415. VID_V_FRONT0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.79 VID_V_FRONT1_VP1 Register (Address = 0x5F) [Default = 0x00]

VID_V_FRONT1_VP1 is shown in Table 7-416.

Return to the Summary Table.

Table 7-416. VID_V_FRONT1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.80 GEN_LATE_THRESH_VP1 Register (Address = 0x60) [Default = 0x00]

GEN_LATE_THRESH_VP1 is shown in Table 7-417.

Return to the Summary Table.

Table 7-417. GEN_LATE_THRESH_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.81 GEN_EARLY_THRESH_VP1 Register (Address = 0x61) [Default = 0x00]

GEN_EARLY_THRESH_VP1 is shown in Table 7-418.

Return to the Summary Table.

Table 7-418. GEN_EARLY_THRESH_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.82 GEN_START_DELAY_VP1 Register (Address = 0x62) [Default = 0x10]

GEN_START_DELAY_VP1 is shown in Table 7-419.

Return to the Summary Table.

Table 7-419. GEN_START_DELAY_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

7.6.2.7.83 PCLK_GEN_M_0_VP1 Register (Address = 0x63) [Default = 0x00]

PCLK_GEN_M_0_VP1 is shown in Table 7-420.

Return to the Summary Table.

Table 7-420. PCLK_GEN_M_0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0} Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.84 PCLK_GEN_M_1_VP1 Register (Address = 0x64) [Default = 0x10]

PCLK_GEN_M_1_VP1 is shown in Table 7-421.

Return to the Summary Table.

Table 7-421. PCLK_GEN_M_1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.85 PCLK_GEN_N_VP1 Register (Address = 0x65) [Default = 0x0F]

PCLK_GEN_N_VP1 is shown in Table 7-422.

Return to the Summary Table.

Table 7-422. PCLK_GEN_N_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{PCLK\_GEN\_M}$. The default setting for this register chooses an N value of 2^{15} or 32,768.

7.6.2.7.86 MAX_M_ADJUST_VP1 Register (Address = 0x66) [Default = 0x08]

MAX_M_ADJUST_VP1 is shown in Table 7-423.

Return to the Summary Table.

Table 7-423. MAX_M_ADJUST_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

7.6.2.7.87 VID_PROC_CFG2_VP1 Register (Address = 0x67) [Default = 0x00]

VID_PROC_CFG2_VP1 is shown in Table 7-424.

Return to the Summary Table.

Video Processor Configuration Register 2

Table 7-424. VID_PROC_CFG2_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (meaasured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

Table 7-424. VID_PROC_CFG2_VP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

7.6.2.7.88 FPD4_PGCTL_VP1 Register (Address = 0x68) [Default = 0x08]

FPD4_PGCTL_VP1 is shown in Table 7-425.

Return to the Summary Table.

Table 7-425. FPD4_PGCTL_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: Checkerboard (White/Black) 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom/Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

Table 7-425. FPD4_PGCTL_VP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	When PATGEN_LEGACY_ENB = 0, Pattern generator, pattern checker and forwarding enable encoding: 00: Disable pattern generator and pattern checker 01: Enable pattern generator 10: Enable pattern checker, do not forward patterns on to the RX datapath 11: Enable pattern checker, forward patterns on to the RX datapath When PAT_ENC_EN = 2 'b10 or PAT_ENC_EN = 2 'b11, the local pattern generator is still enabled internally for comparison with incoming video stream When PAT_ENC_EN = 2 'b11, the local pattern generator 's patterns are forwarded, not the incoming video stream When PATGEN_LEGACY_ENB = 1, PAT_ENC_EN[1]: 1: Enable pattern checker 0: Disable pattern checker PAT_ENC_EN[0]: 1: Enable pattern generator 0: Disable pattern generator Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]

7.6.2.7.89 FPD4_PGCFG_VP1 Register (Address = 0x69) [Default = 0x08]

FPD4_PGCFG_VP1 is shown in Table 7-426.

Return to the Summary Table.

Table 7-426. FPD4_PGCFG_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

Table 7-426. FPD4_PGCFG_VP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

7.6.2.7.90 FPD4_PGIA_VP1 Register (Address = 0x6A) [Default = 0x00]

FPD4_PGIA_VP1 is shown in Table 7-427.

Return to the Summary Table.

Table 7-427. FPD4_PGIA_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

7.6.2.7.91 FPD4_PGID_VP1 Register (Address = 0x6B) [Default = 0x00]

FPD4_PGID_VP1 is shown in Table 7-428.

Return to the Summary Table.

Table 7-428. FPD4_PGID_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

7.6.2.7.92 FPD4_PGDBG_VP1 Register (Address = 0x6C) [Default = 0x00]

FPD4_PGDBG_VP1 is shown in Table 7-429.

Return to the Summary Table.

Table 7-429. FPD4_PGDBG_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN_RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	RH/W1S	0x0	Reserved

7.6.2.7.93 FPD4_PGTSTDAT_VP1 Register (Address = 0x6D) [Default = 0x00]

FPD4_PGTSTDAT_VP1 is shown in Table 7-430.

Return to the Summary Table.

Table 7-430. FPD4_PGTSTDAT_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	RESERVED	R	0x0	Reserved

7.6.2.7.94 VP_STS_VP1 Register (Address = 0x70) [Default = 0x00]

VP_STS_VP1 is shown in Table 7-431.

Return to the Summary Table.

Video Processor Status Register

Table 7-431. VP_STS_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

7.6.2.7.95 INTR_STS_VP_VP1 Register (Address = 0x71) [Default = 0x00]

INTR_STS_VP_VP1 is shown in Table 7-432.

Return to the Summary Table.

Video Interrupt Status Register
The bits in this register will be set on occurrence of the associated event. If the corresponding interrupt mask register is set, an Interrupt will be generated for the event. The interrupt status bits will be cleared on a read of this register.

Table 7-432. INTR_STS_VP_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR		0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR		0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.

Table 7-432. INTR_STS_VP_VP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	IS_TIMING_DATA_ERR		0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR		0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR		0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR		0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

7.6.2.7.96 INTR_CTL_VP_VP1 Register (Address = 0x73) [Default = 0x00]

INTR_CTL_VP_VP1 is shown in Table 7-433.

Return to the Summary Table.

Video Interrupt Control Register
The bits in this register enable interrupts for the associated bits in the Interrupt Status register.

Table 7-433. INTR_CTL_VP_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

7.6.2.7.97 MEAS_H_TOTAL0_VP1 Register (Address = 0x75) [Default = 0x00]

MEAS_H_TOTAL0_VP1 is shown in Table 7-434.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-434. MEAS_H_TOTAL0_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.98 MEAS_H_TOTAL1_VP1 Register (Address = 0x76) [Default = 0x00]

MEAS_H_TOTAL1_VP1 is shown in Table 7-435.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-435. MEAS_H_TOTAL1_VP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.99 VID_PROC_CTL_VP2 Register (Address = 0x80) [Default = 0x00]

VID_PROC_CTL_VP2 is shown in Table 7-436.

Return to the Summary Table.

Video Processor Control Register

Table 7-436. VID_PROC_CTL_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.

Table 7-436. VID_PROC_CTL_VP2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition,Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

7.6.2.7.100 VID_PROC_CFG_VP2 Register (Address = 0x81) [Default = 0xAA]

VID_PROC_CFG_VP2 is shown in Table 7-437.

Return to the Summary Table.

Video Processor Configuration Register

Table 7-437. VID_PROC_CFG_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1: Ignore Line Number 0: Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra horizontal lines of blanking while waiting
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x2	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor. Note: The DP Receiver only provides two streams, so only settings of 0 and 1 are valid.

7.6.2.7.101 DP_H_ACTIVE0_VP2 Register (Address = 0x82) [Default = 0x00]

DP_H_ACTIVE0_VP2 is shown in Table 7-438.

Return to the Summary Table.

Table 7-438. DP_H_ACTIVE0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[7:0]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.102 DP_H_ACTIVE1_VP2 Register (Address = 0x83) [Default = 0x00]

DP_H_ACTIVE1_VP2 is shown in Table 7-439.

Return to the Summary Table.

Table 7-439. DP_H_ACTIVE1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[15:8]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.103 VFILTER_A_VP2 Register (Address = 0x86) [Default = 0x01]

VFILTER_A_VP2 is shown in Table 7-440.

Return to the Summary Table.

Vertical Filter A Register

Table 7-440. VFILTER_A_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A = 1 and VFILTER_N =2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

7.6.2.7.104 VFILTER_N_VP2 Register (Address = 0x87) [Default = 0x01]

VFILTER_N_VP2 is shown in Table 7-441.

Return to the Summary Table.

Vertical Filter B Register

Table 7-441. VFILTER_N_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

7.6.2.7.105 CROP_START_X0_VP2 Register (Address = 0x88) [Default = 0x00]

CROP_START_X0_VP2 is shown in Table 7-442.

Return to the Summary Table.

Crop Start X1 Register

Table 7-442. CROP_START_X0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.106 CROP_START_X1_VP2 Register (Address = 0x89) [Default = 0x00]

CROP_START_X1_VP2 is shown in Table 7-443.

Return to the Summary Table.

Crop Start X1 Register

Table 7-443. CROP_START_X1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.107 CROP_START_Y0_VP2 Register (Address = 0x8A) [Default = 0x00]

CROP_START_Y0_VP2 is shown in Table 7-444.

Return to the Summary Table.

Crop Start Y0 Register

Table 7-444. CROP_START_Y0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.108 CROP_START_Y1_VP2 Register (Address = 0x8B) [Default = 0x00]

CROP_START_Y1_VP2 is shown in Table 7-445.

Return to the Summary Table.

Crop Start Y1 Register

Table 7-445. CROP_START_Y1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.109 CROP_STOP_X0_VP2 Register (Address = 0x8C) [Default = 0x00]

CROP_STOP_X0_VP2 is shown in Table 7-446.

Return to the Summary Table.

Crop Stop X0 Register

Table 7-446. CROP_STOP_X0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.110 CROP_STOP_X1_VP2 Register (Address = 0x8D) [Default = 0x00]

CROP_STOP_X1_VP2 is shown in Table 7-447.

Return to the Summary Table.

Crop Stop X1 Register

Table 7-447. CROP_STOP_X1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.111 CROP_STOP_Y0_VP2 Register (Address = 0x8E) [Default = 0x00]

CROP_STOP_Y0_VP2 is shown in Table 7-448.

Return to the Summary Table.

Crop Stop Y0 Register

Table 7-448. CROP_STOP_Y0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.112 CROP_STOP_Y1_VP2 Register (Address = 0x8F) [Default = 0x00]

CROP_STOP_Y1_VP2 is shown in Table 7-449.

Return to the Summary Table.

Crop Stop Y1 Register

Table 7-449. CROP_STOP_Y1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.113 VID_H_ACTIVE0_VP2 Register (Address = 0x90) [Default = 0x00]

VID_H_ACTIVE0_VP2 is shown in Table 7-450.

Return to the Summary Table.

Table 7-450. VID_H_ACTIVE0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.114 VID_H_ACTIVE1_VP2 Register (Address = 0x91) [Default = 0x00]

VID_H_ACTIVE1_VP2 is shown in Table 7-451.

Return to the Summary Table.

Table 7-451. VID_H_ACTIVE1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.115 VID_H_BACK0_VP2 Register (Address = 0x92) [Default = 0x00]

VID_H_BACK0_VP2 is shown in Table 7-452.

Return to the Summary Table.

Table 7-452. VID_H_BACK0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.116 VID_H_BACK1_VP2 Register (Address = 0x93) [Default = 0x00]

VID_H_BACK1_VP2 is shown in Table 7-453.

Return to the Summary Table.

Table 7-453. VID_H_BACK1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.117 VID_H_WIDTH0_VP2 Register (Address = 0x94) [Default = 0x00]

VID_H_WIDTH0_VP2 is shown in Table 7-454.

Return to the Summary Table.

Table 7-454. VID_H_WIDTH0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.118 VID_H_WIDTH1_VP2 Register (Address = 0x95) [Default = 0x00]

VID_H_WIDTH1_VP2 is shown in Table 7-455.

Return to the Summary Table.

Table 7-455. VID_H_WIDTH1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.119 VID_H_TOTAL0_VP2 Register (Address = 0x96) [Default = 0x00]

VID_H_TOTAL0_VP2 is shown in Table 7-456.

Return to the Summary Table.

Table 7-456. VID_H_TOTAL0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.120 VID_H_TOTAL1_VP2 Register (Address = 0x97) [Default = 0x00]

VID_H_TOTAL1_VP2 is shown in Table 7-457.

Return to the Summary Table.

Table 7-457. VID_H_TOTAL1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.121 VID_V_ACTIVE0_VP2 Register (Address = 0x98) [Default = 0x00]

VID_V_ACTIVE0_VP2 is shown in Table 7-458.

Return to the Summary Table.

Table 7-458. VID_V_ACTIVE0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.122 VID_V_ACTIVE1_VP2 Register (Address = 0x99) [Default = 0x00]

VID_V_ACTIVE1_VP2 is shown in Table 7-459.

Return to the Summary Table.

Table 7-459. VID_V_ACTIVE1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.123 VID_V_BACK0_VP2 Register (Address = 0x9A) [Default = 0x00]

VID_V_BACK0_VP2 is shown in Table 7-460.

Return to the Summary Table.

Table 7-460. VID_V_BACK0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.124 VID_V_BACK1_VP2 Register (Address = 0x9B) [Default = 0x00]

VID_V_BACK1_VP2 is shown in Table 7-461.

Return to the Summary Table.

Table 7-461. VID_V_BACK1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.125 VID_V_WIDTH0_VP2 Register (Address = 0x9C) [Default = 0x00]

VID_V_WIDTH0_VP2 is shown in Table 7-462.

Return to the Summary Table.

Table 7-462. VID_V_WIDTH0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.126 VID_V_WIDTH1_VP2 Register (Address = 0x9D) [Default = 0x00]

VID_V_WIDTH1_VP2 is shown in Table 7-463.

Return to the Summary Table.

Table 7-463. VID_V_WIDTH1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.127 VID_V_FRONT0_VP2 Register (Address = 0x9E) [Default = 0x00]

VID_V_FRONT0_VP2 is shown in Table 7-464.

Return to the Summary Table.

Table 7-464. VID_V_FRONT0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.128 VID_V_FRONT1_VP2 Register (Address = 0x9F) [Default = 0x00]

VID_V_FRONT1_VP2 is shown in Table 7-465.

Return to the Summary Table.

Table 7-465. VID_V_FRONT1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.129 GEN_LATE_THRESH_VP2 Register (Address = 0xA0) [Default = 0x00]

GEN_LATE_THRESH_VP2 is shown in Table 7-466.

Return to the Summary Table.

Table 7-466. GEN_LATE_THRESH_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.130 GEN_EARLY_THRESH_VP2 Register (Address = 0xA1) [Default = 0x00]

GEN_EARLY_THRESH_VP2 is shown in Table 7-467.

Return to the Summary Table.

Table 7-467. GEN_EARLY_THRESH_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.131 GEN_START_DELAY_VP2 Register (Address = 0xA2) [Default = 0x10]

GEN_START_DELAY_VP2 is shown in Table 7-468.

Return to the Summary Table.

Table 7-468. GEN_START_DELAY_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

7.6.2.7.132 PCLK_GEN_M_0_VP2 Register (Address = 0xA3) [Default = 0x00]

PCLK_GEN_M_0_VP2 is shown in Table 7-469.

Return to the Summary Table.

Table 7-469. PCLK_GEN_M_0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0} Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.133 PCLK_GEN_M_1_VP2 Register (Address = 0xA4) [Default = 0x10]

PCLK_GEN_M_1_VP2 is shown in Table 7-470.

Return to the Summary Table.

Table 7-470. PCLK_GEN_M_1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.134 PCLK_GEN_N_VP2 Register (Address = 0xA5) [Default = 0x0F]

PCLK_GEN_N_VP2 is shown in Table 7-471.

Return to the Summary Table.

Table 7-471. PCLK_GEN_N_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{PCLK\_GEN\_M}$. The default setting for this register chooses an N value of 2^{15} or 32,768.

7.6.2.7.135 MAX_M_ADJUST_VP2 Register (Address = 0xA6) [Default = 0x08]

MAX_M_ADJUST_VP2 is shown in Table 7-472.

Return to the Summary Table.

Table 7-472. MAX_M_ADJUST_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

7.6.2.7.136 VID_PROC_CFG2_VP2 Register (Address = 0xA7) [Default = 0x00]

VID_PROC_CFG2_VP2 is shown in Table 7-473.

Return to the Summary Table.

Video Processor Configuration Register 2

Table 7-473. VID_PROC_CFG2_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (meaasured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

Table 7-473. VID_PROC_CFG2_VP2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

7.6.2.7.137 FPD4_PGCTL_VP2 Register (Address = 0xA8) [Default = 0x08]

FPD4_PGCTL_VP2 is shown in Table 7-474.

Return to the Summary Table.

Table 7-474. FPD4_PGCTL_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: Checkerboard (White/Black) 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom/Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

Table 7-474. FPD4_PGCTL_VP2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	When PATGEN_LEGACY_ENB = 0, Pattern generator, pattern checker and forwarding enable encoding: 00: Disable pattern generator and pattern checker 01: Enable pattern generator 10: Enable pattern checker, do not forward patterns on to the RX datapath 11: Enable pattern checker, forward patterns on to the RX datapath When PAT_ENC_EN = 2 'b10 or PAT_ENC_EN = 2 'b11, the local pattern generator is still enabled internally for comparison with incoming video stream When PAT_ENC_EN = 2 'b11, the local pattern generator 's patterns are forwarded, not the incoming video stream When PATGEN_LEGACY_ENB = 1, PAT_ENC_EN[1]: 1: Enable pattern checker 0: Disable pattern checker PAT_ENC_EN[0]: 1: Enable pattern generator 0: Disable pattern generator Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]

7.6.2.7.138 FPD4_PGCFG_VP2 Register (Address = 0xA9) [Default = 0x08]

FPD4_PGCFG_VP2 is shown in Table 7-475.

Return to the Summary Table.

Table 7-475. FPD4_PGCFG_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

Table 7-475. FPD4_PGCFG_VP2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

7.6.2.7.139 FPD4_PGIA_VP2 Register (Address = 0xAA) [Default = 0x00]

FPD4_PGIA_VP2 is shown in Table 7-476.

Return to the Summary Table.

Table 7-476. FPD4_PGIA_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

7.6.2.7.140 FPD4_PGID_VP2 Register (Address = 0xAB) [Default = 0x00]

FPD4_PGID_VP2 is shown in Table 7-477.

Return to the Summary Table.

Table 7-477. FPD4_PGID_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

7.6.2.7.141 FPD4_PGDBG_VP2 Register (Address = 0xAC) [Default = 0x00]

FPD4_PGDBG_VP2 is shown in Table 7-478.

Return to the Summary Table.

Table 7-478. FPD4_PGDBG_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN_RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	RH/W1S	0x0	Reserved

7.6.2.7.142 FPD4_PGTSTDAT_VP2 Register (Address = 0xAD) [Default = 0x00]

FPD4_PGTSTDAT_VP2 is shown in Table 7-479.

Return to the Summary Table.

Table 7-479. FPD4_PGTSTDAT_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	PATGEN_TST_DATA	R	0x0	Test Data: This field contains the Debug Monitor output. See the Debug Monitor section of the Pattern Generator DDS for details.

7.6.2.7.143 VP_STS_VP2 Register (Address = 0xB0) [Default = 0x00]

VP_STS_VP2 is shown in Table 7-480.

Return to the Summary Table.

Video Processor Status Register

Table 7-480. VP_STS_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

7.6.2.7.144 INTR_STS_VP_VP2 Register (Address = 0xB1) [Default = 0x00]

INTR_STS_VP_VP2 is shown in Table 7-481.

Return to the Summary Table.

Video Interrupt Status Register
The bits in this register will be set on occurrence of the associated event. If the corresponding interrupt mask register is set, an Interrupt will be generated for the event. The interrupt status bits will be cleared on a read of this register.

Table 7-481. INTR_STS_VP_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR		0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR		0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.

Table 7-481. INTR_STS_VP_VP2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	IS_TIMING_DATA_ERR		0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR		0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR		0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR		0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

7.6.2.7.145 INTR_CTL_VP_VP2 Register (Address = 0xB3) [Default = 0x00]

INTR_CTL_VP_VP2 is shown in Table 7-482.

Return to the Summary Table.

Video Interrupt Control Register
The bits in this register enable interrupts for the associated bits in the Interrupt Status register.

Table 7-482. INTR_CTL_VP_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

7.6.2.7.146 MEAS_H_TOTAL0_VP2 Register (Address = 0xB5) [Default = 0x00]

MEAS_H_TOTAL0_VP2 is shown in Table 7-483.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-483. MEAS_H_TOTAL0_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.147 MEAS_H_TOTAL1_VP2 Register (Address = 0xB6) [Default = 0x00]

MEAS_H_TOTAL1_VP2 is shown in Table 7-484.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-484. MEAS_H_TOTAL1_VP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.148 VID_PROC_CTL_VP3 Register (Address = 0xC0) [Default = 0x00]

VID_PROC_CTL_VP3 is shown in Table 7-485.

Return to the Summary Table.

Video Processor Control Register

Table 7-485. VID_PROC_CTL_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.

Table 7-485. VID_PROC_CTL_VP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition,Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

7.6.2.7.149 VID_PROC_CFG_VP3 Register (Address = 0xC1) [Default = 0xAB]

VID_PROC_CFG_VP3 is shown in Table 7-486.

Return to the Summary Table.

Video Processor Configuration Register

Table 7-486. VID_PROC_CFG_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1: Ignore Line Number 0: Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra horizontal lines of blanking while waiting
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x3	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor. Note: The DP Receiver only provides two streams, so only settings of 0 and 1 are valid.

7.6.2.7.150 DP_H_ACTIVE0_VP3 Register (Address = 0xC2) [Default = 0x00]

DP_H_ACTIVE0_VP3 is shown in Table 7-487.

Return to the Summary Table.

Table 7-487. DP_H_ACTIVE0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[7:0]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.151 DP_H_ACTIVE1_VP3 Register (Address = 0xC3) [Default = 0x00]

DP_H_ACTIVE1_VP3 is shown in Table 7-488.

Return to the Summary Table.

Table 7-488. DP_H_ACTIVE1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_H_ACTIVE[15:8]	R/W	0x0	DisplayPort video Horizontal Active period This value should be programmed to match the DisplayPort horizontal active video parameter in pixels

7.6.2.7.152 VFILTER_A_VP3 Register (Address = 0xC6) [Default = 0x01]

VFILTER_A_VP3 is shown in Table 7-489.

Return to the Summary Table.

Vertical Filter A Register

Table 7-489. VFILTER_A_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A = 1 and VFILTER_N =2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

7.6.2.7.153 VFILTER_N_VP3 Register (Address = 0xC7) [Default = 0x01]

VFILTER_N_VP3 is shown in Table 7-490.

Return to the Summary Table.

Vertical Filter B Register

Table 7-490. VFILTER_N_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

7.6.2.7.154 CROP_START_X0_VP3 Register (Address = 0xC8) [Default = 0x00]

CROP_START_X0_VP3 is shown in Table 7-491.

Return to the Summary Table.

Crop Start X1 Register

Table 7-491. CROP_START_X0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.155 CROP_START_X1_VP3 Register (Address = 0xC9) [Default = 0x00]

CROP_START_X1_VP3 is shown in Table 7-492.

Return to the Summary Table.

Crop Start X1 Register

Table 7-492. CROP_START_X1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.156 CROP_START_Y0_VP3 Register (Address = 0xCA) [Default = 0x00]

CROP_START_Y0_VP3 is shown in Table 7-493.

Return to the Summary Table.

Crop Start Y0 Register

Table 7-493. CROP_START_Y0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.157 CROP_START_Y1_VP3 Register (Address = 0xCB) [Default = 0x00]

CROP_START_Y1_VP3 is shown in Table 7-494.

Return to the Summary Table.

Crop Start Y1 Register

Table 7-494. CROP_START_Y1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.158 CROP_STOP_X0_VP3 Register (Address = 0xCC) [Default = 0x00]

CROP_STOP_X0_VP3 is shown in Table 7-495.

Return to the Summary Table.

Crop Stop X0 Register

Table 7-495. CROP_STOP_X0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.159 CROP_STOP_X1_VP3 Register (Address = 0xCD) [Default = 0x00]

CROP_STOP_X1_VP3 is shown in Table 7-496.

Return to the Summary Table.

Crop Stop X1 Register

Table 7-496. CROP_STOP_X1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

7.6.2.7.160 CROP_STOP_Y0_VP3 Register (Address = 0xCE) [Default = 0x00]

CROP_STOP_Y0_VP3 is shown in Table 7-497.

Return to the Summary Table.

Crop Stop Y0 Register

Table 7-497. CROP_STOP_Y0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.161 CROP_STOP_Y1_VP3 Register (Address = 0xCF) [Default = 0x00]

CROP_STOP_Y1_VP3 is shown in Table 7-498.

Return to the Summary Table.

Crop Stop Y1 Register

Table 7-498. CROP_STOP_Y1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

7.6.2.7.162 VID_H_ACTIVE0_VP3 Register (Address = 0xD0) [Default = 0x00]

VID_H_ACTIVE0_VP3 is shown in Table 7-499.

Return to the Summary Table.

Table 7-499. VID_H_ACTIVE0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.163 VID_H_ACTIVE1_VP3 Register (Address = 0xD1) [Default = 0x00]

VID_H_ACTIVE1_VP3 is shown in Table 7-500.

Return to the Summary Table.

Table 7-500. VID_H_ACTIVE1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

7.6.2.7.164 VID_H_BACK0_VP3 Register (Address = 0xD2) [Default = 0x00]

VID_H_BACK0_VP3 is shown in Table 7-501.

Return to the Summary Table.

Table 7-501. VID_H_BACK0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.165 VID_H_BACK1_VP3 Register (Address = 0xD3) [Default = 0x00]

VID_H_BACK1_VP3 is shown in Table 7-502.

Return to the Summary Table.

Table 7-502. VID_H_BACK1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

7.6.2.7.166 VID_H_WIDTH0_VP3 Register (Address = 0xD4) [Default = 0x00]

VID_H_WIDTH0_VP3 is shown in Table 7-503.

Return to the Summary Table.

Table 7-503. VID_H_WIDTH0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.167 VID_H_WIDTH1_VP3 Register (Address = 0xD5) [Default = 0x00]

VID_H_WIDTH1_VP3 is shown in Table 7-504.

Return to the Summary Table.

Table 7-504. VID_H_WIDTH1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

7.6.2.7.168 VID_H_TOTAL0_VP3 Register (Address = 0xD6) [Default = 0x00]

VID_H_TOTAL0_VP3 is shown in Table 7-505.

Return to the Summary Table.

Table 7-505. VID_H_TOTAL0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.169 VID_H_TOTAL1_VP3 Register (Address = 0xD7) [Default = 0x00]

VID_H_TOTAL1_VP3 is shown in Table 7-506.

Return to the Summary Table.

Table 7-506. VID_H_TOTAL1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead.

7.6.2.7.170 VID_V_ACTIVE0_VP3 Register (Address = 0xD8) [Default = 0x00]

VID_V_ACTIVE0_VP3 is shown in Table 7-507.

Return to the Summary Table.

Table 7-507. VID_V_ACTIVE0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.171 VID_V_ACTIVE1_VP3 Register (Address = 0xD9) [Default = 0x00]

VID_V_ACTIVE1_VP3 is shown in Table 7-508.

Return to the Summary Table.

Table 7-508. VID_V_ACTIVE1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

7.6.2.7.172 VID_V_BACK0_VP3 Register (Address = 0xDA) [Default = 0x00]

VID_V_BACK0_VP3 is shown in Table 7-509.

Return to the Summary Table.

Table 7-509. VID_V_BACK0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.173 VID_V_BACK1_VP3 Register (Address = 0xDB) [Default = 0x00]

VID_V_BACK1_VP3 is shown in Table 7-510.

Return to the Summary Table.

Table 7-510. VID_V_BACK1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

7.6.2.7.174 VID_V_WIDTH0_VP3 Register (Address = 0xDC) [Default = 0x00]

VID_V_WIDTH0_VP3 is shown in Table 7-511.

Return to the Summary Table.

Table 7-511. VID_V_WIDTH0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.175 VID_V_WIDTH1_VP3 Register (Address = 0xDD) [Default = 0x00]

VID_V_WIDTH1_VP3 is shown in Table 7-512.

Return to the Summary Table.

Table 7-512. VID_V_WIDTH1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

7.6.2.7.176 VID_V_FRONT0_VP3 Register (Address = 0xDE) [Default = 0x00]

VID_V_FRONT0_VP3 is shown in Table 7-513.

Return to the Summary Table.

Table 7-513. VID_V_FRONT0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.177 VID_V_FRONT1_VP3 Register (Address = 0xDF) [Default = 0x00]

VID_V_FRONT1_VP3 is shown in Table 7-514.

Return to the Summary Table.

Table 7-514. VID_V_FRONT1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

7.6.2.7.178 GEN_LATE_THRESH_VP3 Register (Address = 0xE0) [Default = 0x00]

GEN_LATE_THRESH_VP3 is shown in Table 7-515.

Return to the Summary Table.

Table 7-515. GEN_LATE_THRESH_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.179 GEN_EARLY_THRESH_VP3 Register (Address = 0xE1) [Default = 0x00]

GEN_EARLY_THRESH_VP3 is shown in Table 7-516.

Return to the Summary Table.

Table 7-516. GEN_EARLY_THRESH_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

7.6.2.7.180 GEN_START_DELAY_VP3 Register (Address = 0xE2) [Default = 0x10]

GEN_START_DELAY_VP3 is shown in Table 7-517.

Return to the Summary Table.

Table 7-517. GEN_START_DELAY_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

7.6.2.7.181 PCLK_GEN_M_0_VP3 Register (Address = 0xE3) [Default = 0x00]

PCLK_GEN_M_0_VP3 is shown in Table 7-518.

Return to the Summary Table.

Table 7-518. PCLK_GEN_M_0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0} Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.182 PCLK_GEN_M_1_VP3 Register (Address = 0xE4) [Default = 0x10]

PCLK_GEN_M_1_VP3 is shown in Table 7-519.

Return to the Summary Table.

Table 7-519. PCLK_GEN_M_1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

7.6.2.7.183 PCLK_GEN_N_VP3 Register (Address = 0xE5) [Default = 0x0F]

PCLK_GEN_N_VP3 is shown in Table 7-520.

Return to the Summary Table.

Table 7-520. PCLK_GEN_N_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{PCLK\_GEN\_M}$. The default setting for this register chooses an N value of 2^{15} or 32,768.

7.6.2.7.184 MAX_M_ADJUST_VP3 Register (Address = 0xE6) [Default = 0x08]

MAX_M_ADJUST_VP3 is shown in Table 7-521.

Return to the Summary Table.

Table 7-521. MAX_M_ADJUST_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

7.6.2.7.185 VID_PROC_CFG2_VP3 Register (Address = 0xE7) [Default = 0x00]

VID_PROC_CFG2_VP3 is shown in Table 7-522.

Return to the Summary Table.

Video Processor Configuration Register 2

Table 7-522. VID_PROC_CFG2_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (meaasured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is slected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

Table 7-522. VID_PROC_CFG2_VP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

7.6.2.7.186 FPD4_PGCTL_VP3 Register (Address = 0xE8) [Default = 0x08]

FPD4_PGCTL_VP3 is shown in Table 7-523.

Return to the Summary Table.

Table 7-523. FPD4_PGCTL_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: Checkerboard (White/Black) 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom/Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

Table 7-523. FPD4_PGCTL_VP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	When PATGEN_LEGACY_ENB = 0, Pattern generator, pattern checker and forwarding enable encoding: 00: Disable pattern generator and pattern checker 01: Enable pattern generator 10: Enable pattern checker, do not forward patterns on to the RX datapath 11: Enable pattern checker, forward patterns on to the RX datapath When PAT_ENC_EN = 2 'b10 or PAT_ENC_EN = 2 'b11, the local pattern generator is still enabled internally for comparison with incoming video stream When PAT_ENC_EN = 2 'b11, the local pattern generator 's patterns are forwarded, not the incoming video stream When PATGEN_LEGACY_ENB = 1, PAT_ENC_EN[1]: 1: Enable pattern checker 0: Disable pattern checker PAT_ENC_EN[0]: 1: Enable pattern generator 0: Disable pattern generator Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]

7.6.2.7.187 FPD4_PGCFG_VP3 Register (Address = 0xE9) [Default = 0x08]

FPD4_PGCFG_VP3 is shown in Table 7-524.

Return to the Summary Table.

Table 7-524. FPD4_PGCFG_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

Table 7-524. FPD4_PGCFG_VP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

7.6.2.7.188 FPD4_PGIA_VP3 Register (Address = 0xEA) [Default = 0x00]

FPD4_PGIA_VP3 is shown in Table 7-525.

Return to the Summary Table.

Table 7-525. FPD4_PGIA_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

7.6.2.7.189 FPD4_PGID_VP3 Register (Address = 0xEB) [Default = 0x00]

FPD4_PGID_VP3 is shown in Table 7-526.

Return to the Summary Table.

Table 7-526. FPD4_PGID_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

7.6.2.7.190 FPD4_PGDBG_VP3 Register (Address = 0xEC) [Default = 0x00]

FPD4_PGDBG_VP3 is shown in Table 7-527.

Return to the Summary Table.

Table 7-527. FPD4_PGDBG_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	PATGEN_DBG_SEL	R/W	0x0	Test Mux Select: This field selects the signals to be brought out on the test output bus as well as read in the PGTSTDAT register. See the Debug Monitor section of the Pattern Generator DDS for details.
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN_RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.

Table 7-527. FPD4_PGDBG_VP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	RH/W1S	0x0	Reserved

7.6.2.7.191 FPD4_PGTSTDAT_VP3 Register (Address = 0xED) [Default = 0x00]

FPD4_PGTSTDAT_VP3 is shown in Table 7-528.

Return to the Summary Table.

Table 7-528. FPD4_PGTSTDAT_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	RESERVED	R	0x0	Reserved

7.6.2.7.192 VP_STS_VP3 Register (Address = 0xF0) [Default = 0x00]

VP_STS_VP3 is shown in Table 7-529.

Return to the Summary Table.

Video Processor Status Register

Table 7-529. VP_STS_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

7.6.2.7.193 INTR_STS_VP_VP3 Register (Address = 0xF1) [Default = 0x00]

INTR_STS_VP_VP3 is shown in Table 7-530.

Return to the Summary Table.

Video Interrupt Status Register
The bits in this register will be set on occurrence of the associated event. If the corresponding interrupt mask register is set, an Interrupt will be generated for the event. The interrupt status bits will be cleared on a read of this register.

Table 7-530. INTR_STS_VP_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

Table 7-530. INTR_STS_VP_VP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	IS_CROP_VERT_ERR		0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR		0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.
4	IS_TIMING_DATA_ERR		0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR		0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR		0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR		0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE		0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

7.6.2.7.194 INTR_CTL_VP_VP3 Register (Address = 0xF3) [Default = 0x00]

INTR_CTL_VP_VP3 is shown in Table 7-531.

Return to the Summary Table.

Video Interrupt Control Register
The bits in this register enable interrupts for the associated bits in the Interrupt Status register.

Table 7-531. INTR_CTL_VP_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

7.6.2.7.195 MEAS_H_TOTAL0_VP3 Register (Address = 0xF5) [Default = 0x00]

MEAS_H_TOTAL0_VP3 is shown in Table 7-532.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-532. MEAS_H_TOTAL0_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.7.196 MEAS_H_TOTAL1_VP3 Register (Address = 0xF6) [Default = 0x00]

MEAS_H_TOTAL1_VP3 is shown in Table 7-533.

Return to the Summary Table.

Video Processor total horizontal period measure

Table 7-533. MEAS_H_TOTAL1_VP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

7.6.2.8 Page 14: SAR ADC Registers

Table 7-534 lists the memory-mapped registers for the Page 14: SAR ADC registers. All register offset addresses not listed in Table 7-534 should be considered as reserved locations and the register contents should not be modified.

Table 7-534. PAGE 14: SAR ADC Registers

Address	Acronym	Register Name	Section
0x4	ADC_CLK_DIV_SEL	ADC_CLK_DIV_SEL	Go
0x7	ADC_INPUT_EN_LSB	ADC_INPUT_EN_LSB	Go
0x8	SAR_ADC_INPUT_EN_MSB	SAR_ADC_INPUT_EN_MSB	Go
0xD	ADC_MODE	ADC_MODE	Go
0xF	ADC_SRC_CNTR_0	ADC_SRC_CNTR_0	Go
0x10	ADC_SRC_CNTR_1	ADC_SRC_CNTR_1	Go
0x11	ADC_SRC_CNTR_2	ADC_SRC_CNTR_2	Go
0x12	ADC_SRC_CNTR_3	ADC_SRC_CNTR_3	Go
0x13	TEMP_FINAL	TEMP_FINAL	Go
0x15	IV0_FINAL	IV0_FINAL	Go
0x16	IV1_FINAL	IV1_FINAL	Go
0x17	IV2_FINAL	IV2_FINAL	Go
0x18	IV3_FINAL	IV3_FINAL	Go
0x1B	EXT_VOL0_FINAL	EXT_VOL0_FINAL	Go
0x1C	EXT_VOL1_FINAL	EXT_VOL1_FINAL	Go
0x1D	LINE_FAULT0_FINAL	LINE_FAULT0_FINAL	Go
0x1E	LINE_FAULT1_FINAL	LINE_FAULT1_FINAL	Go
0x1F	LINE_FAULT2_FINAL	LINE_FAULT2_FINAL	Go
0x20	LINE_FAULT3_FINAL	LINE_FAULT3_FINAL	Go
0x23	INT_STATUS_LSB_LOW	INT_STATUS_LSB_LOW	Go
0x24	INT_STATUS_MSB_LOW	INT_STATUS_MSB_LOW	Go
0x25	INT_STATUS_LSB_HIGH	INT_STATUS_LSB_HIGH	Go
0x26	INT_STATUS_MSB_HIGH	INT_STATUS_MSB_HIGH	Go
0x27	INT_LINE_FAULT0_M0	INT_LINE_FAULT0_M0	Go
0x28	INT_LINE_FAULT1_M0	INT_LINE_FAULT1_M0	Go
0x29	INT_LINE_FAULT2_M0	INT_LINE_FAULT2_M0	Go
0x2A	INT_LINE_FAULT3_M0	INT_LINE_FAULT3_M0	Go
0x2B	INT_LINE_FAULT0_M1	INT_LINE_FAULT0_M1	Go
0x2C	INT_LINE_FAULT1_M1	INT_LINE_FAULT1_M1	Go
0x2D	INT_LINE_FAULT2_M1	INT_LINE_FAULT2_M1	Go
0x2E	INT_LINE_FAULT3_M1	INT_LINE_FAULT3_M1	Go
0x2F	INT_LINE_FAULT_UNDEF	INT_LINE_FAULT_UNDEF	Go
0x30	INT_LINE_FAULT_SATURATE	INT_LINE_FAULT_SATURATE	Go
0x33	TEMP_HIGH	TEMP_HIGH	Go
0x34	TEMP_LOW	TEMP_LOW	Go
0x35	TEMP_ADC_OFFSET	TEMP_ADC_OFFSET	Go
0x39	IV0_HIGH	IV0_HIGH	Go
0x3A	IV0_LOW	IV0_LOW	Go
0x3B	IV0_ADC_OFFSET	IV0_ADC_OFFSET	Go
0x3C	IV1_HIGH	IV1_HIGH	Go
0x3D	IV1_LOW	IV1_LOW	Go

Table 7-534. PAGE 14: SAR ADC Registers (continued)

Address	Acronym	Register Name	Section
0x3E	IV1_ADC_OFFSET	IV1_ADC_OFFSET	Go
0x3F	IV2_HIGH	IV2_HIGH	Go
0x40	IV2_LOW	IV2_LOW	Go
0x41	IV2_ADC_OFFSET	IV2_ADC_OFFSET	Go
0x42	IV3_HIGH	IV3_HIGH	Go
0x43	IV3_LOW	IV3_LOW	Go
0x44	IV3_ADC_OFFSET	IV3_ADC_OFFSET	Go
0x4B	TEMP_IV_MASK	TEMP_IV_MASK	Go
0x4C	EXT_VOL0_HIGH	EXT_VOL0_HIGH	Go
0x4D	EXT_VOL0_LOW	EXT_VOL0_LOW	Go
0x4E	EXT_VOL0_ADC_OFFSET	EXT_VOL0_ADC_OFFSET	Go
0x4F	EXT_VOL1_HIGH	EXT_VOL1_HIGH	Go
0x50	EXT_VOL1_LOW	EXT_VOL1_LOW	Go
0x51	EXT_VOL1_ADC_OFFSET	EXT_VOL1_ADC_OFFSET	Go
0x52	EXT_VOL_MASK	EXT_VOL_MASK	Go
0x53	LINE_FAULT0_THRESH_0_HI_M0	LINE_FAULT0_THRESH_0_HI_M0	Go
0x54	LINE_FAULT0_THRESH_0_LO_M0	LINE_FAULT0_THRESH_0_LO_M0	Go
0x55	LINE_FAULT0_THRESH_1_HI_M0	LINE_FAULT0_THRESH_1_HI_M0	Go
0x56	LINE_FAULT0_THRESH_1_LO_M0	LINE_FAULT0_THRESH_1_LO_M0	Go
0x57	LINE_FAULT0_THRESH_2_HI_M0	LINE_FAULT0_THRESH_2_HI_M0	Go
0x58	LINE_FAULT0_THRESH_2_LO_M0	LINE_FAULT0_THRESH_2_LO_M0	Go
0x59	LINE_FAULT0_THRESH_3_HI_M0	LINE_FAULT0_THRESH_3_HI_M0	Go
0x5A	LINE_FAULT0_THRESH_3_LO_M0	LINE_FAULT0_THRESH_3_LO_M0	Go
0x5B	LINE_FAULT0_THRESH_4_HI_M0	LINE_FAULT0_THRESH_4_HI_M0	Go
0x5C	LINE_FAULT0_THRESH_4_LO_M0	LINE_FAULT0_THRESH_4_LO_M0	Go
0x5D	LINE_FAULT0_THRESH_5_HI_M0	LINE_FAULT0_THRESH_5_HI_M0	Go
0x5E	LINE_FAULT0_THRESH_5_LO_M0	LINE_FAULT0_THRESH_5_LO_M0	Go
0x5F	LINE_FAULT0_THRESH_6_HI_M0	LINE_FAULT0_THRESH_6_HI_M0	Go
0x60	LINE_FAULT0_THRESH_6_LO_M0	LINE_FAULT0_THRESH_6_LO_M0	Go
0x61	LINE_FAULT0_THRESH_7_HI_M0	LINE_FAULT0_THRESH_7_HI_M0	Go
0x62	LINE_FAULT0_THRESH_7_LO_M0	LINE_FAULT0_THRESH_7_LO_M0	Go
0x66	LINE_FAULT1_THRESH_0_LO_M0	LINE_FAULT1_THRESH_0_LO_M0	Go
0x67	LINE_FAULT1_THRESH_1_HI_M0	LINE_FAULT1_THRESH_1_HI_M0	Go

Table 7-534. PAGE 14: SAR ADC Registers (continued)

Address	Acronym	Register Name	Section
0x68	LINE_FAULT1_THRESH_1_LO_M0	LINE_FAULT1_THRESH_1_LO_M0	Go
0x69	LINE_FAULT1_THRESH_2_HI_M0	LINE_FAULT1_THRESH_2_HI_M0	Go
0x6A	LINE_FAULT1_THRESH_2_LO_M0	LINE_FAULT1_THRESH_2_LO_M0	Go
0x6B	LINE_FAULT1_THRESH_3_HI_M0	LINE_FAULT1_THRESH_3_HI_M0	Go
0x6C	LINE_FAULT1_THRESH_3_LO_M0	LINE_FAULT1_THRESH_3_LO_M0	Go
0x6D	LINE_FAULT1_THRESH_4_HI_M0	LINE_FAULT1_THRESH_4_HI_M0	Go
0x6E	LINE_FAULT1_THRESH_4_LO_M0	LINE_FAULT1_THRESH_4_LO_M0	Go
0x6F	LINE_FAULT1_THRESH_5_HI_M0	LINE_FAULT1_THRESH_5_HI_M0	Go
0x70	LINE_FAULT1_THRESH_5_LO_M0	LINE_FAULT1_THRESH_5_LO_M0	Go
0x71	LINE_FAULT1_THRESH_6_HI_M0	LINE_FAULT1_THRESH_6_HI_M0	Go
0x72	LINE_FAULT1_THRESH_6_LO_M0	LINE_FAULT1_THRESH_6_LO_M0	Go
0x73	LINE_FAULT1_THRESH_7_HI_M0	LINE_FAULT1_THRESH_7_HI_M0	Go
0x74	LINE_FAULT1_THRESH_7_LO_M0	LINE_FAULT1_THRESH_7_LO_M0	Go
0x78	LINE_FAULT2_THRESH_0_LO_M0	LINE_FAULT2_THRESH_0_LO_M0	Go
0x79	LINE_FAULT2_THRESH_1_HI_M0	LINE_FAULT2_THRESH_1_HI_M0	Go
0x7A	LINE_FAULT2_THRESH_1_LO_M0	LINE_FAULT2_THRESH_1_LO_M0	Go
0x7B	LINE_FAULT2_THRESH_2_HI_M0	LINE_FAULT2_THRESH_2_HI_M0	Go
0x7C	LINE_FAULT2_THRESH_2_LO_M0	LINE_FAULT2_THRESH_2_LO_M0	Go
0x7D	LINE_FAULT2_THRESH_3_HI_M0	LINE_FAULT2_THRESH_3_HI_M0	Go
0x7E	LINE_FAULT2_THRESH_3_LO_M0	LINE_FAULT2_THRESH_3_LO_M0	Go
0x7F	LINE_FAULT2_THRESH_4_HI_M0	LINE_FAULT2_THRESH_4_HI_M0	Go
0x80	LINE_FAULT2_THRESH_4_LO_M0	LINE_FAULT2_THRESH_4_LO_M0	Go
0x81	LINE_FAULT2_THRESH_5_HI_M0	LINE_FAULT2_THRESH_5_HI_M0	Go
0x82	LINE_FAULT2_THRESH_5_LO_M0	LINE_FAULT2_THRESH_5_LO_M0	Go
0x83	LINE_FAULT2_THRESH_6_HI_M0	LINE_FAULT2_THRESH_6_HI_M0	Go
0x84	LINE_FAULT2_THRESH_6_LO_M0	LINE_FAULT2_THRESH_6_LO_M0	Go
0x85	LINE_FAULT2_THRESH_7_HI_M0	LINE_FAULT2_THRESH_7_HI_M0	Go

Table 7-534. PAGE 14: SAR ADC Registers (continued)

Address	Acronym	Register Name	Section
0x86	LINE_FAULT2_THRESH_7_LO_M0	LINE_FAULT2_THRESH_7_LO_M0	Go
0x8A	LINE_FAULT3_THRESH_0_LO_M0	LINE_FAULT3_THRESH_0_LO_M0	Go
0x8B	LINE_FAULT3_THRESH_1_HI_M0	LINE_FAULT3_THRESH_1_HI_M0	Go
0x8C	LINE_FAULT3_THRESH_1_LO_M0	LINE_FAULT3_THRESH_1_LO_M0	Go
0x8D	LINE_FAULT3_THRESH_2_HI_M0	LINE_FAULT3_THRESH_2_HI_M0	Go
0x8E	LINE_FAULT3_THRESH_2_LO_M0	LINE_FAULT3_THRESH_2_LO_M0	Go
0x8F	LINE_FAULT3_THRESH_3_HI_M0	LINE_FAULT3_THRESH_3_HI_M0	Go
0x90	LINE_FAULT3_THRESH_3_LO_M0	LINE_FAULT3_THRESH_3_LO_M0	Go
0x91	LINE_FAULT3_THRESH_4_HI_M0	LINE_FAULT3_THRESH_4_HI_M0	Go
0x92	LINE_FAULT3_THRESH_4_LO_M0	LINE_FAULT3_THRESH_4_LO_M0	Go
0x93	LINE_FAULT3_THRESH_5_HI_M0	LINE_FAULT3_THRESH_5_HI_M0	Go
0x94	LINE_FAULT3_THRESH_5_LO_M0	LINE_FAULT3_THRESH_5_LO_M0	Go
0x95	LINE_FAULT3_THRESH_6_HI_M0	LINE_FAULT3_THRESH_6_HI_M0	Go
0x96	LINE_FAULT3_THRESH_6_LO_M0	LINE_FAULT3_THRESH_6_LO_M0	Go
0x97	LINE_FAULT3_THRESH_7_HI_M0	LINE_FAULT3_THRESH_7_HI_M0	Go
0x98	LINE_FAULT3_THRESH_7_LO_M0	LINE_FAULT3_THRESH_7_LO_M0	Go
0x9C	LINE_FAULT0_THRESH_0_LO_M1	LINE_FAULT0_THRESH_0_LO_M1	Go
0x9D	LINE_FAULT0_THRESH_1_HI_M1	LINE_FAULT0_THRESH_1_HI_M1	Go
0x9E	LINE_FAULT0_THRESH_1_LO_M1	LINE_FAULT0_THRESH_1_LO_M1	Go
0x9F	LINE_FAULT0_THRESH_2_HI_M1	LINE_FAULT0_THRESH_2_HI_M1	Go
0xA0	LINE_FAULT0_THRESH_2_LO_M1	LINE_FAULT0_THRESH_2_LO_M1	Go
0xA1	LINE_FAULT0_THRESH_3_HI_M1	LINE_FAULT0_THRESH_3_HI_M1	Go
0xA2	LINE_FAULT0_THRESH_3_LO_M1	LINE_FAULT0_THRESH_3_LO_M1	Go
0xA3	LINE_FAULT0_THRESH_4_HI_M1	LINE_FAULT0_THRESH_4_HI_M1	Go
0xA4	LINE_FAULT0_THRESH_4_LO_M1	LINE_FAULT0_THRESH_4_LO_M1	Go
0xA5	LINE_FAULT0_THRESH_5_HI_M1	LINE_FAULT0_THRESH_5_HI_M1	Go
0xA6	LINE_FAULT0_THRESH_5_LO_M1	LINE_FAULT0_THRESH_5_LO_M1	Go

Table 7-534. PAGE 14: SAR ADC Registers (continued)

Address	Acronym	Register Name	Section
0xA7	LINE_FAULT0_THRESH_6_HI_M1	LINE_FAULT0_THRESH_6_HI_M1	Go
0xA8	LINE_FAULT0_THRESH_6_LO_M1	LINE_FAULT0_THRESH_6_LO_M1	Go
0xA9	LINE_FAULT0_THRESH_7_HI_M1	LINE_FAULT0_THRESH_7_HI_M1	Go
0xAA	LINE_FAULT0_THRESH_7_LO_M1	LINE_FAULT0_THRESH_7_LO_M1	Go
0xAE	LINE_FAULT1_THRESH_0_LO_M1	LINE_FAULT1_THRESH_0_LO_M1	Go
0xAF	LINE_FAULT1_THRESH_1_HI_M1	LINE_FAULT1_THRESH_1_HI_M1	Go
0xB0	LINE_FAULT1_THRESH_1_LO_M1	LINE_FAULT1_THRESH_1_LO_M1	Go
0xB1	LINE_FAULT1_THRESH_2_HI_M1	LINE_FAULT1_THRESH_2_HI_M1	Go
0xB2	LINE_FAULT1_THRESH_2_LO_M1	LINE_FAULT1_THRESH_2_LO_M1	Go
0xB3	LINE_FAULT1_THRESH_3_HI_M1	LINE_FAULT1_THRESH_3_HI_M1	Go
0xB4	LINE_FAULT1_THRESH_3_LO_M1	LINE_FAULT1_THRESH_3_LO_M1	Go
0xB5	LINE_FAULT1_THRESH_4_HI_M1	LINE_FAULT1_THRESH_4_HI_M1	Go
0xB6	LINE_FAULT1_THRESH_4_LO_M1	LINE_FAULT1_THRESH_4_LO_M1	Go
0xB7	LINE_FAULT1_THRESH_5_HI_M1	LINE_FAULT1_THRESH_5_HI_M1	Go
0xB8	LINE_FAULT1_THRESH_5_LO_M1	LINE_FAULT1_THRESH_5_LO_M1	Go
0xB9	LINE_FAULT1_THRESH_6_HI_M1	LINE_FAULT1_THRESH_6_HI_M1	Go
0xBA	LINE_FAULT1_THRESH_6_LO_M1	LINE_FAULT1_THRESH_6_LO_M1	Go
0xBB	LINE_FAULT1_THRESH_7_HI_M1	LINE_FAULT1_THRESH_7_HI_M1	Go
0xBC	LINE_FAULT1_THRESH_7_LO_M1	LINE_FAULT1_THRESH_7_LO_M1	Go
0xC0	LINE_FAULT2_THRESH_0_LO_M1	LINE_FAULT2_THRESH_0_LO_M1	Go
0xC1	LINE_FAULT2_THRESH_1_HI_M1	LINE_FAULT2_THRESH_1_HI_M1	Go
0xC2	LINE_FAULT2_THRESH_1_LO_M1	LINE_FAULT2_THRESH_1_LO_M1	Go
0xC3	LINE_FAULT2_THRESH_2_HI_M1	LINE_FAULT2_THRESH_2_HI_M1	Go
0xC4	LINE_FAULT2_THRESH_2_LO_M1	LINE_FAULT2_THRESH_2_LO_M1	Go
0xC5	LINE_FAULT2_THRESH_3_HI_M1	LINE_FAULT2_THRESH_3_HI_M1	Go
0xC6	LINE_FAULT2_THRESH_3_LO_M1	LINE_FAULT2_THRESH_3_LO_M1	Go
0xC7	LINE_FAULT2_THRESH_4_HI_M1	LINE_FAULT2_THRESH_4_HI_M1	Go

Table 7-534. PAGE 14: SAR ADC Registers (continued)

Address	Acronym	Register Name	Section
0xC8	LINE_FAULT2_THRESH_4_LO_M1	LINE_FAULT2_THRESH_4_LO_M1	Go
0xC9	LINE_FAULT2_THRESH_5_HI_M1	LINE_FAULT2_THRESH_5_HI_M1	Go
0xCA	LINE_FAULT2_THRESH_5_LO_M1	LINE_FAULT2_THRESH_5_LO_M1	Go
0xCB	LINE_FAULT2_THRESH_6_HI_M1	LINE_FAULT2_THRESH_6_HI_M1	Go
0xCC	LINE_FAULT2_THRESH_6_LO_M1	LINE_FAULT2_THRESH_6_LO_M1	Go
0xCD	LINE_FAULT2_THRESH_7_HI_M1	LINE_FAULT2_THRESH_7_HI_M1	Go
0xCE	LINE_FAULT2_THRESH_7_LO_M1	LINE_FAULT2_THRESH_7_LO_M1	Go
0xD2	LINE_FAULT3_THRESH_0_LO_M1	LINE_FAULT3_THRESH_0_LO_M1	Go
0xD3	LINE_FAULT3_THRESH_1_HI_M1	LINE_FAULT3_THRESH_1_HI_M1	Go
0xD4	LINE_FAULT3_THRESH_1_LO_M1	LINE_FAULT3_THRESH_1_LO_M1	Go
0xD5	LINE_FAULT3_THRESH_2_HI_M1	LINE_FAULT3_THRESH_2_HI_M1	Go
0xD6	LINE_FAULT3_THRESH_2_LO_M1	LINE_FAULT3_THRESH_2_LO_M1	Go
0xD7	LINE_FAULT3_THRESH_3_HI_M1	LINE_FAULT3_THRESH_3_HI_M1	Go
0xD8	LINE_FAULT3_THRESH_3_LO_M1	LINE_FAULT3_THRESH_3_LO_M1	Go
0xD9	LINE_FAULT3_THRESH_4_HI_M1	LINE_FAULT3_THRESH_4_HI_M1	Go
0xDA	LINE_FAULT3_THRESH_4_LO_M1	LINE_FAULT3_THRESH_4_LO_M1	Go
0xDB	LINE_FAULT3_THRESH_5_HI_M1	LINE_FAULT3_THRESH_5_HI_M1	Go
0xDC	LINE_FAULT3_THRESH_5_LO_M1	LINE_FAULT3_THRESH_5_LO_M1	Go
0xDD	LINE_FAULT3_THRESH_6_HI_M1	LINE_FAULT3_THRESH_6_HI_M1	Go
0xDE	LINE_FAULT3_THRESH_6_LO_M1	LINE_FAULT3_THRESH_6_LO_M1	Go
0xDF	LINE_FAULT3_THRESH_7_HI_M1	LINE_FAULT3_THRESH_7_HI_M1	Go
0xE0	LINE_FAULT3_THRESH_7_LO_M1	LINE_FAULT3_THRESH_7_LO_M1	Go

Complex bit access types are encoded to fit into small table cells. Table 7-535 shows the codes that are used for access types in this section.

Table 7-535. Page 14: SAR ADC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

Table 7-535. Page 14: SAR ADC Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.8.1 ADC_CLK_DIV_SEL Register (Address = 0x4) [Default = 0xD0]

ADC_CLK_DIV_SEL is shown in Table 7-536.

Return to the Summary Table.

ADC Moving Average Filter and Input Clock Frequency Divider Selection

Table 7-536. ADC_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	ADC_AVG_SEL	R/W	0x3	Moving Average Filter Selection 0x0 = No avg 0x1 = 2 samples 0x2 = 4 samples 0x3 = 8 samples (default)
5:4	ADC_CTRL_CLK_DIV	R/W	0x1	Clock Divider Selection 0x0 = 25Mhz 0x1 = 12.5 Mhz (default) 0x2 = 8.33 Mhz 0x3 = 6.25 Mhz
3:0	RESERVED	R	0x0	Reserved

7.6.2.8.2 ADC_INPUT_EN_LSB Register (Address = 0x7) [Default = 0x3D]

ADC_INPUT_EN_LSB is shown in Table 7-537.

Return to the Summary Table.

Table 7-537. ADC_INPUT_EN_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7	ADC_INPUT_EN_IV6	R/W	0x0	Enables for ADC reading IV6
6	ADC_INPUT_EN_IV5	R/W	0x0	Enables for ADC reading IV5
5	ADC_INPUT_EN_IV4	R/W	0x1	Enables for ADC reading IV4
4	ADC_INPUT_EN_IV3	R/W	0x1	Enables for ADC reading IV3
3	ADC_INPUT_EN_IV2	R/W	0x1	Enables for ADC reading IV2
2	ADC_INPUT_EN_IV1	R/W	0x1	Enables for ADC reading IV1
1	RESERVED	R/W	0x0	Reserved
0	ADC_INPUT_EN_TEMP	R/W	0x1	Enables for ADC reading temp sensor

7.6.2.8.3 SAR_ADC_INPUT_EN_MSB Register (Address = 0x8) [Default = 0x00]

SAR_ADC_INPUT_EN_MSB is shown in Table 7-538.

Return to the Summary Table.

Table 7-538. SAR_ADC_INPUT_EN_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved

Table 7-538. SAR_ADC_INPUT_EN_MSB Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	RESERVED	R/W	0x0	Reserved
5	ADC_INPUT_EN_LINE_FAULT3	R/W	0x0	Enables for ADC reading line fault 3
4	ADC_INPUT_EN_LINE_FAULT2	R/W	0x0	Enables for ADC reading line fault 2
3	ADC_INPUT_EN_LINE_FAULT1	R/W	0x0	Enables for ADC reading line fault 1
2	ADC_INPUT_EN_LINE_FAULT0	R/W	0x0	Enables for ADC reading line fault 0
1	ADC_INPUT_EN_EXT_VOL0	R/W	0x0	Enables for ADC reading external voltage 0
0	ADC_INPUT_EN_EXT_VOL1	R/W	0x0	Enables for ADC reading external voltage 1

7.6.2.8.4 ADC_MODE Register (Address = 0xD) [Default = 0x80]

ADC_MODE is shown in Table 7-539.

Return to the Summary Table.

Table 7-539. ADC_MODE Register Field Descriptions

Bit	Field	Type	Default	Description
7	ADC_MODE	R/W	0x1	ADC Mode 0 = Enabled 1 = Disabled
6	RESERVED	R/W	0x0	Reserved
5:3	RESERVED	R/W	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

7.6.2.8.5 ADC_SRC_CNTR_0 Register (Address = 0xF) [Default = 0xC8]

ADC_SRC_CNTR_0 is shown in Table 7-540.

Return to the Summary Table.

Table 7-540. ADC_SRC_CNTR_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SRC_CNT_VAL_0	R/W	0xC8	Set the number of clock cycles to average for each source (# cycles per second/number of sources enabled)

7.6.2.8.6 ADC_SRC_CNTR_1 Register (Address = 0x10) [Default = 0x32]

ADC_SRC_CNTR_1 is shown in Table 7-541.

Return to the Summary Table.

Table 7-541. ADC_SRC_CNTR_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SRC_CNT_VAL_1	R/W	0x32	Set the number of clock cycles to average for each source (# cycles per second/number of sources enabled)

7.6.2.8.7 ADC_SRC_CNTR_2 Register (Address = 0x11) [Default = 0x00]

ADC_SRC_CNTR_2 is shown in Table 7-542.

Return to the Summary Table.

Table 7-542. ADC_SRC_CNTR_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SRC_CNT_VAL_2	R/W	0x0	Set the number of clock cycles to average for each source (# cycles per second/number of sources enabled)

7.6.2.8.8 ADC_SRC_CNTR_3 Register (Address = 0x12) [Default = 0x00]

ADC_SRC_CNTR_3 is shown in Table 7-543.

Return to the Summary Table.

Table 7-543. ADC_SRC_CNTR_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SRC_CNT_VAL_3	R/W	0x0	Set the number of clock cycles to average for each source (# cycles per second/number of sources enabled)

7.6.2.8.9 TEMP_FINAL Register (Address = 0x13) [Default = 0x00]

TEMP_FINAL is shown in Table 7-544.

Return to the Summary Table.

Table 7-544. TEMP_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_FINAL	R	0x0	holds adc value for temp_final

7.6.2.8.10 IV0_FINAL Register (Address = 0x15) [Default = 0x00]

IV0_FINAL is shown in Table 7-545.

Return to the Summary Table.

Table 7-545. IV0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_FINAL	R	0x0	holds adc value for iv1_final (Refer to internal supply voltage sensing) for debug purposes

7.6.2.8.11 IV1_FINAL Register (Address = 0x16) [Default = 0x00]

IV1_FINAL is shown in Table 7-546.

Return to the Summary Table.

Table 7-546. IV1_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_FINAL	R	0x0	holds adc value for iv2_final (Refer to internal supply voltage sensing) for debug purposes

7.6.2.8.12 IV2_FINAL Register (Address = 0x17) [Default = 0x00]

IV2_FINAL is shown in Table 7-547.

Return to the Summary Table.

Table 7-547. IV2_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_FINAL	R	0x0	holds adc value for iv3_final (Refer to internal supply voltage sensing) for debug purposes

7.6.2.8.13 IV3_FINAL Register (Address = 0x18) [Default = 0x00]

IV3_FINAL is shown in Table 7-548.

Return to the Summary Table.

Table 7-548. IV3_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_FINAL	R	0x0	holds adc value for iv4_final (Refer to internal supply voltage sensing) for debug purposes

7.6.2.8.14 EXT_VOL0_FINAL Register (Address = 0x1B) [Default = 0x00]

EXT_VOL0_FINAL is shown in Table 7-549.

Return to the Summary Table.

Table 7-549. EXT_VOL0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_FINAL	R	0x0	holds adc value for ext_vol0_final (Refer to External Voltage Sensing) for debug purposes

7.6.2.8.15 EXT_VOL1_FINAL Register (Address = 0x1C) [Default = 0x00]

EXT_VOL1_FINAL is shown in Table 7-550.

Return to the Summary Table.

Table 7-550. EXT_VOL1_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_FINAL	R	0x0	holds adc value for ext_vol1_final (Refer to External Voltage Sensing) for debug purposes

7.6.2.8.16 LINE_FAULT0_FINAL Register (Address = 0x1D) [Default = 0x00]

LINE_FAULT0_FINAL is shown in Table 7-551.

Return to the Summary Table.

Table 7-551. LINE_FAULT0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_FINAL	R	0x0	holds adc value for line_fault0_final (Refer to Serial Link Fault Detect) for debug purposes

7.6.2.8.17 LINE_FAULT1_FINAL Register (Address = 0x1E) [Default = 0x00]

LINE_FAULT1_FINAL is shown in Table 7-552.

Return to the Summary Table.

Table 7-552. LINE_FAULT1_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_FINAL	R	0x0	holds adc value for line_fault1_final (Refer to Serial Link Fault Detect) for debug purposes

7.6.2.8.18 LINE_FAULT2_FINAL Register (Address = 0x1F) [Default = 0x00]

LINE_FAULT2_FINAL is shown in Table 7-553.

Return to the Summary Table.

Table 7-553. LINE_FAULT2_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_FINAL	R	0x0	holds adc value for line_fault2_final (Refer to Serial Link Fault Detect) for debug purposes

7.6.2.8.19 LINE_FAULT3_FINAL Register (Address = 0x20) [Default = 0x00]

LINE_FAULT3_FINAL is shown in Table 7-554.

Return to the Summary Table.

Table 7-554. LINE_FAULT3_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_FINAL	R	0x0	holds adc value for line_fault3_final (Refer to Serial Link Fault Detect) for debug purposes

7.6.2.8.20 INT_STATUS_LSB_LOW Register (Address = 0x23) [Default = 0x00]

INT_STATUS_LSB_LOW is shown in Table 7-555.

Return to the Summary Table.

Table 7-555. INT_STATUS_LSB_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R	0x0	
5	INT_STATUS_LOW_IV4		0x0	Interrupt status for IV4 if the value is below the set threshold
4	INT_STATUS_LOW_IV3		0x0	Interrupt status for IV3 if the value is below the set threshold
3	INT_STATUS_LOW_IV2		0x0	Interrupt status for IV2 if the value is below the set threshold
2	INT_STATUS_LOW_IV1		0x0	Interrupt status for IV1 if the value is below the set threshold
1	RESERVED	R	0x0	
0	INT_STATUS_LOW_TEMP		0x0	Interrupt status for temperature if the value is below the set threshold

7.6.2.8.21 INT_STATUS_MSB_LOW Register (Address = 0x24) [Default = 0x00]

INT_STATUS_MSB_LOW is shown in Table 7-556.

Return to the Summary Table.

Table 7-556. INT_STATUS_MSB_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R	0x0	

Table 7-556. INT_STATUS_MSB_LOW Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	RESERVED	R	0x0	Interrupt status for IV4 if the value is below the set threshold
4	RESERVED	R	0x0	Interrupt status for IV3 if the value is below the set threshold
3	RESERVED	R	0x0	Interrupt status for IV2 if the value is below the set threshold
2	RESERVED	R	0x0	Interrupt status for IV1 if the value is below the set threshold
1	INT_STATUS_EXT_VOL1		0x0	Interrupt status for external voltage 1 if the value is below the set threshold
0	INT_STATUS_EXT_VOL0		0x0	Interrupt status for external voltage 0 if the value is below the set threshold

7.6.2.8.22 INT_STATUS_LSB_HIGH Register (Address = 0x25) [Default = 0x00]

INT_STATUS_LSB_HIGH is shown in Table 7-557.

Return to the Summary Table.

Table 7-557. INT_STATUS_LSB_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7	INT_STATUS_HIGH_IV6		0x0	Interrupt status for IV6 if the value is above the set threshold
6	INT_STATUS_HIGH_IV5		0x0	Interrupt status for IV5 if the value is above the set threshold
5	INT_STATUS_HIGH_IV4		0x0	Interrupt status for IV4 if the value is above the set threshold
4	INT_STATUS_HIGH_IV3		0x0	Interrupt status for IV3 if the value is above the set threshold
3	INT_STATUS_HIGH_IV2		0x0	Interrupt status for IV2 if the value is above the set threshold
2	INT_STATUS_HIGH_IV1		0x0	Interrupt status for IV1 if the value is above the set threshold
1	RESERVED	R	0x0	Reserved
0	INT_STATUS_HIGH_TEMP		0x0	Interrupt status for temprature if the value is above the set threshold

7.6.2.8.23 INT_STATUS_MSB_HIGH Register (Address = 0x26) [Default = 0x00]

INT_STATUS_MSB_HIGH is shown in Table 7-558.

Return to the Summary Table.

Table 7-558. INT_STATUS_MSB_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	INT_STATUS_HIGH_EXT_VOL1		0x0	Interrupt status for ext_vol1 if the value is above the set threshold
0	INT_STATUS_HIGH_EXT_VOL0		0x0	Interrupt status for ext_vol0 if the value is above the set threshold

7.6.2.8.24 INT_LINE_FAULT0_M0 Register (Address = 0x27) [Default = 0x00]

INT_LINE_FAULT0_M0 is shown in Table 7-559.

Return to the Summary Table.

Table 7-559. INT_LINE_FAULT0_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_0_M0		0x0	Interrupt status for line_fault0 short to 3.3V
3	SHORT_TO_1_8_0_M0		0x0	Interrupt status for line_fault0 short to 1.8V
2	SHORT_TO_1_15_0_M0		0x0	Interrupt status for line_fault0 short to 1.15V
1	NORMAL_OP_0_M0		0x0	Interrupt status for line_fault0 Normal operation
0	SHORT_TO_GND_0_M0		0x0	Interrupt status for line_fault0 short to ground

7.6.2.8.25 INT_LINE_FAULT1_M0 Register (Address = 0x28) [Default = 0x00]

INT_LINE_FAULT1_M0 is shown in Table 7-560.

Return to the Summary Table.

Table 7-560. INT_LINE_FAULT1_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_1_M0		0x0	Interrupt status for line_fault1 short to 3.3V
3	SHORT_TO_1_8_1_M0		0x0	Interrupt status for line_fault1 short to 1.8V
2	SHORT_TO_1_15_1_M0		0x0	Interrupt status for line_fault1 short to 1.15V
1	NORMAL_OP_1_M0		0x0	Interrupt status for line_fault1 Normal operation
0	SHORT_TO_GND_1_M0		0x0	Interrupt status for line_fault1 short to ground

7.6.2.8.26 INT_LINE_FAULT2_M0 Register (Address = 0x29) [Default = 0x00]

INT_LINE_FAULT2_M0 is shown in Table 7-561.

Return to the Summary Table.

Table 7-561. INT_LINE_FAULT2_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_2_M0		0x0	Interrupt status for line_fault2 short to 3.3V
3	SHORT_TO_1_8_2_M0		0x0	Interrupt status for line_fault2 short to 1.8V
2	SHORT_TO_1_15_2_M0		0x0	Interrupt status for line_fault2 short to 1.15V

Table 7-561. INT_LINE_FAULT2_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	NORMAL_OP_2_M0		0x0	Interrupt status for line_fault2 Normal operation
0	SHORT_TO_GND_2_M0		0x0	Interrupt status for line_fault2 short to ground

7.6.2.8.27 INT_LINE_FAULT3_M0 Register (Address = 0x2A) [Default = 0x00]

INT_LINE_FAULT3_M0 is shown in Table 7-562.

Return to the Summary Table.

Table 7-562. INT_LINE_FAULT3_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_3_M0		0x0	Interrupt status for line_fault3 short to 3.3V
3	SHORT_TO_1_8_3_M0		0x0	Interrupt status for line_fault3 short to 1.8V
2	SHORT_TO_1_15_3_M0		0x0	Interrupt status for line_fault3 short to 1.15V
1	NORMAL_OP_3_M0		0x0	Interrupt status for line_fault3 Normal operation
0	SHORT_TO_GND_3_M0		0x0	Interrupt status for line_fault3 short to ground

7.6.2.8.28 INT_LINE_FAULT0_M1 Register (Address = 0x2B) [Default = 0x00]

INT_LINE_FAULT0_M1 is shown in Table 7-563.

Return to the Summary Table.

Table 7-563. INT_LINE_FAULT0_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_0_M1		0x0	Interrupt status for line_fault0 short to 3.3V
3	SHORT_TO_1_8_0_M1		0x0	Interrupt status for line_fault0 short to 1.8V
2	SHORT_TO_1_15_0_M1		0x0	Interrupt status for line_fault0 short to 1.15V
1	NORMAL_OP_0_M1		0x0	Interrupt status for line_fault0 Normal operation
0	SHORT_TO_GND_0_M1		0x0	Interrupt status for line_fault0 short to ground

7.6.2.8.29 INT_LINE_FAULT1_M1 Register (Address = 0x2C) [Default = 0x00]

INT_LINE_FAULT1_M1 is shown in Table 7-564.

Return to the Summary Table.

Table 7-564. INT_LINE_FAULT1_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_1_M1		0x0	Interrupt status for line_fault1 short to 3.3V
3	SHORT_TO_1_8_1_M1		0x0	Interrupt status for line_fault1 short to 1.8V
2	SHORT_TO_1_15_1_M1		0x0	Interrupt status for line_fault1 short to 1.15V
1	NORMAL_OP_1_M1		0x0	Interrupt status for line_fault1 Normal operation
0	SHORT_TO_GND_1_M1		0x0	Interrupt status for line_fault1 short to ground

7.6.2.8.30 INT_LINE_FAULT2_M1 Register (Address = 0x2D) [Default = 0x00]

INT_LINE_FAULT2_M1 is shown in Table 7-565.

Return to the Summary Table.

Table 7-565. INT_LINE_FAULT2_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_2_M1		0x0	Interrupt status for line_fault2 short to 3.3V
3	SHORT_TO_1_8_2_M1		0x0	Interrupt status for line_fault2 short to 1.8V
2	SHORT_TO_1_15_2_M1		0x0	Interrupt status for line_fault2 short to 1.15V
1	NORMAL_OP_2_M1		0x0	Interrupt status for line_fault2 Normal operation
0	SHORT_TO_GND_2_M1		0x0	Interrupt status for line_fault2 short to ground

7.6.2.8.31 INT_LINE_FAULT3_M1 Register (Address = 0x2E) [Default = 0x00]

INT_LINE_FAULT3_M1 is shown in Table 7-566.

Return to the Summary Table.

Table 7-566. INT_LINE_FAULT3_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_3_M1		0x0	Interrupt status for line_fault3 short to 3.3V
3	SHORT_TO_1_8_3_M1		0x0	Interrupt status for line_fault3 short to 1.8V

Table 7-566. INT_LINE_FAULT3_M1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	SHORT_TO_1_15_3_M1		0x0	Interrupt status for line_fault3 short to 1.15V
1	NORMAL_OP_3_M1		0x0	Interrupt status for line_fault3 Normal operation
0	SHORT_TO_GND_3_M1		0x0	Interrupt status for line_fault3 short to ground

7.6.2.8.32 INT_LINE_FAULT_UNDEF Register (Address = 0x2F) [Default = 0x00]

INT_LINE_FAULT_UNDEF is shown in Table 7-567.

Return to the Summary Table.

Table 7-567. INT_LINE_FAULT_UNDEF Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	INT_LINE_FAULT_UNDEF_M1		0x0	Interrupt status to signal adc value in undefined threshold range for mode 1 0 - line fault 0 1 - line fault 1 2 - line fault 2 3 - line fault 3
3:0	INT_LINE_FAULT_UNDEF_M0		0x0	Interrupt status to signal adc value in undefined threshold range for mode 0 0 - line fault 0 1 - line fault 1 2 - line fault 2 3 - line fault 3

7.6.2.8.33 INT_LINE_FAULT_SATURATE Register (Address = 0x30) [Default = 0x00]

INT_LINE_FAULT_SATURATE is shown in Table 7-568.

Return to the Summary Table.

Table 7-568. INT_LINE_FAULT_SATURATE Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	INT_LINE_FAULT3_SATURATE		0x0	Indicates the ADC code for Line Fault Detectiion is saturated and the voltage sensed is beyond the ADC range
2	INT_LINE_FAULT2_SATURATE		0x0	Indicates the ADC code for Line Fault Detectiion is saturated and the voltage sensed is beyond the ADC range
1	INT_LINE_FAULT1_SATURATE		0x0	Indicates the ADC code for Line Fault Detectiion is saturated and the voltage sensed is beyond the ADC range
0	INT_LINE_FAULT0_SATURATE		0x0	Indicates the ADC code for Line Fault Detectiion is saturated and the voltage sensed is beyond the ADC range

7.6.2.8.34 TEMP_HIGH Register (Address = 0x33) [Default = 0xCE]

TEMP_HIGH is shown in Table 7-569.

Return to the Summary Table.

Table 7-569. TEMP_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_HIGH	R/W	0xCE	Upper threshold for the Die Temperature

7.6.2.8.35 TEMP_LOW Register (Address = 0x34) [Default = 0x7E]

TEMP_LOW is shown in Table 7-570.

Return to the Summary Table.

Table 7-570. TEMP_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_LOW	R/W	0x7E	Lower threshold for the Die Temperature

7.6.2.8.36 TEMP_ADC_OFFSET Register (Address = 0x35) [Default = 0x00]

TEMP_ADC_OFFSET is shown in Table 7-571.

Return to the Summary Table.

Table 7-571. TEMP_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.37 IV0_HIGH Register (Address = 0x39) [Default = 0x86]

IV0_HIGH is shown in Table 7-572.

Return to the Summary Table.

Table 7-572. IV0_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_HIGH	R/W	0x86	Upper threshold for iv0

7.6.2.8.38 IV0_LOW Register (Address = 0x3A) [Default = 0x7A]

IV0_LOW is shown in Table 7-573.

Return to the Summary Table.

Table 7-573. IV0_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_LOW	R/W	0x7A	Lower threshold for iv0

7.6.2.8.39 IV0_ADC_OFFSET Register (Address = 0x3B) [Default = 0x00]

IV0_ADC_OFFSET is shown in Table 7-574.

Return to the Summary Table.

Table 7-574. IV0_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.40 IV1_HIGH Register (Address = 0x3C) [Default = 0x86]

IV1_HIGH is shown in Table 7-575.

Return to the Summary Table.

Table 7-575. IV1_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_HIGH	R/W	0x86	Upper threshold for iv1

7.6.2.8.41 IV1_LOW Register (Address = 0x3D) [Default = 0x7A]

IV1_LOW is shown in Table 7-576.

Return to the Summary Table.

Table 7-576. IV1_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_LOW	R/W	0x7A	Lower threshold for iv1

7.6.2.8.42 IV1_ADC_OFFSET Register (Address = 0x3E) [Default = 0x00]

IV1_ADC_OFFSET is shown in Table 7-577.

Return to the Summary Table.

Table 7-577. IV1_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.43 IV2_HIGH Register (Address = 0x3F) [Default = 0x86]

IV2_HIGH is shown in Table 7-578.

Return to the Summary Table.

Table 7-578. IV2_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_HIGH	R/W	0x86	Upper threshold for iv2

7.6.2.8.44 IV2_LOW Register (Address = 0x40) [Default = 0x7A]

IV2_LOW is shown in Table 7-579.

Return to the Summary Table.

Table 7-579. IV2_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_LOW	R/W	0x7A	Lower threshold for iv2

7.6.2.8.45 IV2_ADC_OFFSET Register (Address = 0x41) [Default = 0x00]

IV2_ADC_OFFSET is shown in Table 7-580.

Return to the Summary Table.

Table 7-580. IV2_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.46 IV3_HIGH Register (Address = 0x42) [Default = 0x86]

IV3_HIGH is shown in Table 7-581.

Return to the Summary Table.

Table 7-581. IV3_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_HIGH	R/W	0x86	Upper threshold for iv3

7.6.2.8.47 IV3_LOW Register (Address = 0x43) [Default = 0x7A]

IV3_LOW is shown in Table 7-582.

Return to the Summary Table.

Table 7-582. IV3_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_LOW	R/W	0x7A	Lower threshold for iv3

7.6.2.8.48 IV3_ADC_OFFSET Register (Address = 0x44) [Default = 0x00]

IV3_ADC_OFFSET is shown in Table 7-583.

Return to the Summary Table.

Table 7-583. IV3_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.49 TEMP_IV_MASK Register (Address = 0x4B) [Default = 0xC2]

TEMP_IV_MASK is shown in Table 7-584.

Return to the Summary Table.

Mask Interrupts for the following thresholds

Table 7-584. TEMP_IV_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	IV3_THRESH_MASK	R/W	0x0	iv3_thresh_mask
4	IV2_THRESH_MASK	R/W	0x0	iv2_thresh_mask
3	IV1_THRESH_MASK	R/W	0x0	iv1_thresh_mask
2	IV0_THRESH_MASK	R/W	0x0	iv0_thresh_mask
1	RESERVED	R/W	0x1	Reserved
0	TEMP_THRESH_MASK	R/W	0x0	temp_thresh_mask

7.6.2.8.50 EXT_VOL0_HIGH Register (Address = 0x4C) [Default = 0x00]

EXT_VOL0_HIGH is shown in Table 7-585.

Return to the Summary Table.

Table 7-585. EXT_VOL0_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_HIGH	R/W	0x0	Upper threshold for ext_vol0

7.6.2.8.51 EXT_VOL0_LOW Register (Address = 0x4D) [Default = 0x00]

EXT_VOL0_LOW is shown in Table 7-586.

Return to the Summary Table.

Table 7-586. EXT_VOL0_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_LOW	R/W	0x0	Lower threshold for ext_vol0

7.6.2.8.52 EXT_VOL0_ADC_OFFSET Register (Address = 0x4E) [Default = 0x00]

EXT_VOL0_ADC_OFFSET is shown in Table 7-587.

Return to the Summary Table.

Table 7-587. EXT_VOL0_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.53 EXT_VOL1_HIGH Register (Address = 0x4F) [Default = 0x00]

EXT_VOL1_HIGH is shown in Table 7-588.

Return to the Summary Table.

Table 7-588. EXT_VOL1_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_HIGH	R/W	0x0	Upper threshold for ext_vol1

7.6.2.8.54 EXT_VOL1_LOW Register (Address = 0x50) [Default = 0x00]

EXT_VOL1_LOW is shown in Table 7-589.

Return to the Summary Table.

Table 7-589. EXT_VOL1_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_LOW	R/W	0x0	Lower threshold for ext_vol1

7.6.2.8.55 EXT_VOL1_ADC_OFFSET Register (Address = 0x51) [Default = 0x00]

EXT_VOL1_ADC_OFFSET is shown in Table 7-590.

Return to the Summary Table.

Table 7-590. EXT_VOL1_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

7.6.2.8.56 EXT_VOL_MASK Register (Address = 0x52) [Default = 0x00]

EXT_VOL_MASK is shown in Table 7-591.

Return to the Summary Table.

Mark Interrupts for following thresholds

Table 7-591. EXT_VOL_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	EXT_VOL1_THRESH_MASK	R/W	0x0	ext_vol1_thresh_mask
0	EXT_VOL0_THRESH_MASK	R/W	0x0	ext_vol0_thresh_mask

7.6.2.8.57 LINE_FAULT0_THRESH_0_HI_M0 Register (Address = 0x53) [Default = 0xAD]

LINE_FAULT0_THRESH_0_HI_M0 is shown in Table 7-592.

Return to the Summary Table.

Table 7-592. LINE_FAULT0_THRESH_0_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_HI_M0	R/W	0xAD	Upper threshold 0 for line_fault0 (Mode0)

7.6.2.8.58 LINE_FAULT0_THRESH_0_LO_M0 Register (Address = 0x54) [Default = 0x72]

LINE_FAULT0_THRESH_0_LO_M0 is shown in Table 7-593.

Return to the Summary Table.

Table 7-593. LINE_FAULT0_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_LO_M0	R/W	0x72	Lower threshold 0 for line_fault0 (Mode0)

7.6.2.8.59 LINE_FAULT0_THRESH_1_HI_M0 Register (Address = 0x55) [Default = 0xDC]

LINE_FAULT0_THRESH_1_HI_M0 is shown in Table 7-594.

Return to the Summary Table.

Table 7-594. LINE_FAULT0_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_HI_M0	R/W	0xDC	Upper threshold 1 for line_fault0 (Mode0)

7.6.2.8.60 LINE_FAULT0_THRESH_1_LO_M0 Register (Address = 0x56) [Default = 0xCD]

LINE_FAULT0_THRESH_1_LO_M0 is shown in Table 7-595.

Return to the Summary Table.

Table 7-595. LINE_FAULT0_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_LO_M0	R/W	0xCD	Lower threshold 1 for line_fault0 (Mode0)

7.6.2.8.61 LINE_FAULT0_THRESH_2_HI_M0 Register (Address = 0x57) [Default = 0xF8]

LINE_FAULT0_THRESH_2_HI_M0 is shown in Table 7-596.

Return to the Summary Table.

Table 7-596. LINE_FAULT0_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_HI_M0	R/W	0xF8	Upper threshold 2 for line_fault0 (Mode0)

7.6.2.8.62 LINE_FAULT0_THRESH_2_LO_M0 Register (Address = 0x58) [Default = 0xE6]

LINE_FAULT0_THRESH_2_LO_M0 is shown in Table 7-597.

Return to the Summary Table.

Table 7-597. LINE_FAULT0_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_LO_M0	R/W	0xE6	Lower threshold 2 for line_fault0 (Mode0)

7.6.2.8.63 LINE_FAULT0_THRESH_3_HI_M0 Register (Address = 0x59) [Default = 0x00]

LINE_FAULT0_THRESH_3_HI_M0 is shown in Table 7-598.

Return to the Summary Table.

Table 7-598. LINE_FAULT0_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for line_fault0 (Mode0)

7.6.2.8.64 LINE_FAULT0_THRESH_3_LO_M0 Register (Address = 0x5A) [Default = 0x00]

LINE_FAULT0_THRESH_3_LO_M0 is shown in Table 7-599.

Return to the Summary Table.

Table 7-599. LINE_FAULT0_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for line_fault0 (Mode0)

7.6.2.8.65 LINE_FAULT0_THRESH_4_HI_M0 Register (Address = 0x5B) [Default = 0x00]

LINE_FAULT0_THRESH_4_HI_M0 is shown in Table 7-600.

Return to the Summary Table.

Table 7-600. LINE_FAULT0_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for line_fault0 (Mode0)

7.6.2.8.66 LINE_FAULT0_THRESH_4_LO_M0 Register (Address = 0x5C) [Default = 0x00]

LINE_FAULT0_THRESH_4_LO_M0 is shown in Table 7-601.

Return to the Summary Table.

Table 7-601. LINE_FAULT0_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for line_fault0 (Mode0)

7.6.2.8.67 LINE_FAULT0_THRESH_5_HI_M0 Register (Address = 0x5D) [Default = 0x00]

LINE_FAULT0_THRESH_5_HI_M0 is shown in Table 7-602.

Return to the Summary Table.

Table 7-602. LINE_FAULT0_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for line_fault0 (Mode0)

7.6.2.8.68 LINE_FAULT0_THRESH_5_LO_M0 Register (Address = 0x5E) [Default = 0x00]

LINE_FAULT0_THRESH_5_LO_M0 is shown in Table 7-603.

Return to the Summary Table.

Table 7-603. LINE_FAULT0_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for line_fault0 (Mode0)

7.6.2.8.69 LINE_FAULT0_THRESH_6_HI_M0 Register (Address = 0x5F) [Default = 0x00]

LINE_FAULT0_THRESH_6_HI_M0 is shown in Table 7-604.

Return to the Summary Table.

Table 7-604. LINE_FAULT0_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for line_fault0 (Mode0)

7.6.2.8.70 LINE_FAULT0_THRESH_6_LO_M0 Register (Address = 0x60) [Default = 0x00]

LINE_FAULT0_THRESH_6_LO_M0 is shown in Table 7-605.

Return to the Summary Table.

Table 7-605. LINE_FAULT0_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for line_fault0 (Mode0)

7.6.2.8.71 LINE_FAULT0_THRESH_7_HI_M0 Register (Address = 0x61) [Default = 0x00]

LINE_FAULT0_THRESH_7_HI_M0 is shown in Table 7-606.

Return to the Summary Table.

Table 7-606. LINE_FAULT0_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for line_fault0 (Mode0)

7.6.2.8.72 LINE_FAULT0_THRESH_7_LO_M0 Register (Address = 0x62) [Default = 0x00]

LINE_FAULT0_THRESH_7_LO_M0 is shown in Table 7-607.

Return to the Summary Table.

Table 7-607. LINE_FAULT0_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for line_fault0 (Mode0)

7.6.2.8.73 LINE_FAULT1_THRESH_0_LO_M0 Register (Address = 0x66) [Default = 0x00]

LINE_FAULT1_THRESH_0_LO_M0 is shown in Table 7-608.

Return to the Summary Table.

Table 7-608. LINE_FAULT1_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_0_LO_M0	R/W	0x0	Lower threshold 0 for line_fault1 (Mode0)

7.6.2.8.74 LINE_FAULT1_THRESH_1_HI_M0 Register (Address = 0x67) [Default = 0xE9]

LINE_FAULT1_THRESH_1_HI_M0 is shown in Table 7-609.

Return to the Summary Table.

Table 7-609. LINE_FAULT1_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_HI_M0	R/W	0xE9	Upper threshold 1 for line_fault1 (Mode0)

7.6.2.8.75 LINE_FAULT1_THRESH_1_LO_M0 Register (Address = 0x68) [Default = 0x60]

LINE_FAULT1_THRESH_1_LO_M0 is shown in Table 7-610.

Return to the Summary Table.

Table 7-610. LINE_FAULT1_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_LO_M0	R/W	0x60	Lower threshold 1 for line_fault1 (Mode0)

7.6.2.8.76 LINE_FAULT1_THRESH_2_HI_M0 Register (Address = 0x69) [Default = 0x00]

LINE_FAULT1_THRESH_2_HI_M0 is shown in Table 7-611.

Return to the Summary Table.

Table 7-611. LINE_FAULT1_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for line_fault1 (Mode0)

7.6.2.8.77 LINE_FAULT1_THRESH_2_LO_M0 Register (Address = 0x6A) [Default = 0x00]

LINE_FAULT1_THRESH_2_LO_M0 is shown in Table 7-612.

Return to the Summary Table.

Table 7-612. LINE_FAULT1_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for line_fault1 (Mode0)

7.6.2.8.78 LINE_FAULT1_THRESH_3_HI_M0 Register (Address = 0x6B) [Default = 0x00]

LINE_FAULT1_THRESH_3_HI_M0 is shown in Table 7-613.

Return to the Summary Table.

Table 7-613. LINE_FAULT1_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for line_fault1 (Mode0)

7.6.2.8.79 LINE_FAULT1_THRESH_3_LO_M0 Register (Address = 0x6C) [Default = 0x00]

LINE_FAULT1_THRESH_3_LO_M0 is shown in Table 7-614.

Return to the Summary Table.

Table 7-614. LINE_FAULT1_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for line_fault1 (Mode0)

7.6.2.8.80 LINE_FAULT1_THRESH_4_HI_M0 Register (Address = 0x6D) [Default = 0x00]

LINE_FAULT1_THRESH_4_HI_M0 is shown in Table 7-615.

Return to the Summary Table.

Table 7-615. LINE_FAULT1_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for line_fault1 (Mode0)

7.6.2.8.81 LINE_FAULT1_THRESH_4_LO_M0 Register (Address = 0x6E) [Default = 0x00]

LINE_FAULT1_THRESH_4_LO_M0 is shown in Table 7-616.

Return to the Summary Table.

Table 7-616. LINE_FAULT1_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for line_fault1 (Mode0)

7.6.2.8.82 LINE_FAULT1_THRESH_5_HI_M0 Register (Address = 0x6F) [Default = 0x00]

LINE_FAULT1_THRESH_5_HI_M0 is shown in Table 7-617.

Return to the Summary Table.

Table 7-617. LINE_FAULT1_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for line_fault1 (Mode0)

7.6.2.8.83 LINE_FAULT1_THRESH_5_LO_M0 Register (Address = 0x70) [Default = 0x00]

LINE_FAULT1_THRESH_5_LO_M0 is shown in Table 7-618.

Return to the Summary Table.

Table 7-618. LINE_FAULT1_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for line_fault1 (Mode0)

7.6.2.8.84 LINE_FAULT1_THRESH_6_HI_M0 Register (Address = 0x71) [Default = 0x00]

LINE_FAULT1_THRESH_6_HI_M0 is shown in Table 7-619.

Return to the Summary Table.

Table 7-619. LINE_FAULT1_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for line_fault1 (Mode0)

7.6.2.8.85 LINE_FAULT1_THRESH_6_LO_M0 Register (Address = 0x72) [Default = 0x00]

LINE_FAULT1_THRESH_6_LO_M0 is shown in Table 7-620.

Return to the Summary Table.

Table 7-620. LINE_FAULT1_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for line_fault1 (Mode0)

7.6.2.8.86 LINE_FAULT1_THRESH_7_HI_M0 Register (Address = 0x73) [Default = 0x00]

LINE_FAULT1_THRESH_7_HI_M0 is shown in Table 7-621.

Return to the Summary Table.

Table 7-621. LINE_FAULT1_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for line_fault1 (Mode0)

7.6.2.8.87 LINE_FAULT1_THRESH_7_LO_M0 Register (Address = 0x74) [Default = 0x00]

LINE_FAULT1_THRESH_7_LO_M0 is shown in Table 7-622.

Return to the Summary Table.

Table 7-622. LINE_FAULT1_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for line_fault1 (Mode0)

7.6.2.8.88 LINE_FAULT2_THRESH_0_LO_M0 Register (Address = 0x78) [Default = 0x72]

LINE_FAULT2_THRESH_0_LO_M0 is shown in Table 7-623.

Return to the Summary Table.

Table 7-623. LINE_FAULT2_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_0_LO_M0	R/W	0x72	Lower threshold 0 for line_fault2 (Mode0)

7.6.2.8.89 LINE_FAULT2_THRESH_1_HI_M0 Register (Address = 0x79) [Default = 0xDC]

LINE_FAULT2_THRESH_1_HI_M0 is shown in Table 7-624.

Return to the Summary Table.

Table 7-624. LINE_FAULT2_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_HI_M0	R/W	0xDC	Upper threshold 1 for line_fault2 (Mode0)

7.6.2.8.90 LINE_FAULT2_THRESH_1_LO_M0 Register (Address = 0x7A) [Default = 0xCD]

LINE_FAULT2_THRESH_1_LO_M0 is shown in Table 7-625.

Return to the Summary Table.

Table 7-625. LINE_FAULT2_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_LO_M0	R/W	0xCD	Lower threshold 1 for line_fault2 (Mode0)

7.6.2.8.91 LINE_FAULT2_THRESH_2_HI_M0 Register (Address = 0x7B) [Default = 0xF8]

LINE_FAULT2_THRESH_2_HI_M0 is shown in Table 7-626.

Return to the Summary Table.

Table 7-626. LINE_FAULT2_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_HI_M0	R/W	0xF8	Upper threshold 2 for line_fault2 (Mode0)

7.6.2.8.92 LINE_FAULT2_THRESH_2_LO_M0 Register (Address = 0x7C) [Default = 0xE6]

LINE_FAULT2_THRESH_2_LO_M0 is shown in Table 7-627.

Return to the Summary Table.

Table 7-627. LINE_FAULT2_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_LO_M0	R/W	0xE6	Lower threshold 2 for line_fault2 (Mode0)

7.6.2.8.93 LINE_FAULT2_THRESH_3_HI_M0 Register (Address = 0x7D) [Default = 0x00]

LINE_FAULT2_THRESH_3_HI_M0 is shown in Table 7-628.

Return to the Summary Table.

Table 7-628. LINE_FAULT2_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for line_fault2 (Mode0)

7.6.2.8.94 LINE_FAULT2_THRESH_3_LO_M0 Register (Address = 0x7E) [Default = 0x00]

LINE_FAULT2_THRESH_3_LO_M0 is shown in Table 7-629.

Return to the Summary Table.

Table 7-629. LINE_FAULT2_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for line_fault2 (Mode0)

7.6.2.8.95 LINE_FAULT2_THRESH_4_HI_M0 Register (Address = 0x7F) [Default = 0x00]

LINE_FAULT2_THRESH_4_HI_M0 is shown in Table 7-630.

Return to the Summary Table.

Table 7-630. LINE_FAULT2_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for line_fault2 (Mode0)

7.6.2.8.96 LINE_FAULT2_THRESH_4_LO_M0 Register (Address = 0x80) [Default = 0x00]

LINE_FAULT2_THRESH_4_LO_M0 is shown in Table 7-631.

Return to the Summary Table.

Table 7-631. LINE_FAULT2_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for line_fault2 (Mode0)

7.6.2.8.97 LINE_FAULT2_THRESH_5_HI_M0 Register (Address = 0x81) [Default = 0x00]

LINE_FAULT2_THRESH_5_HI_M0 is shown in Table 7-632.

Return to the Summary Table.

Table 7-632. LINE_FAULT2_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for line_fault2 (Mode0)

7.6.2.8.98 LINE_FAULT2_THRESH_5_LO_M0 Register (Address = 0x82) [Default = 0x00]

LINE_FAULT2_THRESH_5_LO_M0 is shown in Table 7-633.

Return to the Summary Table.

Table 7-633. LINE_FAULT2_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for line_fault2 (Mode0)

7.6.2.8.99 LINE_FAULT2_THRESH_6_HI_M0 Register (Address = 0x83) [Default = 0x00]

LINE_FAULT2_THRESH_6_HI_M0 is shown in Table 7-634.

Return to the Summary Table.

Table 7-634. LINE_FAULT2_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for line_fault2 (Mode0)

7.6.2.8.100 LINE_FAULT2_THRESH_6_LO_M0 Register (Address = 0x84) [Default = 0x00]

LINE_FAULT2_THRESH_6_LO_M0 is shown in Table 7-635.

Return to the Summary Table.

Table 7-635. LINE_FAULT2_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for line_fault2 (Mode0)

7.6.2.8.101 LINE_FAULT2_THRESH_7_HI_M0 Register (Address = 0x85) [Default = 0x00]

LINE_FAULT2_THRESH_7_HI_M0 is shown in Table 7-636.

Return to the Summary Table.

Table 7-636. LINE_FAULT2_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for line_fault2 (Mode0)

7.6.2.8.102 LINE_FAULT2_THRESH_7_LO_M0 Register (Address = 0x86) [Default = 0x00]

LINE_FAULT2_THRESH_7_LO_M0 is shown in Table 7-637.

Return to the Summary Table.

Table 7-637. LINE_FAULT2_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for line_fault2 (Mode0)

7.6.2.8.103 LINE_FAULT3_THRESH_0_LO_M0 Register (Address = 0x8A) [Default = 0x00]

LINE_FAULT3_THRESH_0_LO_M0 is shown in Table 7-638.

Return to the Summary Table.

Table 7-638. LINE_FAULT3_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_0_LO_M0	R/W	0x0	Lower threshold 0 for line_fault3 (Mode0)

7.6.2.8.104 LINE_FAULT3_THRESH_1_HI_M0 Register (Address = 0x8B) [Default = 0xE9]

LINE_FAULT3_THRESH_1_HI_M0 is shown in Table 7-639.

Return to the Summary Table.

Table 7-639. LINE_FAULT3_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_HI_M0	R/W	0xE9	Upper threshold 1 for line_fault3 (Mode0)

7.6.2.8.105 LINE_FAULT3_THRESH_1_LO_M0 Register (Address = 0x8C) [Default = 0x60]

LINE_FAULT3_THRESH_1_LO_M0 is shown in Table 7-640.

Return to the Summary Table.

Table 7-640. LINE_FAULT3_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_LO_M0	R/W	0x60	Lower threshold 1 for line_fault3 (Mode0)

7.6.2.8.106 LINE_FAULT3_THRESH_2_HI_M0 Register (Address = 0x8D) [Default = 0x00]

LINE_FAULT3_THRESH_2_HI_M0 is shown in Table 7-641.

Return to the Summary Table.

Table 7-641. LINE_FAULT3_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for line_fault3 (Mode0)

7.6.2.8.107 LINE_FAULT3_THRESH_2_LO_M0 Register (Address = 0x8E) [Default = 0x00]

LINE_FAULT3_THRESH_2_LO_M0 is shown in Table 7-642.

Return to the Summary Table.

Table 7-642. LINE_FAULT3_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for line_fault3 (Mode0)

7.6.2.8.108 LINE_FAULT3_THRESH_3_HI_M0 Register (Address = 0x8F) [Default = 0x00]

LINE_FAULT3_THRESH_3_HI_M0 is shown in Table 7-643.

Return to the Summary Table.

Table 7-643. LINE_FAULT3_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for line_fault3 (Mode0)

7.6.2.8.109 LINE_FAULT3_THRESH_3_LO_M0 Register (Address = 0x90) [Default = 0x00]

LINE_FAULT3_THRESH_3_LO_M0 is shown in Table 7-644.

Return to the Summary Table.

Table 7-644. LINE_FAULT3_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for line_fault3 (Mode0)

7.6.2.8.110 LINE_FAULT3_THRESH_4_HI_M0 Register (Address = 0x91) [Default = 0x00]

LINE_FAULT3_THRESH_4_HI_M0 is shown in Table 7-645.

Return to the Summary Table.

Table 7-645. LINE_FAULT3_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for line_fault3 (Mode0)

7.6.2.8.111 LINE_FAULT3_THRESH_4_LO_M0 Register (Address = 0x92) [Default = 0x00]

LINE_FAULT3_THRESH_4_LO_M0 is shown in Table 7-646.

Return to the Summary Table.

Table 7-646. LINE_FAULT3_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for line_fault3 (Mode0)

7.6.2.8.112 LINE_FAULT3_THRESH_5_HI_M0 Register (Address = 0x93) [Default = 0x00]

LINE_FAULT3_THRESH_5_HI_M0 is shown in Table 7-647.

Return to the Summary Table.

Table 7-647. LINE_FAULT3_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for line_fault3 (Mode0)

7.6.2.8.113 LINE_FAULT3_THRESH_5_LO_M0 Register (Address = 0x94) [Default = 0x00]

LINE_FAULT3_THRESH_5_LO_M0 is shown in Table 7-648.

Return to the Summary Table.

Table 7-648. LINE_FAULT3_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for line_fault3 (Mode0)

7.6.2.8.114 LINE_FAULT3_THRESH_6_HI_M0 Register (Address = 0x95) [Default = 0x00]

LINE_FAULT3_THRESH_6_HI_M0 is shown in Table 7-649.

Return to the Summary Table.

Table 7-649. LINE_FAULT3_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for line_fault3 (Mode0)

7.6.2.8.115 LINE_FAULT3_THRESH_6_LO_M0 Register (Address = 0x96) [Default = 0x00]

LINE_FAULT3_THRESH_6_LO_M0 is shown in Table 7-650.

Return to the Summary Table.

Table 7-650. LINE_FAULT3_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for line_fault3 (Mode0)

7.6.2.8.116 LINE_FAULT3_THRESH_7_HI_M0 Register (Address = 0x97) [Default = 0x00]

LINE_FAULT3_THRESH_7_HI_M0 is shown in Table 7-651.

Return to the Summary Table.

Table 7-651. LINE_FAULT3_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for line_fault3 (Mode0)

7.6.2.8.117 LINE_FAULT3_THRESH_7_LO_M0 Register (Address = 0x98) [Default = 0x00]

LINE_FAULT3_THRESH_7_LO_M0 is shown in Table 7-652.

Return to the Summary Table.

Table 7-652. LINE_FAULT3_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for line_fault3 (Mode0)

7.6.2.8.118 LINE_FAULT0_THRESH_0_LO_M1 Register (Address = 0x9C) [Default = 0x39]

LINE_FAULT0_THRESH_0_LO_M1 is shown in Table 7-653.

Return to the Summary Table.

Table 7-653. LINE_FAULT0_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_LO_M1	R/W	0x39	Lower threshold 0 for line_fault0 (Mode1)

7.6.2.8.119 LINE_FAULT0_THRESH_1_HI_M1 Register (Address = 0x9D) [Default = 0x6E]

LINE_FAULT0_THRESH_1_HI_M1 is shown in Table 7-654.

Return to the Summary Table.

Table 7-654. LINE_FAULT0_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_HI_M1	R/W	0x6E	Upper threshold 1 for line_fault0 (Mode1)

7.6.2.8.120 LINE_FAULT0_THRESH_1_LO_M1 Register (Address = 0x9E) [Default = 0x64]

LINE_FAULT0_THRESH_1_LO_M1 is shown in Table 7-655.

Return to the Summary Table.

Table 7-655. LINE_FAULT0_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_LO_M1	R/W	0x64	Lower threshold 1 for line_fault0 (Mode1)

7.6.2.8.121 LINE_FAULT0_THRESH_2_HI_M1 Register (Address = 0x9F) [Default = 0x7C]

LINE_FAULT0_THRESH_2_HI_M1 is shown in Table 7-656.

Return to the Summary Table.

Table 7-656. LINE_FAULT0_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_HI_M1	R/W	0x7C	Upper threshold 2 for line_fault0 (Mode1)

7.6.2.8.122 LINE_FAULT0_THRESH_2_LO_M1 Register (Address = 0xA0) [Default = 0x71]

LINE_FAULT0_THRESH_2_LO_M1 is shown in Table 7-657.

Return to the Summary Table.

Table 7-657. LINE_FAULT0_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_LO_M1	R/W	0x71	Lower threshold 2 for line_fault0 (Mode1)

7.6.2.8.123 LINE_FAULT0_THRESH_3_HI_M1 Register (Address = 0xA1) [Default = 0x9A]

LINE_FAULT0_THRESH_3_HI_M1 is shown in Table 7-658.

Return to the Summary Table.

Table 7-658. LINE_FAULT0_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_HI_M1	R/W	0x9A	Upper threshold 3 for line_fault0 (Mode1)

7.6.2.8.124 LINE_FAULT0_THRESH_3_LO_M1 Register (Address = 0xA2) [Default = 0x89]

LINE_FAULT0_THRESH_3_LO_M1 is shown in Table 7-659.

Return to the Summary Table.

Table 7-659. LINE_FAULT0_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_LO_M1	R/W	0x89	Lower threshold 3 for line_fault0 (Mode1)

7.6.2.8.125 LINE_FAULT0_THRESH_4_HI_M1 Register (Address = 0xA3) [Default = 0xC8]

LINE_FAULT0_THRESH_4_HI_M1 is shown in Table 7-660.

Return to the Summary Table.

Table 7-660. LINE_FAULT0_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_HI_M1	R/W	0xC8	Upper threshold 4 for line_fault0 (Mode1)

7.6.2.8.126 LINE_FAULT0_THRESH_4_LO_M1 Register (Address = 0xA4) [Default = 0xB8]

LINE_FAULT0_THRESH_4_LO_M1 is shown in Table 7-661.

Return to the Summary Table.

Table 7-661. LINE_FAULT0_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_LO_M1	R/W	0xB8	Lower threshold 4 for line_fault0 (Mode1)

7.6.2.8.127 LINE_FAULT0_THRESH_5_HI_M1 Register (Address = 0xA5) [Default = 0x00]

LINE_FAULT0_THRESH_5_HI_M1 is shown in Table 7-662.

Return to the Summary Table.

Table 7-662. LINE_FAULT0_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_HI_M1	R/W	0x0	Upper threshold 5 for line_fault0 (Mode1)

7.6.2.8.128 LINE_FAULT0_THRESH_5_LO_M1 Register (Address = 0xA6) [Default = 0x00]

LINE_FAULT0_THRESH_5_LO_M1 is shown in Table 7-663.

Return to the Summary Table.

Table 7-663. LINE_FAULT0_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_LO_M1	R/W	0x0	Lower threshold 5 for line_fault0 (Mode1)

7.6.2.8.129 LINE_FAULT0_THRESH_6_HI_M1 Register (Address = 0xA7) [Default = 0x00]

LINE_FAULT0_THRESH_6_HI_M1 is shown in Table 7-664.

Return to the Summary Table.

Table 7-664. LINE_FAULT0_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_HI_M1	R/W	0x0	Upper threshold 6 for line_fault0 (Mode1)

7.6.2.8.130 LINE_FAULT0_THRESH_6_LO_M1 Register (Address = 0xA8) [Default = 0x00]

LINE_FAULT0_THRESH_6_LO_M1 is shown in Table 7-665.

Return to the Summary Table.

Table 7-665. LINE_FAULT0_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_LO_M1	R/W	0x0	Lower threshold 6 for line_fault0 (Mode1)

7.6.2.8.131 LINE_FAULT0_THRESH_7_HI_M1 Register (Address = 0xA9) [Default = 0x00]

LINE_FAULT0_THRESH_7_HI_M1 is shown in Table 7-666.

Return to the Summary Table.

Table 7-666. LINE_FAULT0_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_HI_M1	R/W	0x0	Upper threshold 7 for line_fault0 (Mode1)

7.6.2.8.132 LINE_FAULT0_THRESH_7_LO_M1 Register (Address = 0xAA) [Default = 0x00]

LINE_FAULT0_THRESH_7_LO_M1 is shown in Table 7-667.

Return to the Summary Table.

Table 7-667. LINE_FAULT0_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_LO_M1	R/W	0x0	Lower threshold 7 for line_fault0 (Mode1)

7.6.2.8.133 LINE_FAULT1_THRESH_0_LO_M1 Register (Address = 0xAE) [Default = 0x00]

LINE_FAULT1_THRESH_0_LO_M1 is shown in Table 7-668.

Return to the Summary Table.

Table 7-668. LINE_FAULT1_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_0_LO_M1	R/W	0x0	Lower threshold 0 for line_fault1 (Mode1)

7.6.2.8.134 LINE_FAULT1_THRESH_1_HI_M1 Register (Address = 0xAF) [Default = 0x00]

LINE_FAULT1_THRESH_1_HI_M1 is shown in Table 7-669.

Return to the Summary Table.

Table 7-669. LINE_FAULT1_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_HI_M1	R/W	0x0	Upper threshold 1 for line_fault1 (Mode1)

7.6.2.8.135 LINE_FAULT1_THRESH_1_LO_M1 Register (Address = 0xB0) [Default = 0x00]

LINE_FAULT1_THRESH_1_LO_M1 is shown in Table 7-670.

Return to the Summary Table.

Table 7-670. LINE_FAULT1_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_LO_M1	R/W	0x0	Lower threshold 1 for line_fault1 (Mode1)

7.6.2.8.136 LINE_FAULT1_THRESH_2_HI_M1 Register (Address = 0xB1) [Default = 0x00]

LINE_FAULT1_THRESH_2_HI_M1 is shown in Table 7-671.

Return to the Summary Table.

Table 7-671. LINE_FAULT1_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_HI_M1	R/W	0x0	Upper threshold 2 for line_fault1 (Mode1)

7.6.2.8.137 LINE_FAULT1_THRESH_2_LO_M1 Register (Address = 0xB2) [Default = 0x00]

LINE_FAULT1_THRESH_2_LO_M1 is shown in Table 7-672.

Return to the Summary Table.

Table 7-672. LINE_FAULT1_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_LO_M1	R/W	0x0	Lower threshold 2 for line_fault1 (Mode1)

7.6.2.8.138 LINE_FAULT1_THRESH_3_HI_M1 Register (Address = 0xB3) [Default = 0x00]

LINE_FAULT1_THRESH_3_HI_M1 is shown in Table 7-673.

Return to the Summary Table.

Table 7-673. LINE_FAULT1_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_HI_M1	R/W	0x0	Upper threshold 3 for line_fault1 (Mode1)

7.6.2.8.139 LINE_FAULT1_THRESH_3_LO_M1 Register (Address = 0xB4) [Default = 0x00]

LINE_FAULT1_THRESH_3_LO_M1 is shown in Table 7-674.

Return to the Summary Table.

Table 7-674. LINE_FAULT1_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_LO_M1	R/W	0x0	Lower threshold 3 for line_fault1 (Mode1)

7.6.2.8.140 LINE_FAULT1_THRESH_4_HI_M1 Register (Address = 0xB5) [Default = 0x00]

LINE_FAULT1_THRESH_4_HI_M1 is shown in Table 7-675.

Return to the Summary Table.

Table 7-675. LINE_FAULT1_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_HI_M1	R/W	0x0	Upper threshold 4 for line_fault1 (Mode1)

7.6.2.8.141 LINE_FAULT1_THRESH_4_LO_M1 Register (Address = 0xB6) [Default = 0x00]

LINE_FAULT1_THRESH_4_LO_M1 is shown in Table 7-676.

Return to the Summary Table.

Table 7-676. LINE_FAULT1_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_LO_M1	R/W	0x0	Lower threshold 4 for line_fault1 (Mode1)

7.6.2.8.142 LINE_FAULT1_THRESH_5_HI_M1 Register (Address = 0xB7) [Default = 0x00]

LINE_FAULT1_THRESH_5_HI_M1 is shown in Table 7-677.

Return to the Summary Table.

Table 7-677. LINE_FAULT1_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_HI_M1	R/W	0x0	Upper threshold 5 for line_fault1 (Mode1)

7.6.2.8.143 LINE_FAULT1_THRESH_5_LO_M1 Register (Address = 0xB8) [Default = 0x00]

LINE_FAULT1_THRESH_5_LO_M1 is shown in Table 7-678.

Return to the Summary Table.

Table 7-678. LINE_FAULT1_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_LO_M1	R/W	0x0	Lower threshold 5 for line_fault1 (Mode1)

7.6.2.8.144 LINE_FAULT1_THRESH_6_HI_M1 Register (Address = 0xB9) [Default = 0x00]

LINE_FAULT1_THRESH_6_HI_M1 is shown in Table 7-679.

Return to the Summary Table.

Table 7-679. LINE_FAULT1_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_HI_M1	R/W	0x0	Upper threshold 6 for line_fault1 (Mode1)

7.6.2.8.145 LINE_FAULT1_THRESH_6_LO_M1 Register (Address = 0xBA) [Default = 0x00]

LINE_FAULT1_THRESH_6_LO_M1 is shown in Table 7-680.

Return to the Summary Table.

Table 7-680. LINE_FAULT1_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_LO_M1	R/W	0x0	Lower threshold 6 for line_fault1 (Mode1)

7.6.2.8.146 LINE_FAULT1_THRESH_7_HI_M1 Register (Address = 0xBB) [Default = 0x00]

LINE_FAULT1_THRESH_7_HI_M1 is shown in Table 7-681.

Return to the Summary Table.

Table 7-681. LINE_FAULT1_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_HI_M1	R/W	0x0	Upper threshold 7 for line_fault1 (Mode1)

7.6.2.8.147 LINE_FAULT1_THRESH_7_LO_M1 Register (Address = 0xBC) [Default = 0x00]

LINE_FAULT1_THRESH_7_LO_M1 is shown in Table 7-682.

Return to the Summary Table.

Table 7-682. LINE_FAULT1_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_LO_M1	R/W	0x0	Lower threshold 7 for line_fault1 (Mode1)

7.6.2.8.148 LINE_FAULT2_THRESH_0_LO_M1 Register (Address = 0xC0) [Default = 0x39]

LINE_FAULT2_THRESH_0_LO_M1 is shown in Table 7-683.

Return to the Summary Table.

Table 7-683. LINE_FAULT2_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_0_LO_M1	R/W	0x39	Lower threshold 0 for line_fault2 (Mode1)

7.6.2.8.149 LINE_FAULT2_THRESH_1_HI_M1 Register (Address = 0xC1) [Default = 0x6E]

LINE_FAULT2_THRESH_1_HI_M1 is shown in Table 7-684.

Return to the Summary Table.

Table 7-684. LINE_FAULT2_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_HI_M1	R/W	0x6E	Upper threshold 1 for line_fault2 (Mode1)

7.6.2.8.150 LINE_FAULT2_THRESH_1_LO_M1 Register (Address = 0xC2) [Default = 0x64]

LINE_FAULT2_THRESH_1_LO_M1 is shown in Table 7-685.

Return to the Summary Table.

Table 7-685. LINE_FAULT2_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_LO_M1	R/W	0x64	Lower threshold 1 for line_fault2 (Mode1)

7.6.2.8.151 LINE_FAULT2_THRESH_2_HI_M1 Register (Address = 0xC3) [Default = 0x7C]

LINE_FAULT2_THRESH_2_HI_M1 is shown in Table 7-686.

Return to the Summary Table.

Table 7-686. LINE_FAULT2_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_HI_M1	R/W	0x7C	Upper threshold 2 for line_fault2 (Mode1)

7.6.2.8.152 LINE_FAULT2_THRESH_2_LO_M1 Register (Address = 0xC4) [Default = 0x71]

LINE_FAULT2_THRESH_2_LO_M1 is shown in Table 7-687.

Return to the Summary Table.

Table 7-687. LINE_FAULT2_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_LO_M1	R/W	0x71	Lower threshold 2 for line_fault2 (Mode1)

7.6.2.8.153 LINE_FAULT2_THRESH_3_HI_M1 Register (Address = 0xC5) [Default = 0x9A]

LINE_FAULT2_THRESH_3_HI_M1 is shown in Table 7-688.

Return to the Summary Table.

Table 7-688. LINE_FAULT2_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_HI_M1	R/W	0x9A	Upper threshold 3 for line_fault2 (Mode1)

7.6.2.8.154 LINE_FAULT2_THRESH_3_LO_M1 Register (Address = 0xC6) [Default = 0x89]

LINE_FAULT2_THRESH_3_LO_M1 is shown in Table 7-689.

Return to the Summary Table.

Table 7-689. LINE_FAULT2_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_LO_M1	R/W	0x89	Lower threshold 3 for line_fault2 (Mode1)

7.6.2.8.155 LINE_FAULT2_THRESH_4_HI_M1 Register (Address = 0xC7) [Default = 0xC8]

LINE_FAULT2_THRESH_4_HI_M1 is shown in Table 7-690.

Return to the Summary Table.

Table 7-690. LINE_FAULT2_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_HI_M1	R/W	0xC8	Upper threshold 4 for line_fault2 (Mode1)

7.6.2.8.156 LINE_FAULT2_THRESH_4_LO_M1 Register (Address = 0xC8) [Default = 0xB8]

LINE_FAULT2_THRESH_4_LO_M1 is shown in Table 7-691.

Return to the Summary Table.

Table 7-691. LINE_FAULT2_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_LO_M1	R/W	0xB8	Lower threshold 4 for line_fault2 (Mode1)

7.6.2.8.157 LINE_FAULT2_THRESH_5_HI_M1 Register (Address = 0xC9) [Default = 0x00]

LINE_FAULT2_THRESH_5_HI_M1 is shown in Table 7-692.

Return to the Summary Table.

Table 7-692. LINE_FAULT2_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_HI_M1	R/W	0x0	Upper threshold 5 for line_fault2 (Mode1)

7.6.2.8.158 LINE_FAULT2_THRESH_5_LO_M1 Register (Address = 0xCA) [Default = 0x00]

LINE_FAULT2_THRESH_5_LO_M1 is shown in Table 7-693.

Return to the Summary Table.

Table 7-693. LINE_FAULT2_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_LO_M1	R/W	0x0	Lower threshold 5 for line_fault2 (Mode1)

7.6.2.8.159 LINE_FAULT2_THRESH_6_HI_M1 Register (Address = 0xCB) [Default = 0x00]

LINE_FAULT2_THRESH_6_HI_M1 is shown in Table 7-694.

Return to the Summary Table.

Table 7-694. LINE_FAULT2_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_HI_M1	R/W	0x0	Upper threshold 6 for line_fault2 (Mode1)

7.6.2.8.160 LINE_FAULT2_THRESH_6_LO_M1 Register (Address = 0xCC) [Default = 0x00]

LINE_FAULT2_THRESH_6_LO_M1 is shown in Table 7-695.

Return to the Summary Table.

Table 7-695. LINE_FAULT2_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_LO_M1	R/W	0x0	Lower threshold 6 for line_fault2 (Mode1)

7.6.2.8.161 LINE_FAULT2_THRESH_7_HI_M1 Register (Address = 0xCD) [Default = 0x00]

LINE_FAULT2_THRESH_7_HI_M1 is shown in Table 7-696.

Return to the Summary Table.

Table 7-696. LINE_FAULT2_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_HI_M1	R/W	0x0	Upper threshold 7 for line_fault2 (Mode1)

7.6.2.8.162 LINE_FAULT2_THRESH_7_LO_M1 Register (Address = 0xCE) [Default = 0x00]

LINE_FAULT2_THRESH_7_LO_M1 is shown in Table 7-697.

Return to the Summary Table.

Table 7-697. LINE_FAULT2_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_LO_M1	R/W	0x0	Lower threshold 7 for line_fault2 (Mode1)

7.6.2.8.163 LINE_FAULT3_THRESH_0_LO_M1 Register (Address = 0xD2) [Default = 0x00]

LINE_FAULT3_THRESH_0_LO_M1 is shown in Table 7-698.

Return to the Summary Table.

Table 7-698. LINE_FAULT3_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_0_LO_M1	R/W	0x0	Lower threshold 0 for line_fault3 (Mode1)

7.6.2.8.164 LINE_FAULT3_THRESH_1_HI_M1 Register (Address = 0xD3) [Default = 0x00]

LINE_FAULT3_THRESH_1_HI_M1 is shown in Table 7-699.

Return to the Summary Table.

Table 7-699. LINE_FAULT3_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_HI_M1	R/W	0x0	Upper threshold 1 for line_fault3 (Mode1)

7.6.2.8.165 LINE_FAULT3_THRESH_1_LO_M1 Register (Address = 0xD4) [Default = 0x00]

LINE_FAULT3_THRESH_1_LO_M1 is shown in Table 7-700.

Return to the Summary Table.

Table 7-700. LINE_FAULT3_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_LO_M1	R/W	0x0	Lower threshold 1 for line_fault3 (Mode1)

7.6.2.8.166 LINE_FAULT3_THRESH_2_HI_M1 Register (Address = 0xD5) [Default = 0x00]

LINE_FAULT3_THRESH_2_HI_M1 is shown in Table 7-701.

Return to the Summary Table.

Table 7-701. LINE_FAULT3_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_HI_M1	R/W	0x0	Upper threshold 2 for line_fault3 (Mode1)

7.6.2.8.167 LINE_FAULT3_THRESH_2_LO_M1 Register (Address = 0xD6) [Default = 0x00]

LINE_FAULT3_THRESH_2_LO_M1 is shown in Table 7-702.

Return to the Summary Table.

Table 7-702. LINE_FAULT3_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_LO_M1	R/W	0x0	Lower threshold 2 for line_fault3 (Mode1)

7.6.2.8.168 LINE_FAULT3_THRESH_3_HI_M1 Register (Address = 0xD7) [Default = 0x00]

LINE_FAULT3_THRESH_3_HI_M1 is shown in Table 7-703.

Return to the Summary Table.

Table 7-703. LINE_FAULT3_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_HI_M1	R/W	0x0	Upper threshold 3 for line_fault3 (Mode1)

7.6.2.8.169 LINE_FAULT3_THRESH_3_LO_M1 Register (Address = 0xD8) [Default = 0x00]

LINE_FAULT3_THRESH_3_LO_M1 is shown in Table 7-704.

Return to the Summary Table.

Table 7-704. LINE_FAULT3_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_LO_M1	R/W	0x0	Lower threshold 3 for line_fault3 (Mode1)

7.6.2.8.170 LINE_FAULT3_THRESH_4_HI_M1 Register (Address = 0xD9) [Default = 0x00]

LINE_FAULT3_THRESH_4_HI_M1 is shown in Table 7-705.

Return to the Summary Table.

Table 7-705. LINE_FAULT3_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_HI_M1	R/W	0x0	Upper threshold 4 for line_fault3 (Mode1)

7.6.2.8.171 LINE_FAULT3_THRESH_4_LO_M1 Register (Address = 0xDA) [Default = 0x00]

LINE_FAULT3_THRESH_4_LO_M1 is shown in Table 7-706.

Return to the Summary Table.

Table 7-706. LINE_FAULT3_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_LO_M1	R/W	0x0	Lower threshold 4 for line_fault3 (Mode1)

7.6.2.8.172 LINE_FAULT3_THRESH_5_HI_M1 Register (Address = 0xDB) [Default = 0x00]

LINE_FAULT3_THRESH_5_HI_M1 is shown in Table 7-707.

Return to the Summary Table.

Table 7-707. LINE_FAULT3_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_HI_M1	R/W	0x0	Upper threshold 5 for line_fault3 (Mode1)

7.6.2.8.173 LINE_FAULT3_THRESH_5_LO_M1 Register (Address = 0xDC) [Default = 0x00]

LINE_FAULT3_THRESH_5_LO_M1 is shown in Table 7-708.

Return to the Summary Table.

Table 7-708. LINE_FAULT3_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_LO_M1	R/W	0x0	Lower threshold 5 for line_fault3 (Mode1)

7.6.2.8.174 LINE_FAULT3_THRESH_6_HI_M1 Register (Address = 0xDD) [Default = 0x00]

LINE_FAULT3_THRESH_6_HI_M1 is shown in Table 7-709.

Return to the Summary Table.

Table 7-709. LINE_FAULT3_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_HI_M1	R/W	0x0	Upper threshold 6 for line_fault3 (Mode1)

7.6.2.8.175 LINE_FAULT3_THRESH_6_LO_M1 Register (Address = 0xDE) [Default = 0x00]

LINE_FAULT3_THRESH_6_LO_M1 is shown in Table 7-710.

Return to the Summary Table.

Table 7-710. LINE_FAULT3_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_LO_M1	R/W	0x0	Lower threshold 6 for line_fault3 (Mode1)

7.6.2.8.176 LINE_FAULT3_THRESH_7_HI_M1 Register (Address = 0xDF) [Default = 0x00]

LINE_FAULT3_THRESH_7_HI_M1 is shown in Table 7-711.

Return to the Summary Table.

Table 7-711. LINE_FAULT3_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_HI_M1	R/W	0x0	Upper threshold 7 for line_fault3 (Mode1)

7.6.2.8.177 LINE_FAULT3_THRESH_7_LO_M1 Register (Address = 0xE0) [Default = 0x00]

LINE_FAULT3_THRESH_7_LO_M1 is shown in Table 7-712.

Return to the Summary Table.

Table 7-712. LINE_FAULT3_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_LO_M1	R/W	0x0	Lower threshold 7 for line_fault3 (Mode1)

7.6.3 PATGEN Registers

Table 7-713 lists the memory-mapped registers for the PATGEN registers. All register offset addresses not listed in Table 7-713 should be considered as reserved locations and the register contents should not be modified.

Table 7-713. PATGEN Registers

Address	Acronym	Register Name	Section
0x0	PGRS1	PGRS1	Go
0x1	PGRS2	PGRS2	Go
0x2	PGGS1	PGGS1	Go
0x3	PGGS2	PGGS2	Go
0x4	PGBS1	PGBS1	Go
0x5	PGBS2	PGBS2	Go
0x6	PGTFS1	PGTFS1	Go
0x7	PGTFS2	PGTFS2	Go
0x8	PGTFS3	PGTFS3	Go
0x9	PGTFS4	PGTFS4	Go
0xA	PGAFS1	PGAFS1	Go
0xB	PGAFS2	PGAFS2	Go
0xC	PGAFS3	PGAFS3	Go
0xD	PGAFS4	PGAFS4	Go
0xE	PGHSW1	PGHSW1	Go
0xF	PGHSW2	PGHSW2	Go
0x10	PGVSW1		Go
0x11	PGVSW2	PGVSW2	Go
0x12	PGHBP1	PGHBP1	Go
0x13	PGHBP2	PGHBP2	Go
0x14	PGVBP1		Go
0x15	PGVBP2	PGVBP2	Go
0x16	PBSC	PBSC	Go
0x17	PGFT	PGFT	Go
0x18	PGTSC	PGTSC	Go
0x19	PGTSO1	PGTSO1	Go
0x1A	PGTSO2	PGTSO2	Go
0x1B	PGTSO3	PGTSO3	Go
0x1C	PGTSO4	PGTSO4	Go
0x1D	PGTSO5	PGTSO5	Go
0x1E	PGTSO6	PGTSO6	Go
0x1F	PGTSO7	PGTSO7	Go
0x20	PGTSO8	PGTSO8	Go
0x21	PGTSO9	PGTSO9	Go
0x22	PGTSO10	PGTSO10	Go
0x23	PGTSO11	PGTSO11	Go
0x24	PGTSO12	PGTSO12	Go
0x25	PGTSO13	PGTSO13	Go
0x26	PGTSO14	PGTSO14	Go
0x27	PGTSO15	PGTSO15	Go
0x28	PGTSO16	PGTSO16	Go
0x29	PGCE	PGCE	Go

Table 7-713. PATGEN Registers (continued)

Address	Acronym	Register Name	Section
0x2A	PGUPS	PGUPS	Go
0x2B	PGCF	PGCF	Go
0x2C	PGFC	PGFC	Go
0x2D	PGCEF	PGCEF	Go
0x2E	PGPRS1	PGPRS1	Go
0x2F	PGPRS2	PGPRS2	Go
0x30	PGPRS3	PGPRS3	Go
0x31	PGPRS4	PGPRS4	Go
0x32	PGPRS5	PGPRS5	Go
0x33	PGPRS6	PGPRS6	Go
0x34	PGPRSF	PGPRSF	Go
0x35	PGEILSL	PGEILSL	Go
0x36	PGEILSH	PGEILSH	Go
0x37	PGEILEL	PGEILEL	Go
0x38	PGEILEH	PGEILEH	Go
0x39	PGEIPSL	PGEIPSL	Go
0x3A	PGEIPSH	PGEIPSH	Go
0x3B	PGEIPEL	PGEIPEL	Go
0x3C	PGEIPEH	PGEIPEH	Go

Complex bit access types are encoded to fit into small table cells. Table 7-714 shows the codes that are used for access types in this section.

Table 7-714. PATGEN Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.3.1 PGRS1 Register (Address = 0x0) [Default = 0x00]

PGRS1 is shown in Table 7-715.

Return to the Summary Table.

Table 7-715. PGRS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_RSP	R/W	0x0	Red Sub-Pixel: This field is the 8 least significant bits of the Red sub-pixel for the custom color. If Sub pixel bits less than 10, LSB bits are unused to generate custom color patterns. For 24 BPP: bits 1:0 are unused For 18 BPP: bits 3:0 are unused For 30 BPP: all bits are used

7.6.3.2 PGRS2 Register (Address = 0x1) [Default = 0x00]

PGRS2 is shown in Table 7-716.

Return to the Summary Table.

Table 7-716. PGRS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PATGEN_RSP	R/W	0x0	Red Sub-Pixel: This field is the most significant bits of the Red sub-pixel for the custom color. Configure the MSB Values for all BPP

7.6.3.3 PGGS1 Register (Address = 0x2) [Default = 0x00]

PGGS1 is shown in Table 7-717.

Return to the Summary Table.

Table 7-717. PGGS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_GSP	R/W	0x0	Green Sub-Pixel: This field is the 8 least significant bits of the Green sub-pixel for the custom color. If Sub pixel bits less than 10, LSB bits are unused to generate custom color patterns. For 24 BPP: bits 1:0 are unused For 18 BPP: bits 3:0 are unused For 30 BPP: all bits are used

7.6.3.4 PGGS2 Register (Address = 0x3) [Default = 0x00]

PGGS2 is shown in Table 7-718.

Return to the Summary Table.

Table 7-718. PGGS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PATGEN_GSP	R/W	0x0	Green Sub-Pixel: This field is the most significant bits of the Green sub-pixel for the custom color. Configure MSB Values for all BPP

7.6.3.5 PGBS1 Register (Address = 0x4) [Default = 0x00]

PGBS1 is shown in Table 7-719.

Return to the Summary Table.

Table 7-719. PGBS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_BSP	R/W	0x0	Blue Sub-Pixel: This field is the 8 least significant bits of the Blue sub-pixel for the custom color. If Sub pixel bits less than 10, LSB bits are unused to generate custom color patterns. For 24 BPP: bits 1:0 are unused For 18 BPP: bits 3:0 are unused For 30 BPP: all bits are used.

7.6.3.6 PGBS2 Register (Address = 0x5) [Default = 0x00]

PGBS2 is shown in Table 7-720.

Return to the Summary Table.

Table 7-720. PGBS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PATGEN_BSP	R/W	0x0	Blue Sub-Pixel: This field is the most significant bits of the Blue sub-pixel for the custom color. Configure MSB Values for all BPP

7.6.3.7 PGTFS1 Register (Address = 0x6) [Default = 0x98]

PGTFS1 is shown in Table 7-721.

Return to the Summary Table.

Table 7-721. PGTFS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_THW	R/W	0x98	Total Horizontal Width: This field is the 8 least significant bits of the 16-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.8 PGTFS2 Register (Address = 0x7) [Default = 0x08]

PGTFS2 is shown in Table 7-722.

Return to the Summary Table.

Table 7-722. PGTFS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_THW	R/W	0x8	Total Horizontal Width: This field is the 8 most significant bits of the 16-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.9 PGTFS3 Register (Address = 0x8) [Default = 0x65]

PGTFS3 is shown in Table 7-723.

Return to the Summary Table.

Table 7-723. PGTFS3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_TVW	R/W	0x65	Total Vertical Width: This field is the 8 least significant bits of the 16-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.10 PGTFS4 Register (Address = 0x9) [Default = 0x04]

PGTFS4 is shown in Table 7-724.

Return to the Summary Table.

Table 7-724. PGTFS4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_TVW	R/W	0x4	Total Vertical Width: This field is the 8 most significant bits of the 16-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.11 PGAFS1 Register (Address = 0xA) [Default = 0x80]

PGAFS1 is shown in Table 7-725.

Return to the Summary Table.

Table 7-725. PGAFS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AHW	R/W	0x80	Active Horizontal Width: This field is the 8 least significant bits of the 16-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.12 PGAFS2 Register (Address = 0xB) [Default = 0x07]

PGAFS2 is shown in Table 7-726.

Return to the Summary Table.

Table 7-726. PGAFS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_AHW	R/W	0x7	Active Horizontal Width: This field is the 8 most significant bits of the 16-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.13 PGAFS3 Register (Address = 0xC) [Default = 0x38]

PGAFS3 is shown in Table 7-727.

Return to the Summary Table.

Table 7-727. PGAFS3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AVW	R/W	0x38	Active Vertical Width: This field is the 8 least significant bits of the 16-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.14 PGAFS4 Register (Address = 0xD) [Default = 0x04]

PGAFS4 is shown in Table 7-728.

Return to the Summary Table.

Table 7-728. PGAFS4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AVW	R/W	0x4	Active Vertical Width: This field is the 8 most significant bits of the 16-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.15 PGHSW1 Register (Address = 0xE) [Default = 0x2C]

PGHSW1 is shown in Table 7-729.

Return to the Summary Table.

Table 7-729. PGHSW1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_HSW	R/W	0x2C	Horizontal Sync Width: This field controls the 8 least significant bits of the 12-bit Horizontal Sync pulse, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.16 PGHSW2 Register (Address = 0xF) [Default = 0x00]

PGHSW2 is shown in Table 7-730.

Return to the Summary Table.

Table 7-730. PGHSW2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_HSW	R/W	0x0	Horizontal Sync Width: This field controls the 4 most significant bits of the 12-bit Horizontal Sync pulse, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.17 PGVSW1 Register (Address = 0x10) [Default = 0x05]

PGVSW1 is shown in Table 7-731.

Return to the Summary Table.

Table 7-731. PGVSW1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_VSW	R/W	0x5	Vertical Sync Width: This field controls the 8 least significant bits of the 12-bit Vertical Sync pulse, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.18 PGVSW2 Register (Address = 0x11) [Default = 0x00]

PGVSW2 is shown in Table 7-732.

Return to the Summary Table.

Table 7-732. PGVSW2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

Table 7-732. PGVSW2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	PATGEN_VSW	R/W	0x0	Vertical Sync Width: This field controls the 4 most significant bits of the 12-bit Vertical Sync pulse, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.19 PGHBP1 Register (Address = 0x12) [Default = 0x94]

PGHBP1 is shown in Table 7-733.

Return to the Summary Table.

Table 7-733. PGHBP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_HBP	R/W	0x94	Horizontal Back Porch Width: This field controls the 8 least significant bits of the 12-bit Horizontal Back Porch, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.20 PGHBP2 Register (Address = 0x13) [Default = 0x00]

PGHBP2 is shown in Table 7-734.

Return to the Summary Table.

Table 7-734. PGHBP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_HBP	R/W	0x0	Horizontal Back Porch Width: This field controls the 4 most significant bits of the 12-bit Horizontal Back Porch, in units of pixels. This field should only be written when the pattern generator is disabled.

7.6.3.21 PGVBP1 Register (Address = 0x14) [Default = 0x24]

PGVBP1 is shown in Table 7-735.

Return to the Summary Table.

Table 7-735. PGVBP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RESERVED	R/W	0x24	Reserved

7.6.3.22 PGVBP2 Register (Address = 0x15) [Default = 0x00]

PGVBP2 is shown in Table 7-736.

Return to the Summary Table.

Table 7-736. PGVBP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_VBP	R/W	0x0	Vertical Back Porch Width: This field controls the 4 most significant bits of the 12-bit Vertical Back Porch, in units of lines. This field should only be written when the pattern generator is disabled.

7.6.3.23 PBSC Register (Address = 0x16) [Default = 0x03]

PBSC is shown in Table 7-737.

Return to the Summary Table.

Table 7-737. PBSC Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	PATGEN_VS_DIS	R/W	0x0	Vertical Sync Disable: Disable Vertical Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
2	PATGEN_HS_DIS	R/W	0x0	Horizontal Sync Disable: Disable Horizontal Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
1	PATGEN_VS_POL	R/W	0x1	Vertical Sync Polarity: When 1, the pattern generator will invert the Vertical Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
0	PATGEN_HS_POL	R/W	0x1	Horizontal Sync Polarity: When 1, the pattern generator will invert the Horizontal Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled

7.6.3.24 PGFT Register (Address = 0x17) [Default = 0x1E]

PGFT is shown in Table 7-738.

Return to the Summary Table.

Table 7-738. PGFT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_FTIME	R/W	0x1E	Frame Time: When Auto-Scrolling is enabled, this field controls the number of frames to display each pattern in increments of two frames. Valid register values are 1-255, giving a programmable range of even numbers between 2 and 510, inclusive.

7.6.3.25 PGTSC Register (Address = 0x18) [Default = 0x10]

PGTSC is shown in Table 7-739.

Return to the Summary Table.

Table 7-739. PGTSC Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TSLOT	R/W	0x10	Time Slots: This field configures the number of enabled time slots for Auto-Scrolling. Valid Values are 1-16

7.6.3.26 PGTSO1 Register (Address = 0x19) [Default = 0x01]

PGTSO1 is shown in Table 7-740.

Return to the Summary Table.

Table 7-740. PGTSO1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS1	R/W	0x1	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.27 PGTSO2 Register (Address = 0x1A) [Default = 0x02]

PGTSO2 is shown in Table 7-741.

Return to the Summary Table.

Table 7-741. PGTSO2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS2	R/W	0x2	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.28 PGTSO3 Register (Address = 0x1B) [Default = 0x03]

PGTSO3 is shown in Table 7-742.

Return to the Summary Table.

Table 7-742. PGTSO3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS3	R/W	0x3	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.29 PGTSO4 Register (Address = 0x1C) [Default = 0x04]

PGTSO4 is shown in Table 7-743.

Return to the Summary Table.

Table 7-743. PGTSO4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS4	R/W	0x4	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.30 PGTSO5 Register (Address = 0x1D) [Default = 0x05]

PGTSO5 is shown in Table 7-744.

Return to the Summary Table.

Table 7-744. PGTSO5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS5	R/W	0x5	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.31 PGTSO6 Register (Address = 0x1E) [Default = 0x06]

PGTSO6 is shown in Table 7-745.

Return to the Summary Table.

Table 7-745. PGTSO6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS6	R/W	0x6	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.32 PGTSO7 Register (Address = 0x1F) [Default = 0x07]

PGTSO7 is shown in Table 7-746.

Return to the Summary Table.

Table 7-746. PGTSO7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS7	R/W	0x7	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.33 PGTSO8 Register (Address = 0x20) [Default = 0x08]

PGTSO8 is shown in Table 7-747.

Return to the Summary Table.

Table 7-747. PGTSO8 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS8	R/W	0x8	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.34 PGTSO9 Register (Address = 0x21) [Default = 0x09]

PGTSO9 is shown in Table 7-748.

Return to the Summary Table.

Table 7-748. PGTSO9 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS9	R/W	0x9	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.35 PGTSO10 Register (Address = 0x22) [Default = 0x0A]

PGTSO10 is shown in Table 7-749.

Return to the Summary Table.

Table 7-749. PGTSO10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS10	R/W	0xA	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.36 PGTSO11 Register (Address = 0x23) [Default = 0x0B]

PGTSO11 is shown in Table 7-750.

Return to the Summary Table.

Table 7-750. PGTSO11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS11	R/W	0xB	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.37 PGTSO12 Register (Address = 0x24) [Default = 0x0C]

PGTSO12 is shown in Table 7-751.

Return to the Summary Table.

Table 7-751. PGTSO12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS12	R/W	0xC	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.38 PGTSO13 Register (Address = 0x25) [Default = 0x0D]

PGTSO13 is shown in Table 7-752.

Return to the Summary Table.

Table 7-752. PGTSO13 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS13	R/W	0xD	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.39 PGTSO14 Register (Address = 0x26) [Default = 0x0E]

PGTSO14 is shown in Table 7-753.

Return to the Summary Table.

Table 7-753. PGTSO14 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS14	R/W	0xE	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.40 PGTSO15 Register (Address = 0x27) [Default = 0x0F]

PGTSO15 is shown in Table 7-754.

Return to the Summary Table.

Table 7-754. PGTSO15 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS15	R/W	0xF	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.41 PGTSO16 Register (Address = 0x28) [Default = 0x10]

PGTSO16 is shown in Table 7-755.

Return to the Summary Table.

Table 7-755. PGTSO16 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS16	R/W	0x10	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

7.6.3.42 PGCE Register (Address = 0x29) [Default = 0x00]

PGCE is shown in Table 7-756.

Return to the Summary Table.

Table 7-756. PGCE Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_CHK_ERRS		0x0	Pattern Checker Pixel Errors: This field indicates the number of errors encountered during pattern checking, up to a maximum of 255. The value is cleared upon read.

7.6.3.43 PGUPS Register (Address = 0x2A) [Default = 0x00]

PGUPS is shown in Table 7-757.

Return to the Summary Table.

Table 7-757. PGUPS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:1	PATGEN_UNH1S_SCALE	R/W	0x0	Scale the divider for one-second mode of UNH compliance test pattern The 1-second duration is scaled by 2N, where N is the value of this field. 000: 1 second 001: 1/2 second 010: 1/4 second 011: 1/8 second 100: 1/16 second 101: 1/32 second 110: 1/64 second 111: 1/128 second
0	PATGEN_UNH1S	R/W	0x0	One-second mode of UNH compliance test pattern 0: the UNH compliance test pattern is sent out as defined in the timing control registers 1: Each line of the UNH compliance test pattern is sent out roughly 1 second apart.

7.6.3.44 PGCF Register (Address = 0x2B) [Default = 0x00]

PGCF is shown in Table 7-758.

Return to the Summary Table.

Table 7-758. PGCF Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_CHK_FRAME_CNT		0x0	Pattern Checker Frame Counts: This field indicates the number of frames received during pattern checking, up to a maximum of 255. The value is cleared upon read.

7.6.3.45 PGFC Register (Address = 0x2C) [Default = 0x00]

PGFC is shown in Table 7-759.

Return to the Summary Table.

Table 7-759. PGFC Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ FRAME_CNT		0x0	Pattern Generator Frame Counts: This field indicates the number of frames generated/detected by the pattern generator, up to a maximum of 255. The value is cleared upon read.

7.6.3.46 PGCEF Register (Address = 0x2D) [Default = 0x00]

PGCEF is shown in Table 7-760.

Return to the Summary Table.

Table 7-760. PGCEF Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_CHK_ERR_FRAME_CNT		0x0	Pattern Checker Error Frame Counts: This field indicates the number of frames received with errors during pattern checking, up to a maximum of 255. The value is cleared upon read.

7.6.3.47 PGPRS1 Register (Address = 0x2E) [Default = 0x01]

PGPRS1 is shown in Table 7-761.

Return to the Summary Table.

Table 7-761. PGPRS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SEED1	R/W	0x1	Pseudo-Random Pattern Generator SubSeed1: This field sets bits 7:0 of the starting seed for use by the pseudo-random pattern generator. It should be set only before enabling the Random Pattern Generation Select bit (bit 2 of PGDBG register). Registers PGPRS1-6 should together not be programmed zero to avoid lockup. HW will override PGPRS1 to 1 in this case.

7.6.3.48 PGPRS2 Register (Address = 0x2F) [Default = 0x00]

PGPRS2 is shown in Table 7-762.

Return to the Summary Table.

Table 7-762. PGPRS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SEED2	R/W	0x0	Pseudo-Random Pattern Generator SubSeed2: This field sets bits 15:8 of the starting seed for use by the pseudo-random pattern generator. It should be set only before enabling the Random Pattern Generation Select bit (bit 2 of PGDBG register). Registers PGPRS1-6 should together not be programmed zero to avoid lockup. HW will override PGPRS1 to 1 in this case.

7.6.3.49 PGPRS3 Register (Address = 0x30) [Default = 0x00]

PGPRS3 is shown in Table 7-763.

Return to the Summary Table.

Table 7-763. PGPRS3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SEED3	R/W	0x0	Pseudo-Random Pattern Generator SubSeed3: This field sets bits 23:16 of the starting seed for use by the pseudo-random pattern generator. It should be set only before enabling the Random Pattern Generation Select bit (bit 2 of PGDBG register). Registers PGPRS1-6 should together not be programmed zero to avoid lockup. HW will override PGPRS1 to 1 in this case.

7.6.3.50 PGPRS4 Register (Address = 0x31) [Default = 0x00]

PGPRS4 is shown in Table 7-764.

Return to the Summary Table.

Table 7-764. PGPRS4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SEED4	R/W	0x0	Pseudo-Random Pattern Generator SubSeed4: This field sets bits 31:24 of the starting seed for use by the pseudo-random pattern generator. It should be set only before enabling the Random Pattern Generation Select bit (bit 2 of PGDBG register). Registers PGPRS1-6 should together not be programmed zero to avoid lockup. HW will override PGPRS1 to 1 in this case. This register is not used in 8 bits/subpixel mode. Only bits 5:0 are valid in 10 bits/subpixel mode.

7.6.3.51 PGPRS5 Register (Address = 0x32) [Default = 0x00]

PGPRS5 is shown in Table 7-765.

Return to the Summary Table.

Table 7-765. PGPRS5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SEED5	R/W	0x0	Pseudo-Random Pattern Generator SubSeed5: This field sets bits 39:32 of the starting seed for use by the pseudo-random pattern generator. It should be set only before enabling the Random Pattern Generation Select bit (bit 2 of PGDBG register). Registers PGPRS1-6 should together not be programmed zero to avoid lockup. HW will override PGPRS1 to 1 in this case. This register is not used in 8 and 10 bits/subpixel modes. Only bits 3:0 are valid in 12 bits/subpixel mode.

7.6.3.52 PGPRS6 Register (Address = 0x33) [Default = 0x00]

PGPRS6 is shown in Table 7-766.

Return to the Summary Table.

Table 7-766. PGPRS6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SEED6	R/W	0x0	Pseudo-Random Pattern Generator SubSeed6: This field sets bits 47:40 of the starting seed for use by the pseudo-random pattern generator. It should be set only before enabling the Random Pattern Generation Select bit (bit 2 of PGDBG register). Registers PGPRS1-6 should together not be programmed zero to avoid lockup. HW will override PGPRS1 to 1 in this case. This register is not used in 8, 10 and 12 bits/subpixel modes.

7.6.3.53 PGPRSF Register (Address = 0x34) [Default = 0x03]

PGPRSF is shown in Table 7-767.

Return to the Summary Table.

Table 7-767. PGPRSF Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_PRBS_SER_START_FRAME	R/W	0x3	Pseudo-Random Pattern Generator Serializer Start Frame: This field sets the frame number from which PRBS patterns are triggered in the serializer. It is required in order to correctly sync with start of PRBS pattern generation in the deserializer operating in checker mode (see Section 4.5.4 for details). It should be set only when PRBS mode is disabled (PATGEN_RAND bit, PGDBG register bit 2). First frame is assigned the number 1.

7.6.3.54 PGEILSL Register (Address = 0x35) [Default = 0x00]

PGEILSL is shown in Table 7-768.

Return to the Summary Table.

Table 7-768. PGEILSL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_LINE_START_L	R/W	0x0	Error Injection Active Line Count Start Low: This field sets the lower 8 bits of the starting active line number from where to inject errors. Active line numbers start from 0 and go upto (configured/detected active line width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.55 PGEILSH Register (Address = 0x36) [Default = 0x00]

PGEILSH is shown in Table 7-769.

Return to the Summary Table.

Table 7-769. PGEILSH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_LINE_START_H	R/W	0x0	Error Injection Active Line Count Start High: This field sets the upper 8 bits of the starting active line number from where to inject errors. Active line numbers start from 0 and go upto (configured/detected active line width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.56 PGEILEL Register (Address = 0x37) [Default = 0x00]

PGEILEL is shown in Table 7-770.

Return to the Summary Table.

Table 7-770. PGEILEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_LINE_END_L	R/W	0x0	Error Injection Active Line Count End Low: This register sets the lower 8 bits of the ending active line number at which injected errors should stop. Active line numbers start from 0 and go upto (configured/detected active line width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.57 PGEILEH Register (Address = 0x38) [Default = 0x00]

PGEILEH is shown in Table 7-771.

Return to the Summary Table.

Table 7-771. PGEILEH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_LINE_END_H	R/W	0x0	Error Injection Active Line Count End High: This register sets the lower 8 bits of the ending active line number at which injected errors should stop. Active line numbers start from 0 and go upto (configured/detected active line width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.58 PGEIPSL Register (Address = 0x39) [Default = 0x00]

PGEIPSL is shown in Table 7-772.

Return to the Summary Table.

Table 7-772. PGEIPSL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_PXL_START_L	R/W	0x0	Error Injection Active Pixel Count Start Low: This field sets the lower 8 bits of the starting active pixel number from where to inject errors. Active pixel numbers start from 0 and go upto (configured/detected active pixel width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.59 PGEIPSH Register (Address = 0x3A) [Default = 0x00]

PGEIPSH is shown in Table 7-773.

Return to the Summary Table.

Table 7-773. PGEIPSH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_PXL_START_H	R/W	0x0	Error Injection Active Pixel Count Start High: This field sets the upper 8 bits of the starting active pixel number from where to inject errors. Active pixel numbers start from 0 and go upto (configured/detected active pixel width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.60 PGEIPEL Register (Address = 0x3B) [Default = 0x00]

PGEIPEL is shown in Table 7-774.

Return to the Summary Table.

Table 7-774. PGEIPEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_PXL_END_L	R/W	0x0	Error Injection Active Pixel Count End Low: This register sets the lower 8 bits of the ending active pixel number at which injected errors should stop. Active pixel numbers start from 0 and go upto (configured/detected active pixel width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.3.61 PGEIPEH Register (Address = 0x3C) [Default = 0x00]

PGEIPEH is shown in Table 7-775.

Return to the Summary Table.

Table 7-775. PGEIPEH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ERR_INJ_PXL_END_H	R/W	0x0	Error Injection Active Pixel Count End High: This register sets the lower 8 bits of the ending active pixel number at which injected errors should stop. Active pixel numbers start from 0 and go upto (configured/detected active pixel width – 1). This field should only be written to when error injection is disabled (bit 3 PATGEN_ERR_INJ of PGDBG register)

7.6.4 APB (DP RX) Registers

The APB registers are accessed indirectly using 0x48 - 0x4E registers in Main Page.

This indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the APB_CTL (0x48) register to select the desired register block and enable the APB interface
2. Write to the APB_ADR0 (0x49) and APB_ADR1 (0x4A) registers to set the register offset
3. Write the data value to the APB_DATA0 (0x4B), APB_DATA1 (0x4C), APB_DATA2 (0x4D), and APB_DATA3 (0x4E) registers

If auto-increment is set in the APB_CTL register, repeating Step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the APB_ADR0 (0x49) and APB_ADR1 (0x4A) registers to set the register offset
2. Write to the APB_CTL (0x48) register to select the desired register block, enable the APB interface, and start APB read
3. Read the data value from the APB_DATA0 (0x4B), APB_DATA1 (0x4C), APB_DATA2 (0x4D), and APB_DATA3 (0x4E) registers

If auto-increment is set in the APB_CTL register, repeating Step 3 will read additional data bytes from subsequent register offset locations.

When PDB is toggled low to high or digital reset using 0x01[1] or 0x01[0] is applied, any configurations of the APB registers will be reset. These registers will be re-programmed to the default values in the order of this Table 7-776.

Table 7-776. APB POR Default Values

APB Address (16-bit)	Reset Default Values (32-bit)	Comment
0x0	0x00000000	Disable core
0x4	0x00000064	Set AUX clock divider to 100MHz
0x28	0x00000000	Clear AUX request count
0x98	0x00000001	Set audio unsupported
0x94	0x00000001	Set video unsupported
0x0	0x00000001	Enable core
0xA14	0x00000000	Disable DTG
0x18	STRAP	MST and DP/eDP configuration based on strap mode setting MODE_SEL1
0xA28	0x00003020	Set display timing generator
0x2C	0x00000001	Assert interrupt via HPD signal
0x0	0x00000000	Disable core
0xA14	0x00000001	Enable DTG
0xA18	0x00000001	Disable filter on for MSA values
0x98	0x00000000	Clear audio unsupported
0x94	0x00000000	Clear video unsupported
0xA80	0x00000001	Enable secondary channel
0xA84	0x00000000	Disable audio mute
0xA88	0x00000000	Disable secondary data packet
0xA8C	0x00000018	Set audio sample
0xA90	0x00000004	Set audio channel count

Table 7-776. APB POR Default Values (continued)

APB Address (16-bit)	Reset Default Values (32-bit)	Comment
0xA94	0x00000000	Disable inforframe

The APB registers table only lists 0xA00 - 0xAFF for Virtual Sink 0. For Virtual Sink 1, the 0xB00 - 0xBFF registers are identical to registers 0xA00 - 0xAFF as applied to Virtual Sink 1.

7.6.4.1 APB Registers

Table 7-777 lists the memory-mapped registers for the APB registers. All register offset addresses not listed in Table 7-777 should be considered as reserved locations and the register contents should not be modified.

Table 7-777. APB Registers

Address	Acronym	Register Name	Section
0x0	APB_LINK_ENABLE	APB_LINK_ENABLE	Go
0x18	APB_MISC_CONFIG	APB_MISC_CONFIG	Go
0x1C	APB_DISPLAYPORT_VERSION	APB_DISPLAYPORT_VERSION	Go
0x24	APB_REQUEST_ERROR_COUNT	APB_REQUEST_ERROR_COUNT	Go
0x28	APB_REQUEST_COUNT	APB_REQUEST_COUNT	Go
0x30	APB_LANE_REMAP	APB_LANE_REMAP	Go
0x54	APB_VIDEO_INPUT_RESET	APB_VIDEO_INPUT_RESET	Go
0x58	APB_EDP_IGNORE_MSA	APB_EDP_IGNORE_MSA	Go
0x70	APB_MAX_LANE_COUNT	APB_MAX_LANE_COUNT	Go
0x74	APB_MAX_LINK_RATE	APB_MAX_LINK_RATE	Go
0x8C	APB_REMOTE_COMMAND	APB_REMOTE_COMMAND	Go
0x90	APB_REMOTE_COMMAND_NEW	APB_REMOTE_COMMAND_NEW	Go
0x94	APB_VIDEO_UNSUPPORTED	APB_VIDEO_UNSUPPORTED	Go
0x98	APB_AUDIO_UNSUPPORTED	APB_AUDIO_UNSUPPORTED	Go
0x180	APB_INTERRUPT_MASK	APB_INTERRUPT_MASK	Go
0x184	APB_INTERRUPT_STATE	APB_INTERRUPT_STATE	Go
0x188	APB_INTERRUPT_CAUSE	APB_INTERRUPT_CAUSE	Go
0x18C	APB_EVENT_INTERRUPT_ENABLE	APB_EVENT_INTERRUPT_ENABLE	Go
0x190	APB_SINK_0_INTERRUPT_MASK	APB_SINK_0_INTERRUPT_MASK	Go
0x194	APB_SINK_0_INTERRUPT_CAUSE	APB_SINK_0_INTERRUPT_CAUSE	Go
0x198	APB_SINK_1_INTERRUPT_MASK	APB_SINK_1_INTERRUPT_MASK	Go
0x19C	APB_SINK_1_INTERRUPT_CAUSE	APB_SINK_1_INTERRUPT_CAUSE	Go
0x208	APB_PHY_STATUS	APB_PHY_STATUS	Go
0x214	APB_MIN_VOLTAGE_SWING	APB_MIN_VOLTAGE_SWING	Go
0x218	APB_MIN_PRE_EMPHASIS	APB_MIN_PRE_EMPHASIS	Go
0x220	APB_FIXED_ADJUST_REQUEST	APB_FIXED_ADJUST_REQUEST	Go
0x400	APB_DPCD_LINK_BW_SET	APB_DPCD_LINK_BW_SET	Go
0x404	APB_DPCD_LANE_COUNT_SET	APB_DPCD_LANE_COUNT_SET	Go
0x40C	APB_DPCD_TRAINING_PATTERN_SET	APB_DPCD_TRAINING_PATTERN_SET	Go
0x410	APB_DPCD_LINK_QUALITY_PATTERN_SET	APB_DPCD_LINK_QUALITY_PATTERN_SET	Go
0x414	APB_DPCD_RECOVERED_CLOCK_OUT_EN	APB_DPCD_RECOVERED_CLOCK_OUT_EN	Go
0x418	APB_DPCD_SCRAMBLING_DISABLE	APB_DPCD_SCRAMBLING_DISABLE	Go

Table 7-777. APB Registers (continued)

Address	Acronym	Register Name	Section
0x41C	APB_DPCD_SYMBOL_ERROR_COUNT_SELECT	APB_DPCD_SYMBOL_ERROR_COUNT_SELECT	Go
0x420	APB_DPCD_TRAINING_LANE_0_SET	APB_DPCD_TRAINING_LANE_0_SET	Go
0x424	APB_DPCD_TRAINING_LANE_1_SET	APB_DPCD_TRAINING_LANE_1_SET	Go
0x428	APB_DPCD_TRAINING_LANE_2_SET	APB_DPCD_TRAINING_LANE_2_SET	Go
0x42C	APB_DPCD_TRAINING_LANE_3_SET	APB_DPCD_TRAINING_LANE_3_SET	Go
0x430	APB_DPCD_DOWNSPREAD_CONTROL	APB_DPCD_DOWNSPREAD_CONTROL	Go
0x434	APB_DPCD_MAIN_LINK_CHANNEL_CODING_SET	APB_DPCD_MAIN_LINK_CHANNEL_CODING_SET	Go
0x43C	APB_DPCD_LANE01_STATUS	APB_DPCD_LANE01_STATUS	Go
0x440	APB_DPCD_LANE23_STATUS	APB_DPCD_LANE23_STATUS	Go
0x448	APB_DPCD_SOURCE_DEVICE_ID_0	APB_DPCD_SOURCE_DEVICE_ID_0	Go
0x44C	APB_DPCD_SOURCE_DEVICE_ID_1	APB_DPCD_SOURCE_DEVICE_ID_1	Go
0x450	APB_DPCD_SOURCE_REVISION	APB_DPCD_SOURCE_REVISION	Go
0x454	APB_TRAINING_LOST_CAUSE	APB_TRAINING_LOST_CAUSE	Go
0x47C	APB_MSA_TIMING_IGNORE	APB_MSA_TIMING_IGNORE	Go
0x480	APB_EDP_CONFIGURATION_SET	APB_EDP_CONFIGURATION_SET	Go
0x484	APB_DPCD_TRAINING_SCORE	APB_DPCD_TRAINING_SCORE	Go
0x48C	APB_MST_ENABLE	APB_MST_ENABLE	Go
0x500	APB_MSA_HRES	APB_MSA_HRES	Go
0x504	APB_MSA_HSPOL	APB_MSA_HSPOL	Go
0x508	APB_MSA_HSWIDTH	APB_MSA_HSWIDTH	Go
0x50C	APB_MSA_HSTART	APB_MSA_HSTART	Go
0x510	APB_MSA_HTOTAL	APB_MSA_HTOTAL	Go
0x514	APB_MSA_VRES	APB_MSA_VRES	Go
0x518	APB_MSA_VSPOL	APB_MSA_VSPOL	Go
0x51C	APB_MSA_VSWIDTH	APB_MSA_VSWIDTH	Go
0x520	APB_MSA_VSTART	APB_MSA_VSTART	Go
0x524	APB_MSA_VTOTAL	APB_MSA_VTOTAL	Go
0x528	APB_MSA_MISC0	APB_MSA_MISC0	Go
0x52C	APB_MSA_MISC1	APB_MSA_MISC1	Go
0x530	APB_MSA_MVID	APB_MSA_MVID	Go
0x534	APB_MSA_NVID	APB_MSA_NVID	Go
0x538	APB_MSA_VBID	APB_MSA_VBID	Go
0x540	APB_MSA_VIRTUAL_SINK_SELECT	APB_MSA_VIRTUAL_SINK_SELECT	Go
0x700	APB_TEST_REQUEST	APB_TEST_REQUEST	Go
0x704	APB_TEST_LANE_COUNT	APB_TEST_LANE_COUNT	Go
0x708	APB_TEST_LINK_RATE	APB_TEST_LINK_RATE	Go
0x904	APB_MST_PAYLOAD_ID_0	APB_MST_PAYLOAD_ID_0	Go

Table 7-777. APB Registers (continued)

Address	Acronym	Register Name	Section
0x908	APB_MST_PAYLOAD_ID_1	APB_MST_PAYLOAD_ID_1	Go
0x934	APB_MST_CLEAR_PAYLOAD_TABLE	APB_MST_CLEAR_PAYLOAD_TABLE	Go
0xA00	APB_MST_VIRTUAL_SINK_0_ENABLE	APB_MST_VIRTUAL_SINK_0_ENABLE	Go
0xA10	APB_MST_VS0_VIDEO_FIFO_OVERFLOW	APB_MST_VS0_VIDEO_FIFO_OVERFLOW	Go
0xA14	APB_MST_VS0_DTG_ENABLE	APB_MST_VS0_DTG_ENABLE	Go
0xA80	APB_MST_VS0_SECONDARY_ENABLE	APB_MST_VS0_SECONDARY_ENABLE	Go
0xA94	APB_MST_VS0_INFOFRAME_ADVANCE	APB_MST_VS0_INFOFRAME_ADVANCE	Go
0xB00	APB_MST_VIRTUAL_SINK_1_ENABLE	APB_MST_VIRTUAL_SINK_1_ENABLE	Go
0xB10	APB_MST_VS1_VIDEO_FIFO_OVERFLOW	APB_MST_VS1_VIDEO_FIFO_OVERFLOW	Go
0xB14	APB_MST_VS1_DTG_ENABLE	APB_MST_VS1_DTG_ENABLE	Go
0xB80	APB_MST_VS1_SECONDARY_ENABLE	APB_MST_VS1_SECONDARY_ENABLE	Go
0xB94	APB_MST_VS1_INFOFRAME_ADVANCE	APB_MST_VS1_INFOFRAME_ADVANCE	Go

Complex bit access types are encoded to fit into small table cells. Table 7-778 shows the codes that are used for access types in this section.

Table 7-778. APB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WStrap	W Strap	Write Default value loaded from bootstrap pin after reset.
Reset or Default Value		
-n		Value after reset or the default value

7.6.4.1.1 APB_LINK_ENABLE Register (Address = 0x0) [Default = 0x00000001]

APB_LINK_ENABLE is shown in Table 7-779.

Return to the Summary Table.

Enable the DisplayPort receiver core main link for video and secondary data transfer. This register also controls the value of the HPD signal. When this bit is 0, the HPD output signal will also be 0. AUX transactions should not be sent by the source device when the HPD line is a 0 and any AUX transactions received during this time will be ignored.

Table 7-779. APB_LINK_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	LINK_ENABLE	R/W	0x1	0x0 = HPD output signal will also be low. 0x1 = Enable the receiver core and set the HPD line high.

7.6.4.1.2 APB_MISC_CONFIG Register (Address = 0x18) [Default = 0x00000014]

APB_MISC_CONFIG is shown in Table 7-780.

Return to the Summary Table.

This multi-field control register contains bits that affect the behavior of the receiver core. Each bit contained in this register defaults to 0 at reset.

Table 7-780. APB_MISC_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
31:11	RESERVED	R/W	0x0	Reserved
10	RESERVED	R/W	0x0	Reserved
9	RESERVED	R/W	0x0	Reserved
8	MST_FUNCTION_ENABLE	R/WStrap	0x0	Enabling the MST function can be strapped using MODE_SEL1 pin. 0x0 = DPRX core will not report as MST capable to the source device. 0x1 = Enable support for the Multi-Stream Transport (MST) features.
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	EDP_FUNCTION_ENABLE	R/WStrap	0x0	Enabling the eDP function can be strapped using MODE_SEL1 pin. 0x0 = eDP operations will be disabled and the core will not report eDP functionality through the DPCD register set. 0x1 = Enable support for the Embedded DisplayPort functionality.
4	RESERVED	R/W	0x1	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x1	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

7.6.4.1.3 APB_DISPLAYPORT_VERSION Register (Address = 0x1C) [Default = 0x00000014]

APB_DISPLAYPORT_VERSION is shown in Table 7-781.

Return to the Summary Table.

DisplayPort revision level reported through the DPCD register set. This is the reported version supported only and does not change the operation of the DPRx core.

Table 7-781. APB_DISPLAYPORT_VERSION Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R/W	0x0	Reserved
7:0	DISPLAYPORT_VERSION	R/W	0x14	Revision level support as reported through the DPCD register set.

7.6.4.1.4 APB_REQUEST_ERROR_COUNT Register (Address = 0x24) [Default = 0x00000000]

APB_REQUEST_ERROR_COUNT is shown in Table 7-782.

Return to the Summary Table.

Provides a running total of errors detected on inbound AUX Channel requests. When an improperly formatted AUX request is made, the internal AUX controller will flag an error and increment this register by 1. The value of this register is cleared by writing a 0 to the REQUEST_COUNT register.

Table 7-782. APB_REQUEST_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
31:4	RESERVED	R	0x0	Reserved
3:0	REQUEST_ERROR_COUNT	R	0x0	Total number of AUX request transactions detected with errors.

7.6.4.1.5 APB_REQUEST_COUNT Register (Address = 0x28) [Default = 0x00000000]

APB_REQUEST_COUNT is shown in Table 7-783.

Return to the Summary Table.

Provides a running total of the number of AUX Request transactions received. This register is updated after the request is received and before the reply is generated. The value of this register is cleared when a 0 is written to this register.

Table 7-783. APB_REQUEST_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R/W	0x0	Reserved
7:0	REQUEST_COUNT	R/W	0x0	Total number of AUX request transactions detected. This count includes native AUX and I2C-over-AUX transactions.

7.6.4.1.6 APB_LANE_REMAP Register (Address = 0x30) [Default = 0x00000000]

APB_LANE_REMAP is shown in Table 7-784.

Return to the Summary Table.

Used to map the physical lanes of the DisplayPort link to the internal processing lanes of the controller. Using these register bits, any of the four physical lanes may be mapped to any other internal lane for processing.

Table 7-784. APB_LANE_REMAP Register Field Descriptions

Bit	Field	Type	Default	Description
31:20	RESERVED	R/W	0x0	Reserved
19	INVERT_LANE_3	R/W	0x0	Inverts the state of all bits received from the PHY layer on lane 3.
18	INVERT_LANE_2	R/W	0x0	Inverts the state of all bits received from the PHY layer on lane 2.
17	INVERT_LANE_1	R/W	0x0	Inverts the state of all bits received from the PHY layer on lane 1.
16	INVERT_LANE_0	R/W	0x0	Inverts the state of all bits received from the PHY layer on lane 0.
15:9	RESERVED	R/W	0x0	Reserved
8	REMAP_ENABLE	R/W	0x0	0x0 = When set to a 0, the other bits of the LANE_REMAP control register will be ignored. 0x1 = Set to a 1 to enable the remapping function.
7:6	REMAP_LANE_3	R/W	0x0	Specifies which physical lane number (0-3) will be mapped to the internal lane 3.
5:4	REMAP_LANE_2	R/W	0x0	Specifies which physical lane number (0-3) will be mapped to the internal lane 2.
3:2	REMAP_LANE_1	R/W	0x0	Specifies which physical lane number (0-3) will be mapped to the internal lane 1.
1:0	REMAP_LANE_0	R/W	0x0	Specifies which physical lane number (0-3) will be mapped to the internal lane 0.

7.6.4.1.7 APB_VIDEO_INPUT_RESET Register (Address = 0x54) [Default = 0x00000000]

APB_VIDEO_INPUT_RESET is shown in Table 7-785.

Return to the Summary Table.

This individual control bit causes a synchronous reset to be generated to only the logic in the video input clock domain. The logic reset by this control bit includes the video capture and steering logic as well as the video data FIFOs.

Table 7-785. APB_VIDEO_INPUT_RESET Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	VIDEO_INPUT_RESET	R/W	0x0	Writing a 1 to this bit will issue the reset to the video capture clock domain logic. No internal control registers will be modified by this reset. This bit will always read as a 0.

7.6.4.1.8 APB_EDP_IGNORE_MSA Register (Address = 0x58) [Default = 0x00000000]

APB_EDP_IGNORE_MSA is shown in Table 7-786.

Return to the Summary Table.

When configured for eDP support, the EDP_IGNORE_MSA bit transmitted through the DPCD. A 1 indicates that the Sink device does not require the video mode timing parameters to be transmitted through the MSA.

Table 7-786. APB_EDP_IGNORE_MSA Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	EDP_IGNORE_MSA	R/W	0x0	The value of this bit is mirrored in the DPCD at offset 0x000007 bit 6.

7.6.4.1.9 APB_MAX_LANE_COUNT Register (Address = 0x70) [Default = 0x00000004]

APB_MAX_LANE_COUNT is shown in Table 7-787.

Return to the Summary Table.

The maximum number of lanes supported by the DisplayPort receiver core is specified through this control register. At reset, the value of the register is set to the top level core parameter pMAX_LANE_COUNT. The value of this register should be set before the LINK_ENABLE register bit is set to a 1. The DisplayPort source will access this value through offset 0x00002 of the DPCD.

Table 7-787. APB_MAX_LANE_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
31:5	RESERVED	R/W	0x0	Reserved
4:0	MAX_LANE_COUNT	R/W	0x4	Valid values for the maximum lane count are 1, 2 and 4. All other values should be considered reserved.

7.6.4.1.10 APB_MAX_LINK_RATE Register (Address = 0x74) [Default = 0x0000001E]

APB_MAX_LINK_RATE is shown in Table 7-788.

Return to the Summary Table.

Holds the maximum link rate supported by the DisplayPort receiver core. The value of this register is reported to the DisplayPort source device through the DPCD register set at address 0x00001.

Table 7-788. APB_MAX_LINK_RATE Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R/W	0x0	Reserved
7:0	MAX_LINK_RATE	R/W	0x1E	The value of this register should be set to the desired link rate divided by 27. Some example link rates are: 0x06 = 1.62Gbps 0x0A = 2.7 Gbps 0x14 = 5.4Gbps 0x1E = 8.1Gbps

7.6.4.1.11 APB_REMOTE_COMMAND Register (Address = 0x8C) [Default = 0x00000000]

APB_REMOTE_COMMAND is shown in Table 7-789.

Return to the Summary Table.

General byte for passing remote information to the transmitter. This byte is used in conjunction with the REMOTE_COMMAND_NEW and the HPD interrupt to pass remote information to the transmitter.

Table 7-789. APB_REMOTE_COMMAND Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R/W	0x0	Reserved
7:0	REMOTE_COMMAND	R/W	0x0	Remote data byte. This byte is passed through DPCD address 0x81000.

7.6.4.1.12 APB_REMOTE_COMMAND_NEW Register (Address = 0x90) [Default = 0x00000000]

APB_REMOTE_COMMAND_NEW is shown in Table 7-790.

Return to the Summary Table.

Indicates a new command present in the REMOTE_COMMAND register. The host should write this bit to a 1 to indicate a new remote command is present before asserting the HPD interrupt. This bit is cleared by the DisplayPort transmitter.

Table 7-790. APB_REMOTE_COMMAND_NEW Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	REMOTE_COMMAND_NEW	R/W	0x0	Set to a 1 to indicate a new command. On read, this bit will reflect the value of the DPCD register and will clear when a 1 is written to the DEVICE_SERVICE_IRQ_VECTOR register by the transmitter.

7.6.4.1.13 APB_VIDEO_UNSUPPORTED Register (Address = 0x94) [Default = 0x00000001]

APB_VIDEO_UNSUPPORTED is shown in Table 7-791.

Return to the Summary Table.

DPCD register bit to inform the transmitter that video data is not supported. The receiver core sets this bit after verifying the values in the received MSA registers. Please note that very few DisplayPort transmitters tested check this bit.

Table 7-791. APB_VIDEO_UNSUPPORTED Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	VIDEO_UNSUPPORTED	R/W	0x1	Set to a 1 when video data is not supported.

7.6.4.1.14 APB_AUDIO_UNSUPPORTED Register (Address = 0x98) [Default = 0x00000001]

APB_AUDIO_UNSUPPORTED is shown in Table 7-792.

Return to the Summary Table.

DPCD register bit to inform the transmitter that audio data is not supported. The receiver core verifies the values sent in the audio InfoFrame packet before setting this bit appropriately.

Table 7-792. APB_AUDIO_UNSUPPORTED Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	AUDIO_UNSUPPORTED	R/W	0x1	Set to a 1 when the current audio mode sent by the transmitter is not supported.

7.6.4.1.15 APB_INTERRUPT_MASK Register (Address = 0x180) [Default = X]

APB_INTERRUPT_MASK is shown in Table 7-793.

Return to the Summary Table.

Masks the specified interrupt sources from asserting the apb_int signal or being set in the INTERRUPT_CAUSE register. When set to a 1, the specified interrupt source is masked. This register resets to all 1s at power up resulting in all interrupt sources being masked. See the INTERRUPT_CAUSE register for a description of the individual interrupt sources.

Table 7-793. APB_INTERRUPT_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
31:23	RESERVED	R/W	0x0	Reserved
22:0	INTERRUPT_MASK	R/W	X	Interrupt mask register value. The state of this register does not change the value of the INTERRUPT_STATE register.

7.6.4.1.16 APB_INTERRUPT_STATE Register (Address = 0x184) [Default = 0x00000000]

APB_INTERRUPT_STATE is shown in Table 7-794.

Return to the Summary Table.

Maintains the raw state of the interrupt bit field before the interrupt mask has been applied. The bit fields of this register match those of the INTERRUPT_CAUSE register before masking.

Table 7-794. APB_INTERRUPT_STATE Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	INTERRUPT_STATE	R	0x0	Read interrupt state value

7.6.4.1.17 APB_INTERRUPT_CAUSE Register (Address = 0x188) [Default = 0x00000000]

APB_INTERRUPT_CAUSE is shown in Table 7-795.

Return to the Summary Table.

Indicates the cause of a pending host interrupt asserted through the apb_int control signal. Only unmasked interrupt sources are reflected in the state of this register. Individual bits are cleared by writing a 1 to the corresponding bit location.

Table 7-795. APB_INTERRUPT_CAUSE Register Field Descriptions

Bit	Field	Type	Default	Description
31:23	RESERVED	R/W	0x0	Reserved
22	RESERVED	R/W	0x0	Reserved

Table 7-795. APB_INTERRUPT_CAUSE Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
21	LANE_COUNT_CHANGE	R/W	0x0	Asserts when the DPCD register containing the current lane count has changed. The change in value does not verify that a valid lane count has been requested.
20	LINK_RATE_CHANGE	R/W	0x0	Asserts when the DPCD register containing the current link rate has changed. The change in value does not verify that a valid link rate has been requested.
19	RESERVED	R/W	0x0	Reserved
18	RESERVED	R/W	0x0	Reserved
17	RESERVED	R/W	0x0	Reserved
16	TRAINING_PATTERN_SET	R/W	0x0	Set when the core has detected a change in the training state of the core. This interrupt will be triggered by any change in the state of the DPCD register.
15	RESERVED	R/W	0x0	Reserved
14	RESERVED	R/W	0x0	Reserved
13	RESERVED	R/W	0x0	Reserved
12	RESERVED	R/W	0x0	Reserved
11	LINK_CONFIG_CHANGE	R/W	0x0	Asserts when either the DPCD register containing the current link rate or current lane count have changed. The change in value does not verify that a valid link rate or lane count has been requested.
10	RESERVED	R/W	0x0	Reserved
9	RESERVED	R/W	0x0	Reserved
8	TRAINING_COMPLETE	R/W	0x0	Set when the Rx core has successfully completed the training sequence for the number of enabled lanes. This interrupt will only occur when training has been complete for at least 512 microseconds.
7	TRAINING_LOST	R/W	0x0	This interrupt is set whenever the receiver has been trained and subsequently loses clock recovery, symbol lock or inter-lane alignment. This interrupt will only occur when training has been lost for at least 512 microseconds.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	VIRTUAL_SINK_1_INTERRUPT	R/W	0x0	Valid only in MST mode, this bit indicates that a sink specific interrupt has occurred. See the SINK_1_INTERRUPT_CAUSE register for a description of the conditions that can cause an interrupt.
0	VIRTUAL_SINK_0_INTERRUPT	R/W	0x0	In SST mode or MST mode, this bit indicates that a sink specific interrupt has occurred. See the SINK_0_INTERRUPT_CAUSE register for a description of the conditions that can cause an interrupt.

7.6.4.1.18 APB_EVENT_INTERRUPT_ENABLE Register (Address = 0x18C) [Default = X]

APB_EVENT_INTERRUPT_ENABLE is shown in Table 7-796.

Return to the Summary Table.

Enables the generation of event codes on the apb_event_code output of the DPRx core. When set to a 1, the associated internal interrupt will cause a change in the event code output and the toggling of the apb_event_update signal. The specific interrupts for this register are the same as those described in the INTERRUPT_CAUSE register.

Table 7-796. APB_EVENT_INTERRUPT_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	EVENT_INTERRUPT_ENABLE	R/W	X	Set to a 1 to allow the associated interrupt to generate a new event code output.

7.6.4.1.19 APB_SINK_0_INTERRUPT_MASK Register (Address = 0x190) [Default = 0x00000079]

APB_SINK_0_INTERRUPT_MASK is shown in Table 7-797.

Return to the Summary Table.

Masks the corresponding interrupt source from causing the VIRTUAL_SINK_0_INTERRUPT bit from being set in the INTERRUPT_CAUSE register. When a bit is set to a 1, the specified interrupt source is masked. This register resets to all 1s at power up indicating that all interrupt sources are masked. See the SINK_0_INTERRUPT_CAUSE register for a description of the individual interrupt sources.

Table 7-797. APB_SINK_0_INTERRUPT_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
31:7	RESERVED	R/W	0x0	Reserved
6:0	SINK_0_INTERRUPT_MASK	R/W	0x79	Interrupt mask register value.

7.6.4.1.20 APB_SINK_0_INTERRUPT_CAUSE Register (Address = 0x194) [Default = 0x00000000]

APB_SINK_0_INTERRUPT_CAUSE is shown in Table 7-798.

Return to the Summary Table.

Reports the cause of a pending virtual sink status interrupt asserted in the VIRTUAL_SINK_0_INTERRUPT bit of the INTERRUPT_CAUSE register. Only unmasked interrupt sources are reflected in the state of this register. All of these interrupt bits are cleared when the INTERRUPT_CAUSE register is cleared.

Table 7-798. APB_SINK_0_INTERRUPT_CAUSE Register Field Descriptions

Bit	Field	Type	Default	Description
31:7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	INFOFRAME_DEPTH	R	0x0	Set when the secondary channel processing logic has received the number of InfoFrame packets set by the SEC_INFOFRAME_INTERRUPT_DEPTH register.
4	RESERVED	R	0x0	Reserved
3	VERTICAL_BLANKING	R	0x0	This interrupt is set at the start of the vertical blanking interval as indicated by the VerticalBlanking_Flag in the VB-ID field.
2	NO_VIDEO	R	0x0	The receiver has detected the no video flags in the VBID field after active video has been received.
1	VIDEO_DETECT	R	0x0	The receiver has detected the start of active video transmission after the link has previously been in the no video state.
0	VIDEO_MODE_CHANGE	R	0x0	A change has been detected in the current video mode transmitted on the DisplayPort link as indicated by the MSA fields. The horizontal and vertical resolution parameters are monitored for changes.

7.6.4.1.21 APB_SINK_1_INTERRUPT_MASK Register (Address = 0x198) [Default = 0x00000079]

APB_SINK_1_INTERRUPT_MASK is shown in Table 7-799.

Return to the Summary Table.

Interrupt source mask register for virtual sink 1 in MST mode. The definition of this register is equivalent to the SINK_0_INTERRUPT_MASK register. In SST mode, this register will always be zero.

Table 7-799. APB_SINK_1_INTERRUPT_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
31:7	RESERVED	R/W	0x0	Reserved
6:0	SINK_1_INTERRUPT_MASK	R/W	0x79	Interrupt mask register value.

7.6.4.1.22 APB_SINK_1_INTERRUPT_CAUSE Register (Address = 0x19C) [Default = 0x00000000]

APB_SINK_1_INTERRUPT_CAUSE is shown in Table 7-800.

Return to the Summary Table.

Reports the cause of a pending virtual sink status interrupt asserted in the VIRTUAL_SINK_1_INTERRUPT bit of the INTERRUPT_CAUSE register. Only unmasked interrupt sources are reflected in the state of this register. All of these interrupt bits are cleared when the INTERRUPT_CAUSE register is cleared.

Table 7-800. APB_SINK_1_INTERRUPT_CAUSE Register Field Descriptions

Bit	Field	Type	Default	Description
31:7	RESERVED	R	0x0	Reserved
6:0	SINK_1_INTERRUPT_CAUSE	R	0x0	Interrupt cause register value. See the SINK_0_INTERRUPT_CAUSE register for a complete description of these bits.

7.6.4.1.23 APB_PHY_STATUS Register (Address = 0x208) [Default = 0x000000F0]

APB_PHY_STATUS is shown in Table 7-801.

Return to the Summary Table.

The receiver PHY uses this register address to report the current status of the functional elements of the implementation. This register reports the real-time value of these status signals. Reading from this register does not affect the value of any reported bits. Not all PHY implementations will support these status bits.

Table 7-801. APB_PHY_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
31:20	RESERVED	R	0x0	Reserved
19:16	RX_EQUALIZATION_DONE	R	0x0	Indicates to the link controller core training logic that the equalization phase has completed. The controller core uses this signal internally to qualify the completion of second phase of the link training process. A 1 indicates that equalization is complete. A 0 indicates that equalization has not been completed. Bits 11:8 reflect the status of lanes 3:0 respectively. The value of this bit is ignored for lanes that are not enabled by the DisplayPort source device.
15:12	SYMBOL_LOCK	R	0x0	Indicates that the lane has locked onto the correct symbol pattern on the main link. The PHY should only set this bit after the proper alignment of the bit serial data into valid 8 or 10-bit symbols. Lane 0 is bit 12.
11:8	RESERVED	R	0x0	Reserved
7:4	RX_CLOCK_LOCKED	R	0xF	A 1 indicates that clock recovery has completed and the receive data clock is stable. The link controller requires this status signal for the successful completion of the link training process. The clock and data recovery phase of the training process can only complete successfully when this status bit is set to a 1. The value of this bit is ignored for lanes that are not enabled by the DisplayPort source device.

Table 7-801. APB_PHY_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	RESERVED	R	0x0	Reserved

7.6.4.1.24 APB_MIN_VOLTAGE_SWING Register (Address = 0x214) [Default = 0x00000000]

APB_MIN_VOLTAGE_SWING is shown in Table 7-802.

Return to the Summary Table.

Some DisplayPort implementations require the transmitter to set a minimum voltage swing during training before the link can be reliably established. This register is used to set a minimum value which must be met in the TRAINING_LANEX_SET DPCD registers. The internal training logic will force training to fail until this value is met.

Table 7-802. APB_MIN_VOLTAGE_SWING Register Field Descriptions

Bit	Field	Type	Default	Description
31:2	RESERVED	R/W	0x0	Reserved
1:0	MIN_VOLTAGE_SWING	R/W	0x0	The minimum voltage swing setting matches the values defined in the DisplayPort specification for the TRAINING_LANEX_SET register.

7.6.4.1.25 APB_MIN_PRE_EMPHASIS Register (Address = 0x218) [Default = 0x00000000]

APB_MIN_PRE_EMPHASIS is shown in Table 7-803.

Return to the Summary Table.

Similar to the minimum voltage swing registers, the minimum pre-emphasis register defines a minimum pre-emphasis level that must be met by the transmitter before training will be allowed to complete successfully.

Table 7-803. APB_MIN_PRE_EMPHASIS Register Field Descriptions

Bit	Field	Type	Default	Description
31:2	RESERVED	R/W	0x0	Reserved
1:0	MIN_PRE_EMPHASIS	R/W	0x0	The minimum pre-emphasis setting matches the values defined in the DisplayPort specification for the TRAINING_LANEX_SET register.

7.6.4.1.26 APB_FIXED_ADJUST_REQUEST Register (Address = 0x220) [Default = 0x00000000]

APB_FIXED_ADJUST_REQUEST is shown in Table 7-804.

Return to the Summary Table.

Disables the automatic adjust request determination logic and holds the adjust request registers at a fixed value determined by the MIN_VOLTAGE_SWING and MIN_PRE_EMPHASIS registers.

Table 7-804. APB_FIXED_ADJUST_REQUEST Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	FIXED_ADJUST_REQUEST	R/W	0x0	Set to a 1 to fix the adjust request values at the predetermined levels.

7.6.4.1.27 APB_DPCD_LINK_BW_SET Register (Address = 0x400) [Default = 0x00000000]

APB_DPCD_LINK_BW_SET is shown in Table 7-805.

Return to the Summary Table.

The DPCD register reporting values are a copy of the settings written to the sink device by the DisplayPort source connected to the DPRx core. This is the DPCD value for the current link rate as set by the source device.

Table 7-805. APB_DPCD_LINK_BW_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R	0x0	Reserved
7:0	DPCD_LINK_BW_SET	R	0x0	The binary value representing the current link rate setting. For DisplayPort, this value is set to the current link symbol rate divided by 27.

7.6.4.1.28 APB_DPCD_LANE_COUNT_SET Register (Address = 0x404) [Default = 0x00000000]

APB_DPCD_LANE_COUNT_SET is shown in Table 7-806.

Return to the Summary Table.

This is the DPCD value for the number of lanes in use as set by the source device. The DisplayPort Rx device supports 1, 2 and 4 lanes.

Table 7-806. APB_DPCD_LANE_COUNT_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:5	RESERVED	R	0x0	Reserved
4:0	DPCD_LANE_COUNT_SET	R	0x0	The number of lanes currently in use as configured by the source device. The only valid values of this register are 1, 2 and 4.

7.6.4.1.29 APB_DPCD_TRAINING_PATTERN_SET Register (Address = 0x40C) [Default = 0x00000000]

APB_DPCD_TRAINING_PATTERN_SET is shown in Table 7-807.

Return to the Summary Table.

This is the DPCD value for the current training pattern as set by the transmitter. These are bits 2:0 of the DPCD register TRAINING_PATTERN_SET (0x102).

Table 7-807. APB_DPCD_TRAINING_PATTERN_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:3	RESERVED	R	0x0	Reserved
2:0	TRAINING_PATTERN_SET	R	0x0	Sets the link training pattern according to a three-bit code. 0x0 = Training pattern disabled 0x1 = Training Pattern 1 0x2 = Training Pattern 2 0x3 = Training Pattern 3 (HBR2) 0x7 = Training Pattern 4 (HBR3)

7.6.4.1.30 APB_DPCD_LINK_QUALITY_PATTERN_SET Register (Address = 0x410) [Default = 0x00000000]

APB_DPCD_LINK_QUALITY_PATTERN_SET is shown in Table 7-808.

Return to the Summary Table.

This is the DPCD value for current link quality pattern field of the DPCD training pattern register. These are bits 3:2 of the DPCD register TRAINING_PATTERN_SET (0x102).

Table 7-808. APB_DPCD_LINK_QUALITY_PATTERN_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:15	RESERVED	R	0x0	Reserved

Table 7-808. APB_DPCD_LINK_QUALITY_PATTERN_SET Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
14:12	LINK_QUALITY_3	R	0x0	Link quality pattern set for lane 3.
11	RESERVED	R	0x0	Reserved
10:8	LINK_QUALITY_2	R	0x0	Link quality pattern set for lane 2.
7	RESERVED	R	0x0	Reserved
6:4	LINK_QUALITY_1	R	0x0	Link quality pattern set for lane 1.
3	RESERVED	R	0x0	Reserved
2:0	LINK_QUALITY_PATTERN	R	0x0	Transmitter selected link quality pattern used for link integrity testing. 0x0 = Link quality pattern disabled 0x1 = Link quality pattern D10.2 0x2 = Link quality pattern Symbol Error Rate (unscrambled) 0x3 = Link quality pattern PRBS 7 0x4 = 80-bit custom pattern 0x5 = CP2520 Pattern 1 0x6 = CP2520 Pattern 2 0x7 = CP2520 Pattern 3

7.6.4.1.31 APB_DPCD_RECOVERED_CLOCK_OUT_EN Register (Address = 0x414) [Default = 0x00000000]

APB_DPCD_RECOVERED_CLOCK_OUT_EN is shown in Table 7-809.

Return to the Summary Table.

This is the current value of bit 4 of the DPCD register TRAINING_PATTERN_SET (0x102). The bit controls whether or not the clock recovered from the main link is output through the test port on the core.

Table 7-809. APB_DPCD_RECOVERED_CLOCK_OUT_EN Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	DPCD_RECOVERED_CLOCK_OUT_EN	R	0x0	Set to 1 to output the recovered receiver clock on the test port.

7.6.4.1.32 APB_DPCD_SCRAMBLING_DISABLE Register (Address = 0x418) [Default = 0x00000001]

APB_DPCD_SCRAMBLING_DISABLE is shown in Table 7-810.

Return to the Summary Table.

This is the current value of bit 5 of the DPCD register TRAINING_PATTERN_SET (0x102). This bit controls whether or not scrambling is enabled on the data symbols on the main link. Note that for device compatibility, the internal scrambling function will be automatically disabled when the DPCD_TRAINING_PATTERN_SET field is any value other than 00.

Table 7-810. APB_DPCD_SCRAMBLING_DISABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	DPCD_SCRAMBLING_DISABLE	R	0x1	Set to a 1 when the transmitter has disabled the scrambler and transmits all symbols. Set to a 0 for normal link operation.

7.6.4.1.33 APB_DPCD_SYMBOL_ERROR_COUNT_SELECT Register (Address = 0x41C) [Default = 0x00000000]

APB_DPCD_SYMBOL_ERROR_COUNT_SELECT is shown in Table 7-811.

Return to the Summary Table.

These are bits 7:6 of the DPCD register TRAINING_PATTERN_SET (0x102). This controls which symbol errors to count and accumulate in the symbol error count registers.

Table 7-811. APB_DPCD_SYMBOL_ERROR_COUNT_SELECT Register Field Descriptions

Bit	Field	Type	Default	Description
31:2	RESERVED	R	0x0	Reserved
1:0	SYMBOL_ERROR_COUNT_SEL	R	0x0	Selected error count field for link integrity testing. 0x0 = Disparity error and Illegal Symbol Error 0x1 = Disparity Error only 0x2 = Illegal Symbol error only 0x3 = Reserved

7.6.4.1.34 APB_DPCD_TRAINING_LANE_0_SET Register (Address = 0x420) [Default = 0x00000000]

APB_DPCD_TRAINING_LANE_0_SET is shown in Table 7-812.

Return to the Summary Table.

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE0_SET (0x103). Used by the transmitter during link training to configure the receiver PHY for lane 0.

Table 7-812. APB_DPCD_TRAINING_LANE_0_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:6	RESERVED	R	0x0	Reserved
5	MAX_PRE-EMPHASIS_REACHED	R	0x0	Set to a 1 when the maximum pre-emphasis setting is reached.
4:3	PRE-EMPHASIS_SET	R	0x0	Pre-emphasis setting 0x0 = Training pattern 2, preemphasis level 0 0x1 = Training pattern 2, preemphasis level 1 0x2 = Training pattern 2, preemphasis level 2 0x3 = Training pattern 2, preemphasis level 3
2	MAX_SWING_REACHED:	R	0x0	Set to a 1when the maximum driven current setting is reached.
1:0	VOLTAGE_SWING_SET	R	0x0	Voltage swing setting 0x0 = Training pattern 1, voltage swing level 0 0x1 = Training pattern 1, voltage swing level 1 0x2 = Training pattern 1, voltage swing level 2 0x3 = Training pattern 1, voltage swing level 3

7.6.4.1.35 APB_DPCD_TRAINING_LANE_1_SET Register (Address = 0x424) [Default = 0x00000000]

APB_DPCD_TRAINING_LANE_1_SET is shown in Table 7-813.

Return to the Summary Table.

Used by the transmitter during link training to configure the receiver PHY for lane 0. The fields of this register are identical to DPCD_TRAINING_LANE_0_SET.

Table 7-813. APB_DPCD_TRAINING_LANE_1_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:6	RESERVED	R	0x0	Reserved
5	MAX_PRE-EMPHASIS_REACHED	R	0x0	Set to a 1 when the maximum pre-emphasis setting is reached.
4:3	PRE-EMPHASIS_SET	R	0x0	Pre-emphasis setting 0x0 = Training pattern 2, preemphasis level 0 0x1 = Training pattern 2, preemphasis level 1 0x2 = Training pattern 2, preemphasis level 2 0x3 = Training pattern 2, preemphasis level 3
2	MAX_SWING_REACHED:	R	0x0	Set to a 1when the maximum driven current setting is reached.

Table 7-813. APB_DPCD_TRAINING_LANE_1_SET Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	VOLTAGE_SWING_SET	R	0x0	Voltage swing setting 0x0 = Training pattern 1, voltage swing level 0 0x1 = Training pattern 1, voltage swing level 1 0x2 = Training pattern 1, voltage swing level 2 0x3 = Training pattern 1, voltage swing level 3

7.6.4.1.36 APB_DPCD_TRAINING_LANE_2_SET Register (Address = 0x428) [Default = 0x00000000]

APB_DPCD_TRAINING_LANE_2_SET is shown in Table 7-814.

Return to the Summary Table.

Used by the transmitter during link training to configure the receiver PHY for lane 0. The fields of this register are identical to DPCD_TRAINING_LANE_0_SET.

Table 7-814. APB_DPCD_TRAINING_LANE_2_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:6	RESERVED	R	0x0	Reserved
5	MAX_PRE-EMPHASIS_REACHED	R	0x0	Set to a 1 when the maximum pre-emphasis setting is reached.
4:3	PRE-EMPHASIS_SET	R	0x0	Pre-emphasis setting 0x0 = Training pattern 2, preemphasis level 0 0x1 = Training pattern 2, preemphasis level 1 0x2 = Training pattern 2, preemphasis level 2 0x3 = Training pattern 2, preemphasis level 3
2	MAX_SWING_REACHED:	R	0x0	Set to a 1when the maximum driven current setting is reached.
1:0	VOLTAGE_SWING_SET	R	0x0	Voltage swing setting 0x0 = Training pattern 1, voltage swing level 0 0x1 = Training pattern 1, voltage swing level 1 0x2 = Training pattern 1, voltage swing level 2 0x3 = Training pattern 1, voltage swing level 3

7.6.4.1.37 APB_DPCD_TRAINING_LANE_3_SET Register (Address = 0x42C) [Default = 0x00000000]

APB_DPCD_TRAINING_LANE_3_SET is shown in Table 7-815.

Return to the Summary Table.

Used by the transmitter during link training to configure the receiver PHY for lane 0. The fields of this register are identical to DPCD_TRAINING_LANE_0_SET.

Table 7-815. APB_DPCD_TRAINING_LANE_3_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:6	RESERVED	R	0x0	Reserved
5	MAX_PRE-EMPHASIS_REACHED	R	0x0	Set to a 1 when the maximum pre-emphasis setting is reached.
4:3	PRE-EMPHASIS_SET	R	0x0	Pre-emphasis setting 0x0 = Training pattern 2, preemphasis level 0 0x1 = Training pattern 2, preemphasis level 1 0x2 = Training pattern 2, preemphasis level 2 0x3 = Training pattern 2, preemphasis level 3
2	MAX_SWING_REACHED:	R	0x0	Set to a 1 when the maximum driven current setting is reached.

Table 7-815. APB_DPCD_TRAINING_LANE_3_SET Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	VOLTAGE_SWING_SET	R	0x0	Voltage swing setting 0x0 = Training pattern 1, voltage swing level 0 0x1 = Training pattern 1, voltage swing level 1 0x2 = Training pattern 1, voltage swing level 2 0x3 = Training pattern 1, voltage swing level 3

7.6.4.1.38 APB_DPCD_DOWNSPREAD_CONTROL Register (Address = 0x430) [Default = 0x00000000]

APB_DPCD_DOWNSPREAD_CONTROL is shown in Table 7-816.

Return to the Summary Table.

This register reflects the value of DPCD register MAX_DOWNSPREAD (0x003). Note that for DisplayPort 1.1a or greater compliance, this bit will always be set to '1'.

Table 7-816. APB_DPCD_DOWNSPREAD_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	SPREAD_AMP	R	0x0	0: Disable spread spectrum 1: Enable 0.5% spreading

7.6.4.1.39 APB_DPCD_MAIN_LINK_CHANNEL_CODING_SET Register (Address = 0x434) [Default = 0x00000001]

APB_DPCD_MAIN_LINK_CHANNEL_CODING_SET is shown in Table 7-817.

Return to the Summary Table.

This register reflects the value of DPCD register MAIN_LINK_CHANNEL_CODING (0x006). This bit indicates whether or not the receiver supports the coding specification as specified in ANSI X3.230-1994, clause 11.

Table 7-817. APB_DPCD_MAIN_LINK_CHANNEL_CODING_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	DPCD_MAIN_LINK_CHANNEL_CODING_SET	R	0x1	Set to a 0 to disable 8B/10B channel coding. The default is 1.

7.6.4.1.40 APB_DPCD_LANE01_STATUS Register (Address = 0x43C) [Default = 0x00000000]

APB_DPCD_LANE01_STATUS is shown in Table 7-818.

Return to the Summary Table.

This register reflects the value of the DPCD register LANE0_1_STATUS (0x202). It contains the current training and operational state of the main link for lanes 0 and 1.

Table 7-818. APB_DPCD_LANE01_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
31:18	RESERVED	R	0x0	Reserved
17	LANE_1_TRAINING_LOST	R	0x0	Lane 1 training lost
16	LANE_0_TRAINING_LOST	R	0x0	Lane 0 training lost
15:10	RESERVED	R	0x0	Reserved
9	LANE_1_ALIGNED	R	0x0	Lane 1 aligned

Table 7-818. APB_DPCD_LANE01_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
8	LANE_0_ALIGNED	R	0x0	Lane 0 aligned
7	RESERVED	R	0x0	Reserved
6	LANE_1_SYMBOL_LOCKED	R	0x0	Lane 1 symbol locked
5	LANE_1_CHANNEL_EQ_DONE	R	0x0	Lane 1 channel EQ done
4	LANE_1_CLOCK_RECOVERY_DONE	R	0x0	Lane 1 clock recovery done
3	RESERVED	R	0x0	Reserved
2	LANE_0_SYMBOL_LOCKED	R	0x0	Lane 1 symbol locked
1	LANE_0_CHANNEL_EQ_DONE	R	0x0	Lane 1 channel EQ done
0	LANE_0_CLOCK_RECOVERY_DONE	R	0x0	Lane 1 clock recovery done

7.6.4.1.41 APB_DPCD_LANE23_STATUS Register (Address = 0x440) [Default = 0x00000000]

APB_DPCD_LANE23_STATUS is shown in Table 7-819.

Return to the Summary Table.

This register reflects the value of the DPCD register LANE2_3_STATUS (0x203). It contains the current training and operational state of the main link for lanes 2 and 3.

Table 7-819. APB_DPCD_LANE23_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
31:18	RESERVED	R	0x0	Reserved
17	LANE_3_TRAINING_LOST	R	0x0	Lane 3 training lost
16	LANE_2_TRAINING_LOST	R	0x0	Lane 2 training lost
15:10	RESERVED	R	0x0	Reserved
9	LANE_3_ALIGNED	R	0x0	Lane 3 aligned
8	LANE_2_ALIGNED	R	0x0	Lane 2 aligned
7	RESERVED	R	0x0	Reserved
6	LANE_3_SYMBOL_LOCKED	R	0x0	Lane 3 symbol locked
5	LANE_3_CHANNEL_EQ_DONE	R	0x0	Lane 3 channel EQ done
4	LANE_3_CLOCK_RECOVERY_DONE	R	0x0	Lane 3 clock recovery done
3	RESERVED	R	0x0	Reserved
2	LANE_2_SYMBOL_LOCKED	R	0x0	Lane 2 symbol locked
1	LANE_2_CHANNEL_EQ_DONE	R	0x0	Lane 2 channel EQ done
0	LANE_2_CLOCK_RECOVERY_DONE	R	0x0	Lane 2 clock recovery done

7.6.4.1.42 APB_DPCD_SOURCE_DEVICE_ID_0 Register (Address = 0x448) [Default = 0x00000000]

APB_DPCD_SOURCE_DEVICE_ID_0 is shown in Table 7-820.

Return to the Summary Table.

Device identification code written to the receiver DPCD register set at offset 0x303-0x306. This register contains the four least significant bytes of the ID.

Table 7-820. APB_DPCD_SOURCE_DEVICE_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
31:24	SOURCE_ID_3	R	0x0	Byte 3 of the Source device ID code.
23:16	SOURCE_ID_2	R	0x0	Byte 1 of the Source device ID code.
15:8	SOURCE_ID_1	R	0x0	Byte 1 of the Source device ID code.
7:0	SOURCE_ID_0	R	0x0	Byte 0 of the Source device ID code.

7.6.4.1.43 APB_DPCD_SOURCE_DEVICE_ID_1 Register (Address = 0x44C) [Default = 0x00000000]

APB_DPCD_SOURCE_DEVICE_ID_1 is shown in Table 7-821.

Return to the Summary Table.

Device identification code written to the receiver DPCD register set at offset 0x307-0x308. This register contains the two most significant bytes of the ID.

Table 7-821. APB_DPCD_SOURCE_DEVICE_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:8	SOURCE_ID_5	R	0x0	Byte 5 of the Source device ID code.
7:0	SOURCE_ID_4	R	0x0	Byte 4 of the Source device ID code.

7.6.4.1.44 APB_DPCD_SOURCE_REVISION Register (Address = 0x450) [Default = 0x00000000]

APB_DPCD_SOURCE_REVISION is shown in Table 7-822.

Return to the Summary Table.

Contains the hardware and firmware revision levels as written by the DisplayPort Source device to the DPCD register set at offset 0x309-0x30B.

Table 7-822. APB_DPCD_SOURCE_REVISION Register Field Descriptions

Bit	Field	Type	Default	Description
31:24	RESERVED	R	0x0	Reserved
23:16	SOURCE_HARDWARE_REVISION	R	0x0	Revision level for the Source hardware.
15:8	SOURCE_FIRMWARE_MAJOR_REV	R	0x0	Major revision level for the Source firmware.
7:0	SOURCE_FIRMWARE_MINOR_REV	R	0x0	Minor revision level for the Source firmware.

7.6.4.1.45 APB_TRAINING_LOST_CAUSE Register (Address = 0x454) [Default = 0x01010001]

APB_TRAINING_LOST_CAUSE is shown in Table 7-823.

Return to the Summary Table.

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable. The bit definitions for each lane are identical.

Table 7-823. APB_TRAINING_LOST_CAUSE Register Field Descriptions

Bit	Field	Type	Default	Description
31:24	LANE_3_TRAINING_CAUSE	R	0x1	Loss of training cause register for lane 3. 0x0 = Lane inactive 0x1 = Interlane alignment lost 0x2 = Symbol lock lost 0x3 = Clock recovery lost 0x4 = Training pattern 1 active 0x5 = Training pattern 2 active 0x6 = Training pattern 3 active 0x7 = Link bandwidth setting change
23:16	LANE_2_TRAINING_CAUSE	R	0x1	Loss of training cause register for lane 2. 0x0 = Lane inactive 0x1 = Interlane alignment lost 0x2 = Symbol lock lost 0x3 = Clock recovery lost 0x4 = Training pattern 1 active 0x5 = Training pattern 2 active 0x6 = Training pattern 3 active 0x7 = Link bandwidth setting change
15:8	LANE_1_TRAINING_CAUSE	R	0x0	Loss of training cause register for lane 1. 0x0 = Lane inactive 0x1 = Interlane alignment lost 0x2 = Symbol lock lost 0x3 = Clock recovery lost 0x4 = Training pattern 1 active 0x5 = Training pattern 2 active 0x6 = Training pattern 3 active 0x7 = Link bandwidth setting change
7:0	LANE_0_TRAINING_CAUSE	R	0x1	Loss of training cause register for lane 0. 0x0 = Lane inactive 0x1 = Interlane alignment lost 0x2 = Symbol lock lost 0x3 = Clock recovery lost 0x4 = Training pattern 1 active 0x5 = Training pattern 2 active 0x6 = Training pattern 3 active 0x7 = Link bandwidth setting change

7.6.4.1.46 APB_MSA_TIMING_IGNORE Register (Address = 0x47C) [Default = 0x00000000]

APB_MSA_TIMING_IGNORE is shown in Table 7-824.

Return to the Summary Table.

Reflects the current state of the DPCD register bit located at DisplayPort address 00107h bit 7. A 1 indicates that the Source may send invalid data for the MSA timing parameters.

Table 7-824. APB_MSA_TIMING_IGNORE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	MSA_TIMING_IGNORE	R	0x0	Determines if the Main Stream Attribute fields detected by the DisplayPort receiver core contain valid information.

7.6.4.1.47 APB_EDP_CONFIGURATION_SET Register (Address = 0x480) [Default = 0x00000000]

APB_EDP_CONFIGURATION_SET is shown in Table 7-825.

Return to the Summary Table.

Reports the status of the eDP configuration registers at DPCD address 0010Ah.

Table 7-825. APB_EDP_CONFIGURATION_SET Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6:2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	ALTERNATE_SR_ENABLE	R	0x0	Set to a 1 by the Source to enable the alternate scrambler reset for eDP implementations.

7.6.4.1.48 APB_DPCD_TRAINING_SCORE Register (Address = 0x484) [Default = 0x00000000]

APB_DPCD_TRAINING_SCORE is shown in Table 7-826.

Return to the Summary Table.

Contains the value of the training score register from the internal DPRx training logic. The training score is an indication of the number of failures detected during the current training step.

Table 7-826. APB_DPCD_TRAINING_SCORE Register Field Descriptions

Bit	Field	Type	Default	Description
31:24	TRAINING_SCORE_LANE_3	R	0x0	0x00 = indicates lane 3 is inactive. 0x3F = indicates lane 3 is successfully DP link trained. 0xFF = lane 3 failed DP link training.
23:16	TRAINING_SCORE_LANE_2	R	0x0	0x00 = indicates lane 2 is inactive. 0x3F = indicates lane 2 is successfully DP link trained. 0xFF = lane 2 failed DP link training.
15:8	TRAINING_SCORE_LANE_1	R	0x0	0x00 = indicates lane 1 is inactive. 0x3F = indicates lane 1 is successfully DP link trained. 0xFF = lane 1 failed DP link training.
7:0	TRAINING_SCORE_LANE_0	R	0x0	0x00 = indicates lane 0 is inactive. 0x3F = indicates lane 0 is successfully DP link trained. 0xFF = lane 0 failed DP link training.

7.6.4.1.49 APB_MST_ENABLE Register (Address = 0x48C) [Default = 0x00000000]

APB_MST_ENABLE is shown in Table 7-827.

Return to the Summary Table.

Indicates that multi-stream transport mode has been either enabled (1) or disabled (0) by the source device through the DPCD register set.

Table 7-827. APB_MST_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	MST_ENABLE	R	0x0	0x0 = disabled by the source device through the DPCD register set. 0x1 = enabled by the source device through the DPCD register set.

7.6.4.1.50 APB_MSA_HRES Register (Address = 0x500) [Default = 0x00000000]

APB_MSA_HRES is shown in Table 7-828.

Return to the Summary Table.

The horizontal resolution detected in the Main Stream Attributes.

Table 7-828. APB_MSA_HRES Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:0	MSA_HRES	R	0x0	Represents the number of active pixels in a line of video.

7.6.4.1.51 APB_MSA_HSPOL Register (Address = 0x504) [Default = 0x00000000]

APB_MSA_HSPOL is shown in Table 7-829.

Return to the Summary Table.

Main stream attribute horizontal sync polarity.

Table 7-829. APB_MSA_HSPOL Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	MSA_HSPOL	R	0x0	Indicates the polarity of the horizontal sync as requested by the transmitter.

7.6.4.1.52 APB_MSA_HSWIDTH Register (Address = 0x508) [Default = 0x00000000]

APB_MSA_HSWIDTH is shown in Table 7-830.

Return to the Summary Table.

Specifies the width of the horizontal sync pulse.

Table 7-830. APB_MSA_HSWIDTH Register Field Descriptions

Bit	Field	Type	Default	Description
31:15	RESERVED	R	0x0	Reserved
14:0	MSA_HSWIDTH	R	0x0	Specifies the width of the horizontal sync in terms of the recovered video clock.

7.6.4.1.53 APB_MSA_HSTART Register (Address = 0x50C) [Default = 0x00000000]

APB_MSA_HSTART is shown in Table 7-831.

Return to the Summary Table.

This main stream attribute is the number of clock cycles between the leading edge of the horizontal sync and the first cycle of active data. This value can be calculated using the formula (horizontal back porch) + (horizontal sync pulse width).

Table 7-831. APB_MSA_HSTART Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:0	MSA_HSTART	R	0x0	Number of blanking cycles before active data.

7.6.4.1.54 APB_MSA_HTOTAL Register (Address = 0x510) [Default = 0x00000000]

APB_MSA_HTOTAL is shown in Table 7-832.

Return to the Summary Table.

Tells the receiver core how many video clock cycles will occur between leading edges of the horizontal sync pulse. This value can be calculated using the formula (horizontal back porch) + (horizontal front porch) + (horizontal resolution) + (horizontal sync

width)

Table 7-832. APB_MSA_HTOTAL Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:0	MSA_HTOTAL	R	0x0	Total number of video clocks in a line of data.

7.6.4.1.55 APB_MSA_VRES Register (Address = 0x514) [Default = 0x00000000]

APB_MSA_VRES is shown in Table 7-833.

Return to the Summary Table.

Total number of active video lines in a frame of video.

Table 7-833. APB_MSA_VRES Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:0	MSA_VRES	R	0x0	The vertical resolution of the received video.

7.6.4.1.56 APB_MSA_VSPOL Register (Address = 0x518) [Default = 0x00000000]

APB_MSA_VSPOL is shown in Table 7-834.

Return to the Summary Table.

Specifies the vertical sync polarity requested by the transmitter.

Table 7-834. APB_MSA_VSPOL Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R	0x0	Reserved
0	MSA_VSPOL	R	0x0	A value of 1 in this register indicates an active high vertical sync and a 0 indicates an active low vertical sync.

7.6.4.1.57 APB_MSA_VSWIDTH Register (Address = 0x51C) [Default = 0x00000000]

APB_MSA_VSWIDTH is shown in Table 7-835.

Return to the Summary Table.

The transmitter uses this value to specify the width of the vertical sync pulse in lines.

Table 7-835. APB_MSA_VSWIDTH Register Field Descriptions

Bit	Field	Type	Default	Description
31:15	RESERVED	R	0x0	Reserved
14:0	MSA_VSWIDTH	R	0x0	Specifies the number of lines between the leading edge and the trailing edge of the vertical sync pulse.

7.6.4.1.58 APB_MSA_VSTART Register (Address = 0x520) [Default = 0x00000000]

APB_MSA_VSTART is shown in Table 7-836.

Return to the Summary Table.

This main stream attribute specifies the number of lines between the leading edge of the vertical sync pulse and the first line of active data. . This value can be calculated using the formula

(vertical back porch) + (vertical sync pulse width).

Table 7-836. APB_MSA_VSTART Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:0	MSA_VSTART	R	0x0	Number of blanking lines before the start of active data.

7.6.4.1.59 APB_MSA_VTOTAL Register (Address = 0x524) [Default = 0x00000000]

APB_MSA_VTOTAL is shown in Table 7-837.

Return to the Summary Table.

Total number of lines between sequential leading edges of the vertical sync pulse. This value can be calculated using the formula
(vertical back porch) + (vertical front porch) + (vertical resolution) + (vertical sync width)

Table 7-837. APB_MSA_VTOTAL Register Field Descriptions

Bit	Field	Type	Default	Description
31:16	RESERVED	R	0x0	Reserved
15:0	MSA_VTOTAL	R	0x0	The total number of lines per video frame is contained in this value.

7.6.4.1.60 APB_MSA_MISC0 Register (Address = 0x528) [Default = 0x00000000]

APB_MSA_MISC0 is shown in Table 7-838.

Return to the Summary Table.

This read-only register contains the value of the MISC0 attribute data received in the most recently recognized Main Stream Attribute packet. The bit fields of this register are identical to those found in the DisplayPort specification.

Table 7-838. APB_MSA_MISC0 Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R	0x0	Reserved
7:0	MSA_MISC0	R	0x0	The MISC0 field contains clock and colorimetry information for the video stream carried on the virtual sink channel.

7.6.4.1.61 APB_MSA_MISC1 Register (Address = 0x52C) [Default = 0x00000000]

APB_MSA_MISC1 is shown in Table 7-839.

Return to the Summary Table.

This register contains the read-only value of the MISC1 attribute data received in the most recently recognized Main Stream Attribute packet. The bit fields of this register are identical to those found in the DisplayPort specification.

Table 7-839. APB_MSA_MISC1 Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R	0x0	Reserved
7:0	MSA_MISC1	R	0x0	The MISC1 field contains video structure and additional colorimetry information for the video stream carried on the virtual sink channel.

7.6.4.1.62 APB_MSA_MVID Register (Address = 0x530) [Default = 0x00000000]

APB_MSA_MVID is shown in Table 7-840.

Return to the Summary Table.

This attribute value is used to recover the video clock from the link clock. In synchronous clock mode, this value is typically set to the pixel clock frequency for the selected display mode. In asynchronous mode, this value is based on a running counter in the transmitter that is sent periodically in the MSAs when the counter reaches maximum value.

Table 7-840. APB_MSA_MVID Register Field Descriptions

Bit	Field	Type	Default	Description
31:24	RESERVED	R	0x0	Reserved
23:0	MSA_MVID	R	0x0	MVID: Value of the clock recovery M value.

7.6.4.1.63 APB_MSA_NVID Register (Address = 0x534) [Default = 0x00000000]

APB_MSA_NVID is shown in Table 7-841.

Return to the Summary Table.

This attribute value is used to recover the video clock from the link clock. In synchronous clock mode, this value is set to a fixed value based on the current link rate. For asynchronous mode, this value is fixed to a constant value of 32,768.

Table 7-841. APB_MSA_NVID Register Field Descriptions

Bit	Field	Type	Default	Description
31:24	RESERVED	R	0x0	Reserved
23:0	MSA_NVID	R	0x0	NVID: Value of the clock recovery N value.

7.6.4.1.64 APB_MSA_VBID Register (Address = 0x538) [Default = 0x00000019]

APB_MSA_VBID is shown in Table 7-842.

Return to the Summary Table.

The most recently received VB-ID value received through the main link is contained in this register.

Table 7-842. APB_MSA_VBID Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R	0x0	Reserved
7:6	RESERVED	R	0x0	These bits are reserved and will always be set to a 0.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x1	Reserved
3	MSA_VBID_NO_VIDEO	R	0x1	Set to a 1 when video stream information is not present on the link.
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	MSA_VBID_VERTICAL_BLANKING	R	0x1	Set to a 1 during the vertical blanking interval of the source video stream. This bit is set at the end of the last active line of a frame.

7.6.4.1.65 APB_MSA_VIRTUAL_SINK_SELECT Register (Address = 0x540) [Default = 0x00000000]

APB_MSA_VIRTUAL_SINK_SELECT is shown in Table 7-843.

Return to the Summary Table.

When MST is enabled, the value of this register selects the virtual sink device that will report the main stream attributes of the detected video stream. The values of 0x500-0x538 will change based on the value of this register and will reflect the values detected by the selected virtual sink device.

Table 7-843. APB_MSA_VIRTUAL_SINK_SELECT Register Field Descriptions

Bit	Field	Type	Default	Description
31:2	RESERVED	R	0x0	Reserved
1:0	MSA_VIRTUAL_SINK_SELECT	R	0x0	Selects the virtual sink device for MSA value reporting.

7.6.4.1.66 APB_TEST_REQUEST Register (Address = 0x700) [Default = 0x00000000]

APB_TEST_REQUEST is shown in Table 7-844.

Return to the Summary Table.

Requested test from the sink device. Writing this register causes the DPRx core to issue an HPD interrupt to request the specified test from the source. Not all source devices support this functionality. The test parameters must all be properly set before writing to this register.

Table 7-844. APB_TEST_REQUEST Register Field Descriptions

Bit	Field	Type	Default	Description
31:4	RESERVED	R/W	0x0	Reserved
3	PHY_PATTERN_TEST	R/W	0x0	Requests the PHY test pattern as specified in the TEST_PHY_PATTERN register.
2	RESERVED	R/W	0x0	Reserved
1	TEST_PATTERN	R/W	0x0	Set to a 1 to request a test pattern.
0	TEST_LINK_TRAINING	R/W	0x0	Set to a 1 to request a link training test.

7.6.4.1.67 APB_TEST_LANE_COUNT Register (Address = 0x704) [Default = 0x00000000]

APB_TEST_LANE_COUNT is shown in Table 7-845.

Return to the Summary Table.

Set to the number of lanes requested for the current sink device test.

Table 7-845. APB_TEST_LANE_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
31:5	RESERVED	R/W	0x0	Reserved
4:0	TEST_LANE_COUNT	R/W	0x0	Valid values for this register are 1, 2 and 4.

7.6.4.1.68 APB_TEST_LINK_RATE Register (Address = 0x708) [Default = 0x00000000]

APB_TEST_LINK_RATE is shown in Table 7-846.

Return to the Summary Table.

Set to the link rate requested for the current sink device test.

Table 7-846. APB_TEST_LINK_RATE Register Field Descriptions

Bit	Field	Type	Default	Description
31:8	RESERVED	R/W	0x0	Reserved

Table 7-846. APB_TEST_LINK_RATE Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
7:0	TEST_LINK_RATE	R/W	0x0	Valid values are 0x06 through 0x1E.

7.6.4.1.69 APB_MST_PAYLOAD_ID_0 Register (Address = 0x904) [Default = 0x00000000]

APB_MST_PAYLOAD_ID_0 is shown in Table 7-847.

Return to the Summary Table.

Specifies the payload ID of the video stream targeted for sink output port 0. This value matches the stream ID configured in the DisplayPort DPCD register fields. Symbol slots in the MST packet with an allocation ID matching this value will be routed to Sink 0.

Table 7-847. APB_MST_PAYLOAD_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
31:7	RESERVED	R/W	0x0	Reserved
6:0	MST_PAYLOAD_ID_0	R/W	0x0	Seven-bit value matching the payload ID set in the DPCD register fields.

7.6.4.1.70 APB_MST_PAYLOAD_ID_1 Register (Address = 0x908) [Default = 0x00000000]

APB_MST_PAYLOAD_ID_1 is shown in Table 7-848.

Return to the Summary Table.

Specifies the payload ID of the video stream targeted for sink output port 1, if present. This value matches the stream ID configured in the DisplayPort DPCD register fields. Symbol slots in the MST packet with an allocation ID matching this value will be routed to Sink 1.

Table 7-848. APB_MST_PAYLOAD_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
31:7	RESERVED	R/W	0x0	Reserved
6:0	MST_PAYLOAD_ID_1	R/W	0x0	Seven-bit value matching the payload ID set in the DPCD register fields.

7.6.4.1.71 APB_MST_CLEAR_PAYLOAD_TABLE Register (Address = 0x934) [Default = 0x00000000]

APB_MST_CLEAR_PAYLOAD_TABLE is shown in Table 7-849.

Return to the Summary Table.

The internal payload ID table for the MST function must be periodically cleared by the receiver host software. This register should be written after system events that could cause the internal table to become invalid such as an HPD disconnect or at core startup. If the payload table is not cleared, invalid entries may be present when the source begins the payload allocation process.

Table 7-849. APB_MST_CLEAR_PAYLOAD_TABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_CLEAR_PAYLOAD_TABLE	R/W	0x0	Write this bit to a 1 to clear the internal payload ID table. This register will always read 0.

7.6.4.1.72 APB_MST_VIRTUAL_SINK_0_ENABLE Register (Address = 0xA00) [Default = 0x00000001]

APB_MST_VIRTUAL_SINK_0_ENABLE is shown in Table 7-850.

Return to the Summary Table.

When configured for MST mode, this bit enables the functionality for virtual sink device 0. This sink device is associated with video output port 0. After core reset, this bit defaults to a value of 1. For all other virtual sink devices, this register is set to 0 upon reset.

Table 7-850. APB_MST_VIRTUAL_SINK_0_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VIRTUAL_SINK_0_ENABLE	R/W	0x1	Set to 1 to enable the virtual sink device. Video functions for the virtual sink device will remain idle while this bit is set to a 0.

7.6.4.1.73 APB_MST_VS0_VIDEO_FIFO_OVERFLOW Register (Address = 0xA10) [Default = 0x00000000]

APB_MST_VS0_VIDEO_FIFO_OVERFLOW is shown in Table 7-851.

Return to the Summary Table.

This status bit indicates an overflow of the user data FIFO in the virtual sink device output pixel path. This event may occur if the video pixel clock is not fast enough to support the current video mode peak pixel rate.

Table 7-851. APB_MST_VS0_VIDEO_FIFO_OVERFLOW Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS0_VIDEO_FIFO_OVERFLOW	R/W	0x0	A 1 indicates that the internal FIFO has detected an overflow condition. This bit clears when a 1 is written to this register.

7.6.4.1.74 APB_MST_VS0_DTG_ENABLE Register (Address = 0xA14) [Default = 0x00000000]

APB_MST_VS0_DTG_ENABLE is shown in Table 7-852.

Return to the Summary Table.

This bit controls the function of the display timing generator (DTG) in the associated virtual sink device. The DTG should be disabled when the core detects the no video pattern on the link to prevent invalid data from being presented on the output video interface. The DTG should be enabled when a valid video mode has been detected.

Table 7-852. APB_MST_VS0_DTG_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS0_DTG_ENABLE	R/W	0x0	Set to a 1 to enable the DTG. Set to a 0 to disable the DTG.

7.6.4.1.75 APB_MST_VS0_SECONDARY_ENABLE Register (Address = 0xA80) [Default = 0x00000001]

APB_MST_VS0_SECONDARY_ENABLE is shown in Table 7-853.

Return to the Summary Table.

Enable for the DisplayPort Receiver secondary channel function for the virtual sink device. When disabled, the sink will not process any secondary data packets. This enable does not apply to the embedded DisplayPort function, if included, which will continue to operate even when this control register is set to a 0.

Table 7-853. APB_MST_VS0_SECONDARY_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS0_SECONDARY_ENABLE	R/W	0x1	Set to a 1 to enable the secondary channel. A 0 disables all secondary data packet processing by the virtual sink.

7.6.4.1.76 APB_MST_VS0_INFOFRAME_ADVANCE Register (Address = 0xA94) [Default = 0x00000000]

APB_MST_VS0_INFOFRAME_ADVANCE is shown in Table 7-854.

Return to the Summary Table.

Writing a 1 to this bit advances the packet index in the secondary channel InfoFrame buffer. This bit should be written to a 1 after reading a valid packet from the buffer. This bit clears automatically and does not require a subsequent write to a 0.

Table 7-854. APB_MST_VS0_INFOFRAME_ADVANCE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS0_INFOFRAME_ADVANCE	R/W	0x0	Write to a 1 after an InfoFrame packet has been read and parsed.

7.6.4.1.77 APB_MST_VIRTUAL_SINK_1_ENABLE Register (Address = 0xB00) [Default = 0x00000000]

APB_MST_VIRTUAL_SINK_1_ENABLE is shown in Table 7-855.

Return to the Summary Table.

When configured for MST mode, this bit enables the functionality for virtual sink device 0. This sink device is associated with video output port 0. After core reset, this bit defaults to a value of 1. For all other virtual sink devices, this register is set to 0 upon reset.

Table 7-855. APB_MST_VIRTUAL_SINK_1_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VIRTUAL_SINK_1_ENABLE	R/W	0x0	Set to 1 to enable the virtual sink device. Video functions for the virtual sink device will remain idle while this bit is set to a 0.

7.6.4.1.78 APB_MST_VS1_VIDEO_FIFO_OVERFLOW Register (Address = 0xB10) [Default = 0x00000000]

APB_MST_VS1_VIDEO_FIFO_OVERFLOW is shown in Table 7-856.

Return to the Summary Table.

This status bit indicates an overflow of the user data FIFO in the virtual sink device output pixel path. This event may occur if the video pixel clock is not fast enough to support the current video mode peak pixel rate.

Table 7-856. APB_MST_VS1_VIDEO_FIFO_OVERFLOW Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS1_VIDEO_FIFO_OVERFLOW	R/W	0x0	A 1 indicates that the internal FIFO has detected an overflow condition. This bit clears when a 1 is written to this register.

7.6.4.1.79 APB_MST_VS1_DTG_ENABLE Register (Address = 0xB14) [Default = 0x00000000]

APB_MST_VS1_DTG_ENABLE is shown in Table 7-857.

Return to the Summary Table.

This bit controls the function of the display timing generator (DTG) in the associated virtual sink device. The DTG should be disabled when the core detects the no video pattern on the link to prevent invalid data from being presented on the output video interface. The DTG should be enabled when a valid video mode has been detected.

Table 7-857. APB_MST_VS1_DTG_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS1_DTG_ENABLE	R/W	0x0	Set to a 1 to enable the DTG. Set to a 0 to disable the DTG.

7.6.4.1.80 APB_MST_VS1_SECONDARY_ENABLE Register (Address = 0xB80) [Default = 0x00000000]

APB_MST_VS1_SECONDARY_ENABLE is shown in Table 7-858.

Return to the Summary Table.

Enable for the DisplayPort Receiver secondary channel function for the virtual sink device. When disabled, the sink will not process any secondary data packets. This enable does not apply to the embedded DisplayPort function, if included, which will continue to operate even when this control register is set to a 0.

Table 7-858. APB_MST_VS1_SECONDARY_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS1_SECONDARY_ENABLE	R/W	0x0	Set to a 1 to enable the secondary channel. A 0 disables all secondary data packet processing by the virtual sink.

7.6.4.1.81 APB_MST_VS1_INFOFRAME_ADVANCE Register (Address = 0xB94) [Default = 0x00000000]

APB_MST_VS1_INFOFRAME_ADVANCE is shown in Table 7-859.

Return to the Summary Table.

Writing a 1 to this bit advances the packet index in the secondary channel InfoFrame buffer. This bit should be written to a 1 after reading a valid packet from the buffer. This bit clears automatically and does not require a subsequent write to a 0.

Table 7-859. APB_MST_VS1_INFOFRAME_ADVANCE Register Field Descriptions

Bit	Field	Type	Default	Description
31:1	RESERVED	R/W	0x0	Reserved
0	MST_VS1_INFOFRAME_ADVANCE	R/W	0x0	Write to a 1 after an InfoFrame packet has been read and parsed.

7.6.4.2 UNIQID Registers

Table 7-860 lists the memory-mapped registers for the UNIQID registers. All register offset addresses not listed in Table 7-860 should be considered as reserved locations and the register contents should not be modified.

Table 7-860. UNIQID Registers

Address	Acronym	Register Name	Section
0x0	UNIQUE_ID_0	UNIQUE_ID_0	Go
0x1	UNIQUE_ID_1	UNIQUE_ID_1	Go
0x2	UNIQUE_ID_2	UNIQUE_ID_2	Go
0x3	UNIQUE_ID_3	UNIQUE_ID_3	Go
0x4	UNIQUE_ID_4	UNIQUE_ID_4	Go
0x5	UNIQUE_ID_5	UNIQUE_ID_5	Go
0x6	UNIQUE_ID_6	UNIQUE_ID_6	Go
0x7	UNIQUE_ID_7	UNIQUE_ID_7	Go
0x8	UNIQUE_ID_8	UNIQUE_ID_8	Go
0x9	UNIQUE_ID_9	UNIQUE_ID_9	Go
0xA	UNIQUE_ID_10	UNIQUE_ID_10	Go
0xB	UNIQUE_ID_11	UNIQUE_ID_11	Go

Complex bit access types are encoded to fit into small table cells. Table 7-861 shows the codes that are used for access types in this section.

Table 7-861. UNIQID Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.6.4.2.1 UNIQUE_ID_0 Register (Address = 0x0) [Default = 0x0000]

UNIQUE_ID_0 is shown in Table 7-862.

Return to the Summary Table.

Table 7-862. UNIQUE_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID0	R	0x0	Contains the unique ID information byte 0 - 1. This register is read only.

7.6.4.2.2 UNIQUE_ID_1 Register (Address = 0x1) [Default = 0x0000]

UNIQUE_ID_1 is shown in Table 7-863.

Return to the Summary Table.

Table 7-863. UNIQUE_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID1	R	0x0	Contains the unique ID information byte 2 - 3. This register is read only.

7.6.4.2.3 UNIQUE_ID_2 Register (Address = 0x2) [Default = 0x0000]

UNIQUE_ID_2 is shown in Table 7-864.

Return to the Summary Table.

Table 7-864. UNIQUE_ID_2 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID2	R	0x0	Contains the unique ID information byte 4 - 5. This register is read only.

7.6.4.2.4 UNIQUE_ID_3 Register (Address = 0x3) [Default = 0x0000]

UNIQUE_ID_3 is shown in Table 7-865.

Return to the Summary Table.

Table 7-865. UNIQUE_ID_3 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID3	R	0x0	Contains the unique ID information byte 6 - 7. This register is read only.

7.6.4.2.5 UNIQUE_ID_4 Register (Address = 0x4) [Default = 0x0000]

UNIQUE_ID_4 is shown in Table 7-866.

Return to the Summary Table.

Table 7-866. UNIQUE_ID_4 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID4	R	0x0	Contains the unique ID information byte 8 - 9. This register is read only.

7.6.4.2.6 UNIQUE_ID_5 Register (Address = 0x5) [Default = 0x0000]

UNIQUE_ID_5 is shown in Table 7-867.

Return to the Summary Table.

Table 7-867. UNIQUE_ID_5 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID5	R	0x0	Contains the unique ID information byte 10 - 11. This register is read only.

7.6.4.2.7 UNIQUE_ID_6 Register (Address = 0x6) [Default = 0x0000]

UNIQUE_ID_6 is shown in Table 7-868.

Return to the Summary Table.

Table 7-868. UNIQUE_ID_6 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID6	R	0x0	Contains the unique ID information byte 12 - 13. This register is read only.

7.6.4.2.8 UNIQUE_ID_7 Register (Address = 0x7) [Default = 0x0000]

UNIQUE_ID_7 is shown in Table 7-869.

Return to the Summary Table.

Table 7-869. UNIQUE_ID_7 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID7	R	0x0	Contains the unique ID information byte 14 - 15. This register is read only.

7.6.4.2.9 UNIQUE_ID_8 Register (Address = 0x8) [Default = 0x0000]

UNIQUE_ID_8 is shown in Table 7-870.

Return to the Summary Table.

Table 7-870. UNIQUE_ID_8 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID8	R	0x0	Contains the unique ID information byte 16 - 17. This register is read only.

7.6.4.2.10 UNIQUE_ID_9 Register (Address = 0x9) [Default = 0x0000]

UNIQUE_ID_9 is shown in Table 7-871.

Return to the Summary Table.

Table 7-871. UNIQUE_ID_9 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID9	R	0x0	Contains the unique ID information byte 18 - 19. This register is read only.

7.6.4.2.11 UNIQUE_ID_10 Register (Address = 0xA) [Default = 0x0000]

UNIQUE_ID_10 is shown in Table 7-872.

Return to the Summary Table.

Table 7-872. UNIQUE_ID_10 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID10	R	0x0	Contains the unique ID information byte 20 - 21. This register is read only.

7.6.4.2.12 UNIQUE_ID_11 Register (Address = 0xB) [Default = 0x0000]

UNIQUE_ID_11 is shown in Table 7-873.

Return to the Summary Table.

Table 7-873. UNIQUE_ID_11 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID11	R	0x0	Contains the unique ID information byte 22 - 23. This register is read only.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Applications

The DS90UB983-Q1 has one DP input and two FPD-Link outputs. It can be connected to either one or two FPD-Link IV or FPD-Link III deserializers, as shown in Figure 8-1 and Figure 8-2. See Figure 8-3 for typical STP connection diagram and Figure 8-4 for typical coaxial connection diagram.

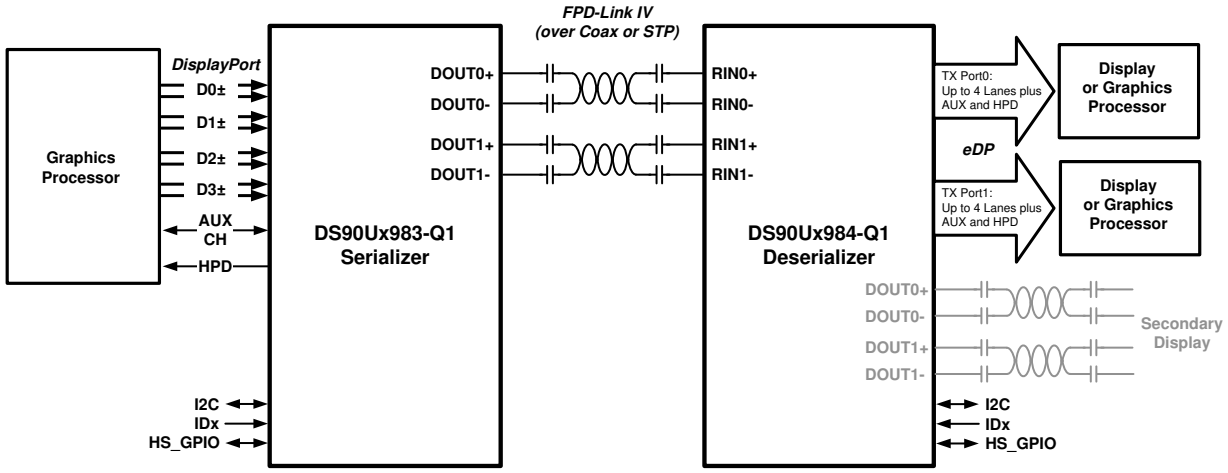


Figure 8-1. FPD-Link IV Typical Application

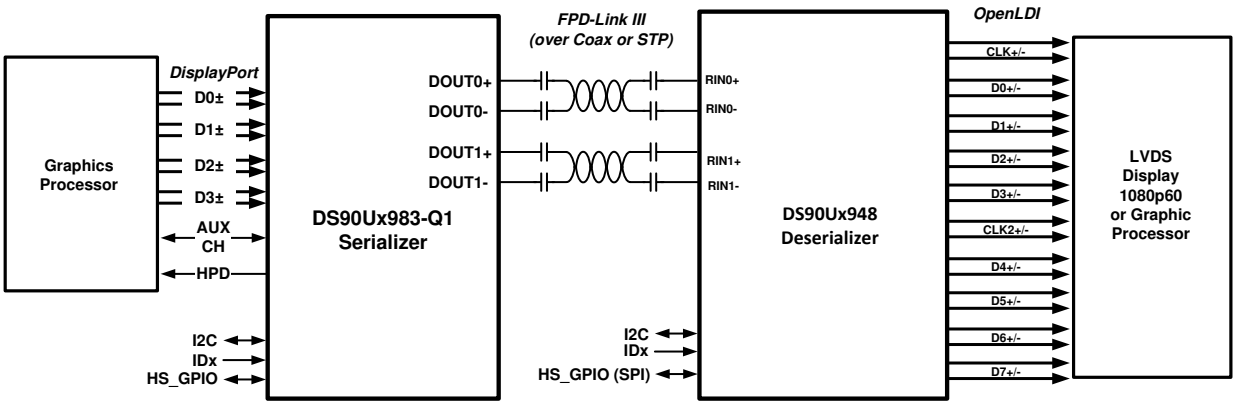


Figure 8-2. FPD-Link III Typical Application

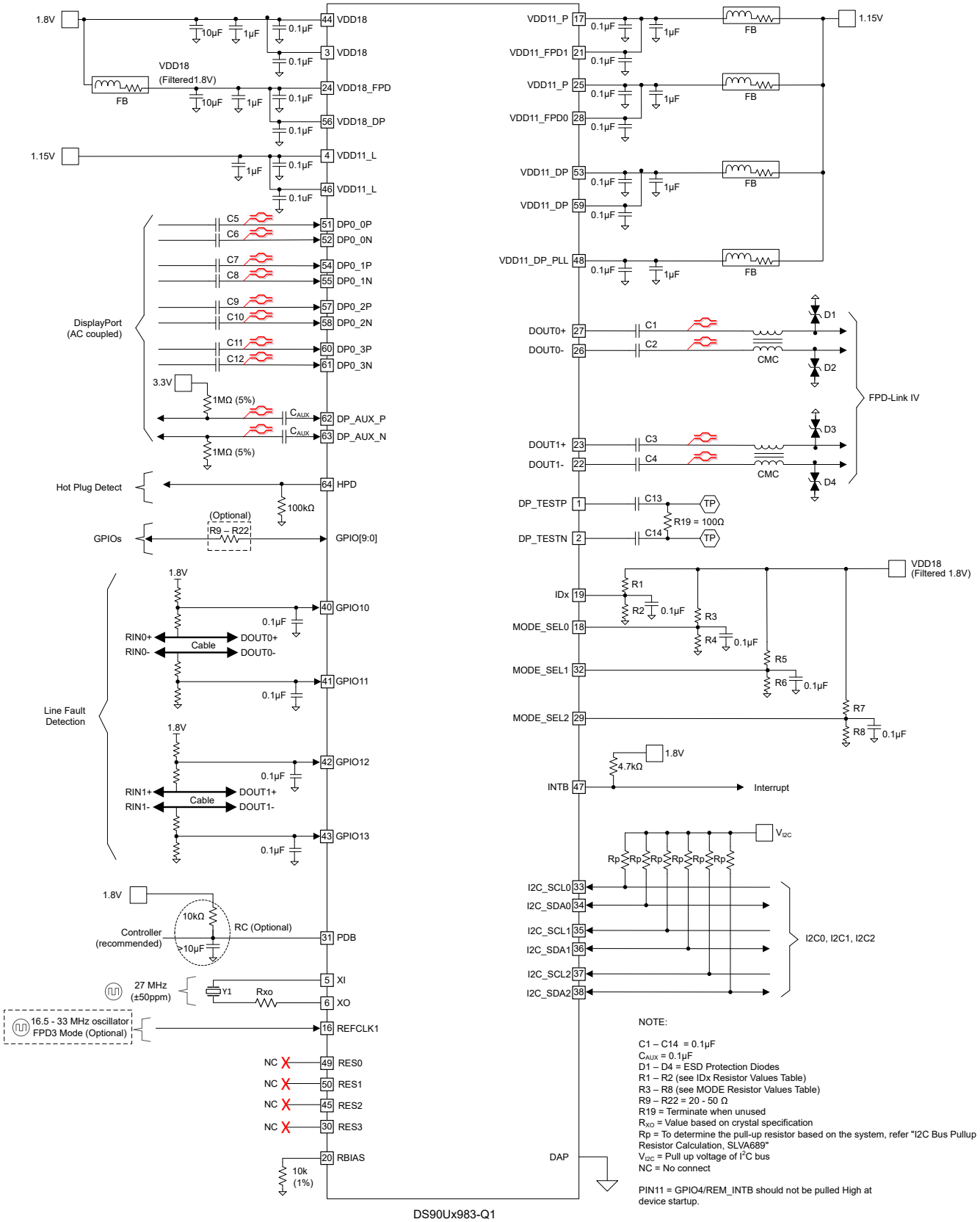


Figure 8-3. Typical Application Connection - STP

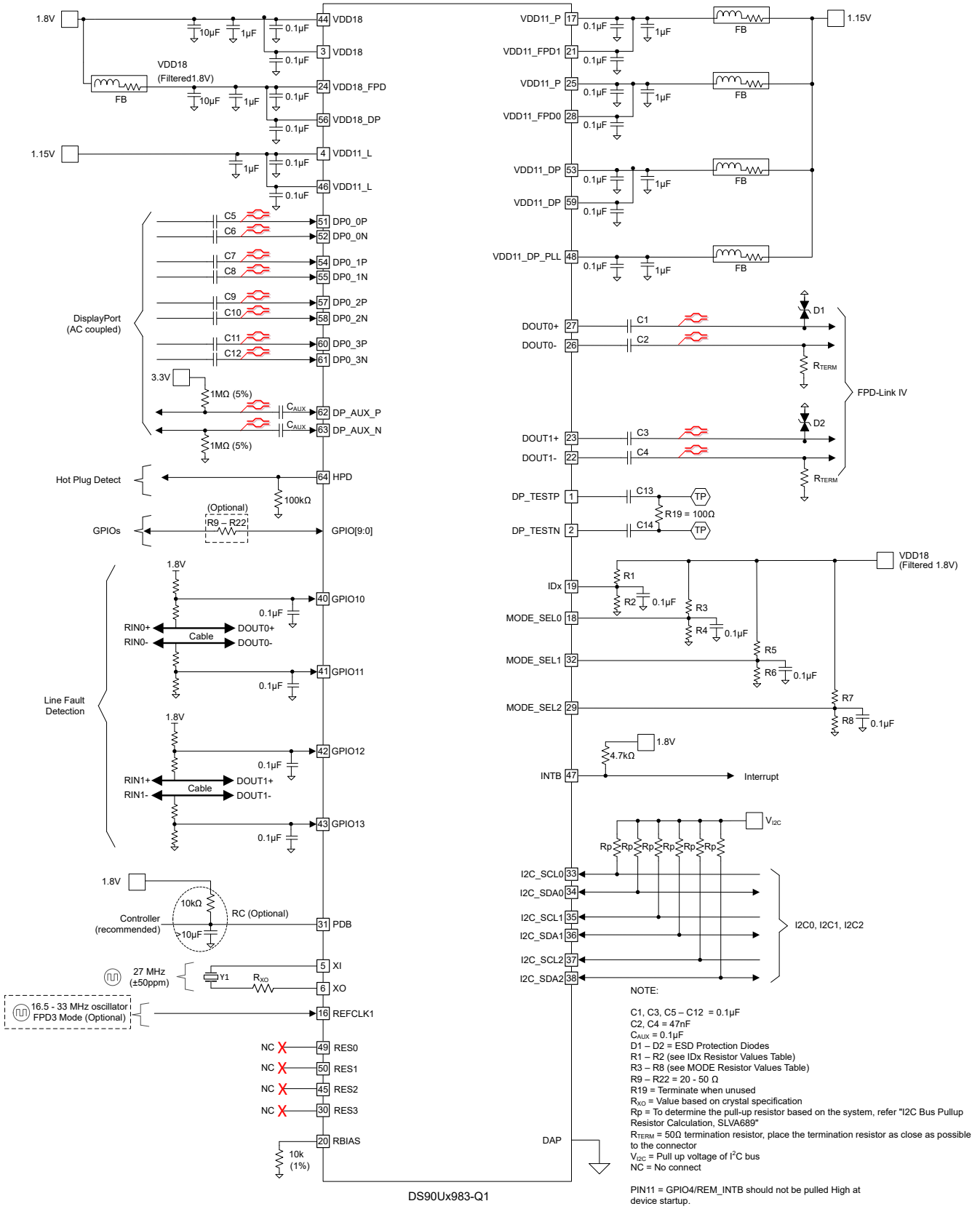


Figure 8-4. Typical Application Connection - Coax

8.2.1 Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link IV signal path as illustrated in Figure 8-5.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD11	1.15 V
VDD18	1.8 V
AC coupling capacitor for DOUT[1:0]± with FPD-Link III and FPD-Link IV deserializers	100 nF
AC coupling capacitor for Coax configuration DOUT[1:0]+ FPD-Link III and FPD-Link IV deserializers	100 nF
AC coupling capacitor for Coax configuration DOUT[1:0]- with FPD-Link III and FPD-Link IV deserializers	47nF

For applications utilizing single-ended 50Ω coaxial cable, the unused data pins (DOUT-) should utilize a 47nF capacitor and should be terminated with a 50Ω resistor.

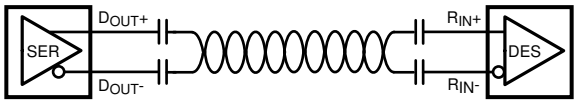


Figure 8-5. AC-Coupled Connection (STP)

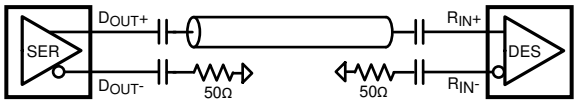


Figure 8-6. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link IV transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

Table 8-2 and Table 8-4 are the external clock requirements for both crystal and oscillator. The DS90UB983-Q1 uses an external 27 MHz clock source as a reference clock input for the internal circuitry in order to generate all the clocks requirement for the PLL setting. The DS90UB983-Q1 supports either an external resonator (crystal) connected across the XI and XO pins, or an external CMOS-level oscillator connected to XI pin only.

Table 8-3 depicts a recommended oscillator and its alternative oscillator. These components are carefully chosen to meet the clock requirements. It is recommended to place the input clock source as close to the DS90UB983-Q1 as possible to avoid any noises coupling into the input clock source.

Table 8-2. XI Oscillator Reference Clock Requirements

Parameter	Conditions	Min	Typ	Max	Units
Frequency tolerance	-40C to 105C	-50		50	ppm
Frequency stability	Aging (10 Years)	-50		50	ppm
Amplitude		800	1200	VDD18	mVpp
Reference clock Duty Cycle		40	50	60	%
Rise/Fall Time	20% - 80%		0.1	3 (1)	ns
Reference clock oscillator frequency	XI input		27		MHz
	REFCLK1	16.5		33	MHz
RMS Jitter	12 kHz - 20 MHz			1.5	ps RMS

Table 8-3. Recommended Oscillators

Manufacturer	Oscillator P/N	Package Dimension (mm)	Package Footprint	Supply Voltage	Description
TXC	AW27070503	2.5x2.0	4-SMD	1.8 V	Oscillator, 27 MHz, 1 ps Max RMS jitter, CMOS, AEC-Q200
Abracon	ASDAIG3-27.000MHZ-X-K-T	2.5x2.0	4-SMD	1.8 V	Oscillator, 27 MHz, <1 ps RMS jitter, HCMOS, AEC-Q200
Diodes	HX2127010Q	2.5x2.0	4-SMD	1.8 V	Oscillator, 27 MHz, 1 ps RMS jitter, CMOS, AEC-Q200
Seiko Epson	X1G005951000416	2.5x2.0	4-SMD	Min: 1.6 V, Max: 3.63 V	Oscillator, 27 MHz, 1 ps Max RMS jitter, L_CMOS, AEC-Q200

The crystal specification normally defines the maximum crystal drive level which represents the power dissipated from the crystal. The DS90UB983-Q1 has the maximum drive level requirement. To maintain the maximum drive level of the DS90UB983-Q1 a series resistor (R_S) should be added in series with XO pin for current limiting to lower the power to 100 µW maximum. The value of the series resistor determine based on the Equivalent Series Resistance (ESR) and Load Capacitance (C_L) specification of the crystal. The matching (shunt) capacitance calculation should be as close as possible to the load capacitance of the crystal. The crystal should be placed as close as possible to DS90UB983-Q1 device with short distance to maintain the C_L less than 20 pF. For more information how to calculate the series resistor (R_S) refer to application note, *FPD-Link IV Component Selection Guide*, SNLA354.

Table 8-4. Crystal Reference Clock Requirements

Parameter	Conditions	Min	Typ	Max	Units
Frequency tolerance	-40C to 105C	-50		50	ppm
Frequency stability	Aging (10 Years)	-50		50	ppm
Frequency	XI, XO input		27		MHz
Load Capacitance				20	pF
ESR				70	Ω
Drive Level				100	μW_{RMS}

Table 8-5. XO Series Resistor Limit

Max ESR (Ω)	R_S (Ω)	C_{LOAD} (pF)	Max Drive Level (µW)
20	1000	20	100
40	800	20	100
50	700	20	100
60	600	20	100
70	500	20	100
20	700	20	200
40	600	20	200
50	500	20	200
60	400	20	200
70	300	20	200

8.2.2 DP/eDP Implementation

The standard DisplayPort connection consists of four lanes of Main Links, auxiliary channel, and HPD. In Figure 8-7 illustrates a typical AUX hardware implementation for DisplayPort. The discrete components outside of DP source and 983 are required in order to ensure proper operation. Note that the typical value of the C_AUX is 0.1µF.

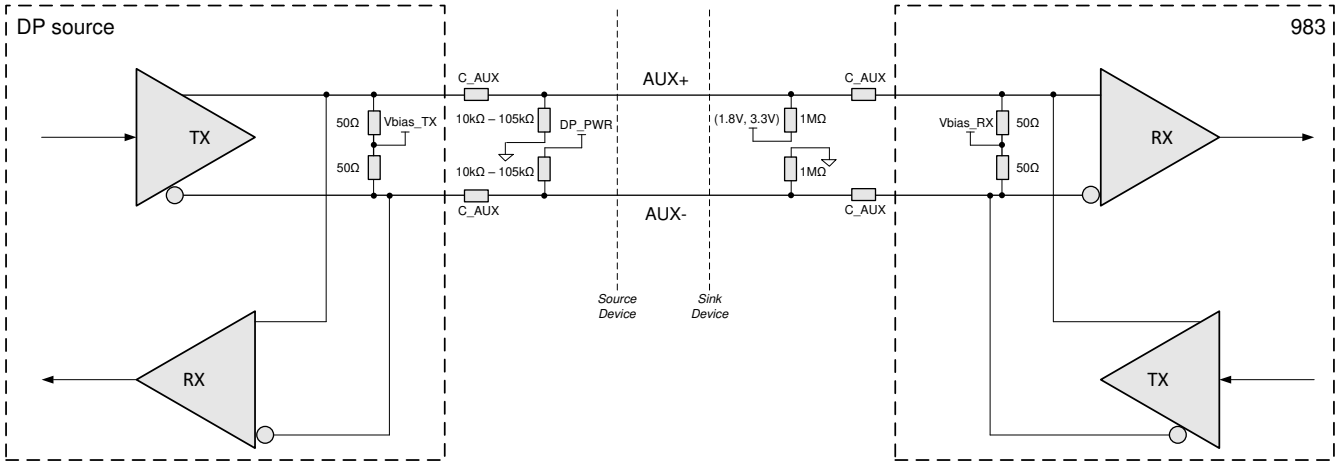


Figure 8-7. DisplayPort AUX CH Differential Pair

The eDP AUX CH topology depicts as shown in Figure 8-8. Main link connections require at least one set of AC capacitors at the transmitter side. The additional set of AC coupling capacitors on the sink side (DS90UB983-Q1) are optional. The DS90UB983-Q1 does not monitor of the eDP AUX± common mode voltage coming from the transmitter side for plug/unplug detection.

eDP AUX CH Configuration:

- For eDP, red marked components are not required, however TI recommends adding stuffing options for all red marked components.
- 50Ω terminations are internal to source and sink devices side.
- Source side C_AUX = 100nF is always required.
- Stuffing Option 1:
  1. Source side pull-up/pull-down = 100kΩ
  2. Sink side pullup/pulldown = 1MΩ
  3. Sink side (DS90UB983-Q1) C_AUX = 100nF
- Stuffing Option 2:
  1. Source side pull-up/pull-down = DNP
  2. Sink side pull-up/pull-down = DNP
  3. Sink side (983) C_AUX replaced with 0Ω resistor

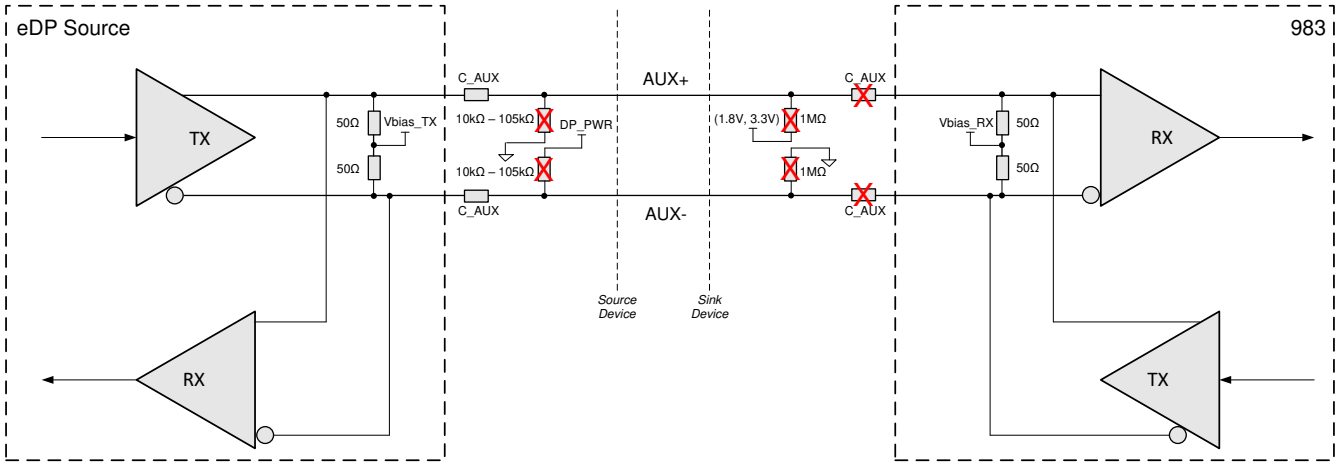


Figure 8-8. eDP AUX CH Differential Pair

8.2.3 Line-Fault Detection Hardware Implementation

Line Fault Detection circuit is implemented at the system level using some external components. The faults that can be detected depends on the cable types and the actual system level implementation. The table below STP vs Coax Line-Faults provides a summary of the types of faults that can be detected in the example configurations using STP or the coax cable. Refer to application note *Diagnostic Features of FPD-Link IV Devices*, SNLA322 for more details.

The serializer device can detect fault conditions in the FPD-Link IV interconnect. If a fault condition occurs, the LINK_DETECT status is '0' (cable is not detected). The serializer device can detect any of the following conditions:

Table 8-6. STP vs Coax Line Faults

Status	STP	Coax
Cable Open	Yes	Yes
“+” to “-“ short	Yes	-
“+” to GND short	Yes	Yes
“-“ to GND short	Yes	-
“+” to Battery Short	Yes	Yes
“-“ to Battery Short	Yes	-

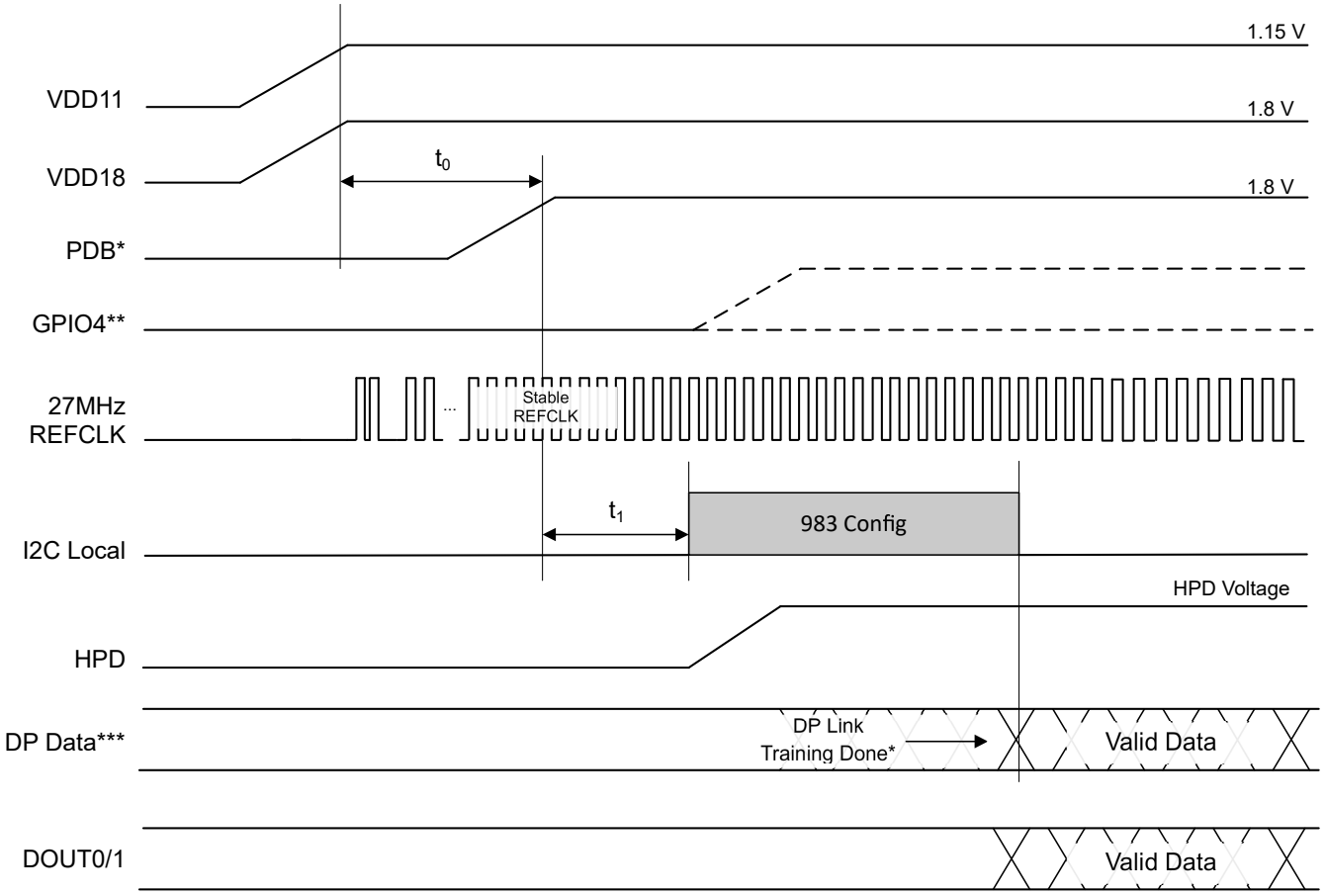
9 Power Supply Recommendations

The DS90UB983-Q1 requires multiple capacitors on each power supply pin with different value. TI recommends surface-mount capacitors with low ESR and ESL due to their smaller parasitic. When using multiple capacitors per power supply pin, place the smaller value closest to the device pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 4.7-µF to 100-µF range, which smooths low-frequency switching noise. In general, bypass capacitors must be placed as close to the power supply pins as possible, and the entry cap must immediately drop down to the ground plane on the other side of the capacitor to minimize the return path impedance.

9.1 Power Up Requirements And PDB Pin

VDD11 and VDD18 can rise in any order. A large capacitor on the PDB pin is needed to make sure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD18, a 10-kΩ pullup and a >10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until all power supplies have reached steady state. GPIO4/REM_INTB must not be pulled high during the power sequence. This causes the device to enter test mode and prevent the serializer from establishing link. If test mode is entered, Page_9 registers 0x84[2:0] and 0x94[2:0] need to be set to 0x2 to return to normal operation.

The recommended power up sequence is shown in Section 9.1



*27MHz REFCLK needs to be stable before PDB goes HIGH.

**During power on reset, GPIO4 pin should remain low to prevent device going into test-mode.

***DP link training time is system dependent.

Figure 9-1. Recommended Power Sequencing

Table 9-1. Power-Up Sequencing Constraints

SYMBOL	DESCRIPTION	REQUIREMENT DESCRIPTION	MIN	TYP	MAX	UNIT
	VDD11 Rise Time	10% to 90%	0.200		50	ms
	VDD18 Rise Time	10% to 90%	0.200		50	ms
t_0	Last power supply to PDB Delay	Time from when the last power supply reaches 90% to PDB reaches V_{IL}	0.05			ms
t_1	PDB to I^2C ready delay		3			ms

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the serializer/deserializer must be designed to provide low-noise power to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance can be greatly improved by using thin dielectrics (>4.4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypassing must be low-ESR ceramic capacitors with high-quality dielectric. The voltage rating of the ceramic capacitors must be at least 2× the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 47-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, a common practice is to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. For serializer/deserializer, only one common ground plane is required to connect all device related ground pins.

TI suggests a six-layer board with dedicated power and ground plane. Locate DP signals away from the single-ended or differential FPD-Link traces to prevent coupling from the DP signals to the TX outputs. The following sections provide important details for routing the FPD-Link and DP traces.

10.1.1 Bypass Capacitors

Figure 10-1 shows an example of how to layout the capacitors. Important to determine where to place the bypass capacitors so there is no unwanted noise coupling into the device. If the device is placed on the top side of the board, then the capacitor must be placed underneath of the device or the other way around. The engineer can place the capacitor close to the power supply pin on the bottom side of the PCB to free up space on the top side of the board for high-speed routing. This bottom placement also allows other signals to access the device pins more easily. TI recommends using a via on each end of the bypass capacitors to connect the power and ground pins directly to the power and ground planes. Connecting the power or ground pins to an external bypass capacitor increases the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass, but a larger cap like 10-µF is not available in a smaller 0603 or 0402 package. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonant frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, common practice is to use two vias from the power and ground pins to the planes to reduce the impedance at high frequency.

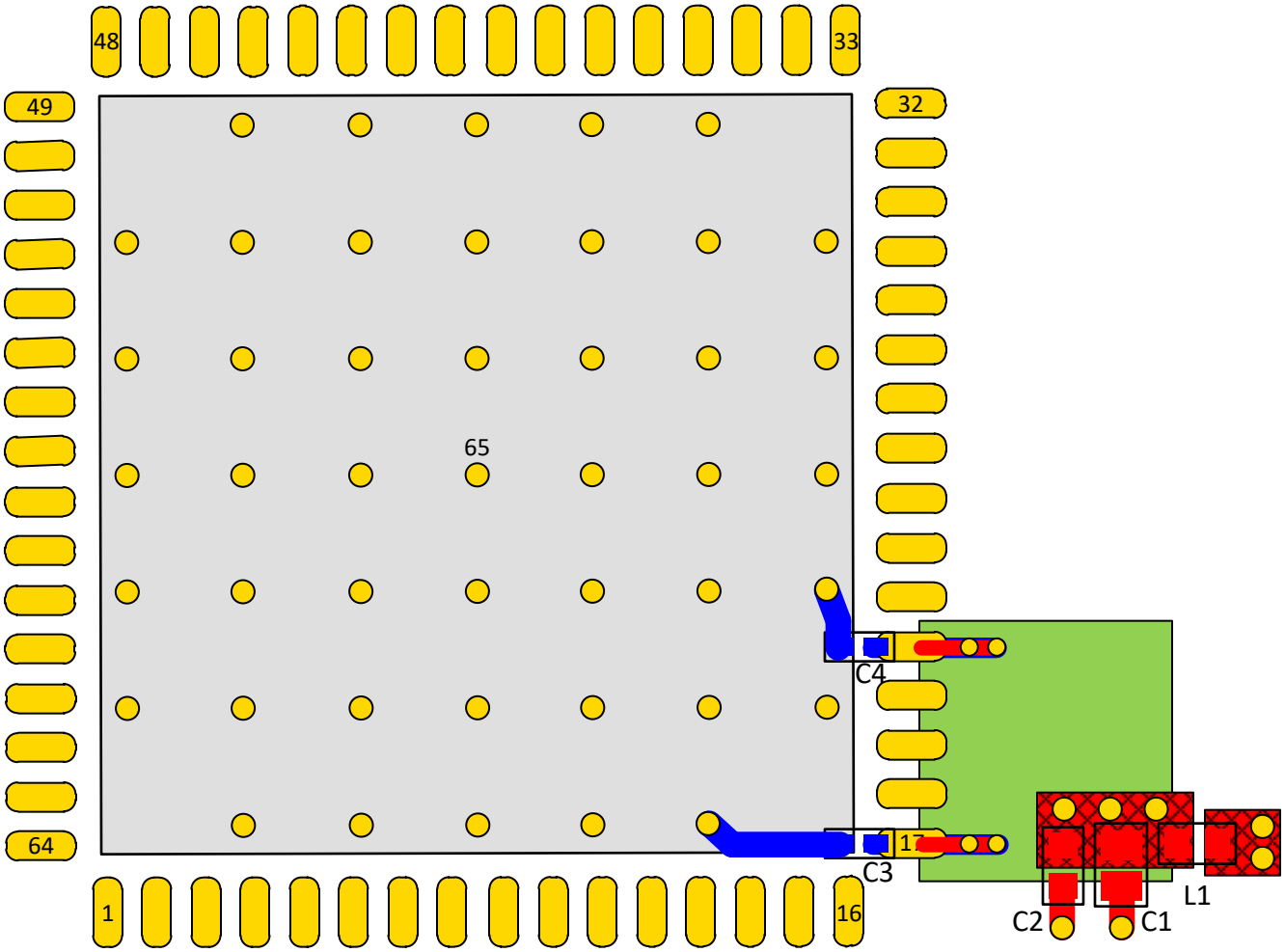


Figure 10-1. Recommended Capacitor Layout

Figure 10-1 is an example of the layout, but is not necessary to replicate the exact same layout. The QFN package has pins that surround the desired dimension with a vacant center courtyard available on the bottom sides. This is a great opportunity to use the space around the power and ground pins that are near the vacant center courtyard. In Figure 10-1, assuming the device is placed on the top side indicated in red, better to place the lowest value bypass capacitor on the bottom side (blue) designed for proximity while using the extra DAP space available. This makes the placing the bypass capacitors on the opposite side of the board in the courtyard area easy. C3 and C4 are the smallest values of the capacitor that can be placed right at the bottom of the power pin. This gives the lowest inductance path for power. C1 and C2 are the large value capacitors, and the inductor can be placed on the top side as shown in Figure 10-1. Each connection point of the components requires at least two vias with 10 mils minimum of hole diameter for the power path. The top red plane at C1 and C2 immediately drops down to the green plane of the power, which fanout the plane to pin 17 and 21 of the device. The trace widths around pins 17 and 21 must be equal and on the bottom side of the connection. The red traces on top of the plane and blue trace widths on the bottom of the plane shown in Figure 10-1 must also be of equal length. Pins 18, 19, and 20 is still accessible on the top side of the board after the connection.

10.1.2 Heat Conduction

There are three methods of heat transfer: heat conduction through solids, heat convection through fluids and gases, and heat generated by radiation. The heat conduction dominates the heat transfer in PCBs and is therefore most relevant to temperature in the PCBs.

Heat conduction is defined as the transfer of heat through a volume or a body. Heat is transferred through microscopic collisions of particles; the more collisions, the hotter the object is. Heat transfer occurs when there

is a temperature difference between two objects or between different areas of an object, and the rate depends on the geometry, thickness, and material of the object. Due to the law of equilibrium, heat transfers from a hotter body to a colder body until the whole system reaches final equilibrium, as shown in Figure 10-2. There is no net heat transfer between two objects that are equilibrium temperature. The equation for heat transfer through conduction is shown below:

$$\frac{Q}{t} = kA\frac{(T_2 - T_1)}{d} \tag{30}$$

where

- Q/t: The rate of heat transfer [J/s]
- k: the thermal conductivity of the material [W/m×K]
- A: Surface of the contact area [m^2]
- ΔT: The temperature difference of T1 temperature of one object and T2 temperature of the other [K]
- d: The thickness of the material [m]

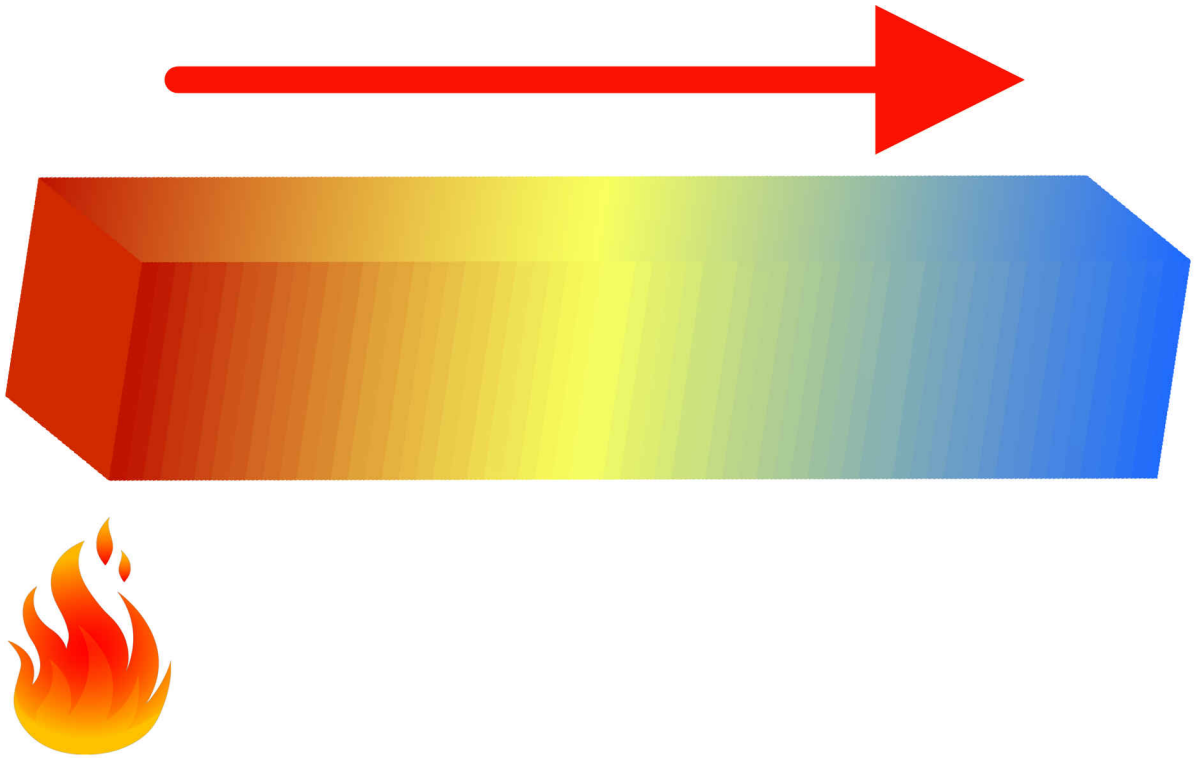


Figure 10-2. Heat Conduction Model

Thermal conductivity (k) is the measure of a material's capability to conduct heat and is used to describe how heat conducts through a material. Metals are highly thermally conductive whereas materials like air, wool, paper, or plastic are poor conductors of heat. Materials with a very low thermal conductivity, such as polystyrene foam, act like a thermal insulator.

The materials that are most relevant to thermal analysis of PCBs are copper, FR4, and solder mask. Copper is an excellent conductor of heat and conducts heat significantly faster than FR4. The table below lists the thermal conductivities found in PCBs. The higher the value, the more efficient the material is in transferring heat, which results in a shorter thermal response time. For low k values, the temperature gradient between the source and the sensor can be significantly large and must be considered carefully during layout.

Table 10-1. Material Thermal Conductivity Coefficients Of Selected Materials

Material	Thermal Conductivity k [W/(m×K)]
Air	0.0275
Solder Mask	0.245
FR4	0.25
Gold	314
Copper	385
Silver	406

10.1.2.1 Exposed Pad Layout Design

Packages with a DAP, such as QFN package, have a large exposed surface area through which heat can transfer quickly. These package types respond quickly to temperature changes of the copper plane which the DAP is soldered onto. Since the die sits directly on top of the exposed pad, heat can transfer rapidly from the die to the thermal pad. In Figure 10-3 depicts the cross section that the die is mounted on top of the metal plate leadframe with a conductive die adhesive, allowing for a fast thermal response transferring through the pins directly to the PCB.

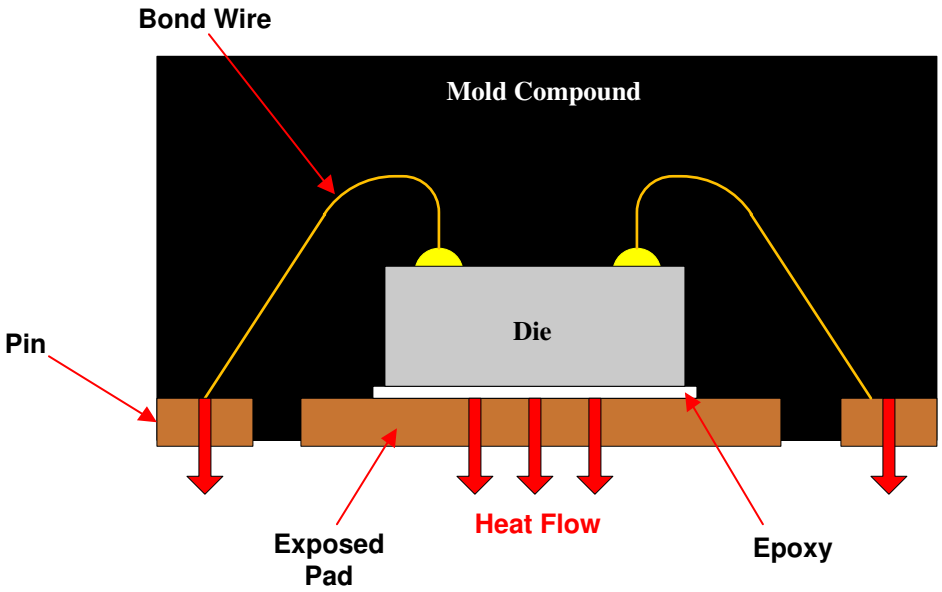


Figure 10-3. Heat Transfer QFN Package Cross Section Example

The Figure 10-4 illustrates the cross-section example when utilizing unused layer to create the similar to exposed pad within the layer stack-up. The copper areas of the PCB acts like a heat sinks for the QFN device where this helps extracting any heat dissipation from the device. The top copper areas of the PCB must be made per landing pattern guidelines. Any unused layer copper planes in the layer stack-up also can be connected to thermal pad using vias to create a thermal tunnel extracting the heat directly from the device out to the PCB bottom layer instead of spreading out across the PCB through the inner layers.

The dimensions of the thermal pad on the PCB must be equal to the exposed pad on the QFN as shown in Figure 10-4. The thermal vias must make their electrical connection to the created exposed pad on the multiple layers stack-up ground plane with a solid connection around the entire circumference of the plated through hole and the copper pour. The connection of the thermal vias from and exposed pad of the device using direct connect. Thermal relief connection is not recommended.

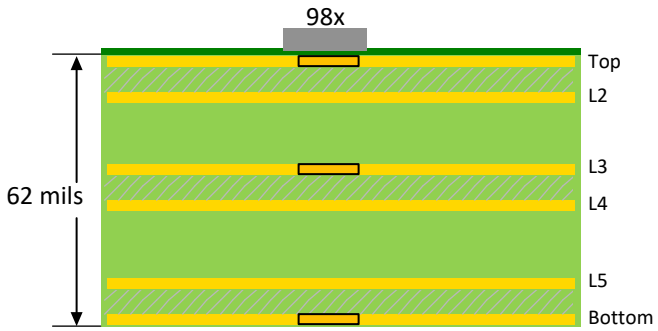


Figure 10-4. Exposed Pad Cross Section Example

10.1.3 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the FPD-Link devices QFN package to the GND plane with vias. TI suggests 45 thermal vias per mechanical drawing from the device center DAP to the ground plane. Refer to the data sheet landing pattern recommendation for more information. Connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the QFN style package, including PCB design and manufacturing requirements, is provided in TI Application Note: AN-1187 and QFN Package Application Note.

10.1.4 High-Speed PCB Layout

Good layout practice involves separating high-frequency or high-level inputs and outputs to minimize unwanted noise coupling and interference. High-speed PCB design requires proper routing and stack-up techniques to ensure the signal integrity of the circuit. The performance of the high-speed FPD-Link device is heavily dependent on the PCB layout, so pay attention to the routing of high-speed lanes. A poor PCB layout can lead to poor performance. As high-speed PCB layouts become more complex the impedance control, crosstalk, reflection, discontinuities, and stack-up guidelines described in the following can help ensure optimal performance of the FPD-Link devices.

10.1.4.1 PCB Stack-Up

During high-speed PCB design planning, constructing the multilayer stack-up prior to PCB design is critical. Planning an optimal circuit board stack up can help determine the routing methodologies quickly and easily. A well-defined stack-up can help reduce impedance mismatch and minimize the interference of external noise sources such as EMI. Circuit board layout and stack-up for the FPD-Link IV devices must be designed to provide low-noise power feed to the device. A four-layer board with a power and ground plane is feasible. TI recommends at least a 6-layer board to ensure optimal performance. Table 10-4 and Table 10-5 show each layer of the multilayer distribution as symmetrical and balanced.

10.1.4.1.1 Material Selection

Choosing the proper dielectric material is important for FPD-Link high-speed performance and impedance control. Each layer material is carefully chosen to meet the desired high-speed specification of the device. A hybrid version mixing high speed material with standard FR4 material can save on cost. The inner layers without high speed signals routing can use standard material for the prepreg/core substrates. When designing for high-speed signals above 10 Gbps, use premium PCB materials with low loss dielectric materials. Route high-speed SerDes traces with low loss PCB material. The PCB material thickness also dictates the characteristic 50-Ω and 100-Ω differential impedance requirements.

Table 10-2. PCB Dielectric Material Insertion Loss

Material	Board Class	Dk	Tan δ (Df)
FR4	Standard Loss	4.3	0.025
Isola 370HR		3.92	0.025
Isola FR406		3.92	0.0127
Isola FR408	Medium Loss	3.66	0.0127
Isola FR408HR		3.64	0.0098
GETEK		3.5	0.009
Isola I-SPEED		3.63	0.0067
Nelco 4000-13 EP		3.6	0.008
Megtron 6	Low Loss	3.33	0.003
Rogers 4350B		3.48	0.0037

Different laminate vendors offer a wide range of products as the value of the dielectric loss (Dk) and loss tangent (Df) differ from various cores and prepregs used in actual PCB constructions. Note that a small differences of Dk or Df can have a huge impact on controlled impedance lines and signal integrity. In order to prevent signal energy loss at high frequencies, the material uses must have a low Dk, Df and signal integrity features. A large loss tangent means higher dielectric absorption. Most of the high-speed material have a flatter Dk and Df as the frequency increasing and maintain a low dielectric loss.

Table 10-3. FPD-Link PCB Recommendations

Parameter	Min	Typ	Max	Units
PCB layer count	4	6	10	Layer
Dielectric (Dk) f < 10 Gbps f > 10 Gbps		 3.92 3.2	 4.3 3.6	Er
Loss tangent (Df) f < 10 Gbps f > 10 Gbps		 0.025 0.004	 0.030 0.010	Tanδ
T_g glass transition temperature	170	180		°C
Copper weight (trace thickness)	0.5	1		Oz
Surface roughness		0.1		mil (RMS)
Trace length, L		2		Inch
Trace width, W	5	8	10	Mils
Single-ended: Gap between P-trace to N-trace, S		3W		W
Differential: Gap between P-trace to N-trace, S Tightly coupled Loosely coupled		 S≤W S=2W		W
Single-ended characteristic impedance	45	50	55	Ω
Differential characteristic impedance	90	100	110	Ω
Differential connector and landing pads impedance	80	100	120	Ω
Intra-pair skew (delay difference between P+ and N- trace)			1	ps

Table 10-3. FPD-Link PCB Recommendations (continued)

Parameter	Min	Typ	Max	Units
Inter-pair skew (pair-to-pair delay difference)			10	ps

10.1.4.1.2 FPD Linerates for 10.8 Gbps or 13.5 Gbps

For linerates exceeding 10 Gbps, TI recommends low-loss dielectric material to ensure impedances are maintained for high-frequency electrical performance such as Megtron-6 and Rogers-4350. Use premium dielectric only where needed for high-speed interface and FPD-Link routing. The 98xEVMs are designed with Megtron6 material to accommodate up to the highest data rates >10Gbps.

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Copper Plating Thickness [mil]	Thickness after lamination [mil]
Soldermask										0.80
l1comp	Signal	H	75			Foil			0.17	0.60 *
				Press thk = 4.53 mil		Prepreg	1035(73) 1035(73)	Megtron 6 Megtron 6		4.53
l2mix	Mixed	1.0	61							1.20
				12.0 mil 1/1		Core		Megtron 6		12.00
l3pp	Plane	1.0	65							1.20
				Press thk = 4.42 mil		Prepreg	106(76) 1080(66)	PCL-370HR PCL-370HR		4.42
l4mix	Mixed	1.0	62							1.20
				10.0 mil 1/1		Core		Megtron 6		10.00
l5mix	Mixed	1.0	63							1.20
				Press thk = 4.44 mil		Prepreg	1080(66) 106(76)	PCL-370HR PCL-370HR		4.44
l6pp	Plane	1.0	65							1.20
				12.0 mil 1/1		Core		Megtron 6		12.00
l7mix	Mixed	1.0	61							1.20
				Press thk = 4.53 mil		Prepreg	1035(73) 1035(73)	Megtron 6 Megtron 6		4.53
l8sold	Signal	H	74			Foil			0.17	0.60 *
Soldermask										0.80

Figure 10-5. 8 Layers Stack-Up Information

Table 10-4. EVM Stack-up Details

# OF LAYER	LAYER	TYPE	THICKNESS(MILS)	COPPER WEIGHT (oz)	DIELECTRIC CONSTANT	LOSS TANGENT	COUPLING TYPE
	MASK	SURFACE	0.8		3.2	0.035	
1	TOP	CONDUCTOR	0.7	0.5			COATED COUPLED MICROSTRIP
		PREPREG	4.53		3.2	0.004	
2	SIGNAL-1	CONDUCTOR	1.4	1			
		CORE	12		3.6	0.004	
3	GND 1	PLANE	1.4	1			
		PREPREG	4.42		3.92	0.025	
4	PWR1	PLANE	1.4	1			
		CORE	10		3.6	0.004	
5	PWR2	PLANE	1.4	1			
		PREPREG	4.44		3.92	0.025	
6	GND 2	PLANE	1.4	1			
		CORE	12		3.6	0.004	
7	SIGNAL-2	CONDUCTOR	1.4	1			
		PREPREG	4.53		3.2	0.004	
8	BOTTOM	CONDUCTOR	0.7	0.5			COATED COUPLED MICROSTRIP
	MASK	SURFACE	0.8		3.2	0.035	

10.1.4.1.3 FPD Linerates for ≤ 6.75 Gbps

When designing for high-speed signals below ≤ 6.75 Gbps, a standard to medium loss material can be used for the stack-up construction. FR4 is the most commonly used PCB material in most lower frequency applications.

Table 10-5. EVM Stack-up Details

# OF LAYER	LAYER	TYPE	THICKNESS (MILS)	COPPER WEIGHT (oz)	DIELECTRIC CONSTANT	LOSS TANGENT	COUPLING TYPE
	MASK	SURFACE	0.8		3.2	0.035	
1	TOP	CONDUCTOR	1.4	0.5			COATED COUPLED MICROSTRIP
		PREPREG	3.324		3.8		
2	SIGNAL-1	CONDUCTOR	1.4	1			
		CORE	9.843		3.8		
3	GND 1	PLANE	1.4	1			
		PREPREG	6.469		4.25		
4	PWR1	PLANE	1.4	1			
		CORE	11.811		4.25		
5	PWR2	PLANE	1.4	1			
		PREPREG	5.907		4.25		
6	GND 2	PLANE	1.4	1			
		CORE	9.843		3.8		
7	SIGNAL-2	CONDUCTOR	1.4	1			
		PREPREG	3.234		3.8		
8	BOTTOM	CONDUCTOR	1.4	0.5			COATED COUPLED MICROSTRIP
	MASK	SURFACE	0.8		3.2	0.035	

10.1.4.2 Controlled Impedance

It is important to maintain DSI, DisplayPort, OLDI and FPD-Link IV differential trace impedance of 100 Ω with a ±10% differential to avoid impedance mismatches in the transmission line that could affect the signal integrity. For eDP interface, the differential trace impedance is 85 Ω ±15%. The mismatch creates discontinuities, which causes reflections on the signal traces. The differential impedance is determined by the combination of the physical dimensions, the trace width, the adjacent ground, and the properties of material used in PCB substrate. Many software tools are available to calculate the properties of the transmission line structures.

Table 10-6. Impedance Controlled for Various Interfaces

Type of Interface	Differential Impedance
DisplayPort (DP)	100 Ω ±10%
Embedded DisplayPort (eDP)	85 Ω ±15%(1)
FPD-Link IV	100 Ω ±10%

(1) Embedded DisplayPort (eDP) differential impedance is targeted at 85 Ω ± 15 % based on eDP standard specification. The differential signals may designs for 100 Ω ±10% PCB traces to maintain signal integrity.

10.1.4.3 Differential Traces

They are all tightly coupled in both separation and equal length to benefit from the electromagnetic field cancellation. When the differential pairs are symmetrical and have the same length, the pairs provide excellent noise immunity. This helps minimize impedance discontinuity because this setup prevents traces from branching out and other sudden changes in large landing pads as shown in Figure 10-13.

10.1.4.4 Microstrip vs Stripline Methodologies

Microstrip and Stripline structures are often used in high-speed PCB design. Between the microstrip and stripline, the decision of which method to use is based on the needs of the design and applications. Both methods are excellent performance for high-speed frequency. Both methods are designed for routed traces that have the correct structure when the return path signals travel along the traces through a plane that is separated by a certain width and height in Figure 10-6 and Figure 10-7.

In Figure 10-6 shows a microstrip configuration with a soldermask top conductor and a dielectric layer separated by bottom ground plane. The P and N traces differential pairs are separated by a uniform distance of S. The spacing between two differential traces can be S = W for tightly coupled traces.

- H = the height distance of the dielectric from the differential pair to the ground reference plane
- S = the separation distance between the two traces of the differential pair
- W = the width of the copper trace
- T = the thickness of the copper trace
- T_{sm} = the thickness of the soldermask
- E_r = the dielectric constant of the substrate between copper trace and the ground reference plane

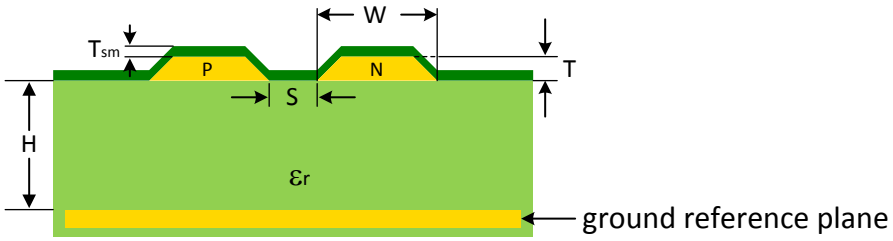


Figure 10-6. Microstrip Differential Pair With Soldermask Coated

For the microstrip, the electric field travels along the trace exposed to the air whereas the trace in the stripline is fully by reference planes.

In Figure 10-7, stripline constructs top and bottom ground planes with dielectric insulator material surrounding a center conductor in a balanced configuration. The two differential traces are sandwiched between ground reference planes 1 and 2, as well as along the traces when there is a ground via stitching. The P and N traces differential pairs are also separated by a uniform distance of S.

- H_1 = the height distance of the dielectric from the ground reference plane 1 to the differential pair
- H_2 = the height distance of the dielectric from the differential pair to the ground reference plane 2
- S = the separation distance between the two traces of the differential pair
- W = W_1 = W_2 = the width of the copper trace
- T = the thickness of the copper trace
- E_{r1} = the dielectric constant of the substrate between the ground reference plane 1 and copper trace
- E_{r2} = the dielectric constant of the substrate between the copper trace and the ground reference plane 2

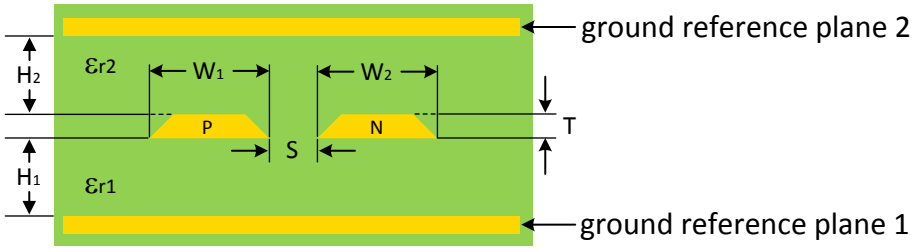


Figure 10-7. Stripline Differential Pair

10.1.4.5 Length Matching

Length matching is also a critical requirement parameter for and FPD-Link IV differential pairs. When the high-speed signal lanes are length matched, it helps closely match the propagation delay between P and N.

The mismatch of the P and N traces introduces skew. To compensate the length mismatch, serpentine routing can be used on the shorter trace length, and most CAD tools are available to implement the serpentine routing as shown in Figure 10-8 by using trace tuning. It is very important that the engineer choose the dimensions of the trace tuning carefully so that all the critical signals simultaneously arrive together at their destination. The serpentine trace must be routed as close to the source as possible.

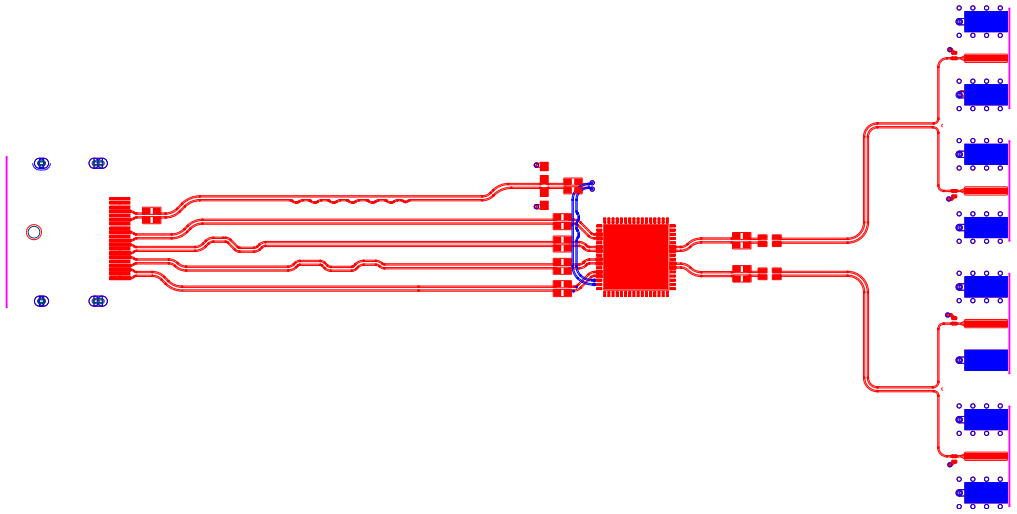


Figure 10-8. Example Layout for Length Matching

10.1.4.5.1 Intra-Pair Skew Matching

Intra-pair skew occurs when the differential signals of P and N are not equal length. When matching the intra-skew of the P and N differential signals, the serpentine routing can be used on the shorter trace length at the source to match the lengths as close as possible. The skew adjustment can be used on the loosely coupled trace to implement the serpentine techniques.

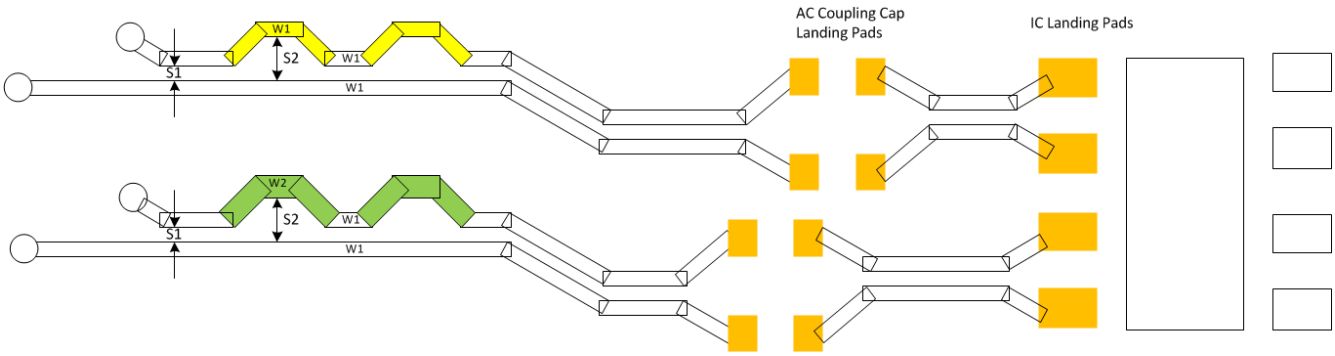


Figure 10-9. Intra-Pair Skew and Inter-Pair Matching

10.1.4.5.2 Inter-Pair Skew Matching

Inter-pair skew is used to compare the difference between a differential pair from another differential pair of the same group, such and two pairs of FPD-Link IV of the serializer device.

10.1.4.6 Width and Spacing

The P and N traces along with the spacing between the P and N, are required to calculate characteristic impedance. The impedance of the differential trace is controlled by the width of the trace, air gap between P and N, stack-up, dielectric, and materials. To maintain a uniform-controlled impedance of the 100-Ω differential pair, the spacing between positive and negative not be exceed 2x the trace width.

10.1.4.7 Crosstalk

The high-speed differential pair of P and N traces must be tightly coupled and routed in parallel with each other as much as possible, and the adjacent differential pair signals must maintain a constant distance away from the other traces to prevent coupling. The electromagnetic energy stays on track when traveling along the coupled traces, but the energy can escape if there is interfere from an adjacent signal. If the electromagnetic energy escapes, the EMI coupling in to the neighboring signals is called crosstalk.

10.1.4.8 Via

The controlled impedance of the differential via is also important to maintain 100-Ω impedance for the high-speed signals. The differential via impedance depends on many parameters, such as the hole size, pad size, anti-pad size, number of VDD/GND layers, via length, via stub, and via pitch. It is possible to create a controlled impedance via of the high-speed differential via by optimizing the physical dimensions of the PCB design. The differential via of the high-speed signal can be in close proximity with oval anti-pad shared by the two vias reduces parasitic capacitance. The engineer must also place a ground via next to each P and N differential via and evenly space the D1 and D2 lengths between the differential via signals to provide a good return path and isolation for the vias. See Figure 10-10 for an example.

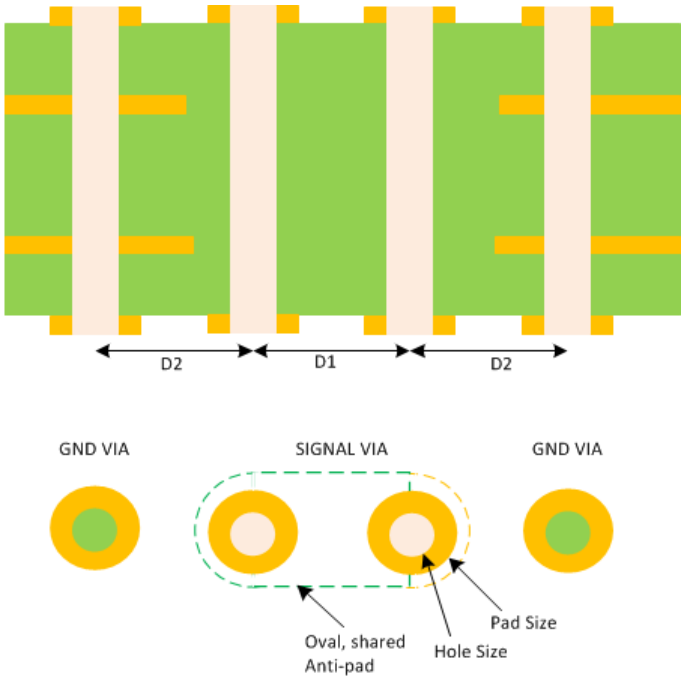


Figure 10-10. Controlled Impedance Differential Via

10.1.4.8.1 Via Stub

Regardless of the routing techniques used for microstrip or stripline methodologies, via stub is not recommended for high-speed differential signals of the DSI, OLDI, DisplayPort andFPD-Link IV. This is because the via stub can bring a capacitive effect to the differential signals and increase the signal loss. Routing the high-speed differential signal traces on the top and bottom layers avoids the use of vias and allows a clean interconnect from the to the device and the device to the output connector. To mitigate a via stub, the engineer can use a blind or buried via, back-drilling, or a through via from the top to bottom using microstrip techniques. For example, in the left image of Figure 10-11, the device is placed on the top layer while the P and N differential signals are routed from the top layer to the bottom through a through via on a microstrip to avoid via stub. If the differential signals are routed through the internal layer, TI recommends a blind or buried via as well as back-drilling to create the shortest stub possible to avoid reflection.

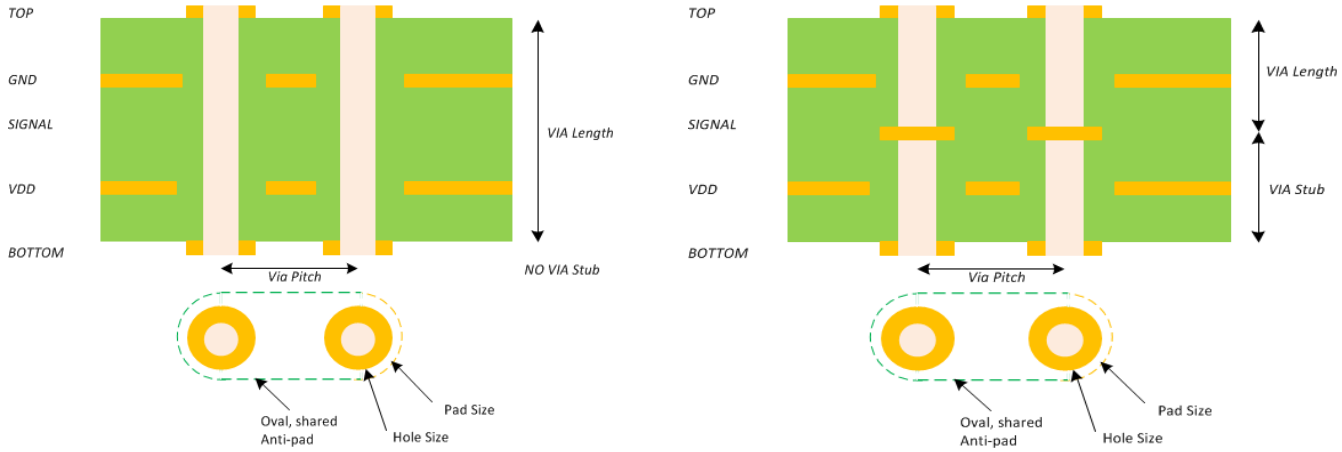


Figure 10-11. Example of Via Stub

In Figure 10-12, the device is placed on the top layer as well as on a top-mount through-hole component. The differential signal traces, therefore, must use bottom trace routing to avoid the via stub. If the top trace routing restricts the top layer routing, the connector can be flipped and placed on the opposite side of the connector.

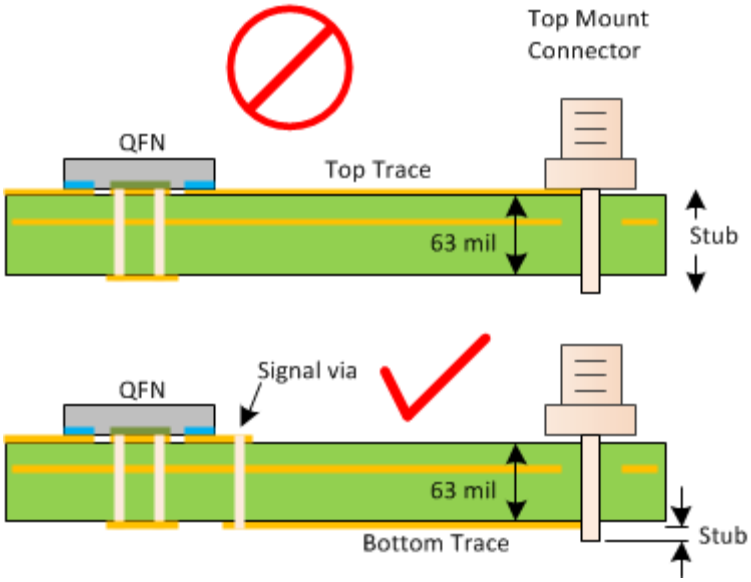


Figure 10-12. Example of Voided Via Stub

10.1.4.9 Anti-Pad

The anti-pad is the unwanted clearance area normally between the pad or trace to the copper plane, or the voided clearance area beneath the high-speed signals landing pad or blinded/buried via in the power or ground plane. Having the anti-pad can help maintain the impedance of the transmission line. The engineer cannot manually calculate the clearance of the anti-pad during layout process, but an electromagnetic field solver such as modeling software can be used to determine the effect and size of the high-speed signal trace behavior of the anti-pad for optimizing the impedance. The initial anti-pad clearance of 20 mils can be used from the trace to the copper plane for DSI, DisplayPort, OLDI and FPD-Link IV signals, and the engineer can add another 2-5 mils to the original discrete components. However, TI recommends to use the modeling software to determine the exact clearance for the design optimizing the impedance compensation.

Figure 10-13 is the example of mismatch when looking into A-A and B-B cross sections. The A-A section is excellently matched, but the cross section B-B does not match. This is due to the bottom ground plane. To

achieve the 100-Ω impedance, an anti-pad can be used as clearance from the pad to a shape or the next power or ground plane. This technique can reduce the parasitic capacitance.

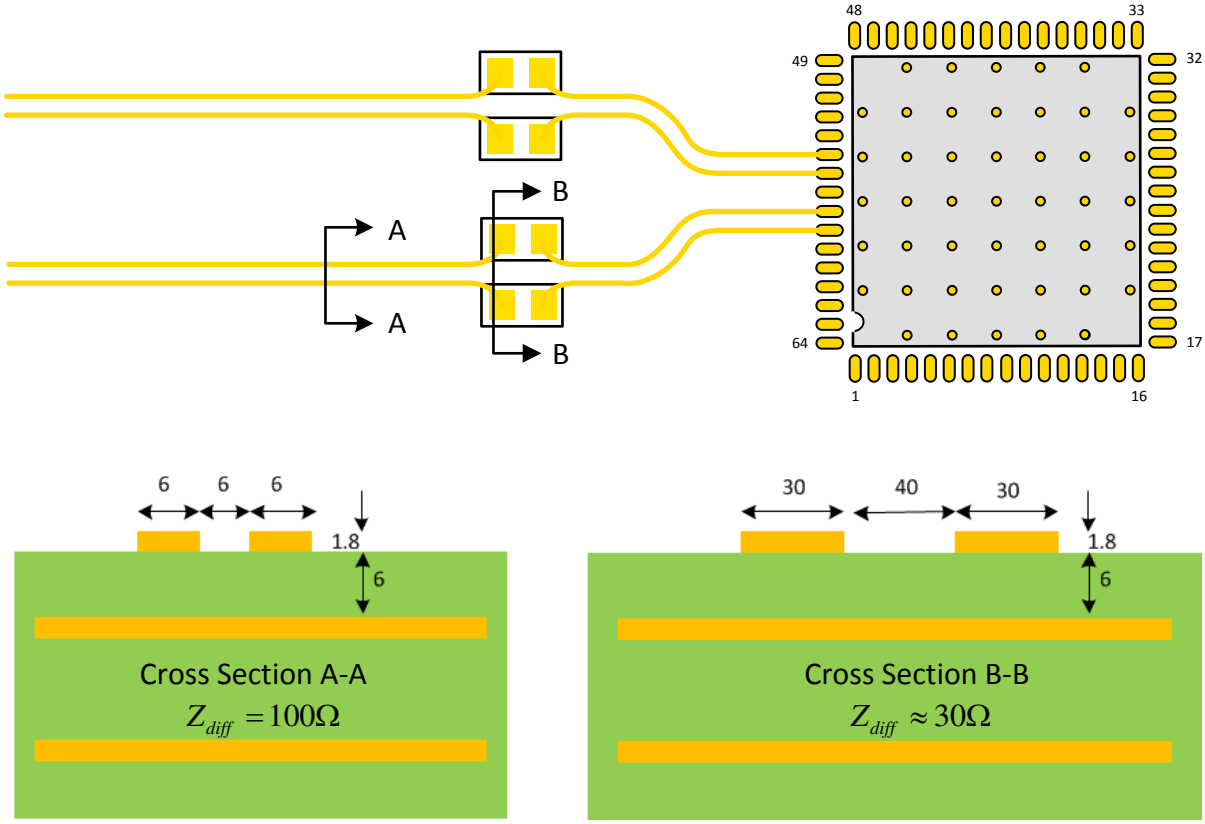


Figure 10-13. Impedance Mismatch From Landing Pads

To compensate the impedance mismatch of the cross section B-B of the landing pads, the power or ground relief layer, and sometimes the next internal layer, must open up and void the clearances underneath the landing pads. This significantly increases the impedance to match cross section A-A. This can be done along the high-speed lanes of the DSI, DisplayPort, OLDI and FPD-Link IV to ensure the 100-Ω differential pair meets the specification.

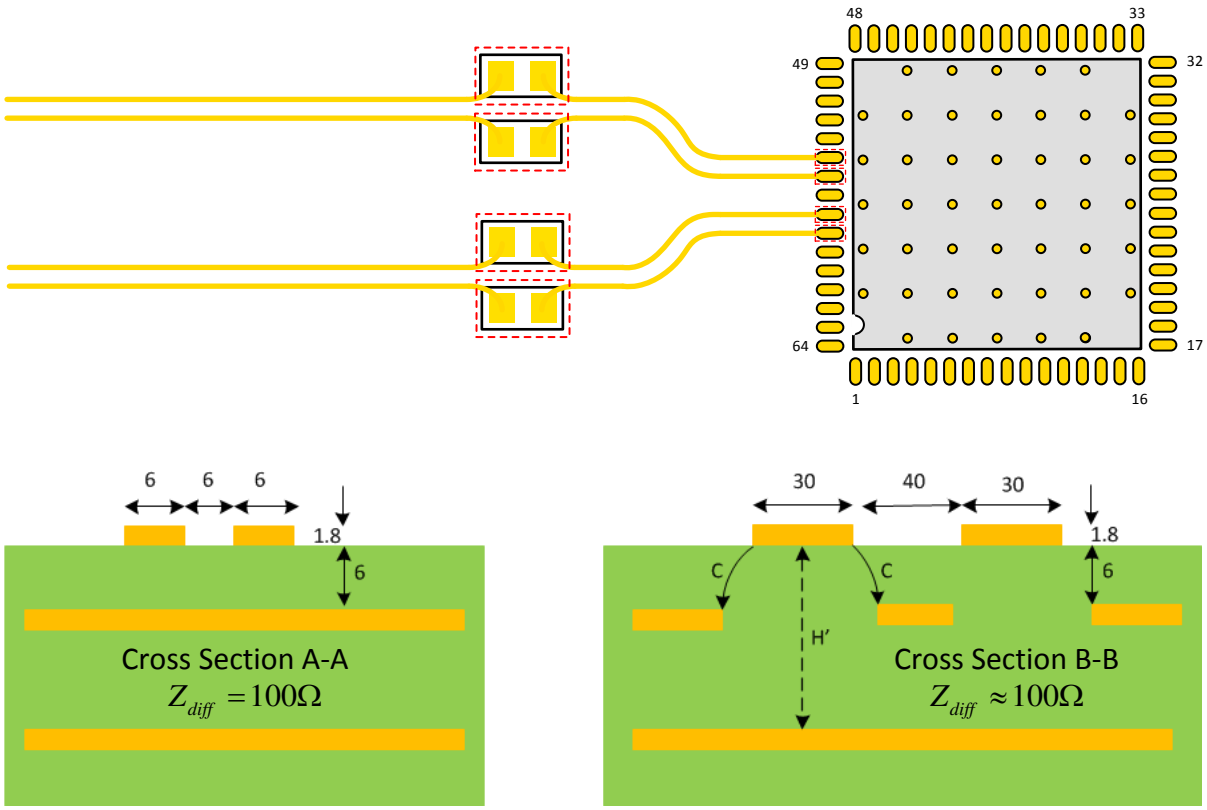


Figure 10-14. Controlled Impedance Landing Pads

The anti-pad for the surface mount connector is very similar to other surface mount IC pad and other discrete components. The ground or power plane must void the clearance area under the landing pad of the connector. The through-hole connector uses the same techniques as a via.

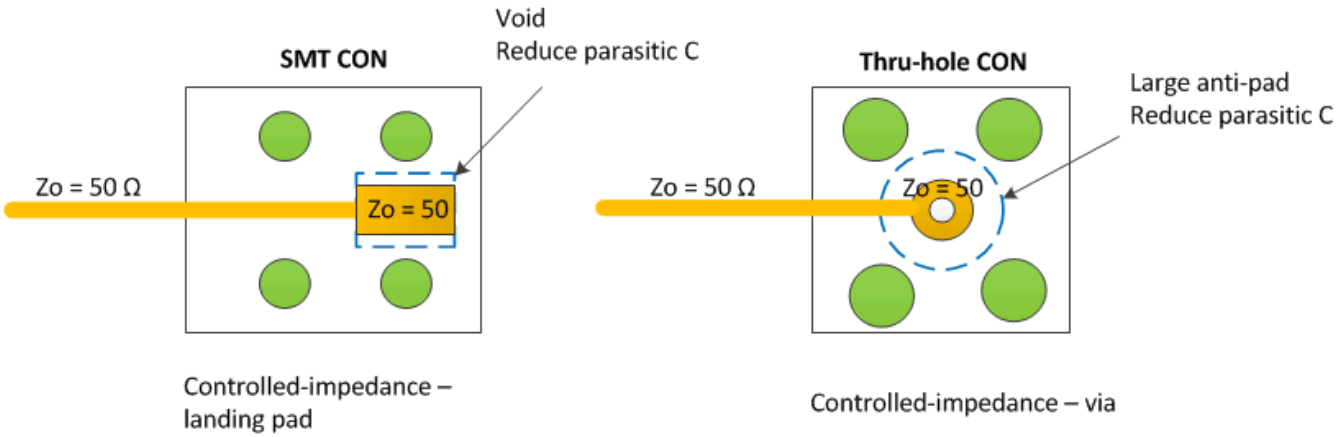


Figure 10-15. Controlled Impedance Footprint for Connectors

10.1.5 Routing FPD-Link Signal Traces

Routing the FPD-Link signal traces between the DOUT pins and the connector is one of the most critical pieces of a successful DS90UB983-Q1 PCB layout.

The following list provides essential recommendations for routing the FPD-Link signal traces between the DS90UB983-Q1 transmitter output pins (DOUT) and the cable connector

- The routing of the FPD-Link traces can be all on the top layer or partially embedded in middle layers if EMI is a concern
- The AC-coupling capacitors can be on the top layer and very close to the DS90UB983-Q1 transmitter output pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the DOUT traces between the AC-coupling capacitor and the cable connector as a 100-Ω differential trace with tight impedance control (±10%). Calculate the proper width of the trace for a 100-Ω impedance based on the PCB stack-up. Make sure to length match the DOUT+ and DOUT- traces.

10.1.6 Routing Coax Signal Traces

The DS90UB983-Q1 can be used to configure coax mode as shown in the Typical Diagram Connection. In single-ended signaling, both P and N signals can be routed differentially and the N signal can be terminated with a 50Ω resistor to ground as close as possible to the coax connector on both ends of the serializer and deserializer devices. Placing the termination close to the connector improves the echo cancellation and reflection before transmitting electrical signal over the wires. A reference plane can be placed near the traces or underneath the next layer maintaining controlled impedance and provides a good shielding against EMI.

10.1.7 Routing DisplayPort Signal Traces

Routing the DisplayPort signal traces between the DP/eDP pins and the DP/eDP connector is also important for a successful DS90UB983-Q1 PCB layout. Recommendations are given in the following list:

1. Route DP pairs as differential coupled with controlled 100-Ω differential impedance (±10%)
2. Route eDP pairs as differential coupled with controlled 85-Ω differential impedance (±15%)
3. Keep the trace length difference between DP/eDP traces to 5 mils of each other.
4. Length matching can be near the location of mismatch.
5. Each pair can be separated at least by 5 times the signal trace width.
6. Keep away from other high-speed signals.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend can be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on one or two layers.
9. Keep the number of signal vias to a minimum — TI recommends keeping the via count to a maximum of two per DP/eDP trace.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.
12. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

Table 10-7. DisplayPort Layout Parameters

Parameter	Value
Frequency	DisplayPort RBR: 0.81 GHz (1.62 Gbps)
	DisplayPort HBR: 1.35 GHz (2.7 Gbps)
	DisplayPort HBR2: 2.7 GHz (5.4 Gbps)
	DisplayPort HBR3: 4.05 GHz (8.1 Gbps)
Max Intra-Pair Skew	1 ps (TI recommends about 5 mils)
Trace Impedance (DP)	100Ω ±10% differential
Trace Impedance (eDP)	85Ω ±15% differential(1)

10.1.8 Summary of High-Speed Differential Signal Design Layout Consideration

- Planning helps avoid re-spin and unexpected issues.
- Do not create a test pad or test points on any high-speed differential signal.
- Avoid high-speed routing near crystals, oscillators, clock signal generators, switching power regulators, or magnetic devices.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent ground layer to avoid via stub.
- Maintain a constant 100-Ω impedance for the differential signal traces along the high-speed path.
- Minimize the use of vias on high-speed signal traces as much as possible.
- Maximize differential pair-to-pair spacing when possible to avoid crosstalk.
- Place ESD and EMI protection devices as close to the connector as possible.
- Place the AC-coupling capacitors on the protected side of the CMC and as close to the CMC as possible.
- Keep the FPD-Link IV high-speed differential signal trace that is close to the connector as short as possible.
- Create a ground pours on the top and bottom layers.
- Do not use splitting ground. Always use solid ground plane.
- Put the largest-value filter bypass capacitors near power entry, and place high-quality X7R decoupling 0.1-µF capacitors close to device pins.
- Minimize intra-pair skew.
- Keep both P and N differential pair signal traces tightly coupled.
- Use angle smoothing techniques for routing traces and do not use right-angle bends.
- To minimize crosstalk, keep the distance between two traces approximately 2 to 3 times the width of the trace.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Soldering Specifications Application Report,* SNOA549
- *Semiconductor and IC Package Thermal Metrics Application Report,* SPRA953
- *Leadless Leadframe Package (LLP) Application Report,* SNOA401
- *LVDS Owner's Manual,* SNLA187
- *I2C Communication Over FPD-Link III with Bidirectional Control Channel,* SNLA131A
- *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices,* SNLA132
- *I2C Bus Pullup Resistor Calculation,* SLVA689
- *FPD-Link Fundamental Material FPD-Link Learning Center,*
- *LVDS SerDes Gen I PCB and Interconnect Design-In Guidelines* SNLA008A
- *Ten tips for successfully designing with automotive EMC/EMI requirements*
- *DS90Ux983-Q1 Schematic and PCB Layout Guidelines*
- *Serial Line-Fault Detection Application Report* SNLA322

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

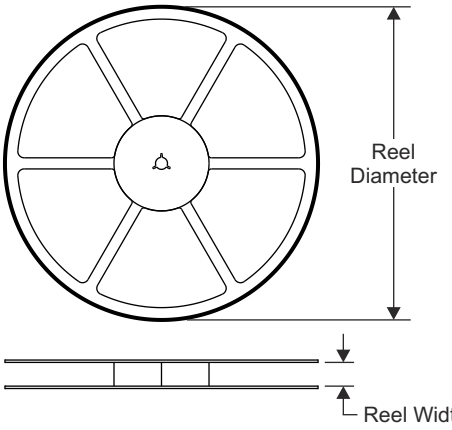
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

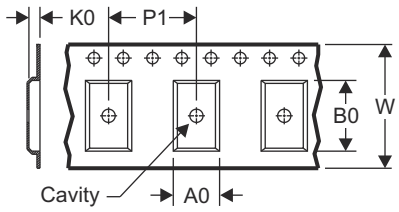
Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4/5)
DS90UB983RTDRQ1	ACTIVE	VQFN	RTD	64	2000	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-40 to 105	UB983
DS90UB983RTDTQ1	ACTIVE	VQFN	RTD	64	250	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-40 to 105	UB983

12.2 Tape and Reel Information

REEL DIMENSIONS

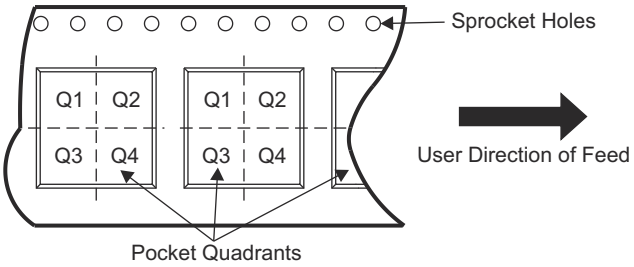


TAPE DIMENSIONS



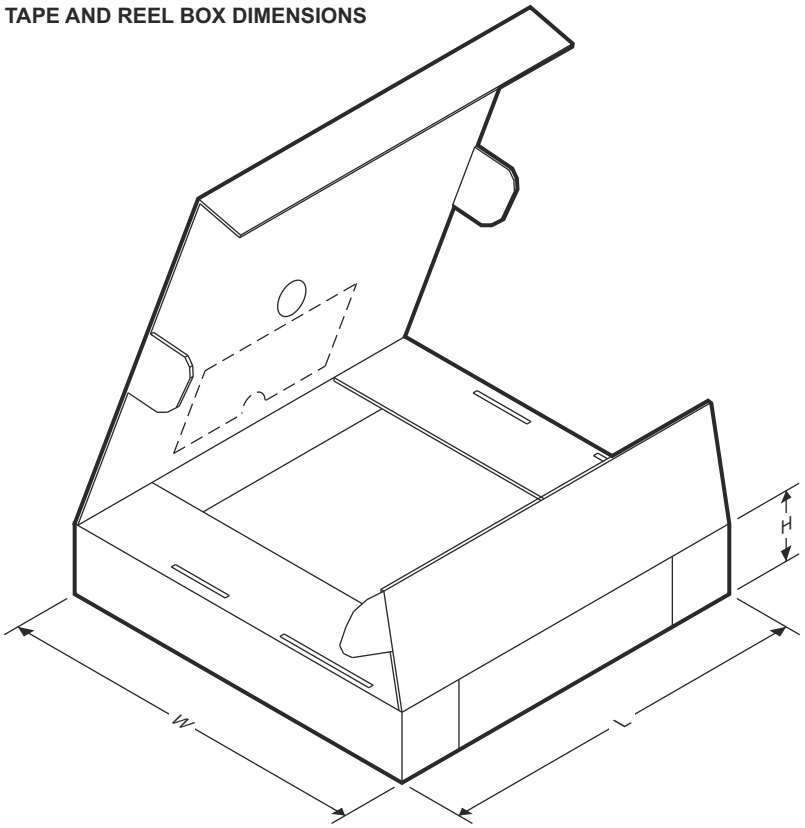
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB983RTDRQ1	VQFN	RTD	64	2000	330	16.4	9.3	9.3	1.1	12	16	Q2
DS90UB983RTDTQ1	VQFN	RTD	64	250	180	16.4	9.3	9.3	1.1	12	16	Q2

TAPE AND REEL BOX DIMENSIONS



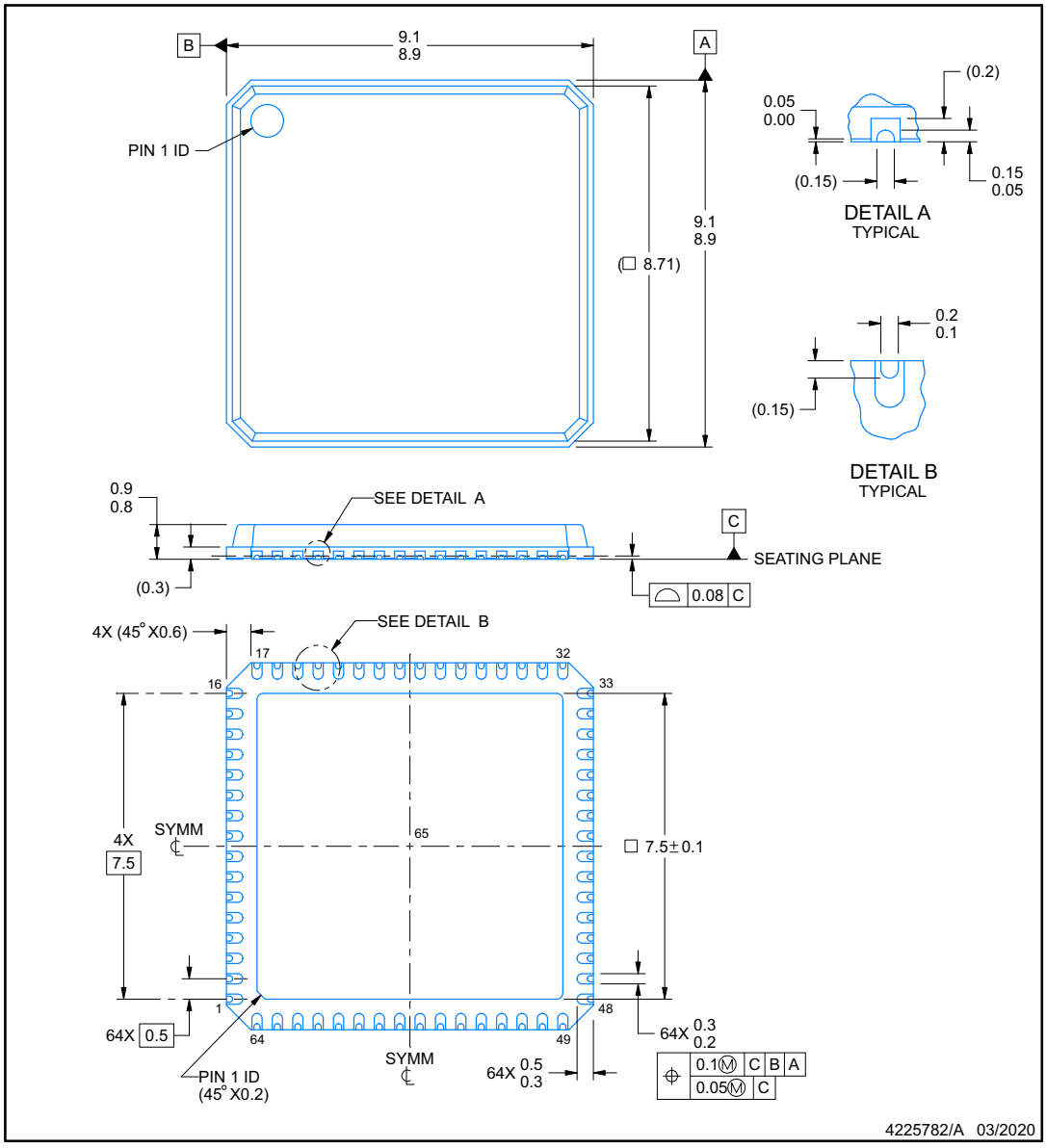
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB983RTDRQ1	VQFN	RTD	64	2000	367	367	35
DS90UB983RTDTQ1	VQFN	RTD	64	250	210	185	35

PACKAGE OUTLINE

RTD0064M

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

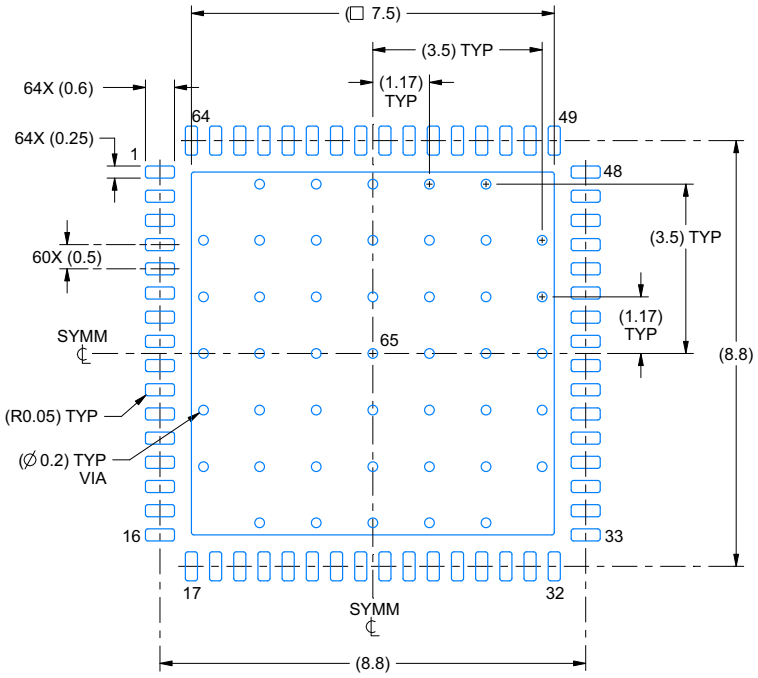
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

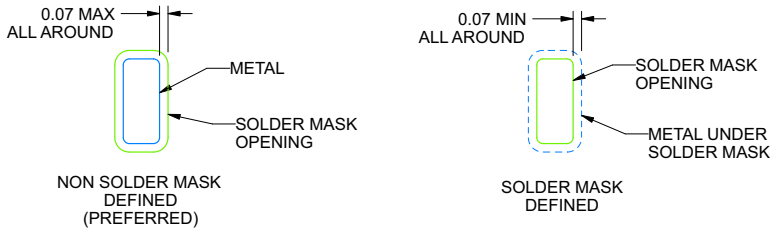
RTD0064M

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4225782/A 03/2020

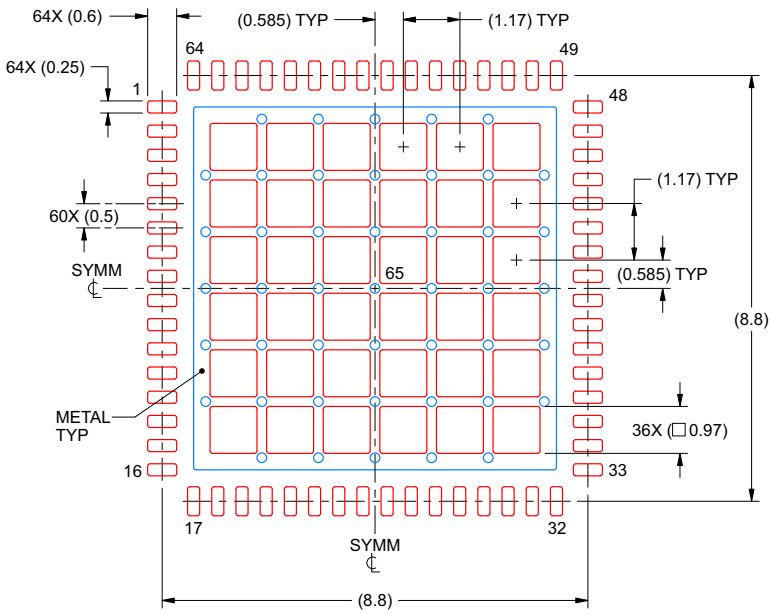
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTD0064M — **VQFN - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

4225782/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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>>TI(德州仪器)