

Integrated Power Management/Audio CODEC

FEATURES

- **Power**
 - Three Efficient Stepdown Converters
 - Four External Linear Low-Dropout Regulators (LDOs) for Clocks and Peripherals
 - SmartReflex™ Dynamic Voltage Management
- **Audio**
 - Differential Input Main Microphones
 - Mono Auxiliary/FM Input
 - External Predrivers for Class-D (Stereo)
 - TDM Interface
 - Automatic Level Control (ALC)
 - Digital and Analog Mixing
 - 16-bit Linear Audio Stereo DAC (96 kHz, 48 kHz, 44.1 kHz, 32 kHz, and Derivatives)
 - 16-Bit Linear Audio Stereo Analog-to-Digital (ADC) (48 kHz, 44.1 kHz, 32 kHz, and Derivatives)
- **USB**
 - USB 2.0 OTG-Compliant High-Speed Transceivers
 - 12-Bit (UTMI) + Low Pin Interface (ULPI)
 - USB Power Supply (5V charge pump for VBUS)
 - CEA-2011: OTG Transceiver Interface Specification
 - CEA-936A: Mini-USB Analog CarKit Specification
- **Additional**
 - LED Driver Circuit for Two External LEDs
 - Two External 10-Bit Monitoring ADC Inputs
 - Real-Time Clock (RTC) and Retention Modules
 - High-Speed I²C Serial Control
 - Thermal Shutdown and Hot-Die Detection
 - Keypad Interface (up to 6 × 6)
 - External Vibrator Control
 - 15 GPIOs
 - 0,65mm Pitch, 139 Pin, 10 × 10 mm Package

DESCRIPTION

The TPS65930 is an integrated power-management/audio codec device for use in portable cellular phones, portable media players, and other portable devices that derive their power from batteries based on Li-ion, Li-ion polymer, or manganese-cobalt chemistries. The TPS65930 receives commands from the host controller and provides power conversion/regulation and a complete audio codec section and class-D audio amplifier.

In addition to generic support capabilities, the TPS65930 meets the specific power requirements of the TI OMAPV1230, OMAP2430, and OMAP3430 devices.



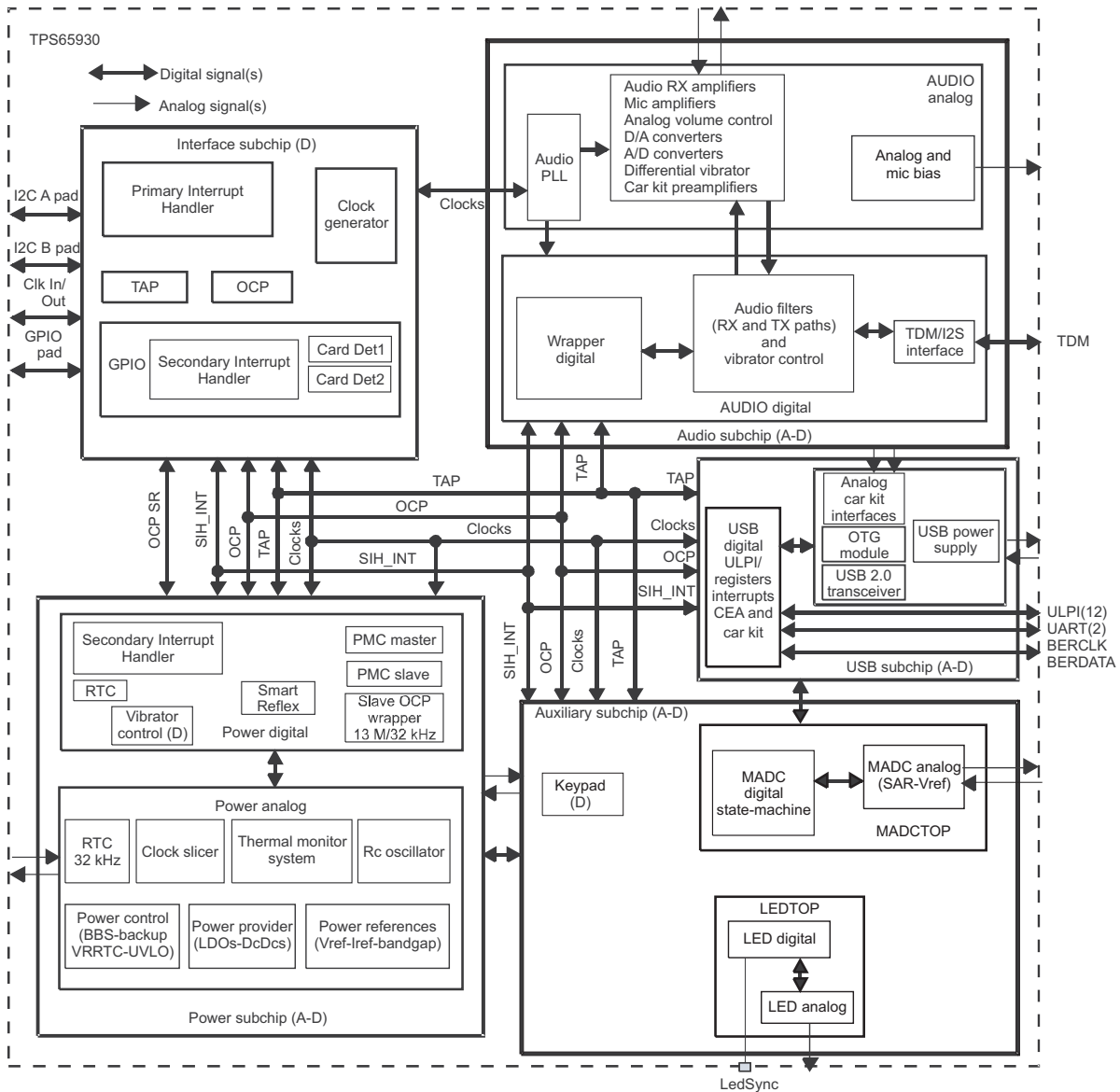
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Figure 1. Block Diagram

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MODULE DESCRIPTION

Power subchip:

The SMPS have configurable output voltages. The LDO regulators provide power to internal analog and digital circuits and to the external components. The output voltages of the external LDOs are also configurable.

The power resources also have configurable modes of operation. The possible modes for the power resources are SLEEP, ACTIVE, and OFF. The modes and output values can be programmed using the I2C interface on the TPS65930 device.

Programming for all the power resources is done through the I2C interface. The power subchip interfaces the interface subchip and carries out commands to the rest of the device. The digital section has a finite state-machine (FSM) that manages commands to the resources through the power bus.

Audio subchip:

The audio subchip has one interface: I2S for audio signaling. I2S can function as master or slave.

Sampling modes available are:

Audio channel with 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48-kHz sampling modes. 96 kHz is supported on the RX path voice codec with MCLK = 26MHz.

The audio phase-locked loop (PLL) supports 26-MHz, 19.2-MHz, or 38.4-MHz ability to work with two ports with the clock frequencies 19.2 MHz or 26 MHz, or with a single TDM port with the frequencies 19.2 MHz, 26 MHz, or 38.4 MHz.

The audio supports common features like pop-noise reduction, sidetone functionality, bass boost function, uplink and downlink programmable gain amplifiers, and the DTMF tone generator.

The external vibrator control is provided in this module and can be controlled through an audio signal or direct I2C writes to the registers.

USB subchip:

The primary function of the universal serial bus (USB) physical layer (PHY) is to transmit and receive USB data at high speed (480M bit/s), full speed (12M bit/s), and low speed (1.5M bit/s). It also provides a pin-optimized standard ULPI interface to a main USB controller device (LINK). In addition to the higher speeds, it supports 3-pin and 4-pin serial modes of operation.

The TPS65930 has a 5V-tolerant data line at all supported speeds. VBUS is tolerant up to 6 V. This device has an on-chip 480MHz PLL from the internal system clock.

Auxiliary subchip:

The auxiliary subchip includes the following modules:

- Monitoring Analog-to-Digital Conversion (MADC)
- Keypad
- LED

MADC:

The MADC enables the host processors to monitor analog signals (such as RF module temperature, battery temperature, battery type, and battery level) using analog-to-digital conversion (ADC) on the input source. After the conversion is complete, the host processor reads the results of the conversion through the I2C interface. The MADC also performs analog signal conversion for the USB subchip.

Keypad:

The keypad controller supports up to 6×6 keypad matrix. The keypad includes an integrated programmable timer for debounce, long key press, and time-out events. It supports programmable interrupt generation on key events, multikey press detection and decoding, and long key detection on prolonged key press.

The keypad can be used in software scanning mode or hardware decoding mode.

LED:

The TPS65930 device provides light-emitting diode (LED) driver circuitry to power two LED (dc power) circuits that can illuminate a panel or provide user indicators. The two circuits (LEDA and LEDB) are identical except for their current capabilities: LEDA is rated for 160 mA and LEDB is rated for 60 mA.

Interface subchip:

The interface subchip is the main interface between the external components and the TPS65930 device. This module includes the primary and secondary interrupt handlers that generate interrupt and provides it to the host processor for further action. There is one interrupt line that can be routed to external host. The device provides the interrupt mapping to track down the interrupt originator. Each subchip has several interrupts that get mapped on to the external interrupt.

The device handles all I2C communication with the external host processors, and internal communication is managed by the OCP (Open Core Protocol) standard. This also includes the GPIOs.

PACKAGING INFORMATION**Package Thermal Resistance Characteristics**

Table 1 lists the thermal resistance characteristics for the recommended package types used on the TPS65930 device.

Table 1. TPS65930 Thermal Resistance Characteristics

PACKAGE	R _{θJA} (C/W)	R _{θJB} (C/W)	R _{θJC} (C/W)	BOARD TYPE
TPS65930	33.42	13.81	6.74 ⁽¹⁾	2S2P ⁽²⁾
TPS65930	57.05	14.51	6.74 ⁽¹⁾	1S0P ⁽²⁾

(1) This measurement is not affected by the board that the device is mounted on.

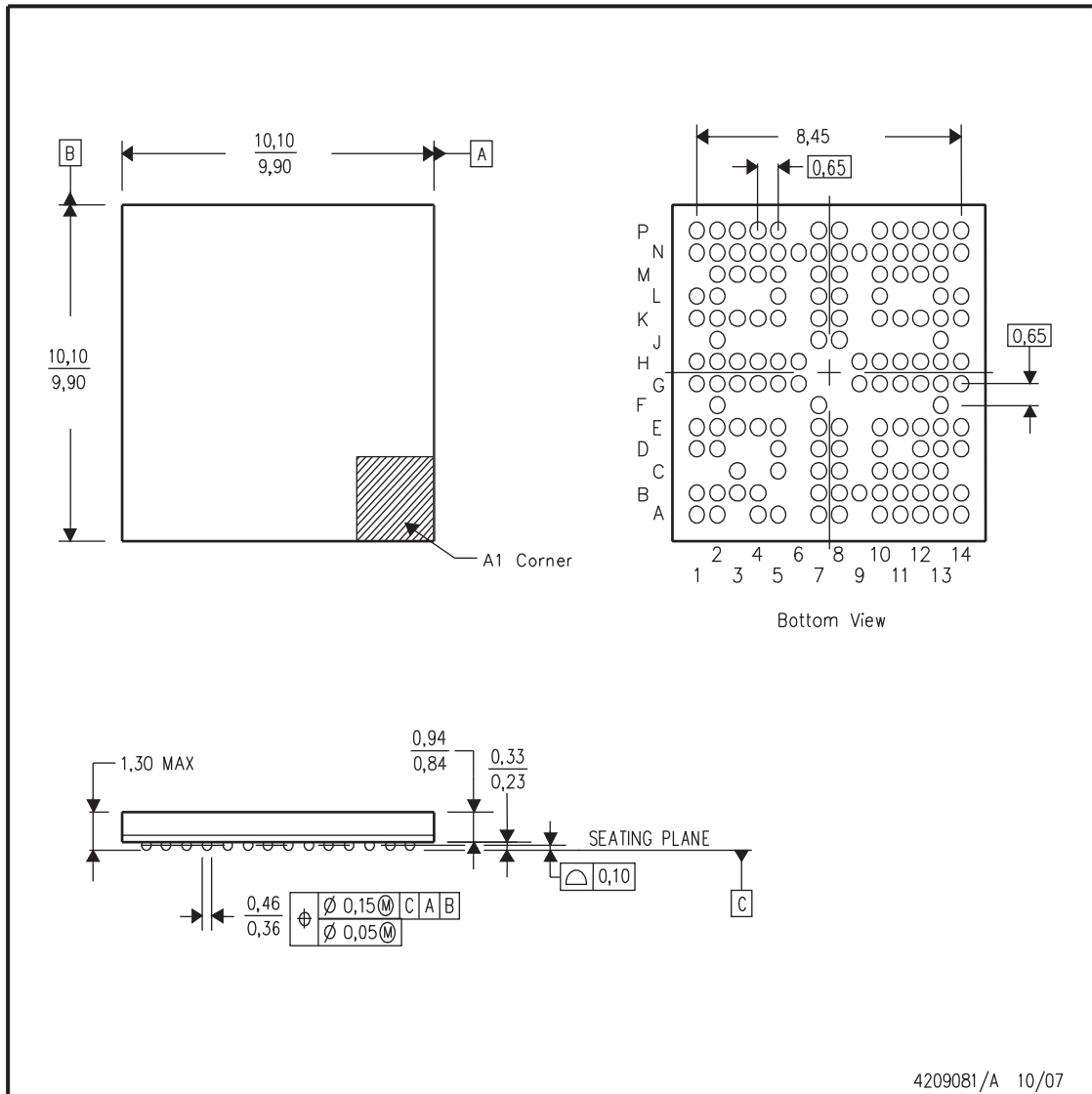
(2) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

Mechanical Data

Figure 2, Figure 3, and Figure 4 show the TPS65930 mechanical package.

ZCH (S-PBGA-N139)

PLASTIC BALL GRID ARRAY



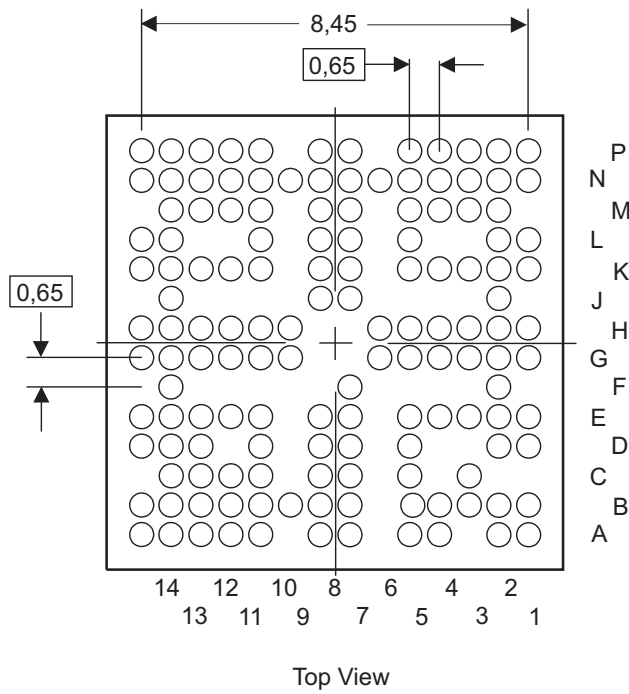
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. nFBGA configuration
 - D. This is a lead-free solder ball design.

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Figure 2. TPS65930 Mechanical Package

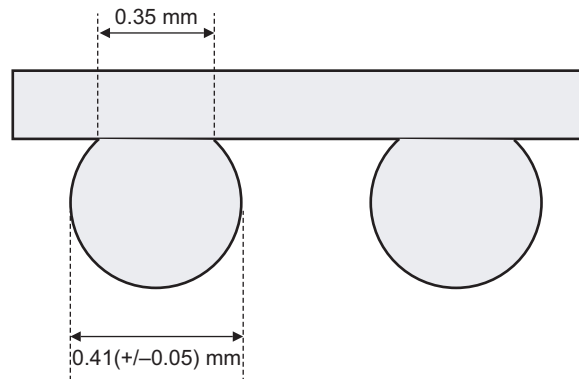
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Figure 3. TPS65930 Mechanical Package — Top View



035-004

Figure 4. TPS65930 Ball Size

GLOSSARY

TERM	MEANING
DTMF	<p>Dual Tone Multi-Frequency</p> <p>Sixteen pairs of audio tones developed when telephones in the United States evolved from rotary to push-button dialing.</p>
GPIO	<p>General Purpose Input/Output</p> <p>Input and output port of a device that has no dedicated purpose and so is available for general applications.</p>
PCM	<p>Pulse Code Modulation</p> <p>The process of representing a signal by a sequence of pulses. Two commonly used forms of PCM are pulse-width modulation (PWM) and pulse-frequency modulation (PFM).</p>
SMPS	<p>Switched Mode Power Supply</p> <p>A power supply in which the output is being turned on and off at a rapid rate and the output voltage is controlled by changing the duty cycle; that is, the percentage of time it is turned on compared to the amount of time it is turned off. The desired dc output is obtained from the SMPS by use of a filtering network that converts the switched output to its averaged value. The output of a SMPS is fully on or off; it is not partially on or off as is true of a linear power supply.</p>
TDM	<p>Time Division Multiplex</p> <p>The technique used to put multiple digital signals onto the same path by assigning each signal its own time slot.</p>

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