

LM193, LM293, LM393, LM2903, LM393B and LM2903B Dual Comparators

1 Features

- Single-Supply or Dual Supplies
- Wide range of supply voltage
 - Maximum rating: 2 V to 36 V
 - Tested to 30 V: non-V devices
 - Tested to 32 V: V-suffix devices
 - Tested to 36 V: B-suffix devices
- Low supply-current drain independent of supply voltage: 0.2 mA (typical) per comparator
- Low input bias current: 15 nA (typical, 'B' device)
- Low current: 2 nA (Typical)
- Low input offset voltage: 0.37 mV (typical, 'B' device)
- Common-mode input voltage range Includes Ground
- Differential input voltage range equal to maximum-rated supply voltage: ± 36 V
- Low output saturation voltage
- Output compatible with TTL, MOS, and CMOS

2 Applications

- [Chemical or gas sensor](#)
- [Desktop PC](#)
- [Motor/trol: AC induction](#)
- [Weigh scale](#)

3 Description

The LM393B and LM2903B devices are the next generation versions of the industry-standard LM393 and LM2903 comparator family. These next generation devices provide outstanding value for cost-sensitive applications, with features including lower offset voltage, higher supply voltage capability, lower supply current, lower input bias current, lower propagation delay, and improved 2kV ESD performance with drop-in replacement convenience.

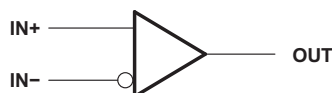
All devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is within 2 V to 36 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM193, LM293, LM293A, LM393, LM393A, LM2903, LM2903V, LM2903AV, LM393B, LM2903B	SOIC (8)	4.90 mm x 3.91 mm
LM293, LM293A, LM393, LM393A, LM2903, LM393B, LM2903B	VSSOP (8)	3.00 mm x 3.00 mm
LM293, LM393, LM393A, LM2903	PDIP (8)	9.81 mm x 6.35 mm
LM393, LM393A, LM2903	SO (8)	6.20 mm x 5.30 mm
LM393, LM393A, LM2903, LM2903V, LM2903AV, LM393B, LM2903B	TSSOP (8)	3.00 mm x 4.40 mm
LM393	WSON (8)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features	1	6.14 Typical Characteristics	12
2 Applications	1	7 Detailed Description	13
3 Description	1	7.1 Overview	13
4 Revision History	2	7.2 Functional Block Diagram	13
5 Pin Configuration and Functions	4	7.3 Feature Description	13
6 Specifications	5	7.4 Device Functional Modes	13
6.1 Absolute Maximum Ratings	5	8 Application and Implementation	14
6.2 ESD Ratings	5	8.1 Application Information	14
6.3 Recommended Operating Conditions	5	8.2 Typical Application	14
6.4 Thermal Information: LM193	6	9 Power Supply Recommendations	17
6.5 Thermal Information: LM293, LM393, LM2903 (all 'V' and 'A' suffixes)	6	10 Layout	17
6.6 Thermal Information: LM393B and LM2903B	6	10.1 Layout Guidelines	17
6.7 Electrical Characteristics LM393B	7	10.2 Layout Example	17
6.8 Electrical Characteristics LM2903B	8	11 Device and Documentation Support	18
6.9 Switching Characteristics LM393B and LM2903B	8	11.1 Related Links	18
6.10 Electrical Characteristics for LM193, LM293, and LM393 (without A suffix)	9	11.2 Receiving Notification of Documentation Updates	18
6.11 Electrical Characteristics for LM293A and LM393A	10	11.3 Community Resources	18
6.12 Electrical Characteristics for LM2903, LM2903V, and LM2903AV	11	11.4 Trademarks	18
6.13 Switching Characteristics (all devices)	11	11.5 Electrostatic Discharge Caution	18
		11.6 Glossary	18
		12 Mechanical, Packaging, and Orderable Information	18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Z (October 2017) to Revision AA

Page

• Added "B" devices with various text changes throughout datasheet.	1
• Deleted from Device Information old LM193 CDIP and LCCC package references and drawings. These are on the LM139-MIL datasheet.	1
• Added LM393 WSON package	1
• Added "B" devices Thermal Information table.	6
• Added "B" device electrical tables	7

Changes from Revision Y (June 2015) to Revision Z

Page

• Changed data sheet title	1
• Added LM2903 part numbers	1
• Added LM2903 part numbers	1
• Changed VCC and ground pin function from: input to: –	4
• Changed 25C to -25C due to typo in LM293 Temperature Tablenote	9
• Remove text "four comparators" from I, CC,	10
• Changed 25C to -25C due to typo in LM293 Temperature Tablenote	10
• Changed input error in <i>Feature Description</i> text	13
• Changed Design Paramter maximum current from: 20 mA to: 4 mA	14
• Changed and revised text in <i>Response Time</i> section	15
• Added <i>Receiving Notification of Documentation Updates</i> section	18

Changes from Revision X (January 2014) to Revision Y Page

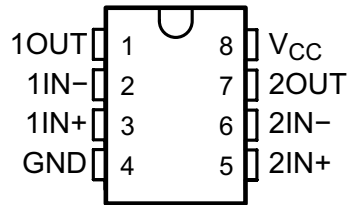
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Changes from Revision W (July 2010) to Revision X Page

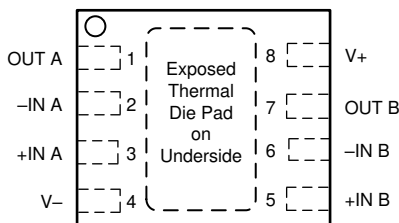
- Updated document to new TI data sheet format - no specification changes. 1
- Removed *Ordering Information* table 4
- Added ESD warning. 18

5 Pin Configuration and Functions

D, DGK, JG, P, PS, or PW Package
8-Pin SOIC, VSSOP, PDIP, SO, or TSSOP
 Top View



DSG Package
8-Pin WSON With Exposed Pad
 Top View



Connect thermal pad to V-

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, VSSOP, PDIP, SO, DDF and TSSOP	DSG		
1OUT	1	1	Output	Output pin of comparator 1
1IN-	2	2	Input	Negative input pin of comparator 1
1IN+	3	3	Input	Positive input pin of comparator 1
GND	4	4	—	Ground
2IN+	5	5	Input	Positive input pin of comparator 2
2IN-	6	6	Input	Negative input pin of comparator 2
2OUT	7	7	Output	Output pin of comparator 2
V _{CC}	8	8	—	Positive Supply
Thermal Pad	—	PAD	—	Connect to V-

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	-0.3	36	V
	Non-B Versions		38	
V _{ID}	Differential input voltage ⁽³⁾	-38	36	V
	B Versions Only		38	
V _I	Input voltage (either input)	-0.3	36	V
	B Versions Only		38	
I _{IK}	Input current ⁽⁴⁾		-50	mA
V _O	Output voltage	-0.3	36	V
	B Versions Only		38	
I _O	Output current		20	mA
I _{SC}	Duration of output short circuit to ground ⁽⁵⁾		Unlimited	
T _J	Operating virtual-junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Production Processing Does Not Necessarily Include Testing of All Parameters.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Input current flows through parasitic diode to ground and turns on parasitic transistors that increases I_{CC} and may cause output to be incorrect. Normal operation resumes when input current is removed.
- (5) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
LM393B and LM2903B Only				
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
All Other Versions				
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V _S = (V+) – (V-)	non-V devices	2	30	V
	V devices	2	32	
	"B" version devices	3	36	
Input voltage range, V _{IVR}		0	(V+) - 2.0V	V
Ambient temperature, T _A	LM193	-55	125	°C
	LM2903, LM2903V, LM2903AV, LM2903B	-40	125	
	LM393B	-40	85	
	LM293, LM293A	-25	85	
	LM393, LM393A	0	70	

6.4 Thermal Information: LM193

THERMAL METRIC ⁽¹⁾		LM193	
		D (SOIC)	UNIT
		8 pin	
R _{θJA}	Junction-to-ambient thermal resistance	126.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	70	°C/W
R _{θJB}	Junction-to-board thermal resistance	64.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	20.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	64.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: LM293, LM393, LM2903 (all 'V' and 'A' suffixes)

THERMAL METRIC ⁽¹⁾		LM293, LM393, LM2903					UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	
		8 pin	8 pin	8 pin	8 pin	8 pin	
R _{θJA}	Junction-to-ambient thermal resistance	131.8	199.4	73.7	139	194.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.4	90.2	62.6	98.9	77.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	72.2	120.8	50.8	83.7	123.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	26.5	21.5	39.2	47.4	13.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	71.1	119.1	50.7	83	121.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: LM393B and LM2903B

THERMAL METRIC ⁽¹⁾		LM393B, LM2903B			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 pin	8 pin	8 pin	
R _{θJA}	Junction-to-ambient thermal resistance	148.5	193.7	200.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.2	82.9	89.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	91.8	115.5	131.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	38.5	20.8	22.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	91.1	113.9	129.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics LM393B

 $V_S = 5\text{ V}$, $V_{CM} = (V-)$; $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_S = 5\text{ to }36\text{V}$	-2.5	± 0.37	2.5	mV
		$V_S = 5\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$	-3.5		3.5	
I_B	Input bias current			-15	-25	nA
		$T_A = -40^\circ\text{C to }+85^\circ\text{C}$			-100	nA
I_{OS}	Input offset current		-10	± 2	10	nA
		$T_A = -40^\circ\text{C to }+85^\circ\text{C}$	-50		50	nA
V_{CM}	Input voltage range	$V_S = 3\text{ to }36\text{V}$	(V-)		(V+) - 1.5	V
		$V_S = 3\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$	(V-)		(V+) - 2.0	V
A_{VD}	Large signal differential voltage amplification	$V_S = 15\text{V}$, $V_O = 1.4\text{V to }11.4\text{V}$; $R_L \geq 15\text{k to } (V+)$	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V-)} }	$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$		110	400	mV
		$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$ $T_A = -40^\circ\text{C to }+85^\circ\text{C}$			700	mV
I_{OH-LKG}	High-level output leakage current	High-level output leakage current $(V+) = V_O = 5\text{ V}$; $V_{ID} = 1\text{ V}$		0.1	25	nA
I_{OL}	Low level output current	$V_{OL} = 1.5\text{V}$; $V_{ID} = -1\text{V}$; $V_S = 5\text{V}$	6	18		mA
I_Q	Quiescent current (all comparators)	$V_S = 5\text{ V}$, no load		400	1000	μA
		$V_S = 36\text{ V}$, no load, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$		550	1200	μA

6.8 Electrical Characteristics LM2903B

 $V_S = 5\text{ V}$, $V_{CM} = (V_-)$; $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_S = 5$ to 36V	-2.5	± 0.37	2.5	mV
		$V_S = 5$ to 36V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-4		4	
I_B	Input bias current			-15	-25	nA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			-100	nA
I_{OS}	Input offset current		-10	± 2	10	nA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-50		50	nA
V_{CM}	Input voltage range	$V_S = 3$ to 36V	(V_-)		(V_+) - 1.5	V
		$V_S = 3$ to 36V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	(V_-)		(V_+) - 2.0	V
A_{VD}	Large signal differential voltage amplification	$V_S = 15\text{V}$, $V_O = 1.4\text{V}$ to 11.4V ; $R_L \geq 15\text{k}$ to (V_+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V_-)}	$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$		110	400	mV
		$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$ $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			700	mV
I_{OH-LKG}	High-level output leakage current	High-level output leakage current (V_+) = $V_O = 5\text{V}$; $V_{ID} = 1\text{V}$		0.1	25	nA
I_{OL}	Low level output current	$V_{OL} = 1.5\text{V}$; $V_{ID} = -1\text{V}$; $V_S = 5\text{V}$	6	18		mA
I_Q	Quiescent current (all comparators)	$V_S = 5\text{V}$, no load		400	1000	μA
		$V_S = 36\text{V}$, no load, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		550	1200	μA

6.9 Switching Characteristics LM393B and LM2903B

 $V_S = 5\text{V}$, $V_{O_PULLUP} = 5\text{V}$, $V_{CM} = V_S/2$, $C_L = 15\text{pF}$, $R_L = 5.1\text{k Ohm}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{response}	Propagation delay time, high-to-low; TTL input signal ⁽¹⁾	TTL input with $V_{\text{ref}} = 1.4\text{V}$		300		ns
t_{response}	Propagation delay time, high-to-low; Small scale input signal ⁽¹⁾	Input overdrive = 5mV , Input step = 100mV		1000		ns

(1) High-to-low and low-to-high refers to the transition at the input.

6.10 Electrical Characteristics for LM193, LM293, and LM393 (without A suffix)

 at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	LM193			LM293 LM393			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to }30\text{ V}$, $V_{IC} = V_{ICR\text{ min}}$, $V_O = 1.4\text{ V}$	25°C		2	5		2	5	mV	
		Full range				9		9		
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		3	25		5	50	nA	
		Full range			100		250			
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		-25	-100		-25	-250	nA	
		Full range			-300		-400			
V_{ICR} Common-mode input-voltage range ⁽²⁾		25°C		0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$		V	
		Full range		0 to $V_{CC} - 2$			0 to $V_{CC} - 2$			
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to }11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega\text{ to }V_{CC}$	25°C		50	200		50	200	V/mV	
I_{OH} High-level output current	$V_{OH} = 5\text{ V}$	$V_{ID} = 1\text{ V}$	25°C		0.1		0.1	50	nA	
	$V_{OH} = 30\text{ V}$	$V_{ID} = 1\text{ V}$	Full range			1		1	μA	
V_{OL} Low-level output voltage	$I_{OL} = 4\text{ mA}$, $V_{ID} = -1\text{ V}$	25°C		150	400		130	400	mV	
		Full range			700		700			
I_{OL} Low-level output current	$V_{OL} = 1.5\text{ V}$, $V_{ID} = -1\text{ V}$	25°C		6			6		mA	
I_{CC} Supply current	$R_L = \infty$	$V_{CC} = 5\text{ V}$	25°C		0.8	1		0.45	1	mA
		$V_{CC} = 30\text{ V}$	Full range			2.5		0.55	2.5	

- (1) Full range (minimum or maximum) for LM193 is -55°C to 125°C , for LM293 is -25°C to 85°C , and for LM393 is 0°C to 70°C . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2\text{V}$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

6.11 Electrical Characteristics for LM293A and LM393A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	LM293A LM393A			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to }30\text{ V}, V_O = 1.4\text{ V}$ $V_{IC} = V_{ICR(min)}$	25°C		1	2	mV
		Full range			4	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50	nA
		Full range			150	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		-25	-250	nA
		Full range			-400	
V_{ICR} Common-mode input-voltage range ⁽²⁾		25°C	0 to $V_{CC} - 1.5$			V
		Full range	0 to $V_{CC} - 2$			
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}, V_O = 1.4\text{ V to }11.4\text{ V},$ $R_L \geq 15\text{ k}\Omega\text{ to }V_{CC}$	25°C	50	200		V/mV
I_{OH} High-level output current	$V_{OH} = 5\text{ V}, V_{ID} = 1\text{ V}$	25°C		0.1	50	nA
	$V_{OH} = 30\text{ V}, V_{ID} = 1\text{ V}$	Full range			1	μA
V_{OL} Low-level output voltage	$I_{OL} = 4\text{ mA}, V_{ID} = -1\text{ V}$	25°C		110	400	mV
		Full range			700	
I_{OL} Low-level output current	$V_{OL} = 1.5\text{ V}, V_{ID} = -1\text{ V},$	25°C	6			mA
I_{CC} Supply current	$R_L = \infty$	$V_{CC} = 5\text{ V}$	25°C	0.60	1	mA
		$V_{CC} = 30\text{ V}$	Full range	0.72	2.5	

- (1) Full range (minimum or maximum) for LM293A is -25°C to 85°C , and for LM393A is 0°C to 70°C . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2\text{V}$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

6.12 Electrical Characteristics for LM2903, LM2903V, and LM2903AV

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	LM2903, LM2903V			LM2903AV			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to MAX}^{(2)}$, $V_O = 1.4\text{ V}$, $V_{IC} = V_{ICR(min)}$	25°C		2	7		1	2	mV
		Full range			15			4	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50		5	50	nA
		Full range			200			200	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		-25	-250		-25	-250	nA
		Full range			-500			-500	
V_{ICR} Common-mode input-voltage range ⁽³⁾		25°C	0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$			V
		Full range	0 to $V_{CC} - 2$			0 to $V_{CC} - 2$			
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to } 11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega\text{ to } V_{CC}$	25°C	25	100		25	100	V/mV	
I_{OH} High-level output current	$V_{OH} = 5\text{ V}$, $V_{ID} = 1\text{ V}$	25°C		0.1	50		0.1	50	nA
	$V_{OH} = V_{CC}\text{ MAX}^{(2)}$, $V_{ID} = 1\text{ V}$	Full range			1			1	μA
V_{OL} Low-level output voltage	$I_{OL} = 4\text{ mA}$, $V_{ID} = -1\text{ V}$	25°C		150	400		150	400	mV
		Full range			700			700	
I_{OL} Low-level output current	$V_{OL} = 1.5\text{ V}$, $V_{ID} = -1\text{ V}$	25°C	6			6		mA	
I_{CC} Supply current	$R_L = \infty$	$V_{CC} = 5\text{ V}$		0.8	1		0.8	1	mA
		Full range			2.5			2.5	

- (1) Full range (minimum or maximum) for LM2903 is -40°C to 125°C . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) $V_{CC}\text{ MAX} = 30\text{ V}$ for non-V devices and 32 V for V-suffix devices.
- (3) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2\text{V}$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

6.13 Switching Characteristics (all devices)

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	R_L connected to 5 V through $5.1\text{ k}\Omega$, $C_L = 15\text{ pF}^{(1)(2)}$	100-mV input step with 5-mV overdrive	1.3
		TTL-level input step	0.3

- (1) C_L includes probe and jig capacitance.
- (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V .

6.14 Typical Characteristics

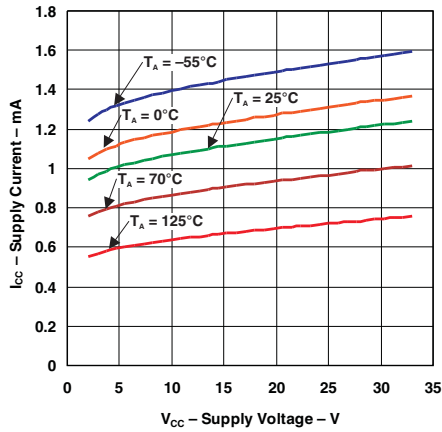


Figure 1. Supply Current vs Supply Voltage

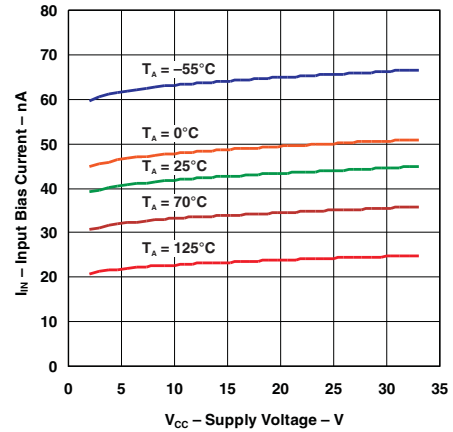


Figure 2. Input Bias Current vs Supply Voltage

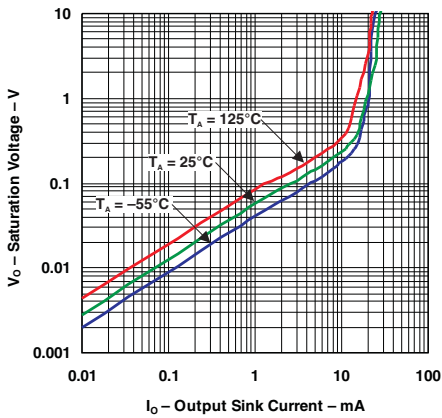


Figure 3. Output Saturation Voltage

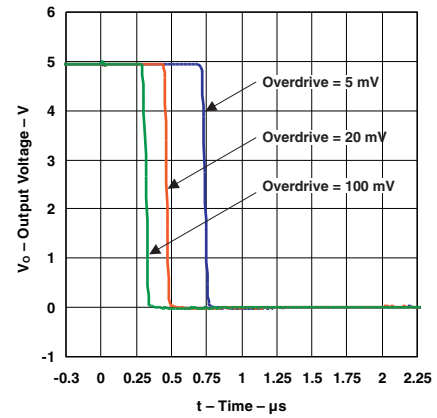


Figure 4. Response Time for Various Overdrives Negative Transition

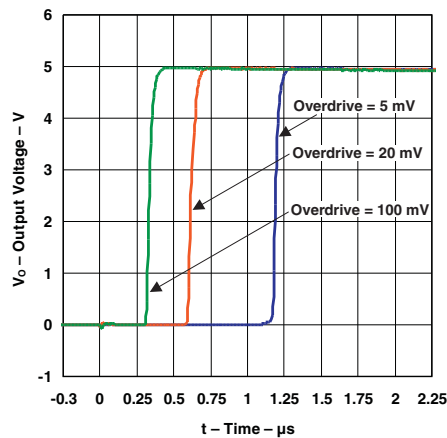


Figure 5. Response Time for Various Overdrives Positive Transition

7 Detailed Description

7.1 Overview

These dual comparators have the ability to operate up to absolute maximum of 36 V on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V to 36 V), low I_q and fast response of the devices.

The open-drain output allows the user to configure the output's logic high voltage (V_{OH}) and can be used to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram

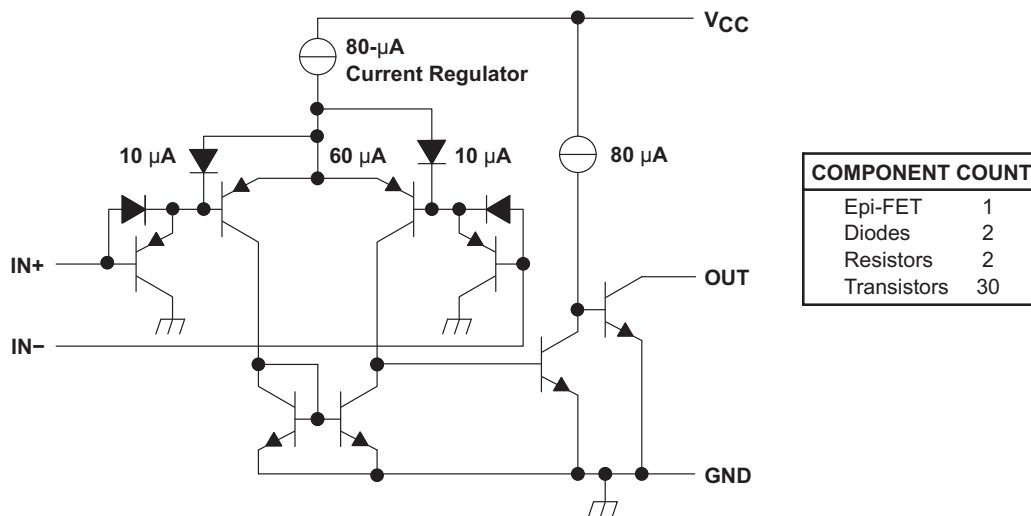


Figure 6. Schematic (Each Comparator)

7.3 Feature Description

The comparator consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to $V_{CC} - 1.5$ V input. Allow for $V_{CC} - 2$ V at cold temperature.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. See [Figure 3](#) for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The device operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is typically used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes this comparator optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

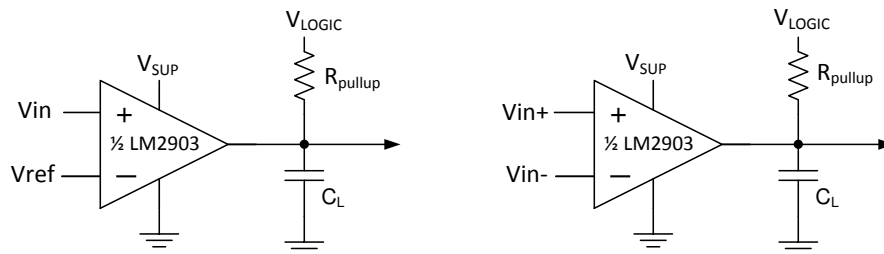


Figure 7. Single-Ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to $V_{sup}-2$ V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 μ A to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using the device in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0 V to $V_{CC}-2.0$ V. This limits the input voltage range to as high as $V_{CC}-2.0$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common-mode range:
 - a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 8](#) and [Figure 9](#) show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use [Typical Characteristics](#) to determine V_{OL} based on the output current.

The output current can also effect the transient response. See [Response Time](#) for more information.

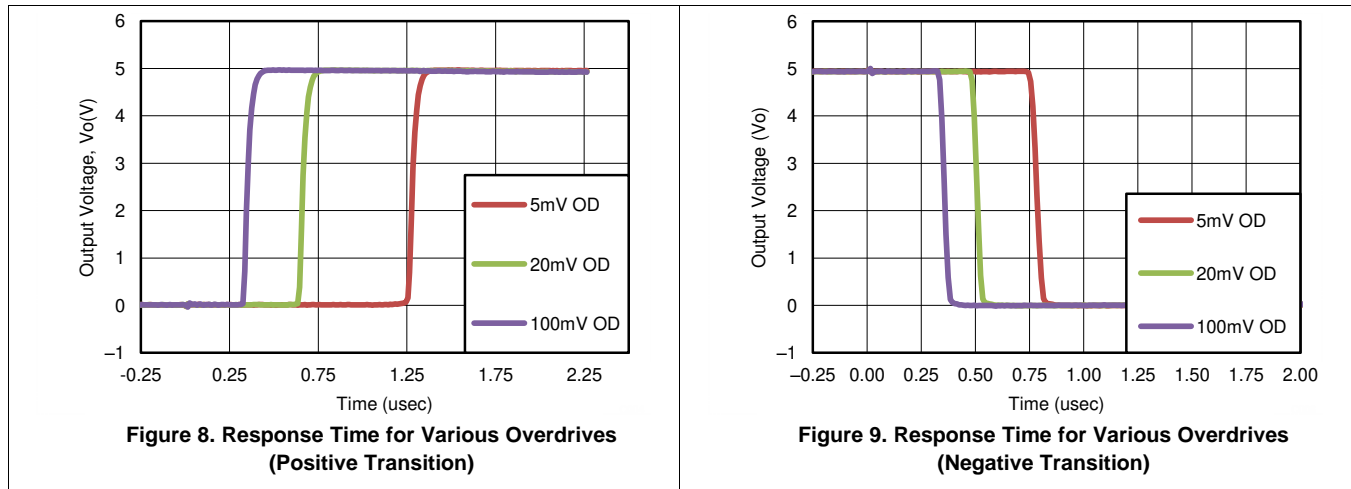
8.2.2.4 Response Time

Response time is a function of input over drive. See [Application Curves](#) for typical response times. The rise and falls times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
 - R_{CE} can be determine by taking the slope of [Typical Characteristics](#) in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic} , $R_{PULLUP} = 5.1\text{ k}\Omega$, and 50 pF scope probe.



9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the input common-mode range of the comparator and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

10.2 Layout Example

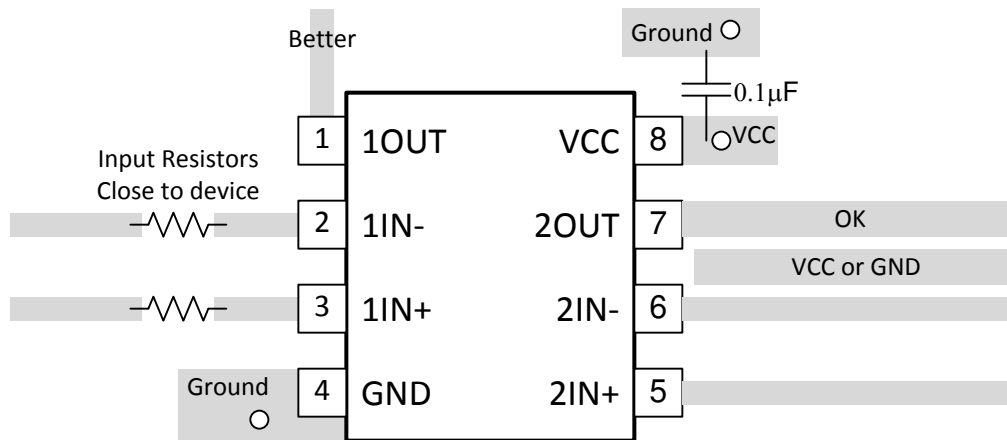


Figure 10. LM2903 Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM193	Click here	Click here	Click here	Click here	Click here
LM293	Click here	Click here	Click here	Click here	Click here
LM293A	Click here	Click here	Click here	Click here	Click here
LM393	Click here	Click here	Click here	Click here	Click here
LM393A	Click here	Click here	Click here	Click here	Click here
LM2903	Click here	Click here	Click here	Click here	Click here
LM2903V	Click here	Click here	Click here	Click here	Click here
LM393B	Click here	Click here	Click here	Click here	Click here
LM2903B	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM193DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM193DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM2903AVQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903BIDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L2903B	
LM2903D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MAP, MAS, MAU)	Samples
LM2903DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MAP, MAS, MAU)	Samples
LM2903DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	LM2903P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903VQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM293AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MDP, MDS, MDU)	Samples
LM293ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MDP, MDS, MDU)	Samples
LM293ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM293D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MCP, MCS, MCU)	Samples
LM293DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MCP, MCS, MCU)	Samples
LM293DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM293PE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM393AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M8P, M8S, M8U)	Samples
LM393ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M8P, M8S, M8U)	Samples
LM393ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	N / A for Pkg Type	0 to 70	LM393AP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393APE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM393AP	Samples
LM393APSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393BIDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LM393B	
LM393D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M9P, M9S, M9U)	Samples
LM393DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M9P, M9S, M9U)	Samples
LM393DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE3	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM393P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
PLM2903BIDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
PLM393BIDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

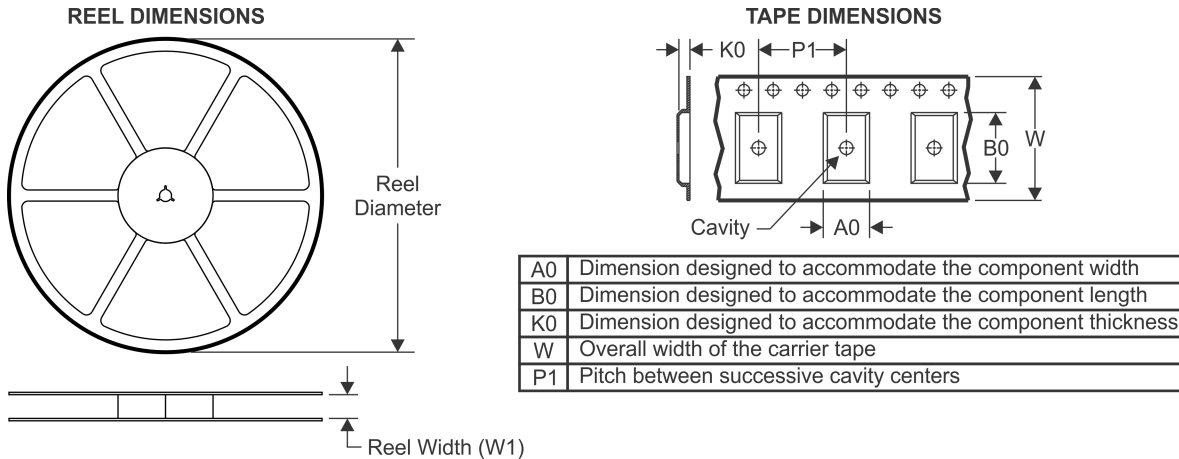
OTHER QUALIFIED VERSIONS OF LM2903, LM293 :

- Automotive: [LM2903-Q1](#)
- Enhanced Product: [LM293-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



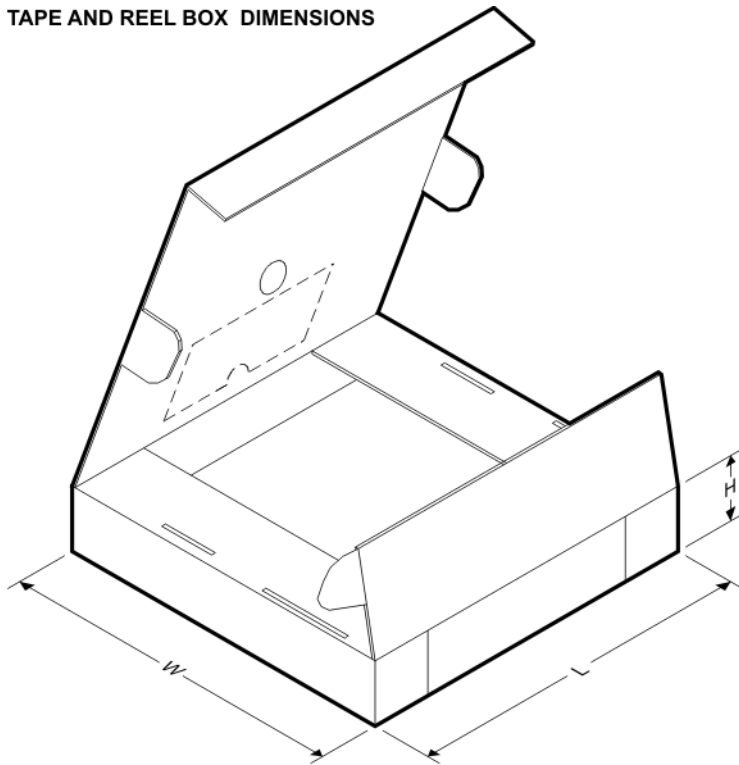
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM193DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM193DR	SOIC	D	8	2500	350.0	350.0	43.0
LM2903AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903AVQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2903DR	SOIC	D	8	2500	367.0	367.0	35.0
LM2903DR	SOIC	D	8	2500	333.2	345.9	28.6
LM2903DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2903DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM2903DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903QDRG4	SOIC	D	8	2500	350.0	350.0	43.0
LM2903VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903VQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM293ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM293ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM293ADR	SOIC	D	8	2500	333.2	345.9	28.6
LM293ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM293DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM293DR	SOIC	D	8	2500	364.0	364.0	27.0
LM293DR	SOIC	D	8	2500	367.0	367.0	35.0
LM293DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM293DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM393ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM393ADR	SOIC	D	8	2500	333.2	345.9	28.6
LM393ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM393ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM393APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393APWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM393APWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM393DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393DR	SOIC	D	8	2500	340.5	338.1	20.6
LM393DR	SOIC	D	8	2500	367.0	367.0	35.0
LM393DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM393DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM393DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM393PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM393PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

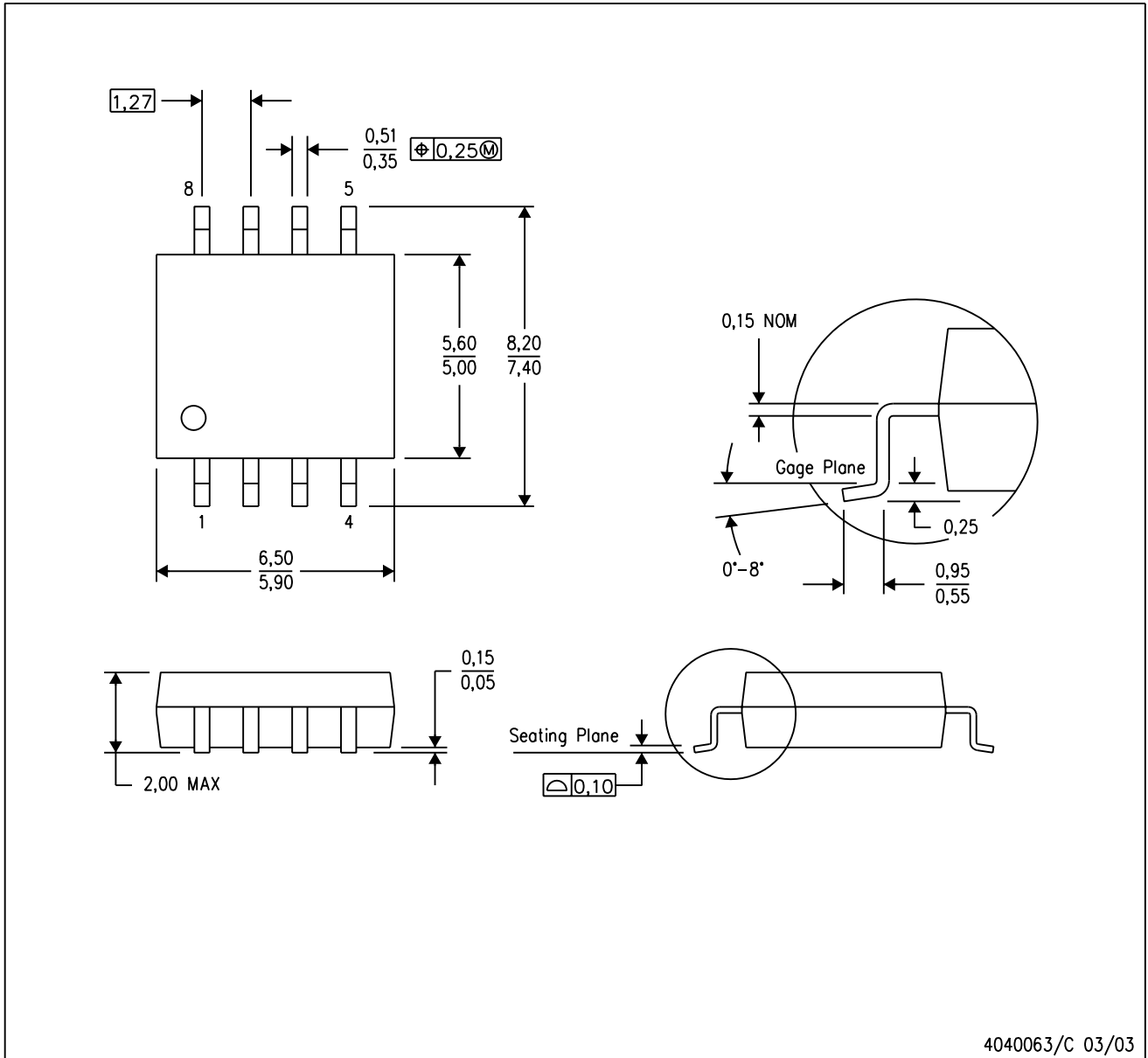
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

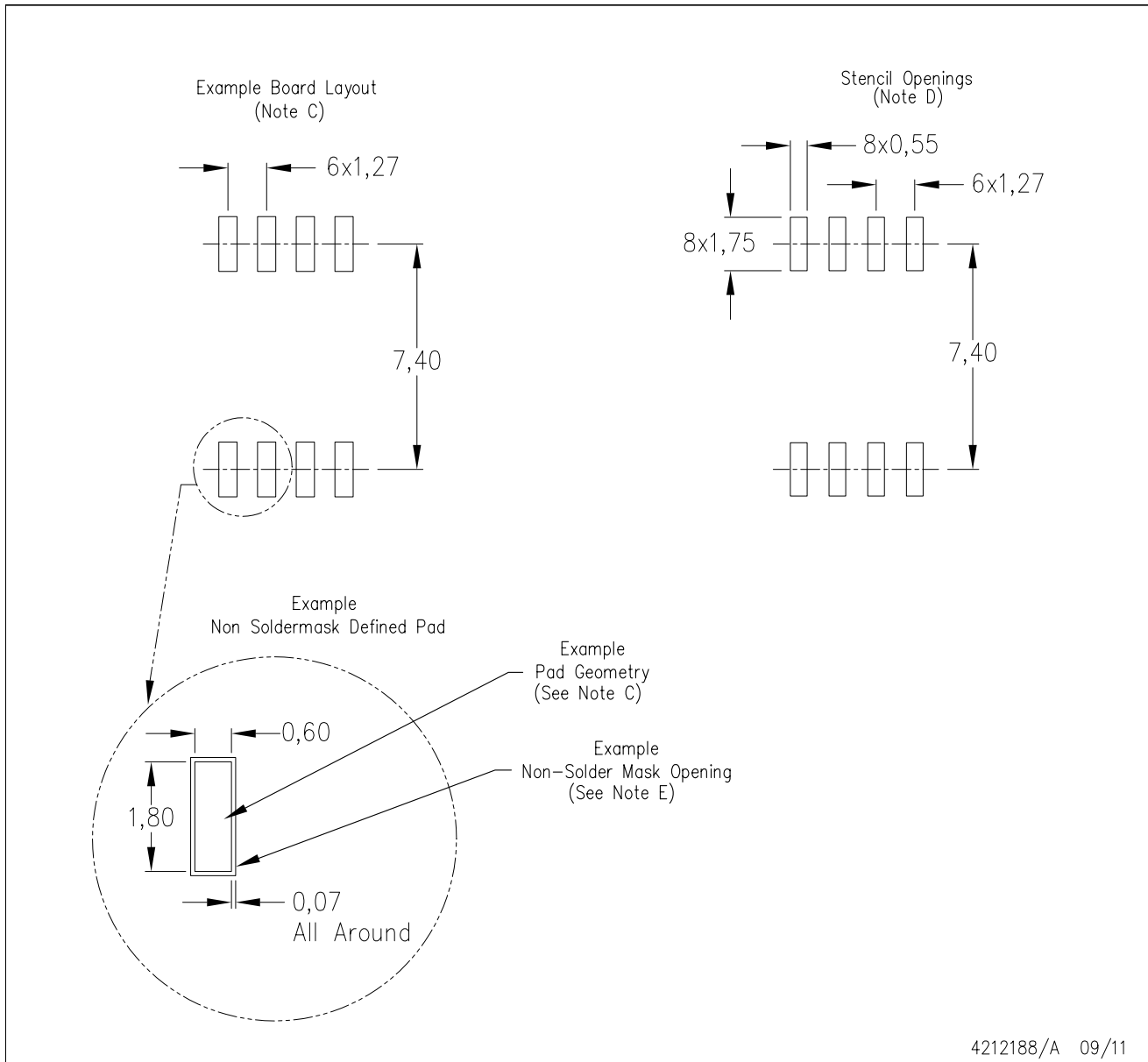
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE

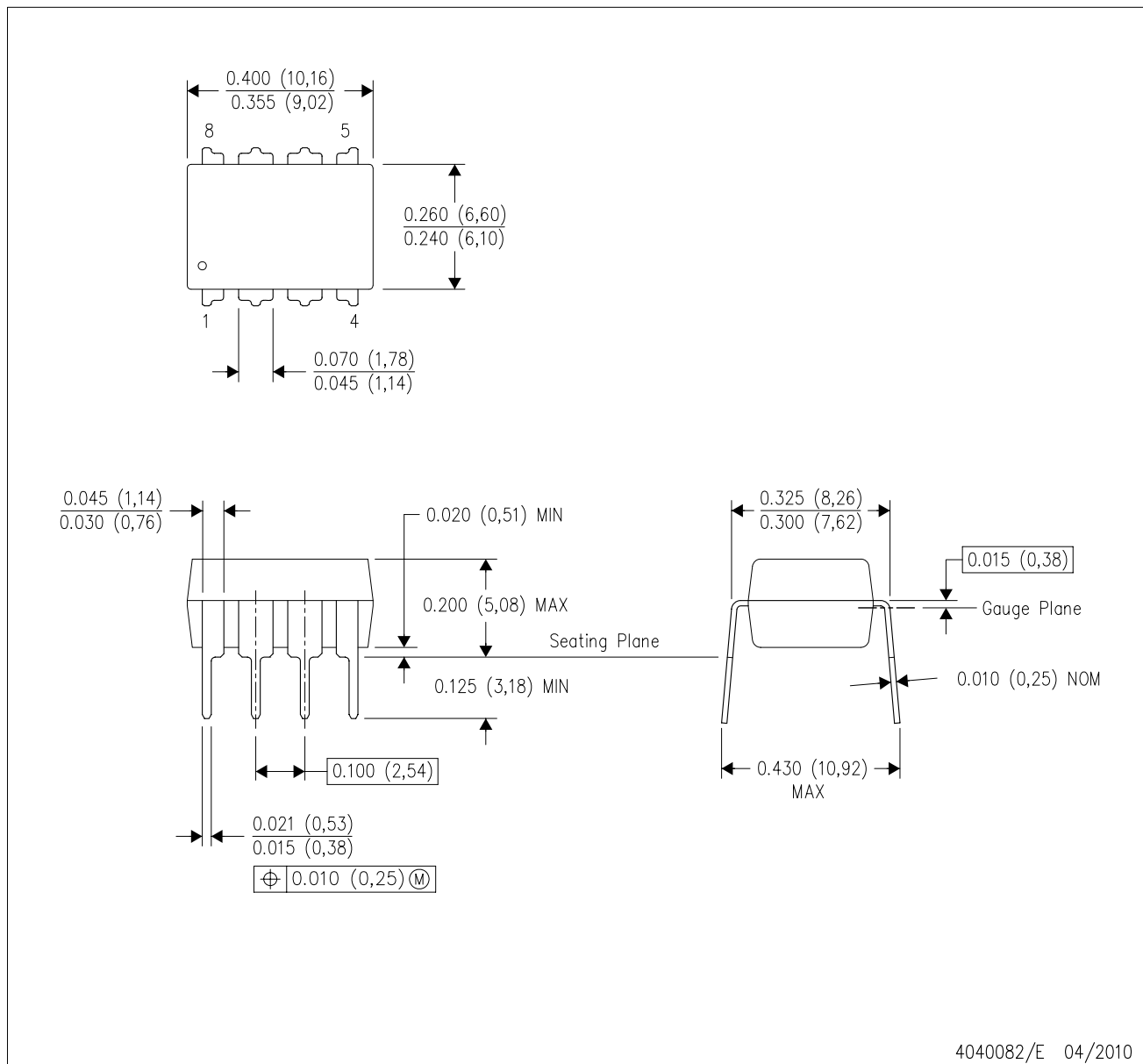


4212188/A 09/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

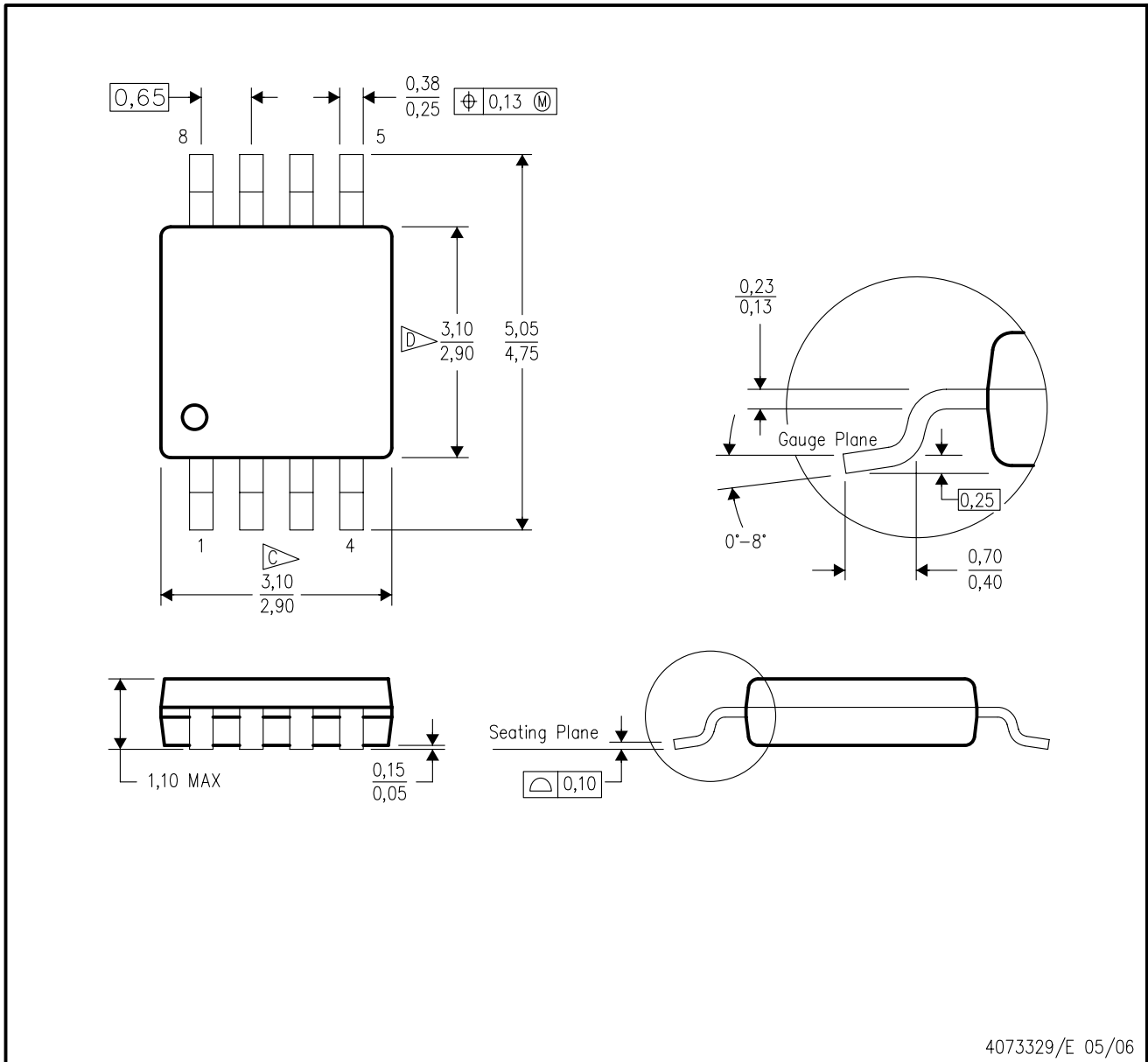
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

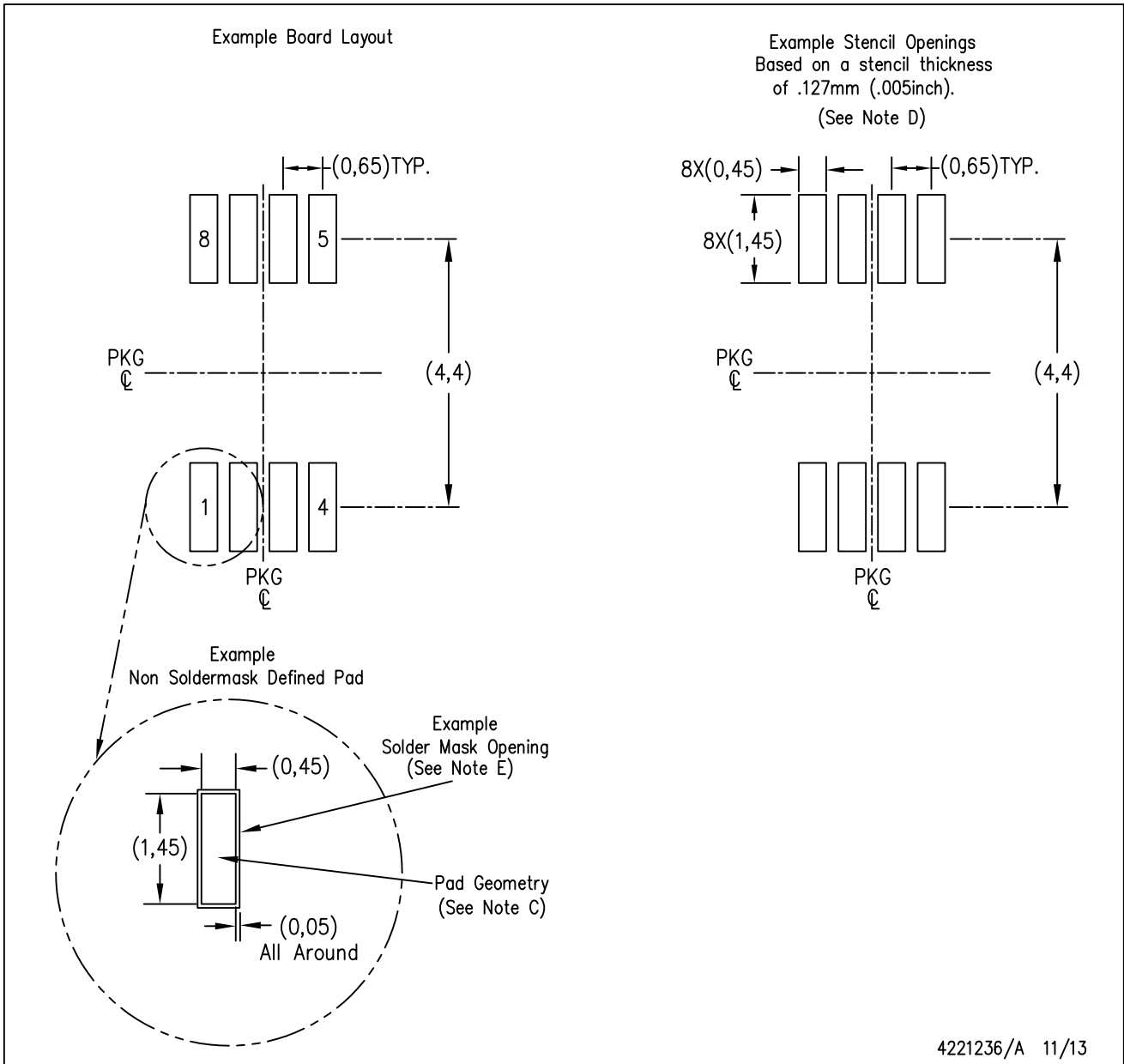
DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

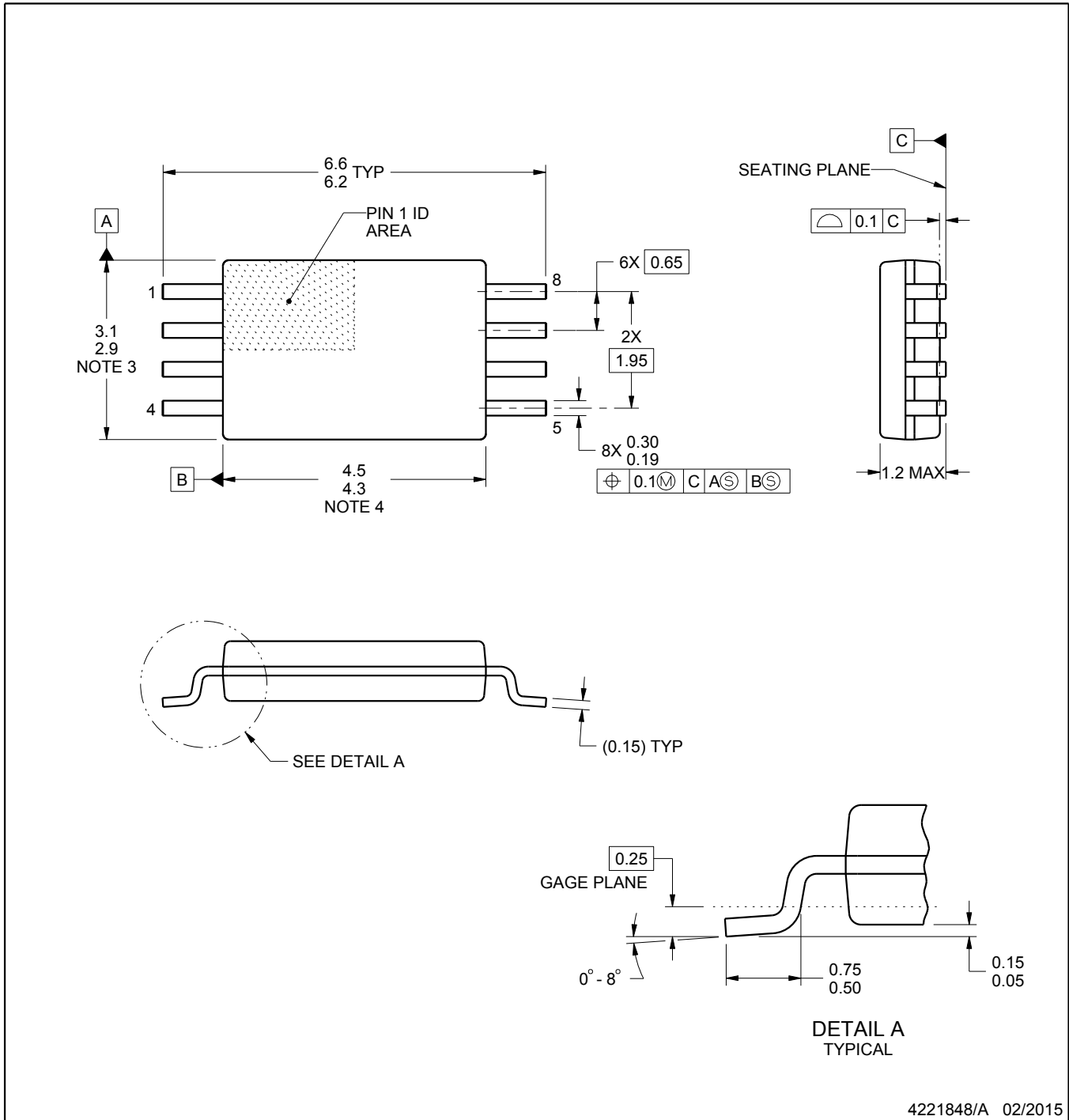
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

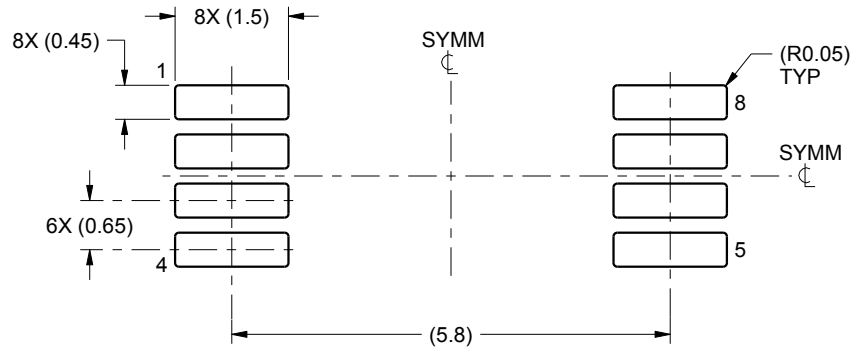
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

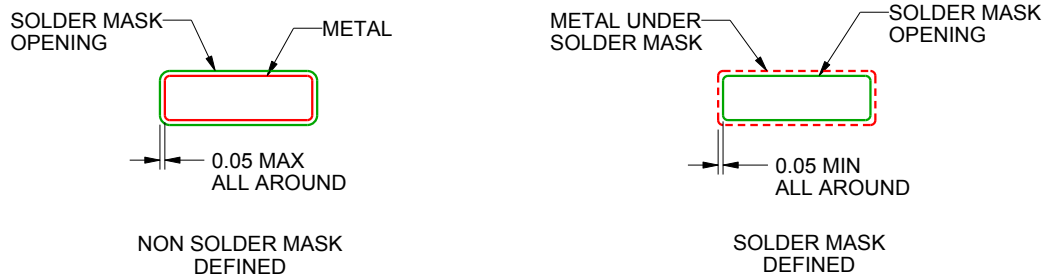
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

单击下面可查看定价，库存，交付和生命周期等信息

[>>TI\(德州仪器\)](#)