P82B715 I²C Bus Extender

1 Features

- Operating Power-Supply Voltage Range of 3 V to 12 V
- Supports Bidirectional Data Transfer of I²C Bus Signals
- Allows Bus Capacitance of 400 pF on Main I²C Bus (Sx/Sy Side) and 3000 pF on Transmission Side (Lx/Ly Side)
- Dual Bidirectional Unity-Voltage-Gain Buffer With No External Directional Control Required
- Drives 10× Lower-Impedance Bus Wiring for Improved Noise Immunity
- Multi-Drop Distribution of I²C Signals Using Low-Cost Twisted-Pair Cables
- I²C Bus Operation Over 50 Meters of Twisted-Pair Wire
- Latch-up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2500-V Human-Body Model (A114-A)
  - 400-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- HDMI DDC
- Long I²C Communications
- Industrial Communications

3 Description

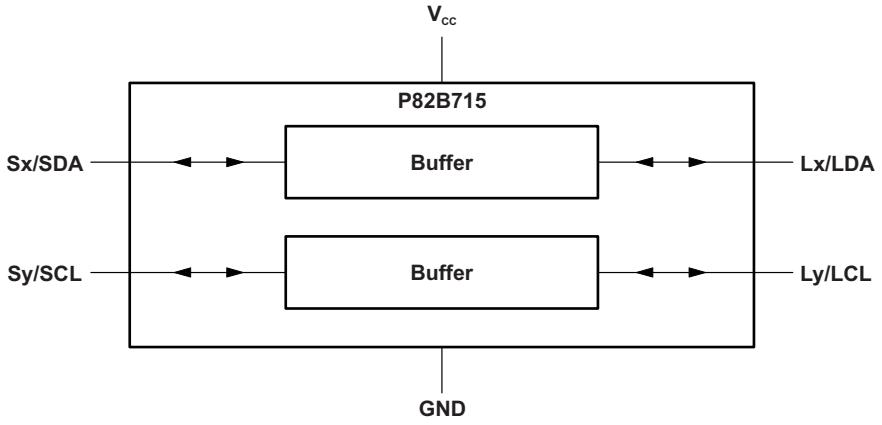
The P82B715 is a device for buffering highly-capacitive I²C bus systems, and it supports bidirectional data transfer through the I²C bus. The P82B715 buffers both the serial data (SDA) and serial clock (SCL) signals on the I²C bus and allows for extension of the I²C bus, while retaining all the operating modes and features of the I²C system.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
P82B715	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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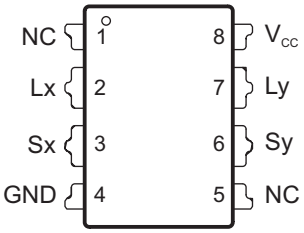
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2008) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

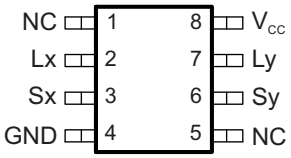
5 Pin Configuration and Functions

P Package
8-Pin PDIP
Top View



NC – No internal connection

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	No connection
2	Lx	I/O	Buffered serial data bus or LDA
3	Sx	I/O	Serial data bus or SDA. Connect to V_{CC} of I^2C master through a pullup resistor.
4	GND	—	Ground
5	NC	—	No connection
6	Sy	I/O	Serial clock bus or SCL. Connect to V_{CC} of I^2C master through a pullup resistor.
7	Ly	I/O	Buffered serial clock bus or LCL
8	V_{CC}	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	12	V
V_b	I^2C bus voltage	Sx or Sy	0	V_{CC}	V
	Buffered bus voltage	Lx or Ly	0	V_{CC}	
I_O	Continuous output current	Sx or Sy		60	mA
		Lx or Ly		60	
I_{CC}	Continuous current through V_{CC} or GND			60	mA
T_{stg}	Storage temperature		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
	Machine model (MM)	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage(1)	4.5	12	V
T_A	Operating free-air temperature	–40	85	°C

(1) Operation with reduced performance is possible down to 3 V. Typical static sinking performance is not degraded at 3 V, but the dynamic sink currents while the output is being driven through $V_{CC}/2$ are reduced and can increase fall times. Timing-critical designs should accommodate the specified minimums.

6.4 Thermal Information

THERMAL METRIC(1)		P82B715		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.3	48.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.2	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.6	26	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 5 V, T_A = 25°C, voltages are specified with respect to GND (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Quiescent supply current	Sx = Sy = V_{CC}			14		mA
		V_{CC} = 12 V			15		
		Both I^2C inputs low, Both buffered outputs sinking 30 mA			22		
I_{IOS}	Output sink current on I^2C bus	Sx, Sy	V_{CC} > 3 V, V_{Sx}, V_{Sy} (low) = 0.4 V, V_{Lx}, V_{Ly} (low) on buffered bus = 0.3 V, I_{Lx}, I_{Ly} = –3 mA (1)	2.6			mA
I_{IOL}	Output sink current on buffered bus	Lx, Ly	V_{Lx}, V_{Ly} (low) = 0.4 V, V_{Sx}, V_{Sy} (low) on I^2C bus = 0.3 V	30			mA
			3 V < V_{CC} < 4.5 V, V_{Lx}, V_{Ly} (low) = 0.4 V to 1.5 V, I_{Sx}, I_{Sy} sinking on I^2C bus < –4 mA	24			
			3 V < V_{CC} < 4.5 V, V_{Lx}, V_{Ly} (low) = 1.5 V to V_{CC}, I_{Sx}, I_{Sy} sinking on I^2C bus = –7 mA	24			
I_I	Input current from I^2C bus	Sx, Sy	I_{Lx}, I_{Ly} sink on buffered bus = 30 mA			–3.2	mA
	Input current from buffered bus (1)	Lx, Ly	V_{CC} > 3 V, I_{Sx}, I_{Sy} sink on I^2C bus = 3 mA (1)			–3	
	Leakage current on buffered bus		V_{CC} = 3 V to 12 V, V_{Lx}, V_{Ly} = V_{CC}, V_{Sx}, V_{Sy} = V_{CC}			200	µA
Z_{in}/Z_{out}	Input/output impedance	V_{Sx} < V_{Lx}, Buffer is active		8	10	13	

(1) Buffer is passive in this test. The Sx/Sy sink current flows through an internal resistor to the driver connected at the Lx/Ly I/O.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C, no capacitive loads, voltages are specified with respect to GND (unless otherwise specified)

PARAMETER		TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
BUFFER DELAY TIMES								
$t_{rise/fall}$	Delay time to V_{Lx} voltage crossing $V_{CC}/2$ for input drive current step I_{Sx} at Sx (1) (see Figure 2)	R_{Lx} pullup = 270 Ω	I_{Sx} I_{Sy}	V_{Lx} V_{Ly}		250		ns
	Buffer delay time, switching edges between V_{Lx} input and V_{Sx} output (2)	R_{Lx} pullup = 4700 Ω	V_{Lx} V_{Ly}	V_{Sx} V_{Sy}		0		ns

(1) A conventional input-output delay is not observed in the Sx/Lx voltage waveforms, because the input and output pins are internally tied with a 30-Ω resistor so they show equal logic voltage levels to within 100 mV. When connected in an I^2C system, an Sx/Sy input pin cannot rise/fall until the buffered bus load at the output pin has been driven by the internal amplifier. This test measures the bus propagation delay caused to falling or rising voltages at the Lx/Ly output (as well as the Sx/Sy input) by the amplifier's response time. The figure given is measured with a drive current as shown in Figure 2. Because this is a dynamic bus test in which a corresponding bus driving IC has an output voltage well above 0.4 V, 6 mA is used instead of the static 3 mA.

(2) The signal path Lx to Sx and Ly to Sy is passive through the internal 30-Ω resistor. There is no amplifier involved and essentially no signal propagation delay.

6.7 Typical Characteristics

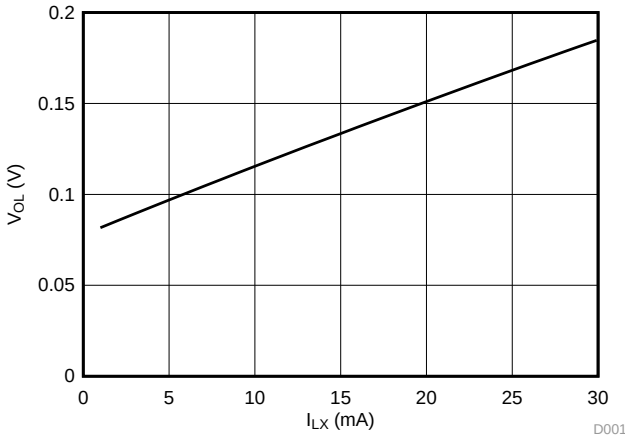


Figure 1. Typical V_{OL} of Lx/Ly (R_{PU} on Sx = 4.7 kΩ, T_A = 25 C, V_{SX} = 0 V)

7 Parameter Measurement Information

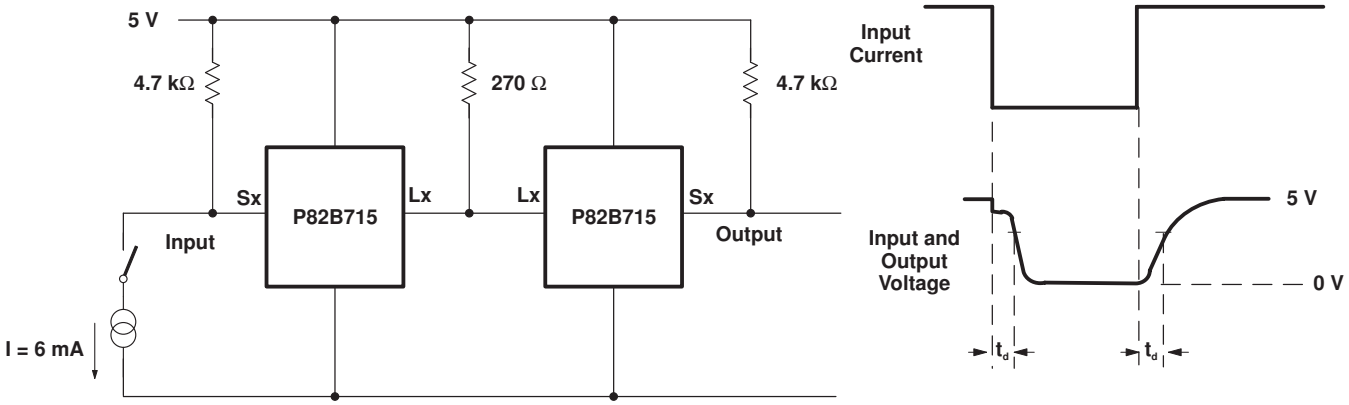


Figure 2. Test Circuit for Delay Times

8 Detailed Description

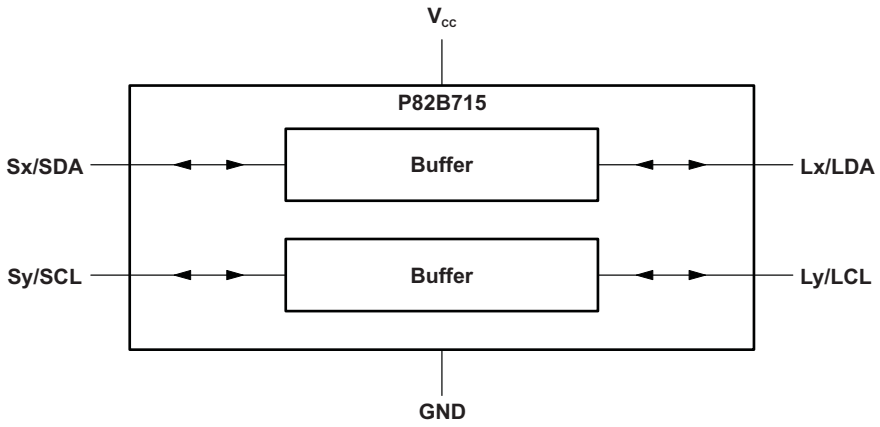
8.1 Overview

The I^2C bus capacitance limit of 400 pF restricts practical communication distances to a few meters. One of the advantages of the P82B715 is that it can isolate bus capacitance such that the total loading (devices, connectors, traces and wires) of the new bus or remote I^2C nodes are not apparent to other I^2C buses (or nodes). This is achieved by using one P82B715 device at each end of a long cable. The pin Lx of one P82B715 device must be connected to Lx of the second P82B715 (similarly for Ly). This allows the total system capacitance load to be around 3000 pF. The P82B715 uses unidirectional analog current amplification to increase the current sink capability of I^2C chips to change the 400-pF I^2C bus specification limit into a 3-nF bus wiring capacitance limit. That means longer cables or lower-cost general-purpose wiring may be used to connect two separate I^2C-based systems, without worrying about the special voltage levels associated with other I^2C bus buffers.

Multiple P82B715s can be connected together in a star or multipoint architecture by their Lx/Ly ports, without limit, as long as the total capacitance of the system remains less than about 3000 pF (400 pF or less when referenced to any Sx/Sy connection). In that arrangement, the master and/or slave devices are attached to the Sx/Sy port of each P82B715. In normal use, the power-supply voltages at each end of the low-impedance buffered bus line should be the same. If these differ by a significant amount, noise margin is sacrificed.

Two or more Sx or Sy I/Os can be interconnected and are also fully compatible with bus buffers that use voltage-level offsets (such as the TCA9517) because it duplicates and transmits the offset voltage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Sx and Sy

The I^2C pins (Sx and Sy) are designed to interface with a normal I^2C bus. The maximum I^2C bus supply voltage is 12 V. The Sx and Sy pins contain identical circuitry and can be used interchangeably as SCL or SDA.

8.3.2 Lx and Ly

The Lx and Ly pins are designed to interface with the high capacitance bus. This port of the device features circuitry to assist in sinking large amounts of currents required to operate a large capacitance bus at high speeds. More on this circuitry can be found in *Lx/Ly Buffered Bus Circuitry*.

8.3.3 Lx/Ly Buffered Bus Circuitry

On the special low-impedance or buffered-line side, the corresponding output becomes the LDA data line or LCL clock line. The P82B715 provides current amplification from its I^2C bus to its low impedance or buffered bus. Whenever current is flowing out of Sx into an I^2C chip driving the I^2C bus low, its amplifier sinks ten times that current into Lx, to drive the buffered bus low (see Figure 3). To minimize interference and ensure stability, the current rise and fall times of the Lx drive amplifier are internally controlled. The P82B715 does not amplify signal

Feature Description (continued)

currents flowing into Sx on the I^2C bus driven by currents flowing out of Lx on the buffered side. A buffered bus logic low signal at Lx passes through the internal 30-Ω resistor to drive the I^2C bus low. This signal current amplification, dependent on its direction, preserves the multi-master bidirectional open-collector/open-drain characteristic of any connected I^2C bus lines and the new low-impedance bus. Bus logic-signal voltage levels are clamped at (V_{CC} + 0.7 V) but, otherwise, are independent of the supply voltage, V_{CC}.

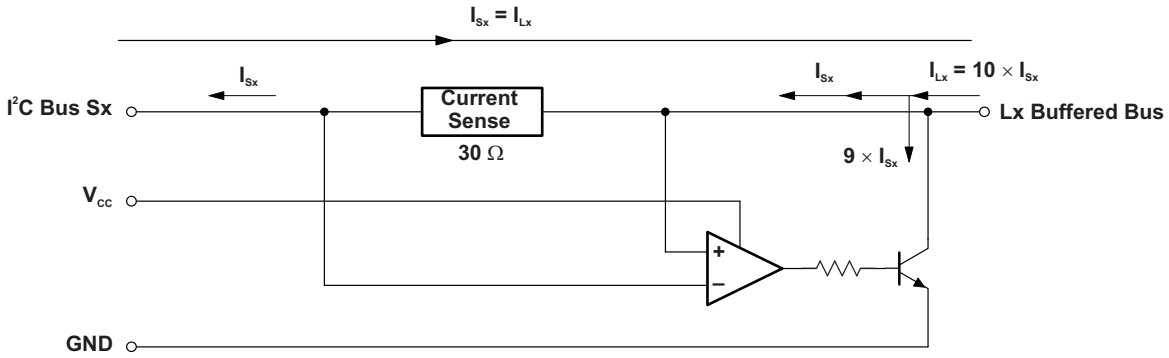


Figure 3. Equivalent Circuit (One-Half of P82B715)

8.4 Device Functional Modes

The P82B715 has two modes when powered, which depend on the state of the I^2C bus.

8.4.1 Idle Bus

When the I^2C bus is idle and high, little or no current flows through the device. In this case, the Lx/Ly buffer is not turned on.

8.4.2 Active-Low Bus

When a device connected to the Sx / Sy side of the device is transmitting a 0, a large amount of current will flow through the P82B715, which activates the internal pulldown to assist with the large capacitance.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The P82B715 can operate with a supply voltage from 3 V to 12 V, but the logic-signal levels at Sx/Lx are independent of the supply voltage. They remain at the levels presented to the chip by the attached devices. The maximum static I^2C bus sink current, 3 mA, flowing in either direction in the internal current sense resistor, causes a difference less than 100 mV in the bus logic low levels at Sx and Lx. This makes P82B715 fully compatible with all logic signal drivers, including TTL. The P82B715 cannot modify the bus logic signal voltage levels, but it contains internal diodes connected between Lx/Sx and V_{CC} that conduct and limit the logic signal swing if the applied logic levels would have exceeded the supply voltage by more than 0.7 V.

In normal applications, external pullup resistors pull the connected buses up to the desired voltage high level. Usually this is the supply voltage, V_{CC}, but for very low logic voltages, it is necessary to use a V_{CC} of at least 3.3 V and preferably higher. Note that full performance over temperature is ensured only from 4.5 V. Specification deratings apply when its supply voltage is reduced below 4.5 V. The absolute minimum V_{CC} is 3 V.

9.2 Typical Application

By using two (or more) P82B715 devices, a subsystem can be built that retains the interface characteristics of a normal I^2C device so that the subsystem may be included in, or added to, any I^2C or related system.

The subsystem features a low-impedance or buffered bus capable of driving large wiring capacitance (see Figure 4).

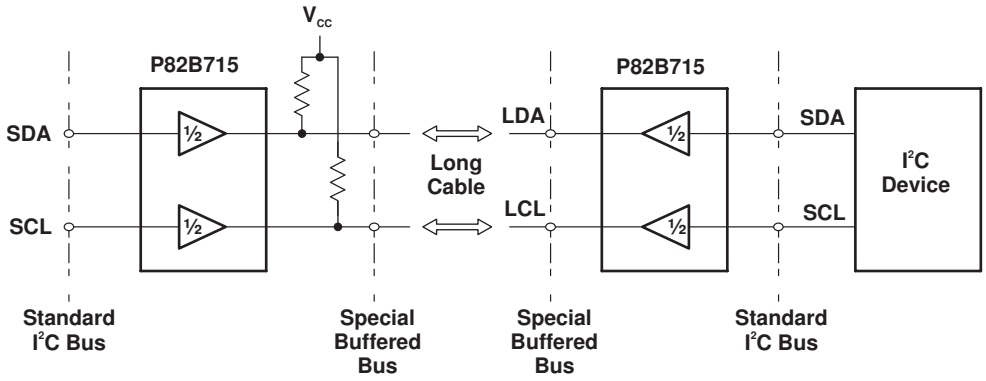


Figure 4. Minimum Subsystem Diagram

9.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

PARAMETER	DESCRIPTION	VALUE
V_{CC}	Supply Voltage	3.3 V
C_{Lx}	Capacitance on the Lx / Ly bus	3000 pF
R_{PU_Sx}	Pullup resistor for the Sx / Sy bus	4700 Ω
R_{PU_Lx}	Pullup resistor for the Lx / Ly bus	330 Ω

9.2.2 Detailed Design Procedure

9.2.2.1 I^2C Systems

As in standard I^2C systems, pullup resistors are required to provide the logic high levels on the buffered bus, as the standard open-collector configuration is retained. The size and number of pullup resistors depends on the system.

If P82B715 devices are to be permanently connected into a system, the circuit may be configured with only one pullup resistor on the buffered bus and none on the I^2C buses, but the system design is simplified, and performance is improved by fitting separate pullups on each section of the bus. When a subsystem using P82B715 may be optionally connected to an existing I^2C system that already has a pullup, the effects of the subsystem pullups acting in parallel with the existing I^2C bus pullup must be considered.

9.2.2.2 Pullup Resistance Calculation

When calculating the pullup resistance values, the gain of the buffer introduces scaling factors that must be applied to the system components. In practical systems, the pullup resistance value is calculated to meet the rise time limit for I^2C systems. As an approximation, this limit is satisfied in a 100-kHz system if the time constant of the total system (product of the net resistance and net capacitance) is set to 1 µs or less.

In systems using the P82B715, it is convenient to set the total system time constant by considering each bus node separately (that is, the I^2C nodes and the buffered bus node) and selecting a separate pullup resistor for each node to provide time constants of less than 1 µs. If each node complies then the system requirement is also met.

This arrangement, using multiple pullups as shown in Figure 5, provides the best system performance and allows stand-alone operation of individual I^2C buses if parts of the extended system are disconnected or reconnected. For each bus section, the pullup resistor is calculated as:

$$R = 1\ \mu s/(C_{device} + C_{wiring}) \quad (1)$$

where

- C_{device} = Sum of any connected device capacitances
- C_{wiring} = Total wiring and stray capacitance on the bus section

The 1 µs is an approximation with a safety factor to the theoretical time constant necessary to meet the specified 1-µs bus rise-time specification in a system with variable logic thresholds, where the CMOS limits of 30% and 70% of V_{CC} apply. The calculated value is 1.18 µs.

If these capacitances cannot be measured or calculated, an approximation can be made by assuming that each device presents 10 pF of load capacitance and 10 pF of trace capacitance, and that cables range from 50 pF to 100 pF per meter.

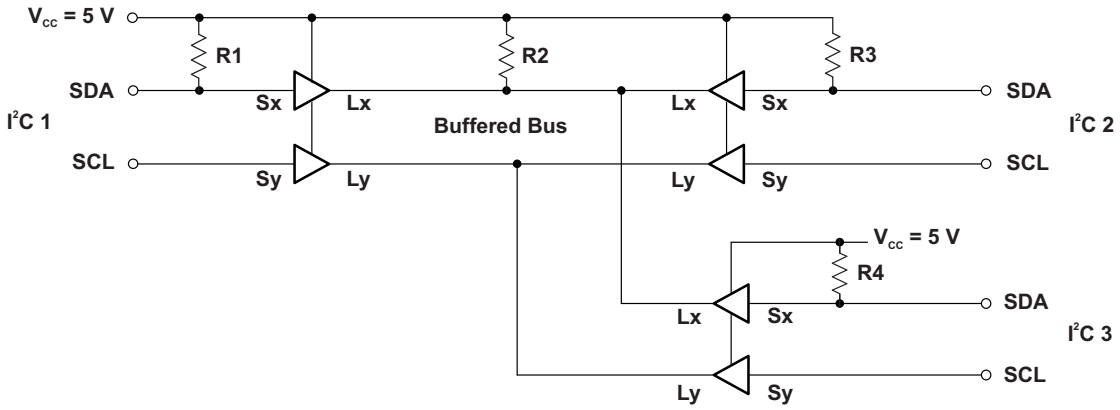


Figure 5. Single Pullup Buffered Bus

If only a single pullup is used, it must be placed on the buffered bus (as R2 in Figure 5) and the associated total system capacitance calculated by combining the individual bus capacitances into an equivalent capacitive loading on the buffered bus.

This equivalent capacitance is the sum of the capacitance on the buffered bus plus ten times the sum of the capacitances on all the connected I^2C nodes. The calculated value should not exceed 4 nF. The single buffered bus pullup resistor is then calculated to achieve the 1-µs rise time, and it provides the pullup for the buffered bus and for all other connected I^2C bus nodes included in the calculation.

9.2.2.3 Calculating Bus Drive Currents

Figure 5 shows three P82B715 devices connected to a common buffered bus. The associated bus capacitances are omitted for clarity, but assume the resistors have been selected to give R-C products of less than 1 µs so the bus rise-time requirement is satisfied. An I^2C device connected at I^2C 1 and holding the SDA bus low must sink the current flowing in its local pullup R1, plus, with assistance from the P82B715, the currents in R2, R3, and R4. Because the resistors R3 and R4 act to pull the bus nodes I^2C 2 and I^2C 3 and their corresponding Sx pins to a voltage higher than the voltage at the Lx pins, their buffer amplifiers are inactive. The SDA at Sx of I^2C 2 and I^2C 3 is pulled low by the low at Lx through the internal 30-Ω resistor that links Lx to Sx. So the effective current that must be sunk by the P82B715 buffer on I^2C 1 at its Lx pin is the sum of the currents in R2, R3, and R4. The Sx current that must be sunk by an I^2C device at I^2C 1 due to the buffer gain action is 1/10 of the Lx current. So the effective pullup determining the current to be sunk by an I^2C device at I^2C 1 is R1 in parallel with resistors ten times the values of R2, R3, and R4. If R1 = R3 = R4 = 10 kΩ, and R2 = 1 kΩ, the effective pullup load at I^2C 1 is 10 kΩ||10 kΩ||100 kΩ||100 kΩ = 4.55 kΩ.

The same calculation applies for I^2C 2 or I^2C 3.

To calculate the current sunk by the Lx pin of the buffer at I^2C 1, note that the current in R1 is sunk directly by the device at I^2C 1. The buffer, therefore, sinks only the currents flowing in R2, R3, and R4, so the effective pullup is R2 in parallel with R3 and R4.

In this example that is 1 kΩ||10 kΩ||10 kΩ = 833 Ω. For a 5.5-V supply and 0.4-V low, the buffer is sinking 16.3 mA.

The P82B715 has a static sink rating of 30 mA at Lx. The requirement is that the pullup on the buffered bus, in parallel with all other pullups that it is indirectly pulling low on Sx pins of other P82B715 devices, does not cause this 30-mA limit to be exceeded.

The minimum pullup resistance in a 5-V ± 10% system is 170 Ω.

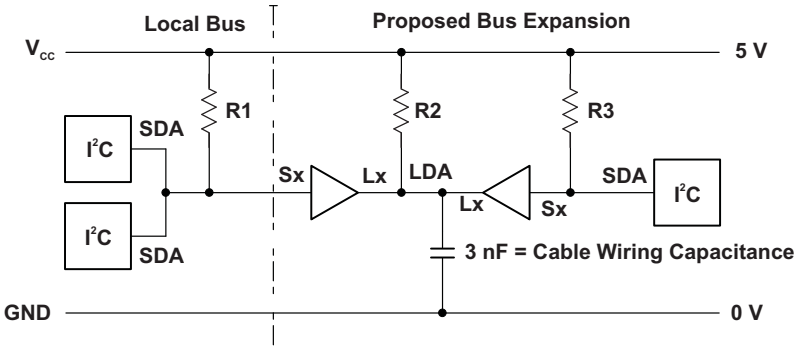
The general requirement is:

$$(V_{CC}(max) - 0.4)/R_P < 30\ mA \quad (2)$$

where

- R_p = Parallel combination of all pullup resistors driven by the Lx pin of the P82B715

Figure 6 shows calculations for an expanded I^2C bus with 3 nF of cable capacitance.



Effective Capacitance Local Bus I²C Devices

2 × I²C Devices	20 pF
Strays	20 pF
P82B715	10 pF
Total	50 pF

Local I²C Pullup

$$R1 = \frac{1\ \mu s}{50\ pF} = 20\ k\Omega$$

Effective Capacitance Buffered Line

Wiring Capacitance	3000 pF
Total	3000 pF

Buffered Bus Pullup

$$R2 = \frac{1\ \mu s}{3000\ pF} = 330\ \Omega$$

Effective Capacitance Remote I²C Devices

1 × I²C Devices	10 pF
Strays	10 pF
P82B715	10 pF
Total	30 pF

Remote I²C Pullup

$$R3 = \frac{1\ \mu s}{30\ pF} = 33\ k\Omega$$

Figure 6. Typical Loading Calculations

9.2.3 Application Curve

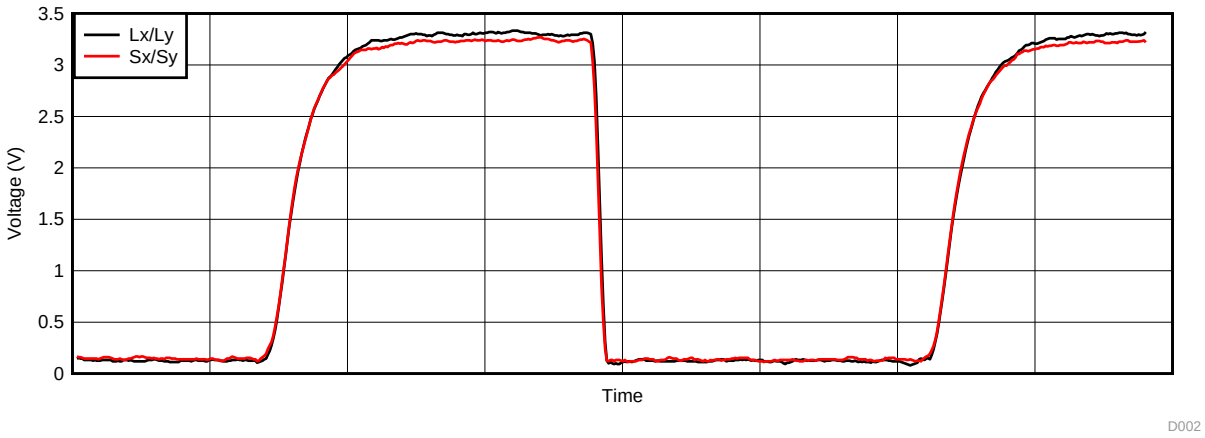


Figure 7. Voltage On Bus (3000 pF on Lx/Ly With R_{PU} = 330 Ω)

10 Power Supply Recommendations

The P82B715 power supply requirements can be see in the *Recommended Operating Conditions*. Note that the P82B715 can operate down to 3 V, but at reduced performance.

11 Layout

11.1 Layout Guidelines

General layout best practices are recommended. It is common to have a dedicated ground plane on an inner layer of the board, and pins that are connected to ground must have a low-impedance path to the ground place in the form of wide polygon pours, and multiple vias.

Bypass and decoupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch (typically 1 µF), and a smaller capacitor (typically 0.1 µF) to filter out high-frequency ripple.

11.2 Layout Example

◌ = VIA to ground plane

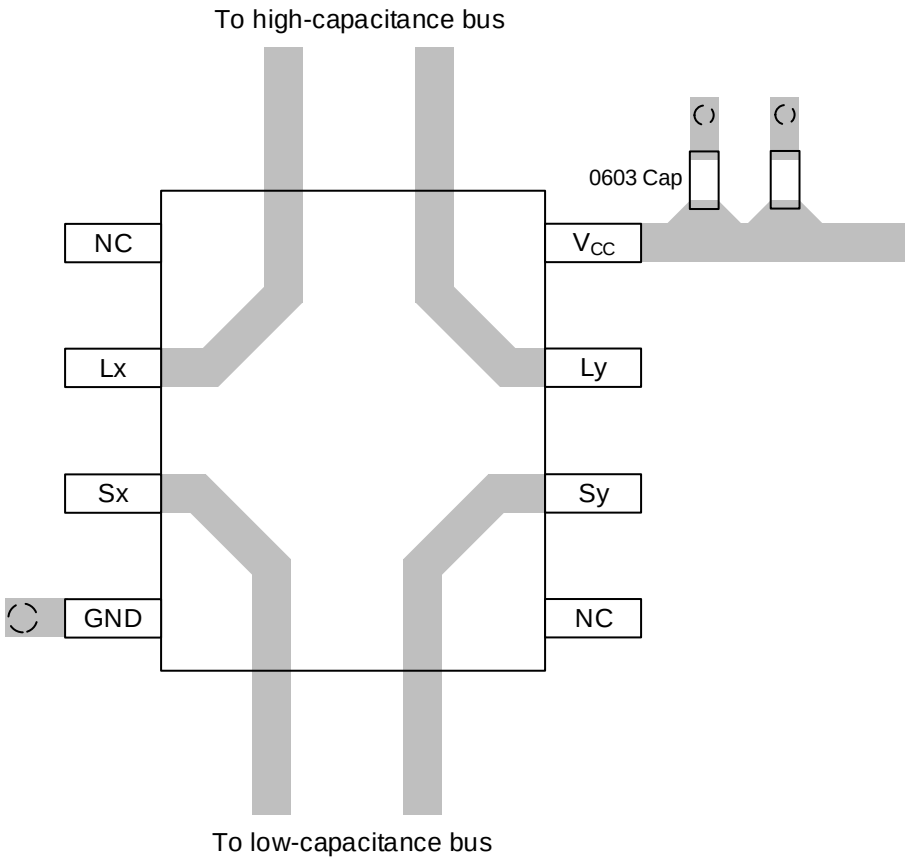


Figure 8. D Package Example Layout

12 Device and Documentation Support

12.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

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All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
P82B715D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG715	
P82B715DG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG715	
P82B715DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG715	Samples
P82B715DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG715	Samples
P82B715P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	P82B715P	Samples
P82B715PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	P82B715P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

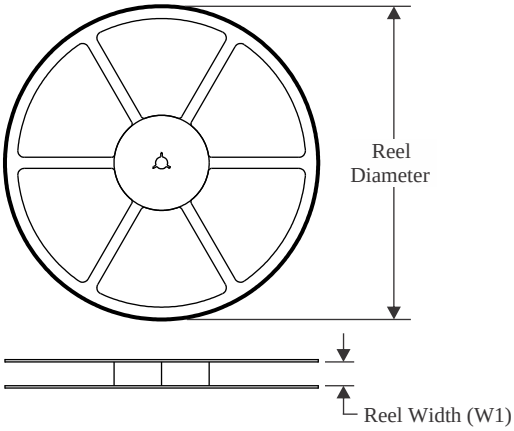
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

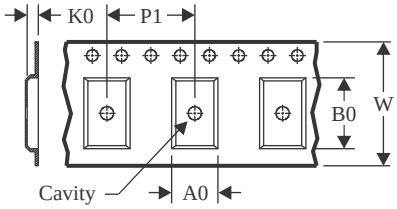
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

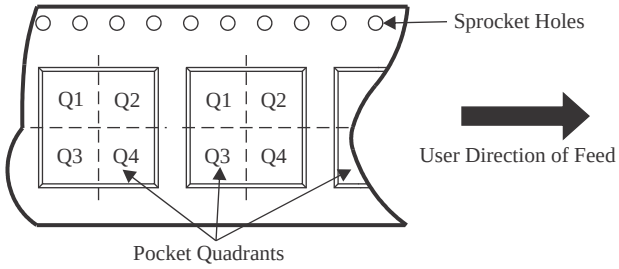


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

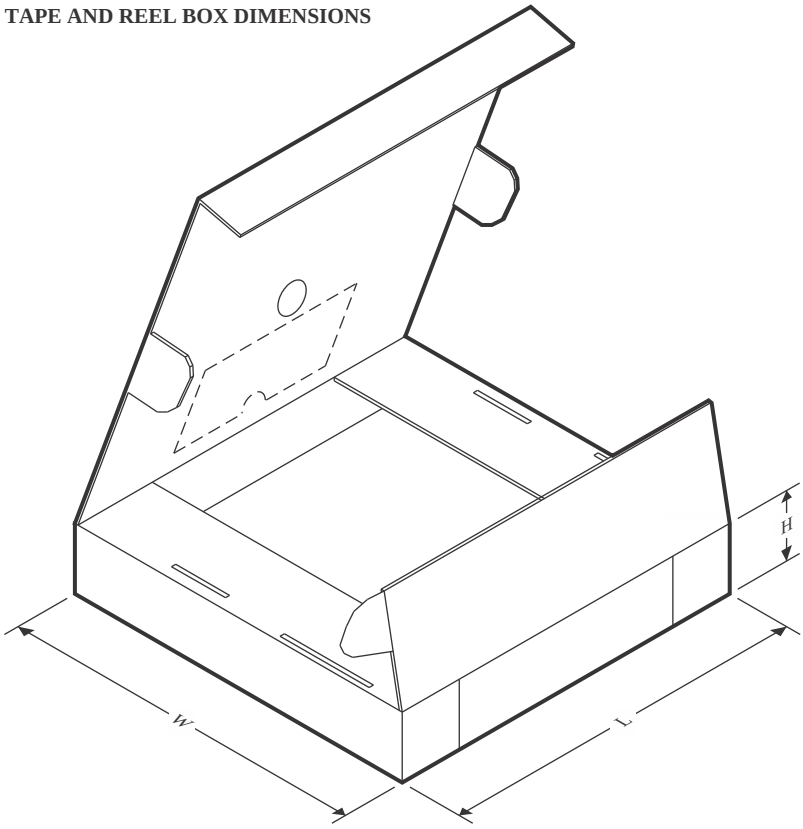
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P82B715DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

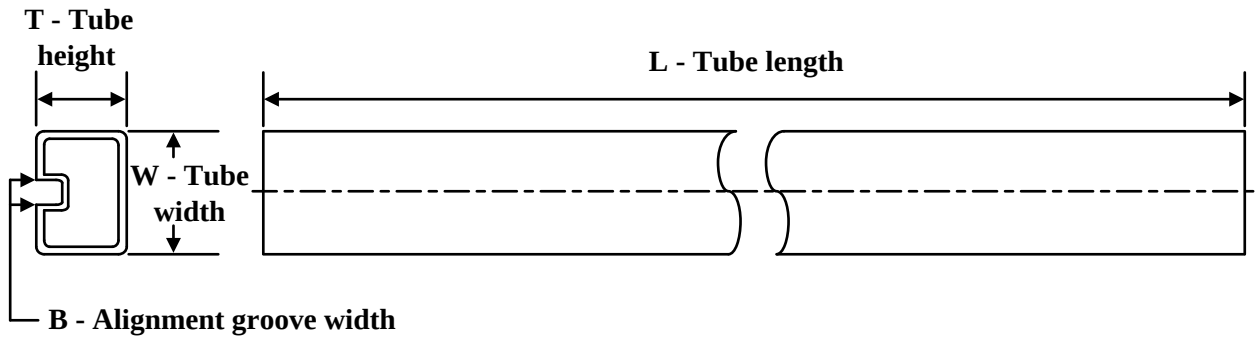
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P82B715DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

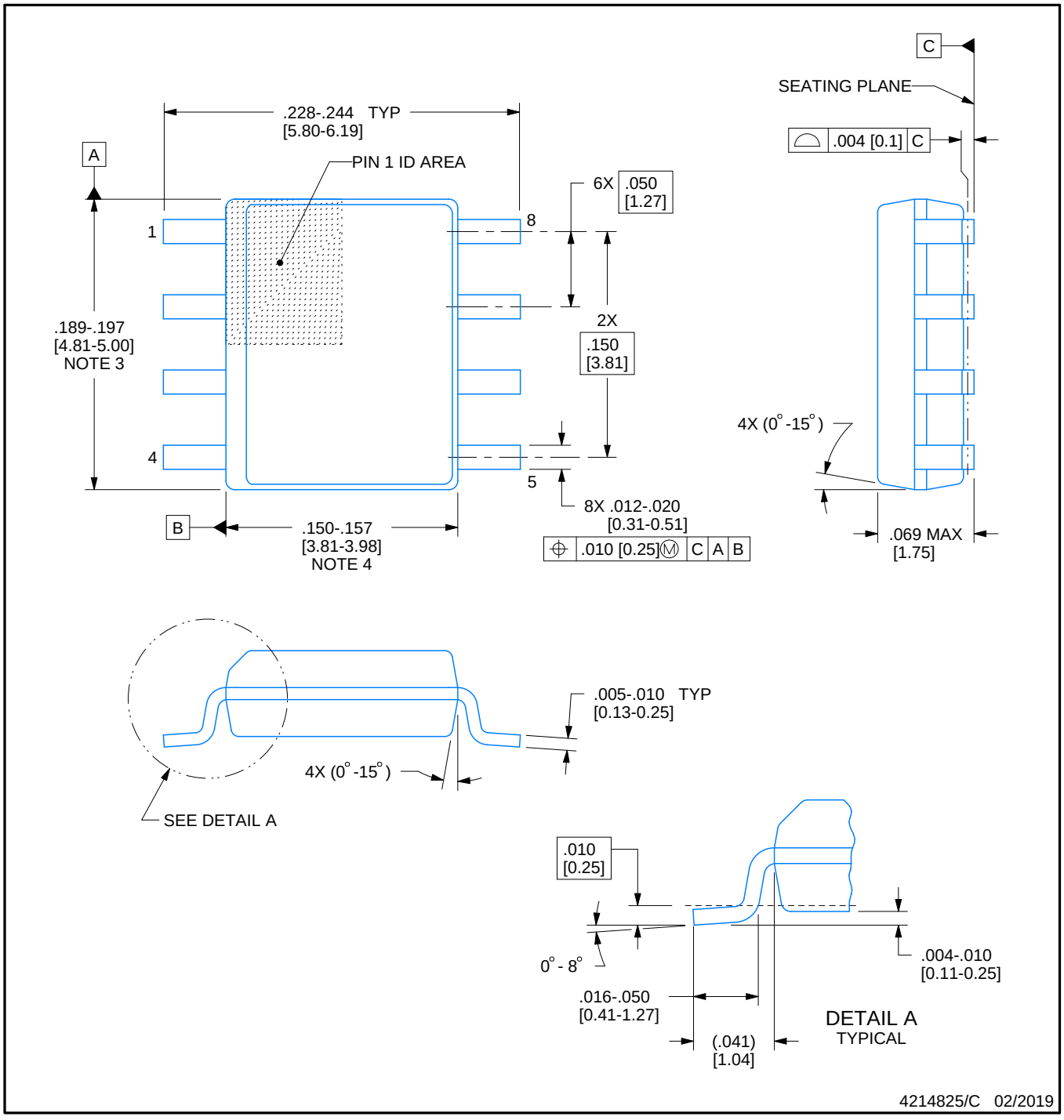
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
P82B715D	D	SOIC	8	75	506.6	8	3940	4.32
P82B715DG4	D	SOIC	8	75	506.6	8	3940	4.32
P82B715P	P	PDIP	8	50	506	13.97	11230	4.32
P82B715PE4	P	PDIP	8	50	506	13.97	11230	4.32

PACKAGE OUTLINE

D0008A

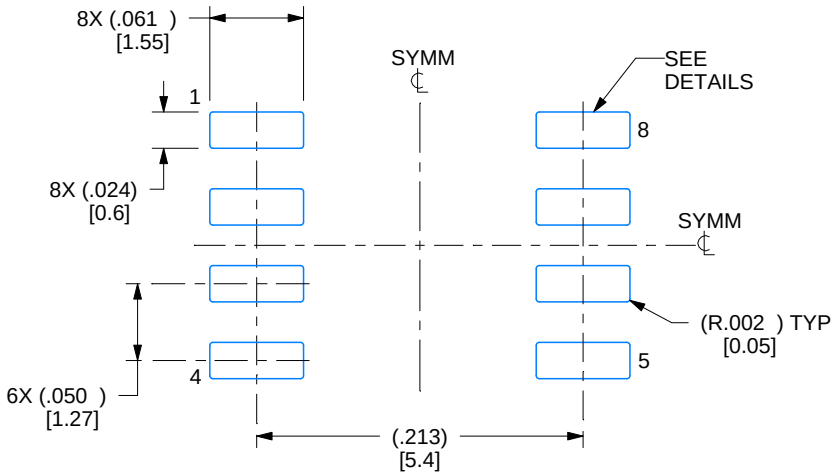
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

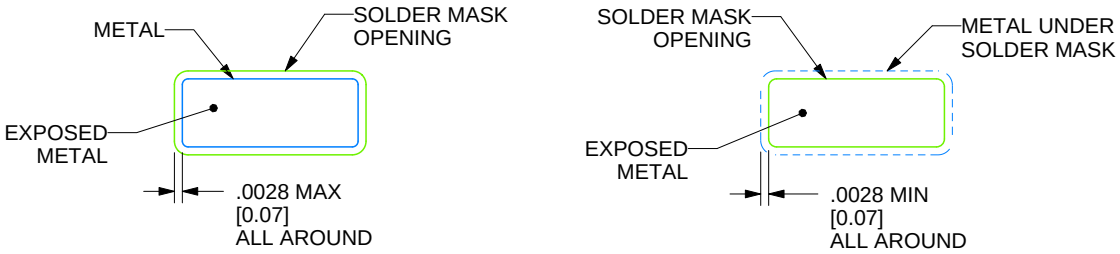


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

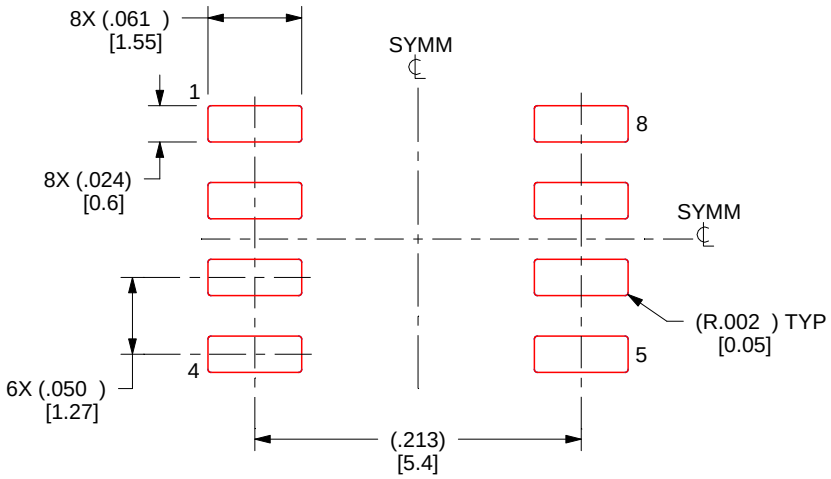
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



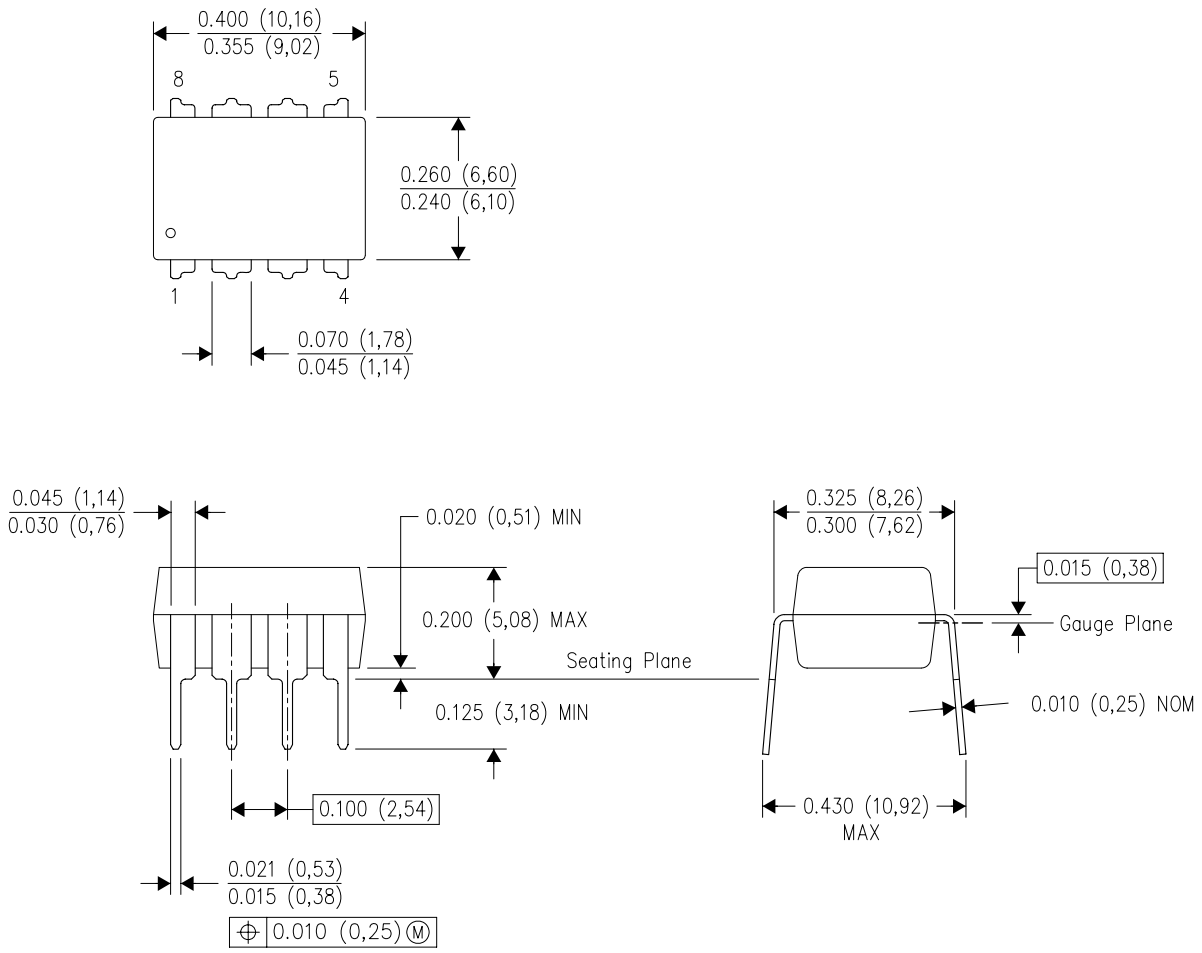
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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>>TI(德州仪器)