

AM26LV31 低压、高速四路差分线路驱动器

1 特性

- 开关速率高达 32MHz
- 由一个 3.3V 单电源供电运行
- 传播延迟时间: 8ns (典型值)
- 脉冲偏斜时间: 500ps (典型值)
- 高输出驱动电流: $\pm 30\text{mA}$
- 可控的上升和下降时间: 3ns (典型值)
- 具有 100 Ω 负载时的差分输出电压: 1.5V (典型值)
- 超低功耗
 - 直流, 0.3mW (最大值)
 - 所有通道 32MHz (空载), 385mW (典型值)
- 接受 5V 逻辑输入及 3.3V 电源
- 针对 AM26C31、AM26LS31 和 MB571 的低压引脚对引脚兼容替换产品
- 断电时具有高输出阻抗
- 驱动器输出短路保护电路
- 封装选项包括小外形 (D, NS) 塑料封装

2 应用

- 电机控制: 无刷直流和刷式直流
- 现场发送器: 温度传感器和压力传感器
- 采用 Modbus 的温度传感器或控制器

3 说明

AM26LV31C 和 AM26LV31I 是具有三态输出的 BiCMOS 四路差分线路驱动器。它们与 TIA/EIA-422-B 和 ITU Recommendation V.11 驱动器类似, 但电源电压范围较小。

这些器件经过优化, 可在高达 32MHz 的开关速率下实现平衡总线传输。输出端可提供非常高的电流, 从而驱动双绞线传输线路等平衡线路, 并在关断情况下提供高阻抗。四个驱动器均具有使能功能, 该功能提供了两种可选输入: 有源高电平使能输入和有源低电平使能输入。AM26LV31C 和 AM26LV31I 在设计中使用了德州仪器 (TI) 的 LinIMPACT-C60™ 专利技术, 可在不牺牲速度的情况下实现超低功耗。这些器件会在与 AM26LV32 四路线路接收器配合使用时提供最佳的性能。

AM26LV31C 的工作温度范围是 0°C 至 70°C。

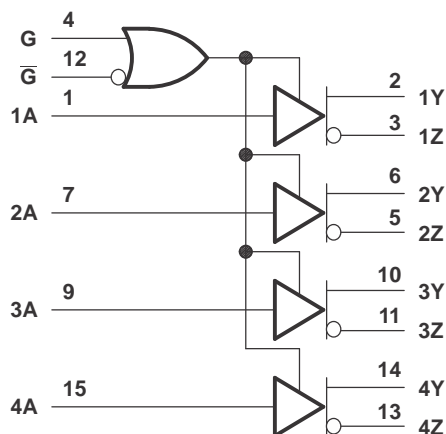
AM26LV31I 的工作温度范围是 45°C 至 85°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
AM26LV31C	SOIC (D) 16	9.90mm x 3.91mm
AM26LV31I	SOIC (D) 16	9.90mm x 3.91mm
	SO (NS) 16	10.3mm x 5.30mm

(1) 要了解所有可用封装, 请参见数据表末尾的可订购产品附录。

逻辑图 (正逻辑)



目录

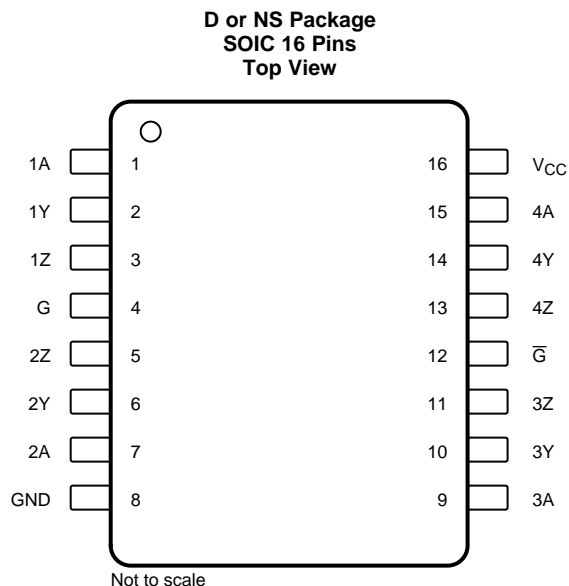
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (May 2005) to Revision H	Page
• 添加了器件信息表、ESD 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
• Changed the t_{PLH} and t_{PHL} MAX value From: 12 ns To: 20 ns in the <i>Switching Characteristics</i>	5
• Changed the $t_{sk(p)}$ and $t_{sk(o)}$ MAX value From: 1.5 ns To: 3 ns in the <i>Switching Characteristics</i>	5

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Driver 1 input
2	1Y	O	Driver 1 output
3	1Z	O	Driver 1 inverted output
4	G	I	Active high enable
5	2Z	O	Driver 2 inverted output
6	2Y	O	Driver 2 output
7	2A	I	Driver 2 input
8	GND	—	Ground pin
9	3A	I	Driver 3 input
10	3Y	O	Driver 3 output
11	3Z	O	Driver 3 inverted output
12	\bar{G}	I	Active low enable
13	4Z	O	Driver 4 inverted output
14	4Y	O	Driver 4 output
15	4A	I	Driver 4 input
16	V _{CC}	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage range, V_{CC} ⁽²⁾	-0.3	6	V
Input voltage range, V_I	-0.3	6	V
Output voltage range, V_O	-0.3	6	V
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-30	mA
I_{OL}	Low-level output current			30	mA
T_A	Operating free-air temperature	AM26LV31C	0	70	°C
		AM26LV31I	-45	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	NS (SO)	UNIT
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.9	76.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.1	37.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.9	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.8	37.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating supply-voltage and free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = 18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{IH} = 2 V, I _{OH} = -12 mA	1.85	2.3		V
V _{OL}	Low-level output voltage	V _{IL} = 0.8 V, I _{OH} = 12 mA		0.8	1.05	V
V _{OD}	Differential output voltage ⁽²⁾	R _L = 100 Ω	0.95	1.5		V
V _{OC}	Common-mode output voltage		1.3	1.55	1.8	V
Δ V _{OC}	Change in magnitude of common-mode output voltage ⁽²⁾				±0.2	V
I _O	Output current with power off	V _O = -0.25 V or 6 V, V _{CC} = 0			±100	μA
I _{OZ}	Off-state (high-impedance state) output current	V _O = -0.25 V or 6 V, G = 0.8 V or \overline{G} = 2 V			±100	μA
I _H	High-level input current	V _{CC} = 0 or 3 V, V _I = 5.5 V			10	μA
I _L	Low-level input current	V _{CC} = 3.6 V, V _I = 0			-10	μA
I _{OS}	Short-circuit output current	V _{CC} = 3.6 V, V _O = 0			-200	mA
I _{CC}	Supply current (all drivers)	V _I = V _{CC} or GND, No load			100	μA
C _{pd}	Power-dissipation capacitance (all drivers) ⁽³⁾	No load		160		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

(3) C_{pd} determines the no-load dynamic current consumption. I_S = C_{pd} × V_{CC} × f + I_{CC}

6.6 Switching Characteristics

V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	See Figure 3	4	8	20	ns
t _{PHL}	Propagation delay time, high- to low-level output		4	8	20	ns
t _t	Transition time (t _r or t _f)			3		ns
SR	Slew rate, single-ended output voltage	See Note ⁽²⁾ and Figure 3		0.3	1	V/ns
t _{PZH}	Output-enable time to high level	See Figure 4		10	20	ns
t _{PZL}	Output-enable time to low level	See Figure 5		10	20	ns
t _{PHZ}	Output-disable time from high level	See Figure 4		10	20	ns
t _{PLZ}	Output-disable time from low level	See Figure 5		10	20	ns
t _{sk(p)}	Pulse skew	f = 32 MHz, See Note ⁽³⁾		0.5	3	ns
t _{sk(o)}	Skew limit	f = 32 MHz			3	ns
t _{sk(lim)}	Skew limit (device to device)	f = 32 MHz, See Note ⁽⁴⁾			3	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) Slew rate is defined by [Equation 1](#)

(3) Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

(4) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

$$SR = \frac{90\%(V_{OH} - V_{OL}) - 10\%(V_{OH} - V_{OL})}{t_r}, \text{ the differential slew rate of } V_{CC} \text{ is } 2 \times SR. \quad (1)$$

6.7 Typical Characteristics

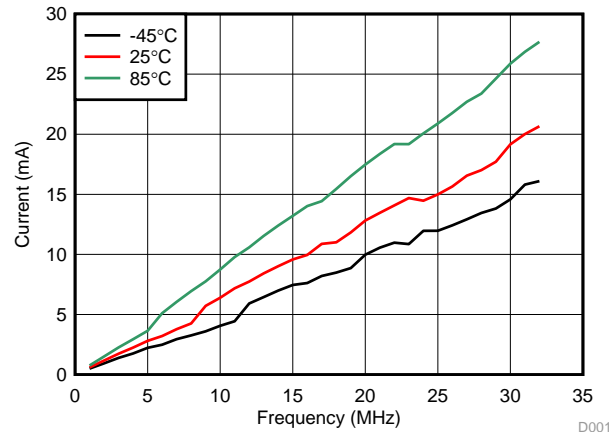


图 1. Current vs Frequency

7 Parameter Measurement Information

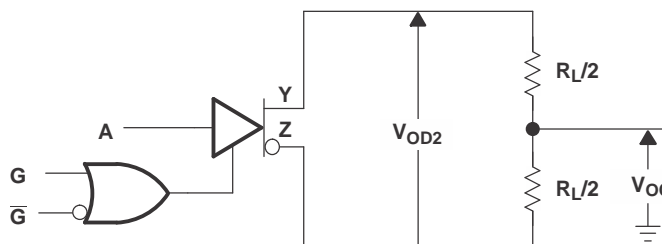
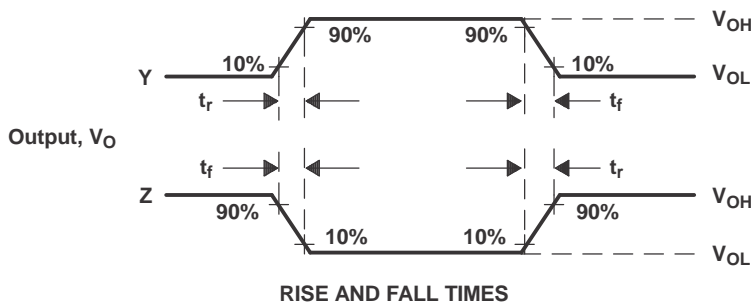
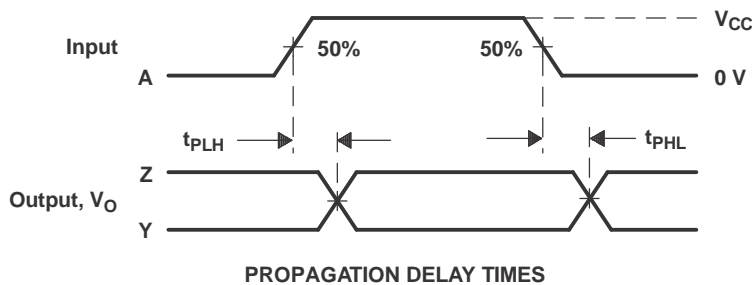
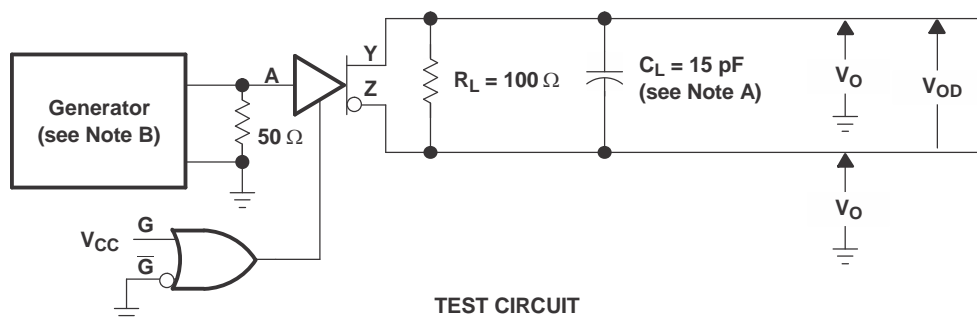


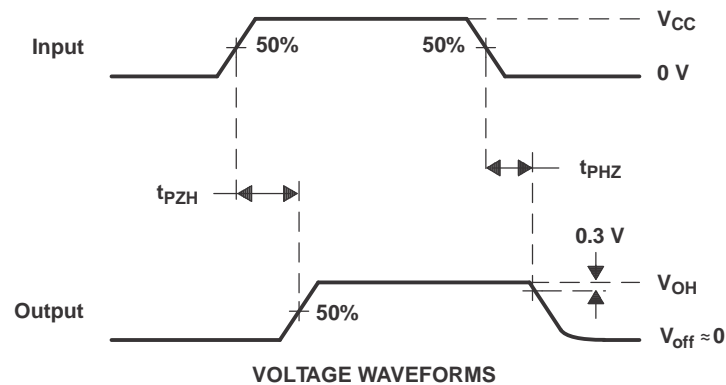
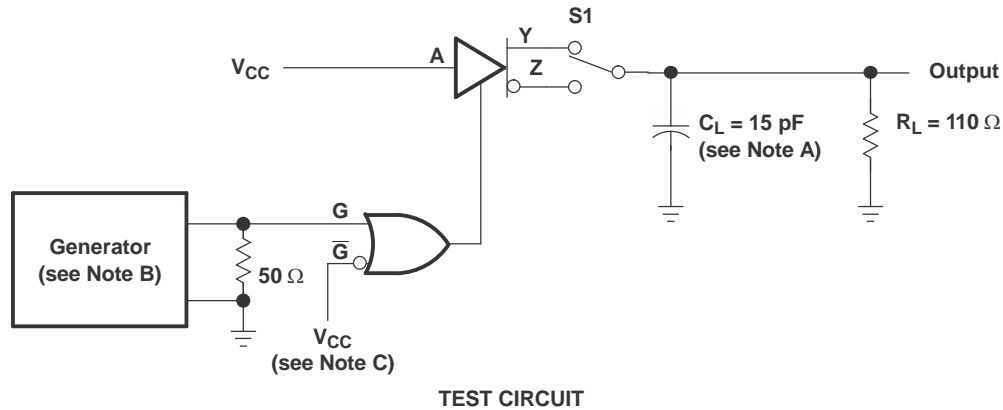
图 2. Differential and Common-Mode Output Voltages



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, $Z_0 = 50 \Omega$, 50%v duty cycle, t_r and $t_f \leq 2$ ns.

图 3. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

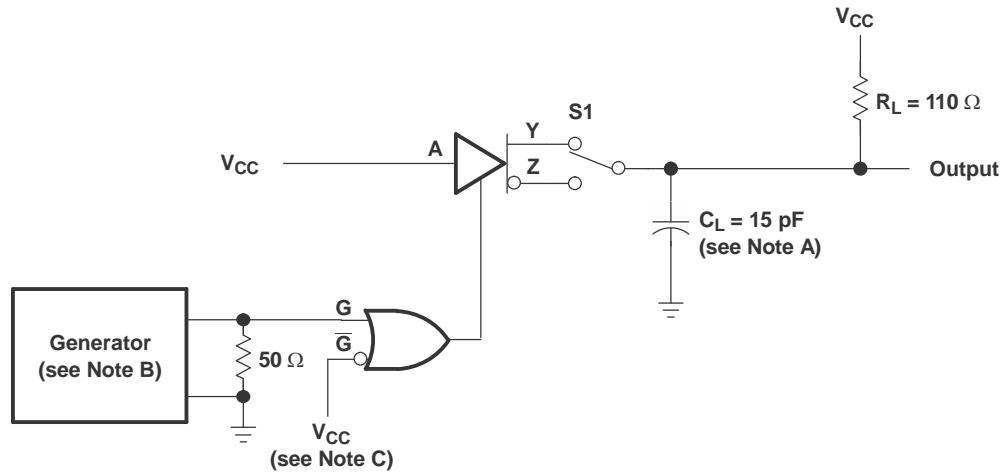
Parameter Measurement Information (接下页)



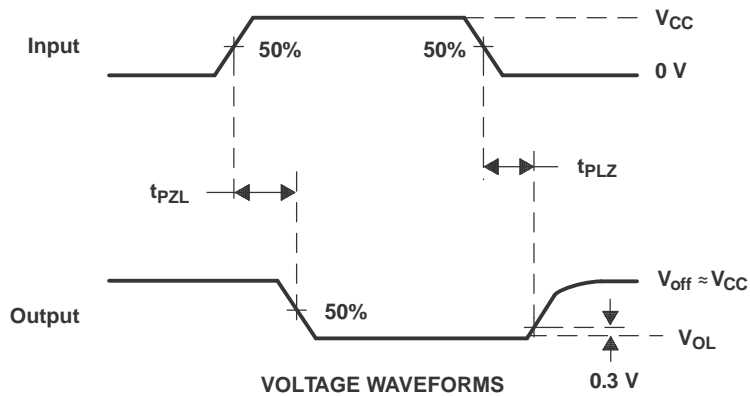
- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_O = 50 \Omega$, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
- C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

图 4. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

Parameter Measurement Information (接下页)



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_O = 50 \Omega$, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
- C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

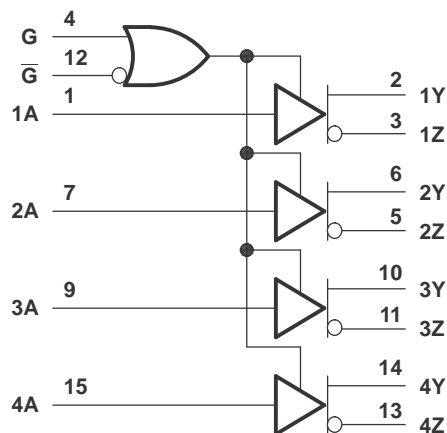
图 5. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

8 Detailed Description

8.1 Overview

The AM26LV31C and AM26LV31I are BiCMOS quadruple differential line drivers with 3-state outputs. The devices are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with a single 3.3-V power supply. The drivers also integrate active-high and active-low enables for precise device control.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Active high and active low

The devices can be configured using the G and G logic inputs to select transmitter output. A logic high on the G pin or a logic low on the G pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.3.2 Operates from a 3.3-V Supply with up to 5-V Logic

While the transmitters operate from a single 3.3-V rail, the logic can operate off the same rail or another 5-V rail, making designs much more flexible to communicate to controllers.

8.3.3 High Speed Transmission

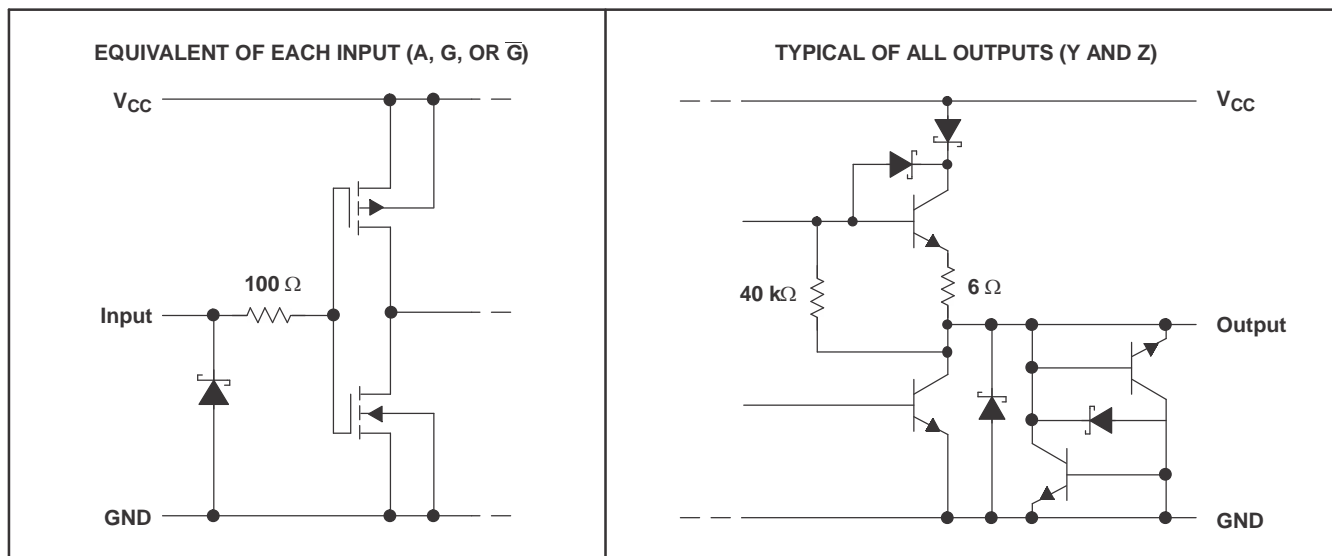
The AM26LV31C and AM26LV31I are optimized for balanced-bus transmission at switching rates up to 32 MHz. The devices are designed using Texas Instruments proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

8.4 Device Functional Modes

表 1. Function Table⁽¹⁾

INPUT A	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)



If resistor values are nominal.

图 6. Schematic (Each Driver)

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. If termination is used, it can be placed at the end of the cable near the last receiver. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31C and AM26LV32C, respectively, were tested at room temperature with a 3.3-V supply voltage. The first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

9.2 Typical Application

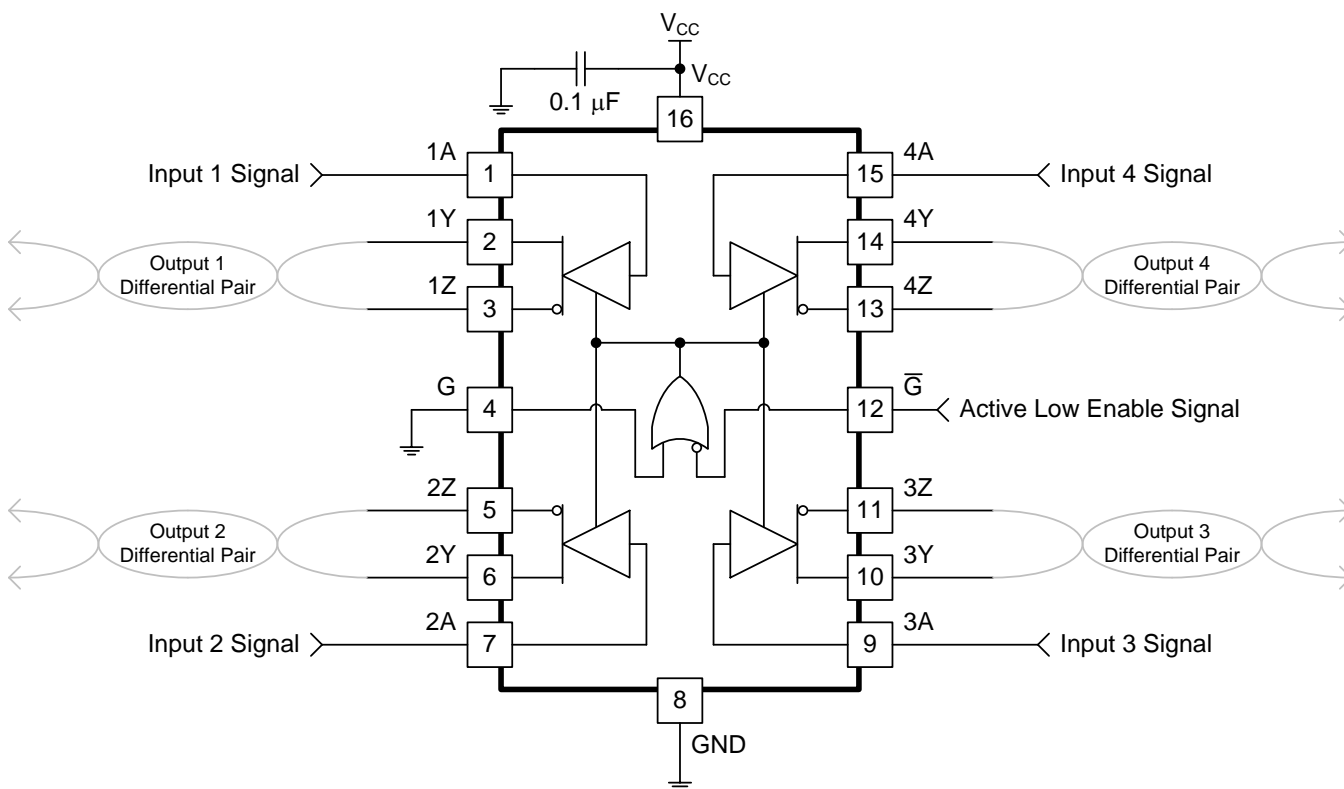


图 7. Differential Terminated Configuration With All Channels and Active Low Enable Used

Typical Application (接下页)

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T , must be within 20% of the characteristic impedance, Z_0 , of the cable and can vary from about 80 Ω to 120 Ω .

This example requires the following:

- 3.3-V power source
- RS-485 bus operating at 32 MHz or less
- Connector that ensures the correct polarity for port pins

9.2.2 Detailed Design Procedure

Ensure values in Absolute Maximum Ratings are not exceeded. Supply voltage, V_{IH} , and V_{IL} must comply with Recommended Operating Conditions.

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see Failsafe in RS-485 data buses).

9.2.3 Application Curves

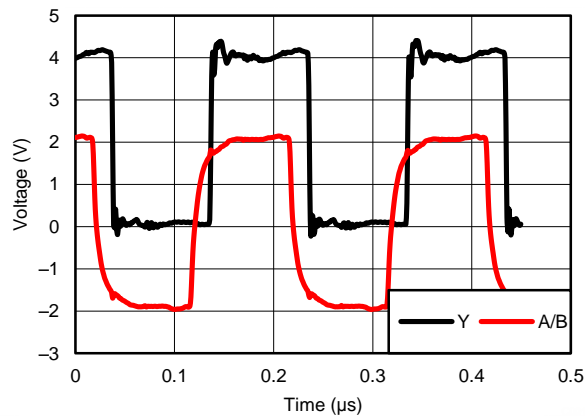


图 8. Differential 120- Ω Terminated Output Waveforms (Cat 5E Cable)

10 Power Supply Recommendations

Place a 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry. Connect low-ESR, 0.1- μ F ceramic bypass capacitors between supply pin and ground, placed as close to the device as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

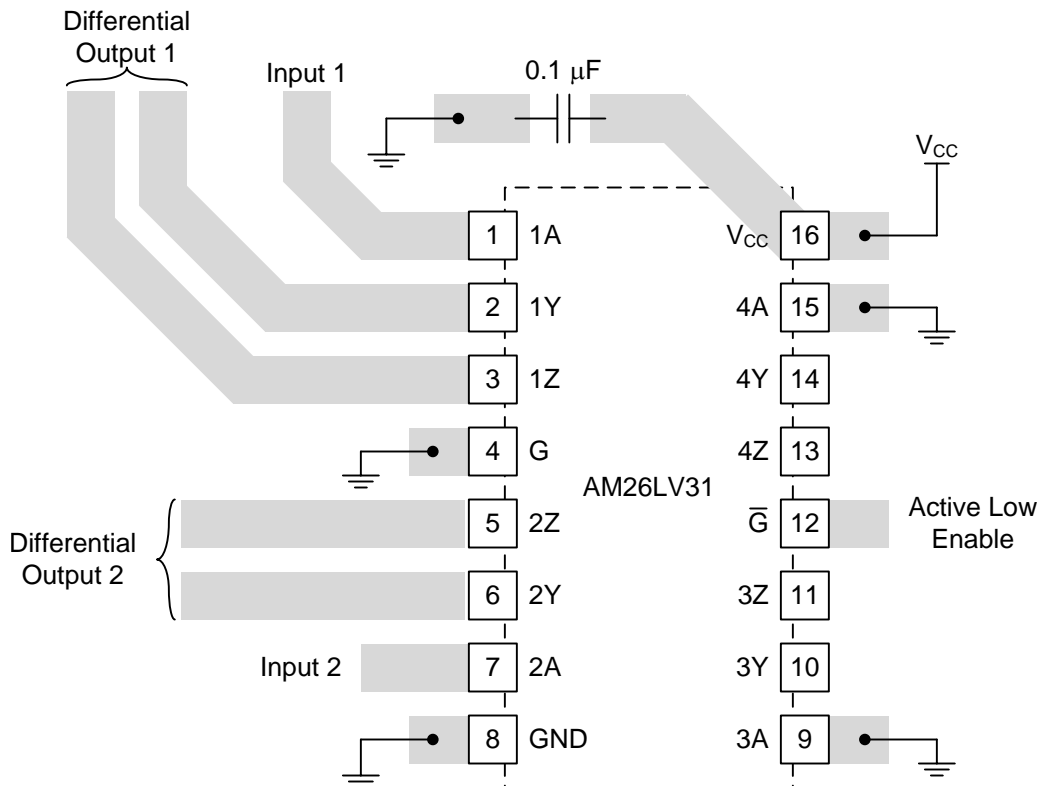


图 9. Trace Layout on PCB and Recommendations

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

LinIMPACT-C60, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV31CD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	
AM26LV31CDE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	
AM26LV31CDG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	
AM26LV31CDR	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	AM26LV31C	
AM26LV31CDRE4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	
AM26LV31CDRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV31C	
AM26LV31CNSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LV31	
AM26LV311D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV311	
AM26LV311DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV311	Samples
AM26LV311NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 85	26LV311	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31CDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31CDRG4	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31CNSR	SO	NS	16	2000	367.0	367.0	38.0
AM26LV31IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31INSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
AM26LV31CD	D	SOIC	16	40	507	8	3940	4.32
AM26LV31CDE4	D	SOIC	16	40	507	8	3940	4.32
AM26LV31CDG4	D	SOIC	16	40	507	8	3940	4.32
AM26LV31ID	D	SOIC	16	40	507	8	3940	4.32



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



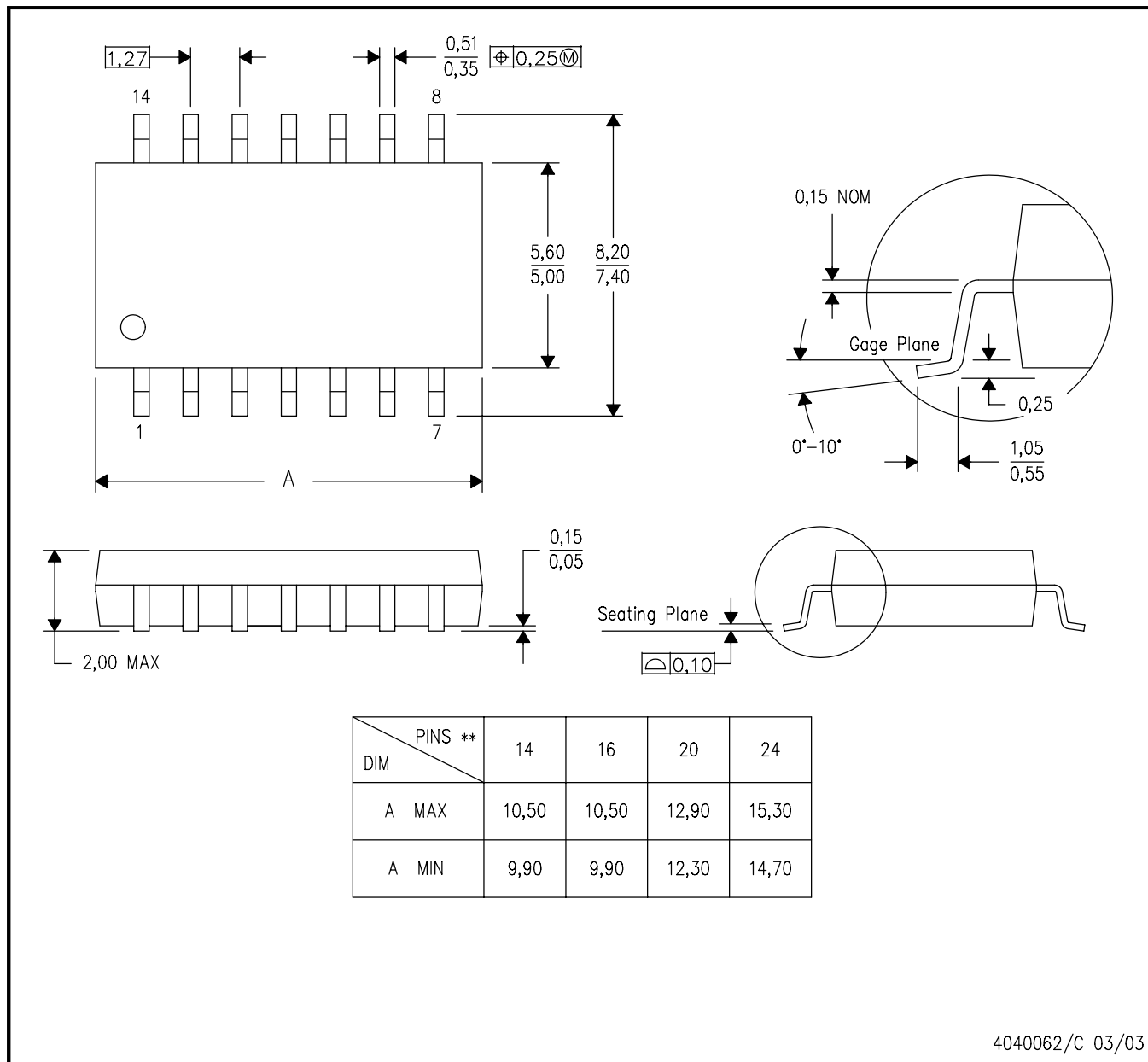
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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