ISOx5 Isolated 3.3-V Half- and Full-Duplex RS-485 Transceivers

1 Features

- Meets or Exceeds TIA/EIA RS-485 Requirements
- 1/8 Unit Load – Up to 256 Nodes on a Bus
- Signaling Rates up to 1 Mbps
- Thermal Shutdown Protection
- Low Bus Capacitance – 16 pF (Typical)
- 50 kV/μs Typical Transient Immunity
- Fail-safe Receiver for Bus Open, Short, Idle
- 3.3-V Inputs are 5-V Tolerant
- Safety and Regulatory Approvals
  - 4000-V_{PK} V_{IOTM}, 560-V_{PK} V_{IORM} per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation Rating per UL 1577
  - 2500 V_{RMS} Isolation Rating per CSA CA5A and IEC 60950-1

2 Applications

- Security Systems
- Chemical Production
- Factory Automation
- Motor and Motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

3 Description

The ISO15 is an isolated half-duplex differential line transceiver while the ISO35 is an isolated full-duplex differential line driver and receiver for TIA/EIA 485/422 applications. The ISO15M and ISO35M have extended ambient temperature ratings of –55°C to 125°C while the ISO15 and ISO35 are specified over –40°C to 85°C.

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical barrier of the device is tested to provide isolatlion of 4000 V_{PK} per VDE and 2500 V_{RMS} per UL and CSA between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

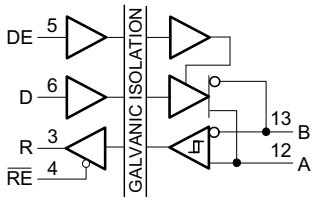
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO15	SOIC (16)	10.30 mm × 7.50 mm
ISO35		

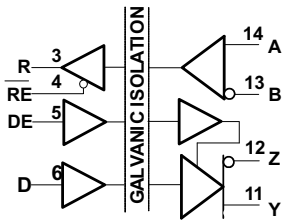
(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematics

ISO15x



ISO35x



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2012) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed VDE standard to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12. ... 1

Changes from Revision E (April 2010) to Revision F — **Page**

- Changed the FEATURES From: 4000-V_{peak} 560-V_{peak} V_{IORM} per IEC....Rev 2) To: 4000-V_{PK} V_{IOTM}, 560-$V_{PK}$$V_{IORM}$, IEC 60747-5-2 (VDE 0884, Rev 2) ... 1
- Changed Description From: The symmetrical isolation.....interface. To; The symmetrical isolation barrier of the device is tested to provide isolatlion of 4000 V_{PK} per VDE and 2500 V_{RMS} per UL and CSA between ....interface. ... 1
- Changed CTI From: ≥175 V To: ≥400 V ... 7
- Changed the Regulatory Information Table ... 7

Changes from Revision D (March 2009) to Revision E — **Page**

- Added devices ISO15M and ISO35M to the data sheet ... 1
- Changed Description - From: The ISO15 and ISO35 are qualified for use from –40°C to 85°C. To: The ISO15M and ISO35M have extended ambient temperature ratings of –55°C to 125°C while the ISO15 and ISO35 are specified over –40°C to 85°C ... 1
- Added Added Ambient Temp information in the RECOMMENDED OPERATING CONDITIONS table ... 5
- Added ISO15M and ISO35M to the Operating junction temperature in the RECOMMENDED OPERATING CONDITIONS table ... 5
- Changed the DRIVER ELECTRICAL table, I_{OZ} High-impedance state output current - Test Condition V_Y or V_Z = 12 V, V_{CC} = 0 values From: TYP = -10 , MAX = - To: TYP = -, MAX = 90. ... 6
- Changed the DRIVER ELECTRICAL table, I_{OZ} High-impedance state output current - Test Condition V_Y or V_Z = –7

Changes from Revision C (December 2008) to Revision D **Page**

- Changed Propagation delay values From: µs To: ns in the DRIVER SWITCHING table 7

Changes from Revision B (July 2008) to Revision C **Page**

- Added added IEC.....Approved 1
- Added added CSA information column back in table 7

Changes from Revision A (June 2008) to Revision B **Page**

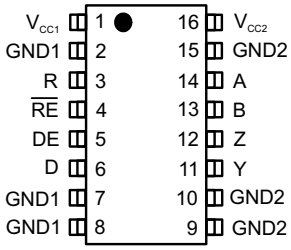
- Changed From: 4000-Vpeak Isolation To: 4000-Vpeak Isolation, 560-Vpeak VIORM UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2) 1
- Changed Figure 15, Full-Duplex Common-Mode Transient Immunity Test Circuit 12

Changes from Original (May 2008) to Revision A **Page**

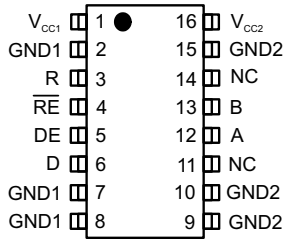
- Changed L(101) Minimum air gap (Clearance) From 7.7mm To 8.34mm. 7
- Changed From 40014131 To 40016131 7
- Deleted CSA information from the Regulatory Information Table. 7

6 Pin Configuration and Functions

ISO35x DW Package
16-Pin SOIC
Top View



ISO15x DW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO15x NO.	ISO35x NO.		
V_{CC1}	1	1	–	Logic side power supply
GND1	2,7,8	2,7,8	–	Logic side ground; internally connected
R	3	3	O	Receiver output
$\overline{RE}$	4	4	I	Receiver logic-low enable
DE	5	5	I	Driver logic-high enable input
D	6	6	I	Driver input
GND2	9,10,15	9,10,15	–	Bus side ground; internally connected
NC	11,14	–	–	Not connected internally; may be left floating
A	12	14	I/O	ISO15x: Noninverting bus input / output
			I	ISO35x: Noninverting bus input
B	13	13	I/O	ISO15x: Inverting bus input / output
			I	ISO35x: Inverting bus input
Y	–	11	O	Noninverting bus output
Z	–	12	O	Inverting bus output
V_{CC2}	16	16	–	Bus side power supply

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MAX	MAX	UNIT
V_{CC}	Input supply voltage. (2) V_{CC1}, V_{CC2}	–0.3	6	V
V_O	Voltage at any bus I/O terminal	–9	14	V
V_{IT}	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 13)	–50	50	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND1	±6000	V
			Bus pins and GND2	±16000	
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±1000	
		Machine model ANSI/ESDS5.2-1996		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage, V_{CC1}, V_{CC2}		3.15	3.3	3.6	V
V_{OC}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
R_L	Differential input resistance		54	60		Ω
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
$1/t_{UI}$	Signaling rate	ISO15x and ISO35x			1	Mbps
T_A	Ambient temperature	ISO15 and ISO35	–40	25	85	°C
		ISO15M and ISO35M	–55	25	125	
T_J	Operating junction temperature	ISO15 and ISO35	–40		150	°C
		ISO15M and ISO35M	–55		150	

7.4 Thermal Information

THERMAL METRIC[1]			ISO15, ISO35 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K board	79.6	°C/W
		Low-K board	168	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.7	
$R_{\theta JB}$	Junction-to-board thermal resistance		44.6	
ψ_{JT}	Junction-to-top characterization parameter		11.8	
ψ_{JB}	Junction-to-board characterization parameter		44	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Dissipation Ratings

			VALUE	UNIT
P_D	Device Power Dissipation	$V_{CC1} = V_{CC2} = 3.6$ V, $T_J = 150°C$, $C_L = 15$ pF, Input a 0.5 MHz 50% duty cycle square wave	220	mW

7.6 Supply Current

over recommended operating condition (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Logic-side supply current	ISO35x and ISO15x	$\overline{RE}$ at 0 V or V_{CC}, DE at 0 V, No load (driver disabled)			8	mA
			$\overline{RE}$ at 0 V or V_{CC}, DE at V_{CC}, No Load (driver enabled)			8	
I_{CC2}	Bus-side supply current	ISO35x and ISO15x	$\overline{RE}$ at 0 V or V_{CC}, DE at 0 V, No load (driver disabled)			15	mA
			$\overline{RE}$ at 0 V or V_{CC}, DE at V_{CC}, No Load (driver enabled)			19	

7.7 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage magnitude	$I_O = 0$ mA, no load			2.5		V_{CC}	V
		$R_L = 54\ \Omega$, See Figure 3			1.5	2		
		$R_L = 100\ \Omega$ (RS-422), See Figure 3			2	2.3		
		V_{test} from –7 V to +12 V, See Figure 4			1.5			
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of the differential output voltage	See Figure 3 and Figure 4			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 5			1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.1		0.1	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 5				0.5		V
I_I	Input current	D, DE, V_I at 0 V or V_{CC1}			–10		10	µA
I_{OZ}	High-impedance state output current	ISO15	See receiver input current					µA
		ISO35	V_Y or V_Z = 12 V	Other input at 0 V			90	
			V_Y or V_Z = 12 V, V_{CC} = 0				90	
			V_Y or V_Z = –7 V		–10			
			V_Y or V_Z = –7 V, V_{CC} = 0		-10			
I_{OS}	Short-circuit output current	V_A or V_B at –7 V		Other input at 0 V	–250		250	mA
		V_A or V_B at 12 V						
C_{OD}	Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V				16		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 14 and Figure 15			25	50		kV/µs

7.8 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage		I_O = –8 mA				–20	mV
$V_{IT(–)}$	Negative-going input threshold voltage		I_O = 8 mA		–200			mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					50		mV
V_O	Output voltage		V_{ID} = 200 mV, See Figure 9	I_O = –8 mA	2.4			V
				I_O = 8 mA			0.4	
I_{OZ}	High-impedance state output current		V_I = –7 to 12 V, Other input = 0 V		–1		1	µA
I_A or I_B	Bus input current	-55°C ≤ T_A ≤ 85°C	V_A or V_B = 12 V	Other input at 0 V		50	100	µA
			V_A or V_B = 12 V, V_{CC} = 0			50	100	
		85°C ≤ T_A ≤ 125°C	V_A or V_B = 12 V				200	
			V_A or V_B = 12 V, V_{CC} = 0				200	
		-55°C ≤ T_A ≤ 125°C	V_A or V_B = –7 V		–100	–40		
			V_A or V_B = –7 V, V_{CC} = 0		–100	–30		
I_{IH}	High-level input current, $\overline{RE}$		V_{IH} = 2 V		–10			µA
I_{IL}	Low-level input current, $\overline{RE}$		V_{IL} = 0.8 V		–10			µA
R_{ID}	Differential input resistance		A, B		48			kΩ
C_{ID}	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5V, DE at 0 V			16		pF

7.9 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay		See Figure 6			340	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} – t_{PLH} \rvert$)				6		
t_r, t_f	Differential output signal rise time, fall time	ISO15 and ISO35		120	180	300	
		ISO15M and ISO35M		120	180	350	
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 7			205	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output					530	
t_{PLZ}	Propagation delay, low-level to high-impedance output		See Figure 8			330	ns
t_{PZL}	Propagation delay, standby-to-low-level output					530	

7.10 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO15x and ISO35x	See Figure 10			100	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} – t_{PLH} \rvert$)	ISO15 and ISO35				13	
		ISO15M and ISO35M				18	
t_r, t_f	Output signal rise and fall time	ISO15 and ISO35			2	4	
		ISO15M and ISO35M			2	6	
t_{PZH}, t_{PZL}	Propagation delay, high-impedance-to-high-level output Propagation delay, high-impedance-to-low-level output		DE at 0 V, See Figure 11 and Figure 12		13	25	ns
t_{PHZ}, t_{PLZ}	Propagation delay, high-level-to-high-impedance output Propagation delay, low-level to high-impedance output				13	25	

7.11 Typical Characteristics

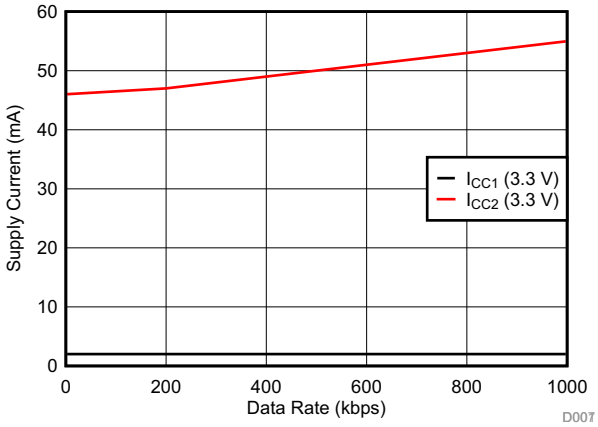


Figure 1. ISOx5 Supply Current vs Data Rate With Load

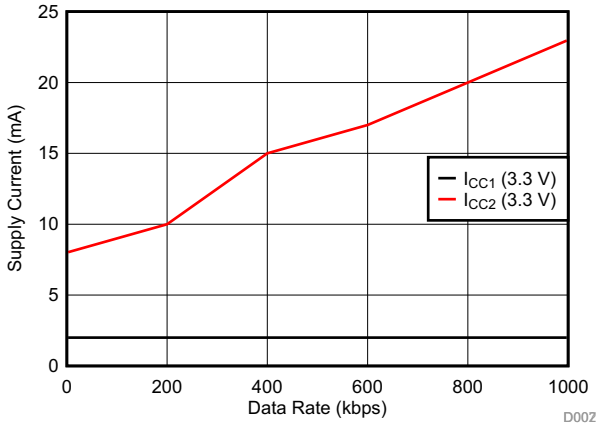


Figure 2. ISOx5 Supply Current vs Data Rate With No Load

8 Parameter Measurement Information

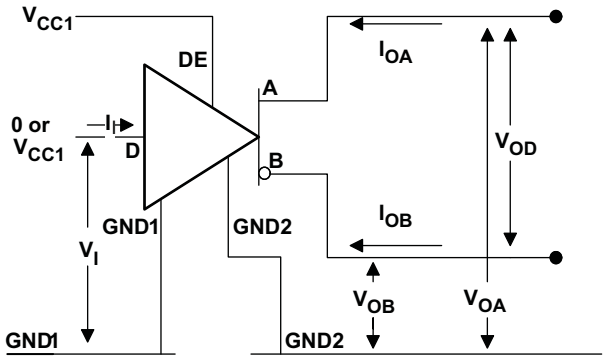


Figure 3. Driver V_{OD} Test and Current Definitions

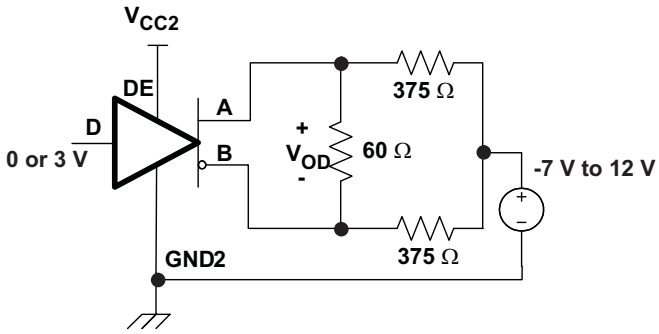
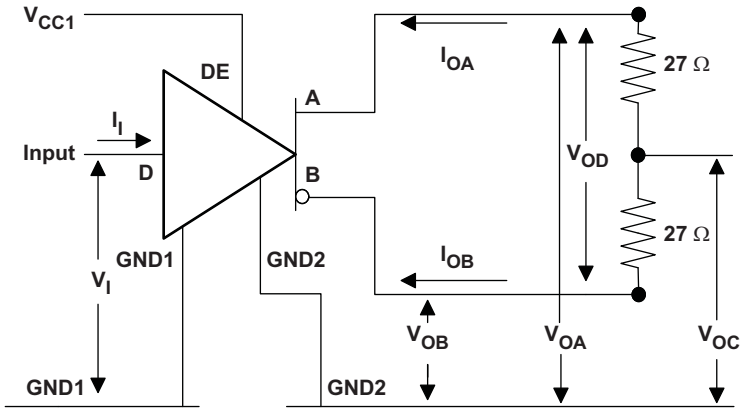


Figure 4. Driver V_{OD} With Common-Mode Loading Test Circuit



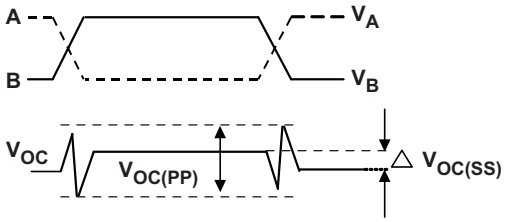
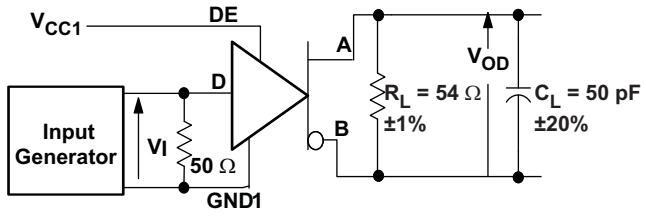
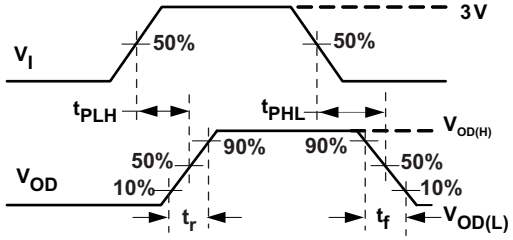


Figure 5. Test Circuit and Waveform Definitions for the Driver Common-Mode Output Voltage





Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50 Ω

C_L includes fixture and Instrumentation Capacitance

Figure 6. Driver Switching Test Circuit and Voltage Waveforms

NOTE

Driver output pins are A and B for the ISO15 (see Figure 3 through Figure 6). These correspond to ISO35 pins Y and Z

Parameter Measurement Information (continued)

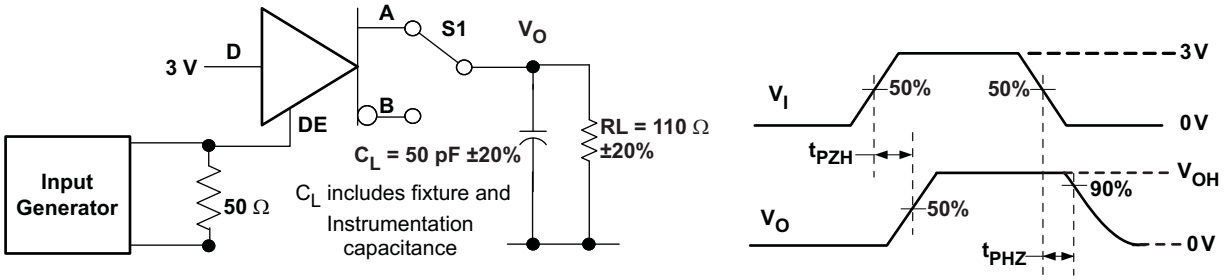
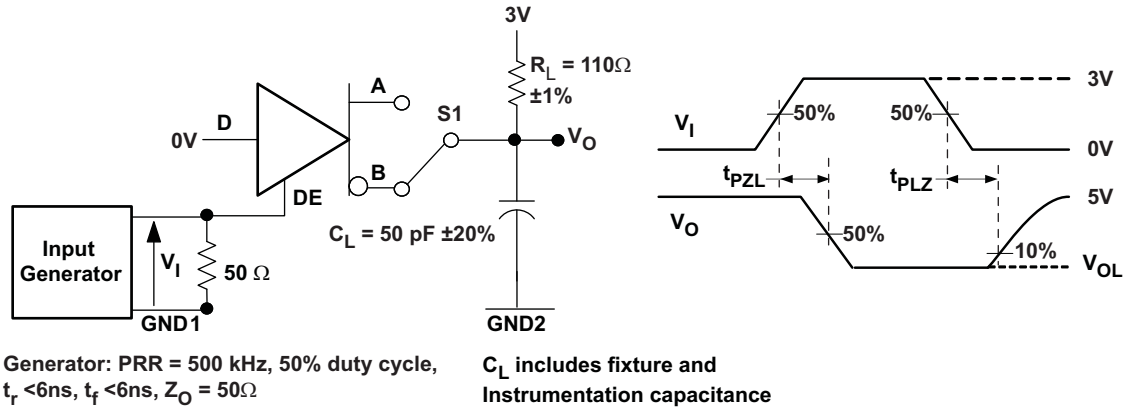


Figure 7. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50Ω

C_L includes fixture and Instrumentation capacitance

Figure 8. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

NOTE

Driver output pins are A and B for the ISO15 (see Figure 7 through Figure 8). These correspond to ISO35 pins Y and Z

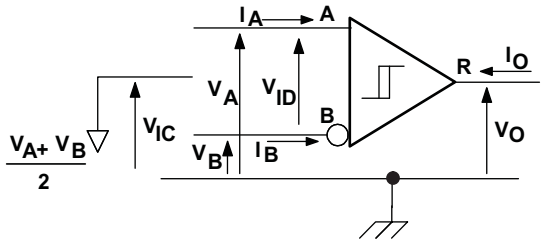
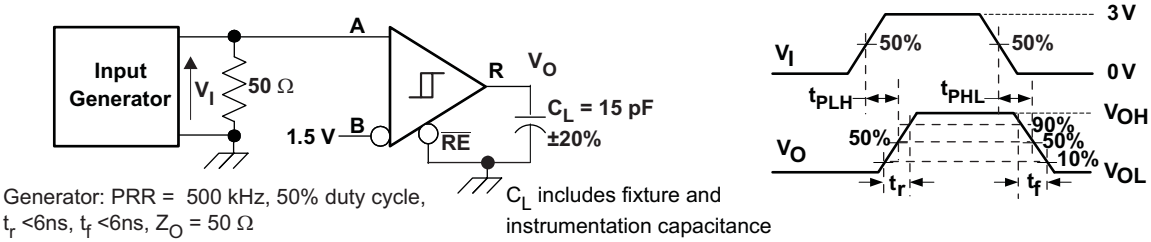


Figure 9. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50 Ω

C_L includes fixture and instrumentation capacitance

Figure 10. Receiver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

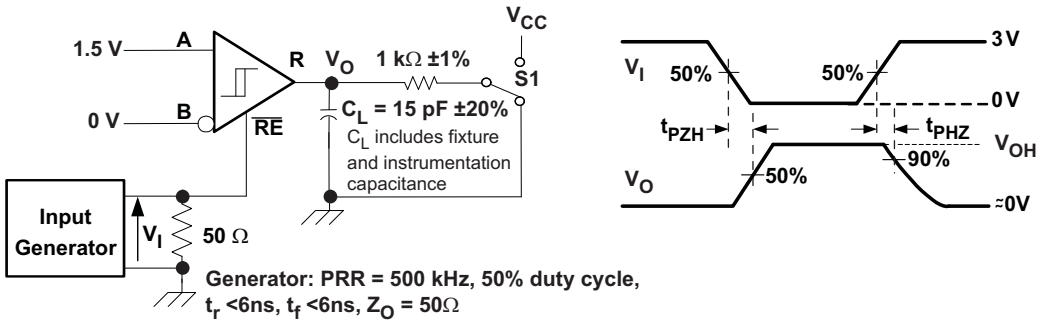


Figure 11. Receiver Enable Test Circuit and Waveforms, Data Output High

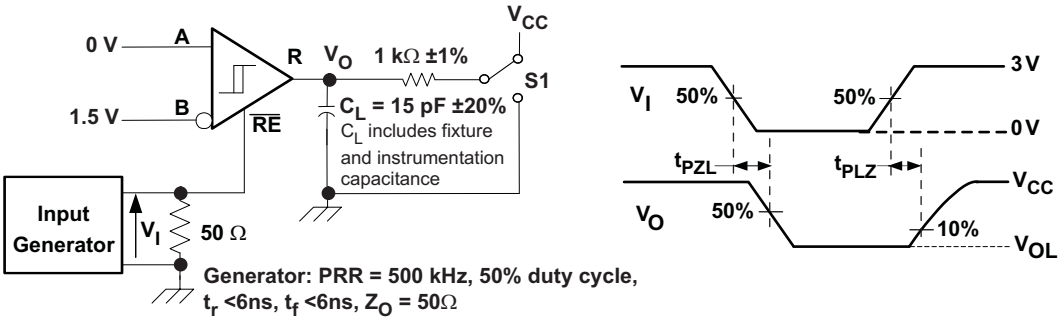
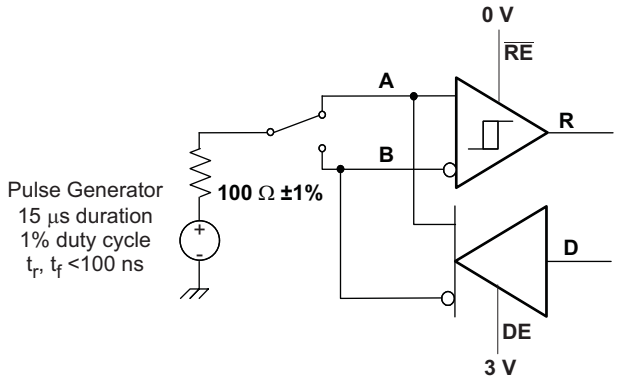


Figure 12. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 13. Transient Overvoltage Test Circuit

Parameter Measurement Information (continued)

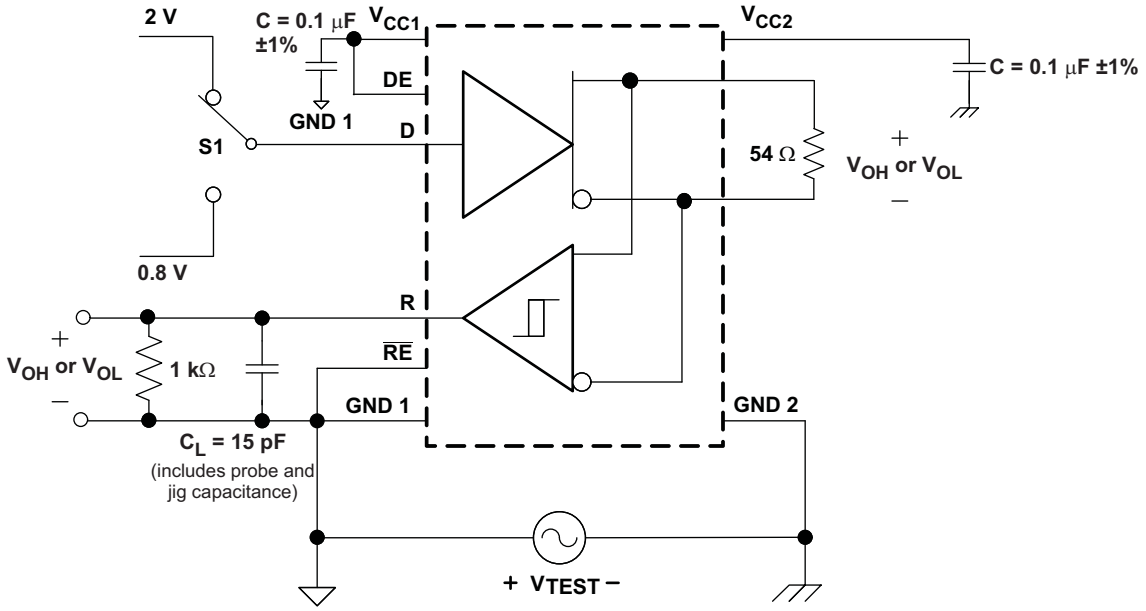


Figure 14. Half-Duplex Common-Mode Transient Immunity Test Circuit

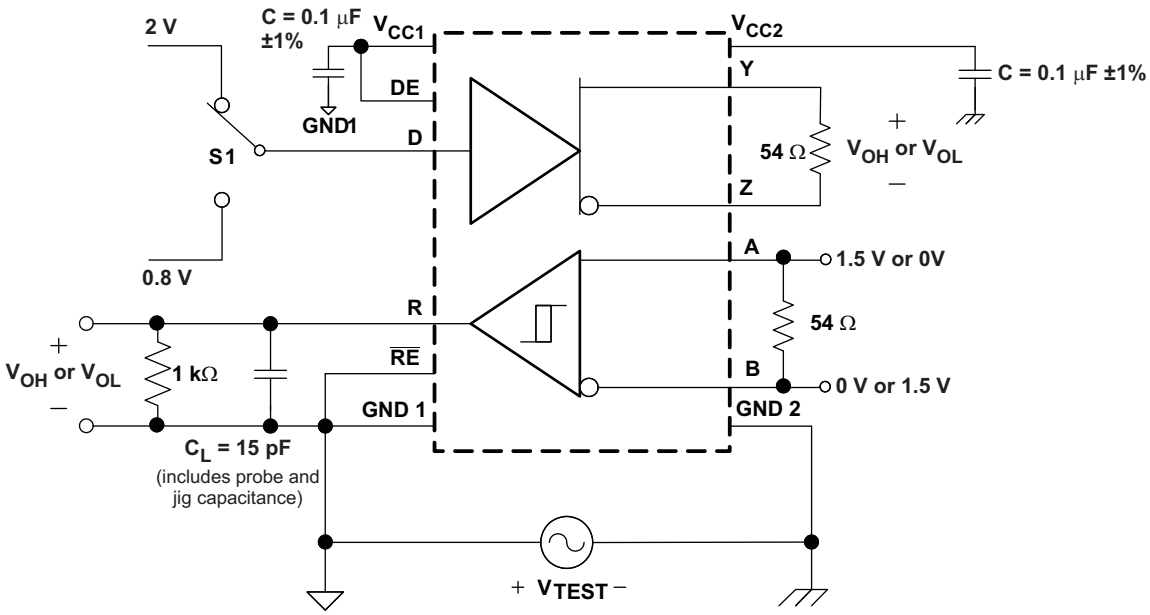


Figure 15. Full-Duplex Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

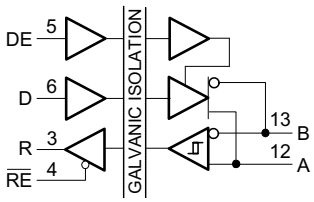
The ISO15 and ISO15M are isolated half-duplex differential line drivers and receivers while the ISO35 and ISO35M are isolated full-duplex differential line transceivers for TIA/EIA 485/422 applications. They are rated to provide galvanic isolation of up to 2500 V_{rms} for 60 sec as per the standard. They have active-high driver enables and active-low receiver enables to control the data flow.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

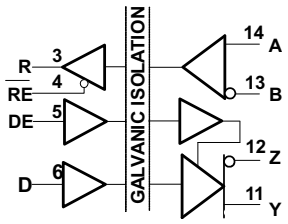
When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

9.2 Functional Block Diagrams

ISO15x



ISO35x



9.3 Feature Description

9.3.1 Insulation and Safety-Related Package Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)(1)	Shortest terminal to terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
DTI	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, T_A = 25°C, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input to output	VI = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	VI = 0.4 sin (4E6πt)		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

9.3.2 DIN V VDE V 0884-10 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOTM}	Transient overvoltage	Method a, t = 60 s, Qualification test	4000	V_{PK}
V_{IORM}	Maximum working insulation voltage		560	V_{PK}
V_{PR}	Input to output test voltage	Method b1, V_{PR} = V_{IORM} × 1.875, 100% Production test with t = 1 s, Partial discharge < 5 pC	1050	V_{PK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(2) Climatic Classification 40/125/21

9.3.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III
	Rated mains voltage ≤ 400 V_{RMS}	I-II

9.3.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Approved under CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program(1)
Basic insulation, 4000 V_{PK} Maximum transient overvoltage, 560 V_{PK} Maximum working voltage	2500 V_{RMS} Isolation rating, 396 V_{PK} Basic working voltage per CSA 60950-1-07 and IEC 60950-1 (2nd Ed)	Single Protection, 2500 V_{RMS}
Certificate number: 40016131	Master contract number: 220991	File number: E181974

(1) Production tested ≥3000 V_{RMS} for 1 second in accordance with UL 1577.

9.3.5 Safety-Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER				MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 168 °C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			240	mA
T_S	Maximum case temperature	DW-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in *Thermal Information* is that of a device installed in a Low-Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

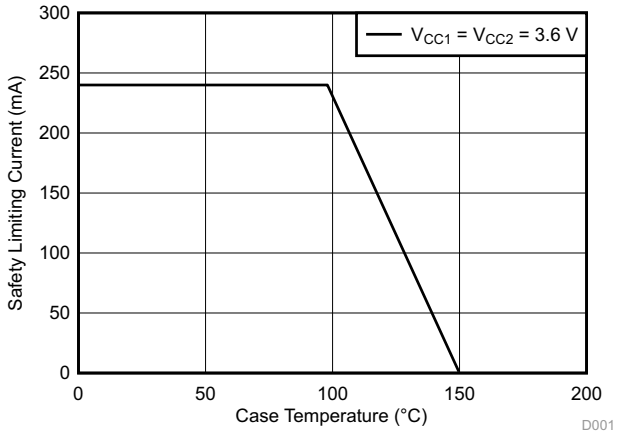


Figure 16. DW-16 θ_{JC} Thermal Derating Curve per VDE

9.4 Device Functional Modes

Table 1. Driver Function Table(1)

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS(2)	
				Y / A	Z / B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Hi-Z	Hi-Z
PU	PU	X	OPEN	Hi-Z	Hi-Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z
PD	PD	X	X	Hi-Z	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (off)
(2) Driver output pins are Y and Z for full-duplex devices and A & B for half-duplex devices.

Table 2. Receiver Function Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$-0.01\ V \le V_{ID}$	L	H
PU	PU	$-0.2\ V < V_{ID} < -0.01\ V$	L	?
PU	PU	$V_{ID} \le -0.2\ V$	L	L
PU	PU	X	H	Hi-Z
PU	PU	X	OPEN	Hi-Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (off), ? = Indeterminate

9.4.1 Device I/O Schematics

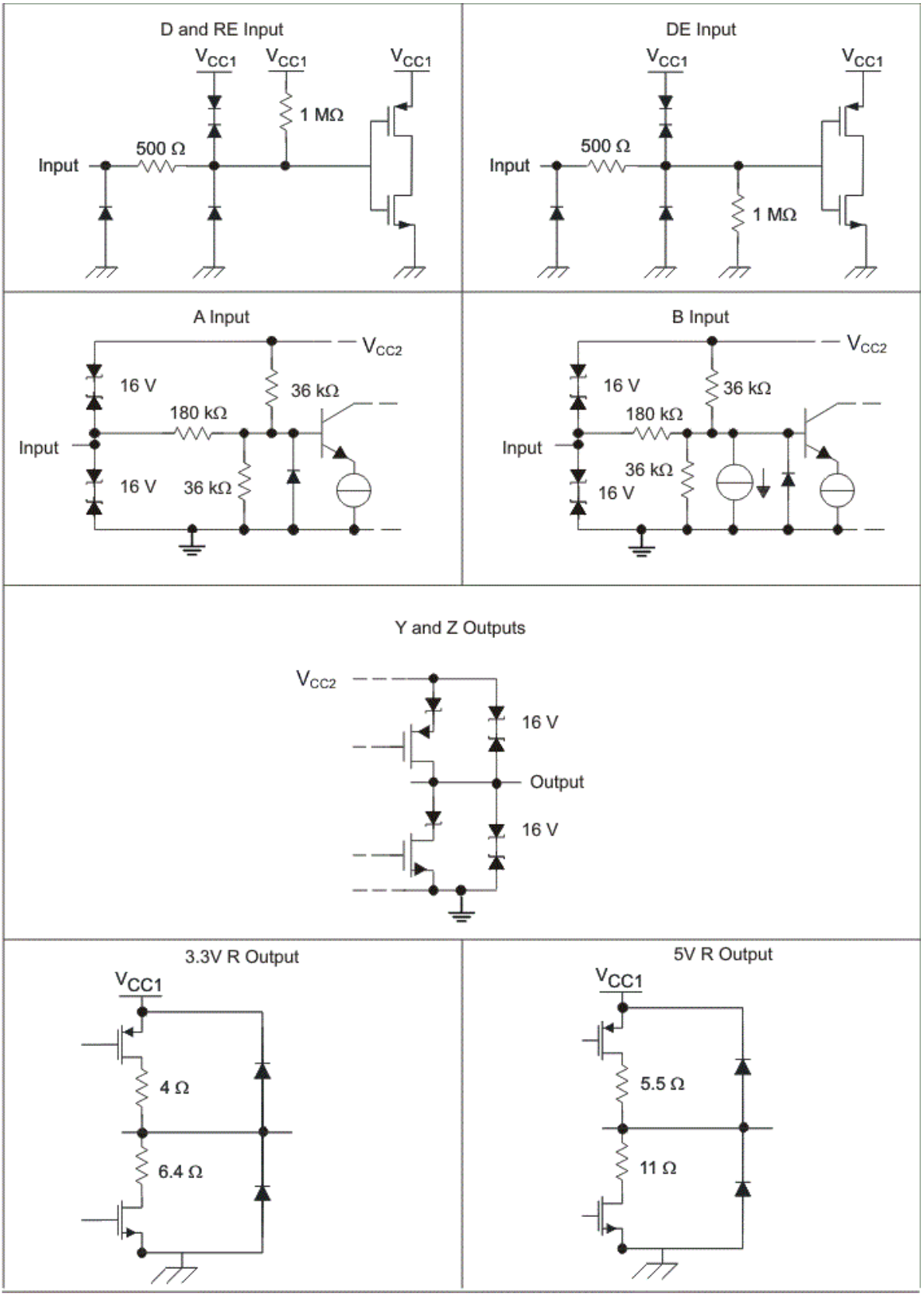


Figure 17. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO15x and ISO35x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission there is only one pair which shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

10.2 Typical Application

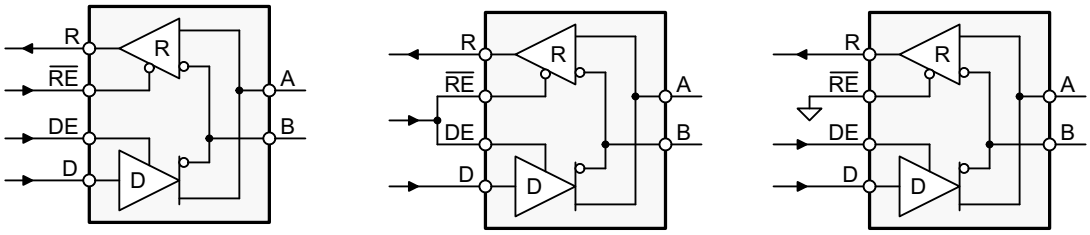


Figure 18. Half-Duplex Transceiver Configurations

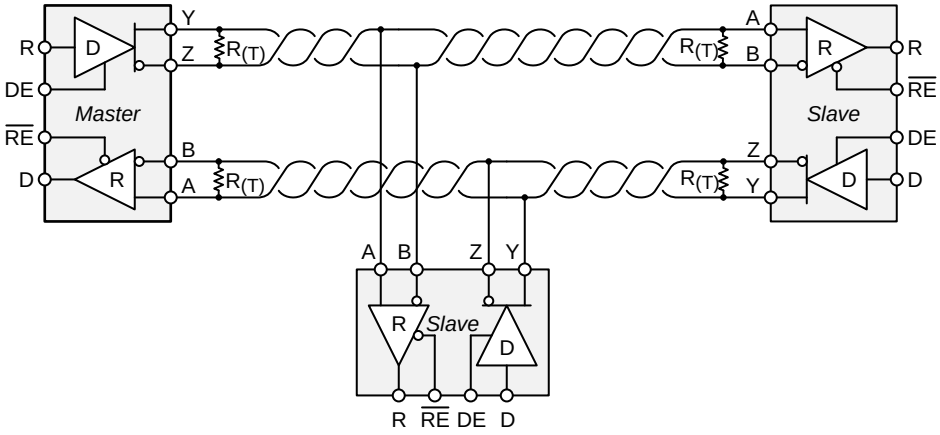


Figure 19. Typical RS-485 Network With Full-Duplex Transceivers

Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Table 3. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

10.2.2 Detailed Design Procedure

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver. The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because these devices consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

10.2.3 Application Curve

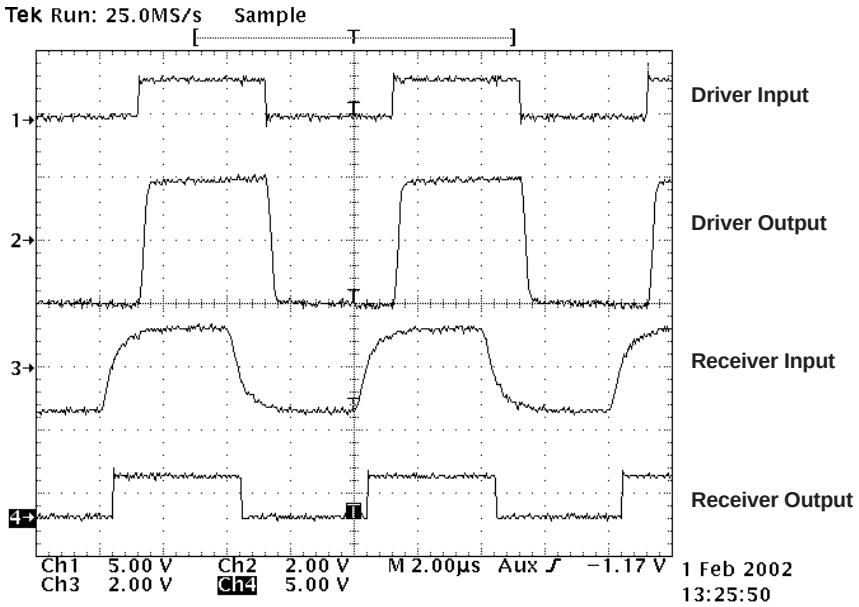


Figure 20. Typical Input and Output Waveforms

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 . For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

12 Layout

12.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, highfrequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 21).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating the board.
- Use VCC and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC-pins of transceiver, UART, controller ICs on the board (see Figure 21).
- Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see Figure 21).
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in theses lines during transient events (see Figure 21).
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see Figure 21).
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Layout Guidelines (continued)

NOTE

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

12.2 Layout Example

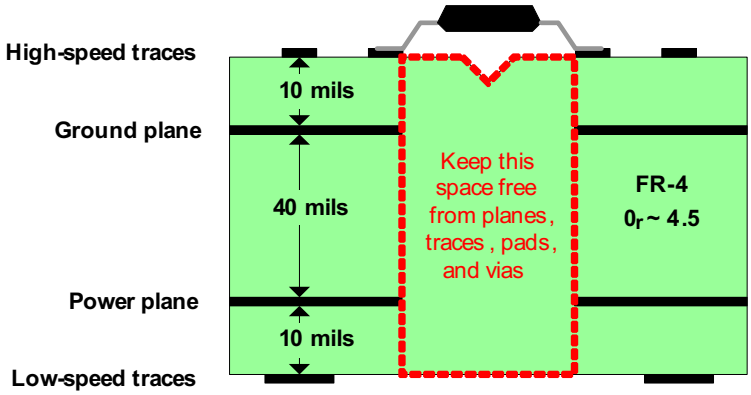


Figure 21. Recommended Layer Stack

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*, SLLSEA0
- *Transformer Driver for Isolated Power Supplies*, SLLA284

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO15	Click here	Click here	Click here	Click here	Click here
ISO35	Click here	Click here	Click here	Click here	Click here
ISO15M	Click here	Click here	Click here	Click here	Click here
ISO35M	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

SLLA353 -- *Isolation Glossary.*

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO15DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	Samples
ISO15DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	Samples
ISO15DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	Samples
ISO15MDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO15M	Samples
ISO15MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO15M	Samples
ISO35DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	Samples
ISO35DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	Samples
ISO35DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	Samples
ISO35MDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO35M	Samples
ISO35MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO35M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

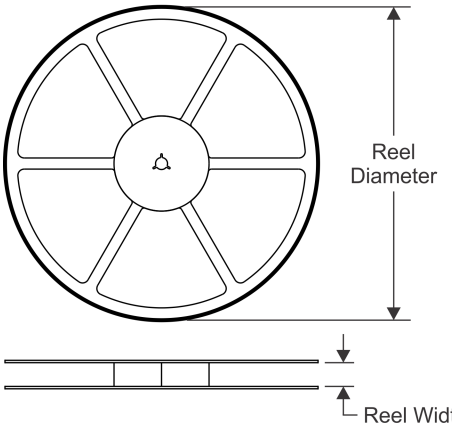
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

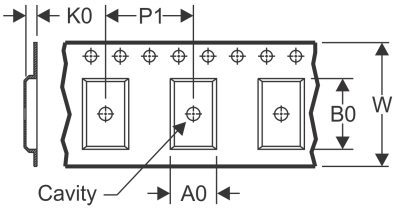
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

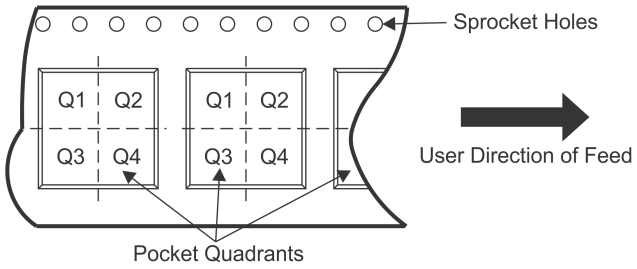


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

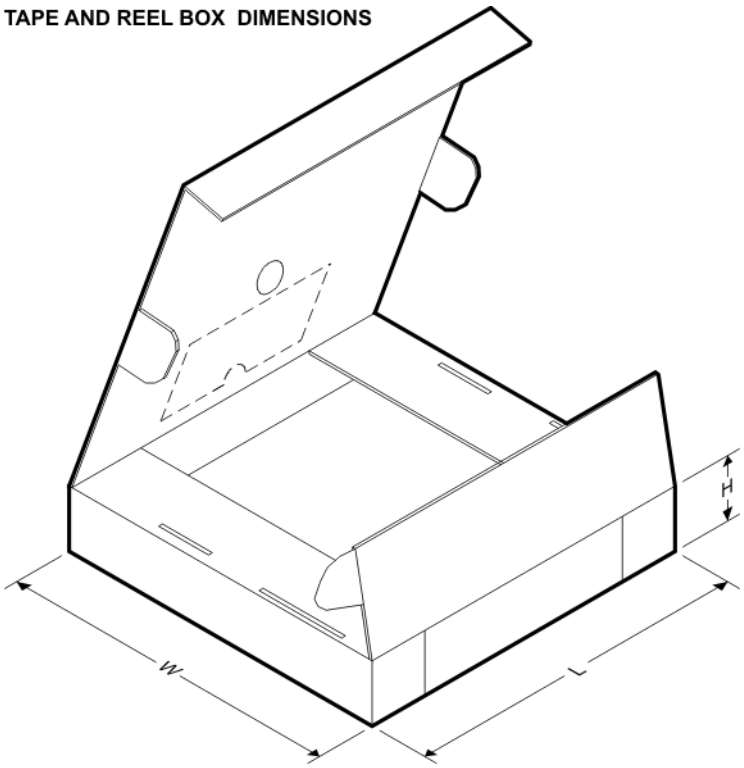
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO15DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO15MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

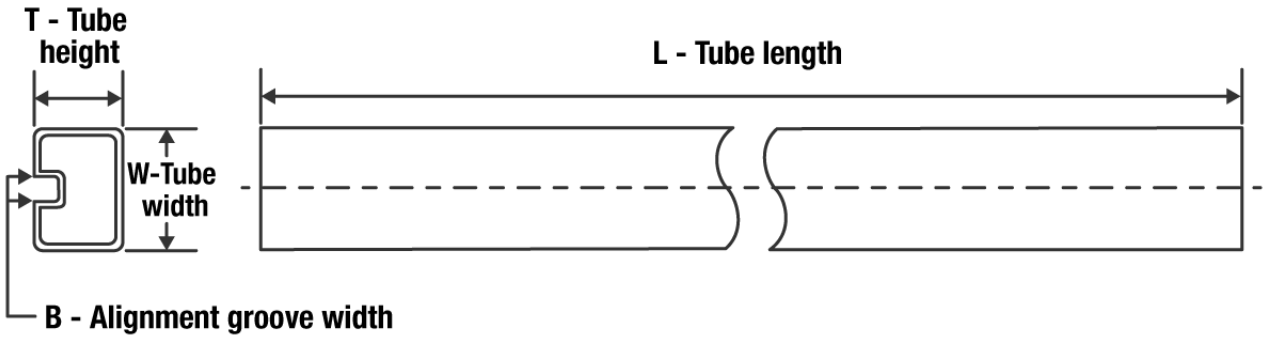
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO15DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO15MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO35DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO35MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO15DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO15DWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO15MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO35DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO35DWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO35MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

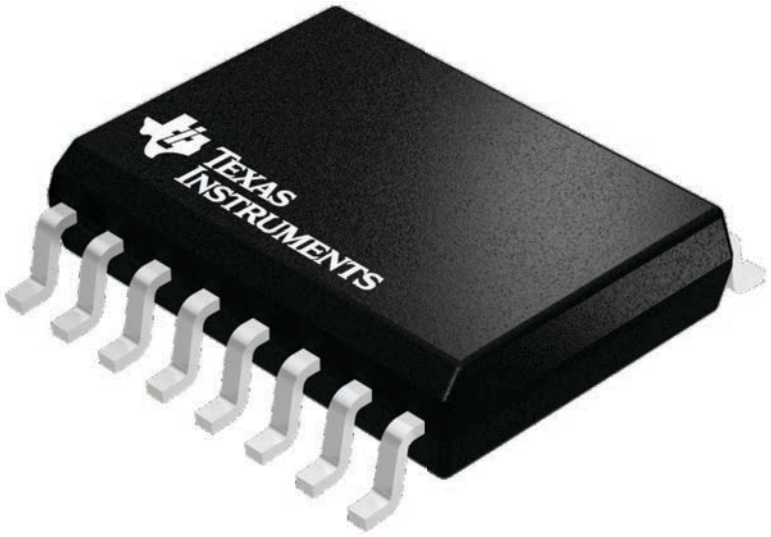
DW 16

SOIC - 2.65 mm max height

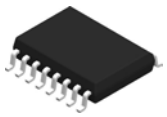
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

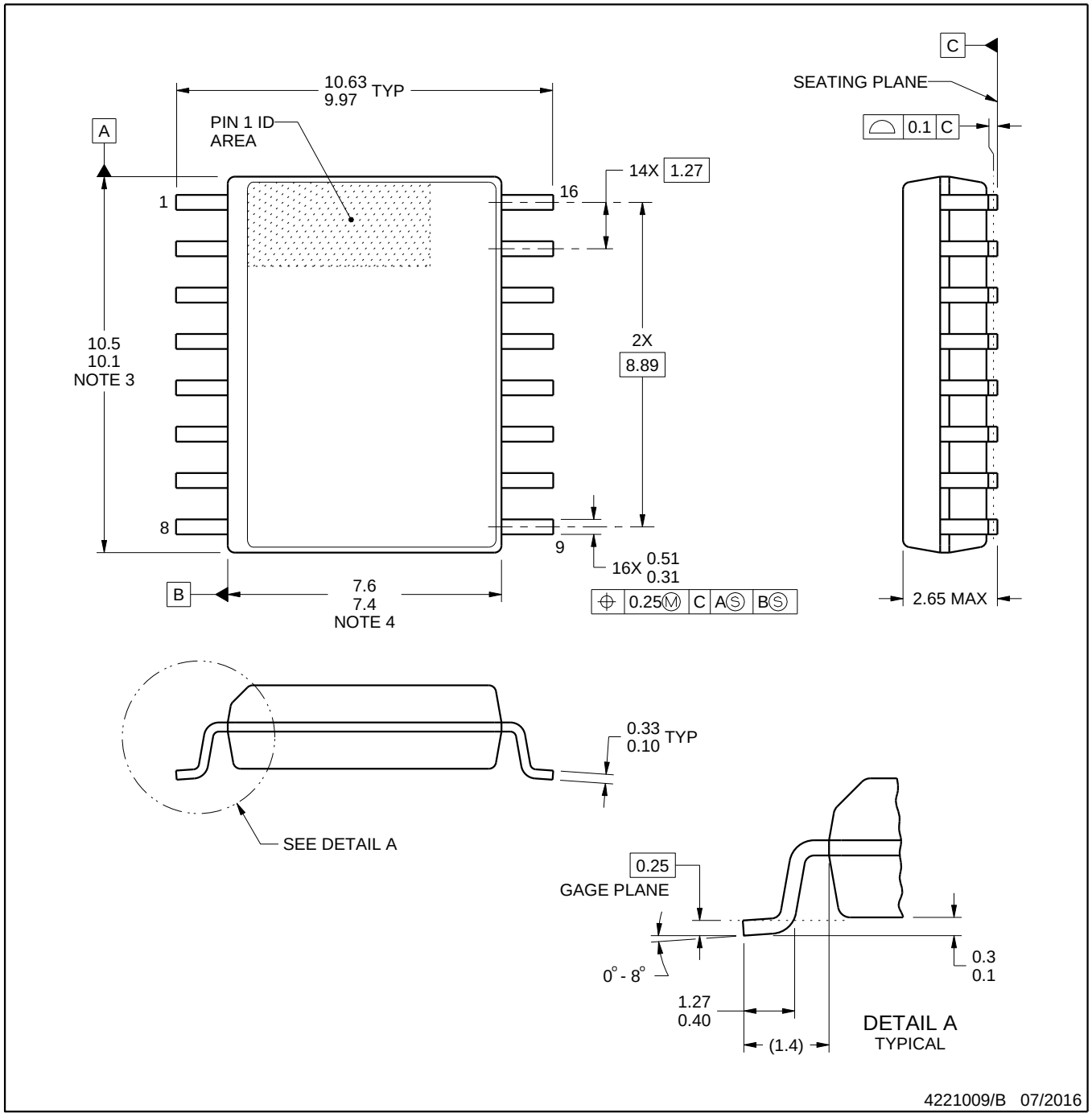


PACKAGE OUTLINE

DW0016B

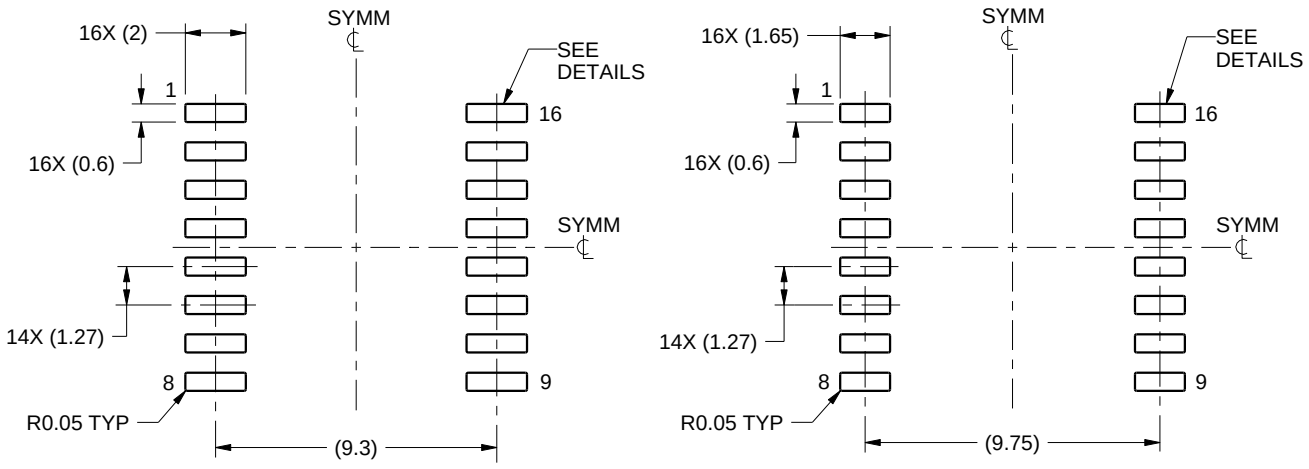
SOIC - 2.65 mm max height

SOIC



NOTES:

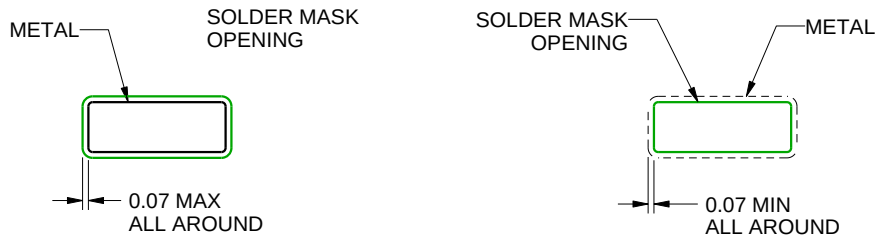
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

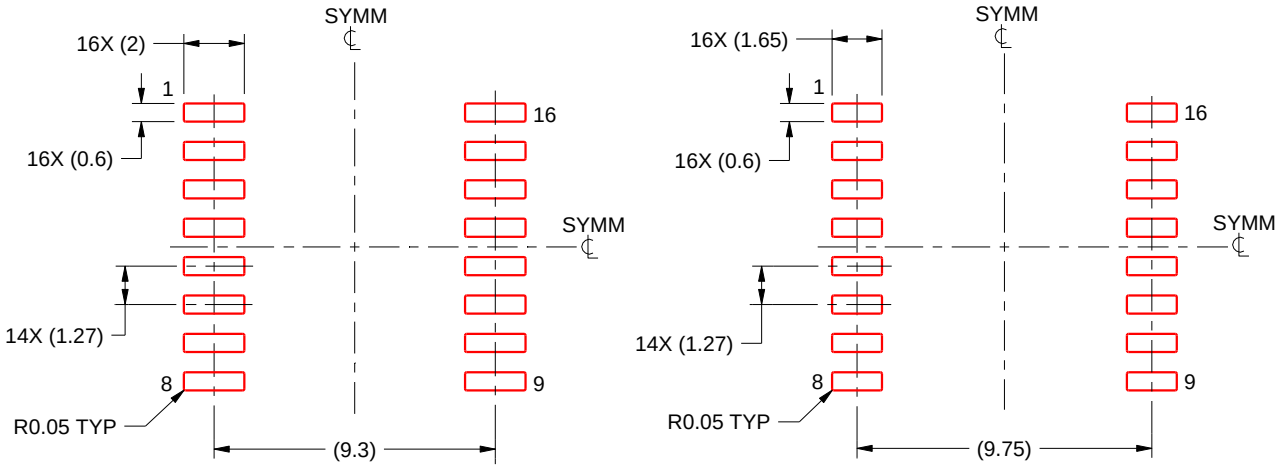
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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