

INA154

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High-Speed, Precision DIFFERENCE AMPLIFIER (G = 1)

FEATURES

- DESIGNED FOR LOW COST
- LOW OFFSET VOLTAGE: $\pm 750\mu\text{V}$ max
- LOW OFFSET DRIFT: $\pm 2\mu\text{V}/^\circ\text{C}$
- LOW GAIN ERROR: $\pm 0.05\%$ max
- WIDE BANDWIDTH: 3MHz
- HIGH SLEW RATE: $14\text{V}/\mu\text{s}$
- FAST SETTLING TIME: $3\mu\text{s}$ to 0.01%
- WIDE SUPPLY RANGE: $\pm 4\text{V}$ to $\pm 18\text{V}$
- LOW QUIESCENT CURRENT: 2.4mA
- SO-8 SURFACE-MOUNT PACKAGE

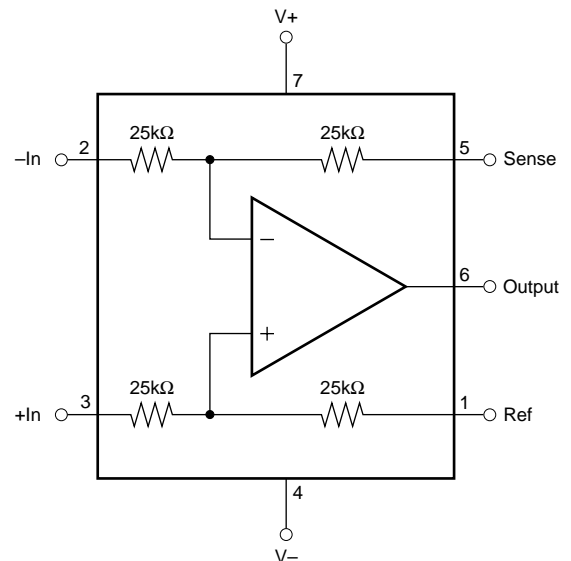
APPLICATIONS

- DIFFERENTIAL INPUT AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- SUMMING AMPLIFIER
- DIFFERENTIAL CURRENT RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- SYNCHRONOUS DEMODULATOR

DESCRIPTION

The INA154 is a high slew rate, unity-gain difference amplifier consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on $\pm 4\text{V}$ to $\pm 18\text{V}$ supplies.

The difference amplifier is the foundation of many commonly used circuits. The INA154 provides this circuit function without using an expensive precision resistor network. The INA154 is available in a SO-8 surface-mount package and is specified for operation over the extended industrial temperature range, -40°C to $+85^\circ\text{C}$.



SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = +25^\circ C$, $V_S = \pm 15V$, $R_L = 2k\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.

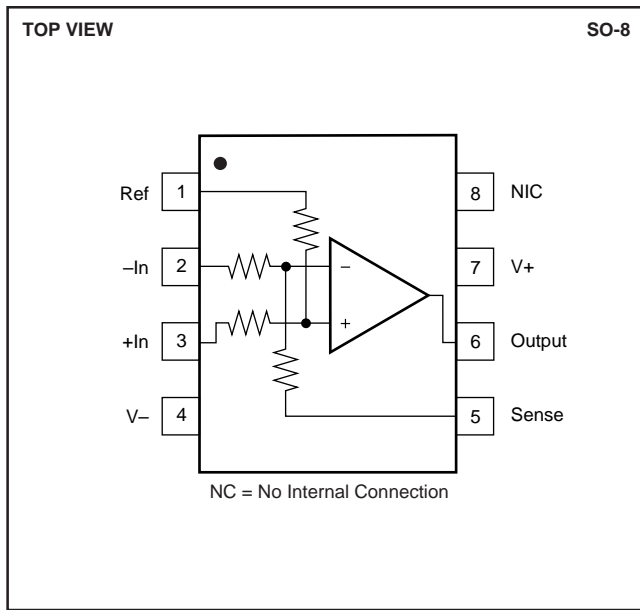
PARAMETER	CONDITIONS	INA154U			INA154UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾	RTO							
Initial			± 100	± 750		*	± 1500	μV
vs Temperature			± 2	± 20		*	*	$\mu V/^\circ C$
vs Power Supply	$V_S = \pm 4V$ to $\pm 18V$		± 5	± 60		*	*	$\mu V/V$
vs Time			0.5			*		$\mu V/mo$
INPUT IMPEDANCE⁽²⁾								
Differential			50			*		k Ω
Common-Mode			50			*		k Ω
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range								
Positive	$V_O = 0V$	$2(V+) - 5$	$2(V+) - 4$		*	*		V
Negative	$V_O = 0V$	$2(V-) + 5$	$2(V-) + 2$		*	*		V
Common-Mode Rejection Ratio	$V_{CM} = -25V$ to $25V$, $R_S = 0\Omega$	80	90		74	*		dB
OUTPUT VOLTAGE NOISE⁽³⁾	RTO							
$f = 0.1Hz$ to $10Hz$			2.6			*		$\mu Vp-p$
$f = 1kHz$			52			*		nV/\sqrt{Hz}
GAIN								
Initial			1			*		V/V
Error	$V_O = -13V$ to $+13V$		± 0.02	± 0.05		*	± 0.1	%
vs Temperature			± 1	± 10		*	*	$ppm/^\circ C$
Nonlinearity	$V_O = -13V$ to $+13V$		± 0.0001	± 0.001		*	± 0.002	% of FS
OUTPUT								
Voltage, Positive		$(V+) - 2$	$(V+) - 1.8$		*	*		V
Negative		$(V-) + 2$	$(V-) + 1.6$		*	*		V
Current Limit, Continuous to Common			± 60			*		mA
Capacitive Load (stable operation)			500			*		pF
FREQUENCY RESPONSE								
Small-Signal Bandwidth	-3dB		3.1			*		MHz
Slew Rate			14			*		V/ μs
Settling Time: 0.1%	10V Step, $C_L = 100pF$		2			*		μs
0.01%	10V Step, $C_L = 100pF$		3			*		μs
Overload Recovery Time	50% Overdrive		3			*		μs
POWER SUPPLY								
Rated Voltage			± 15			*		V
Operating Voltage Range		± 4		± 18	*		*	V
Quiescent Current	$I_O = 0mA$		± 2.4	± 2.9		*	*	mA
TEMPERATURE RANGE								
Specified		-40		+85	*		*	$^\circ C$
Operation		-55		+125	*		*	$^\circ C$
Storage		-55		+125	*		*	$^\circ C$
Thermal Resistance, θ_{JA}								
SO-8 Surface-Mount			150			*		$^\circ C/W$

*Specifications the same as INA154U.

NOTES: (1) Includes effects of amplifier's input bias and offset currents. (2) 25k Ω resistors are ratio matched but have $\pm 20\%$ absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	40V
Input Voltage Range	±80V
Output Short Circuit (to ground)	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

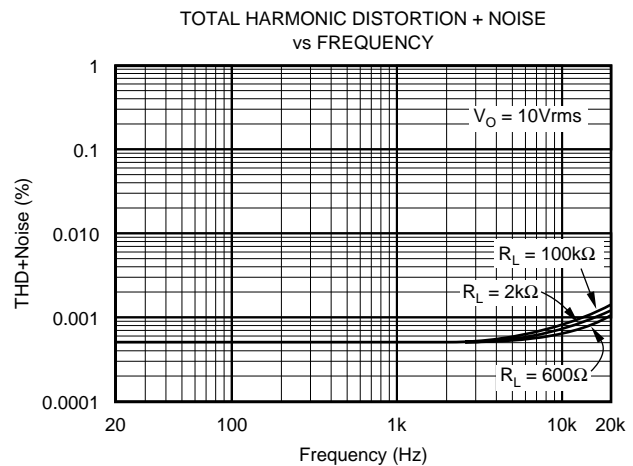
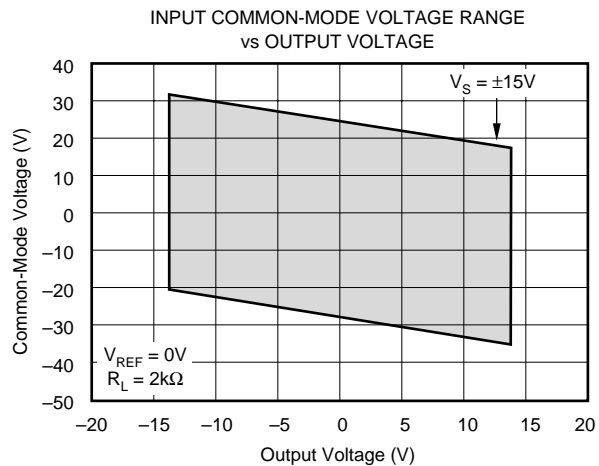
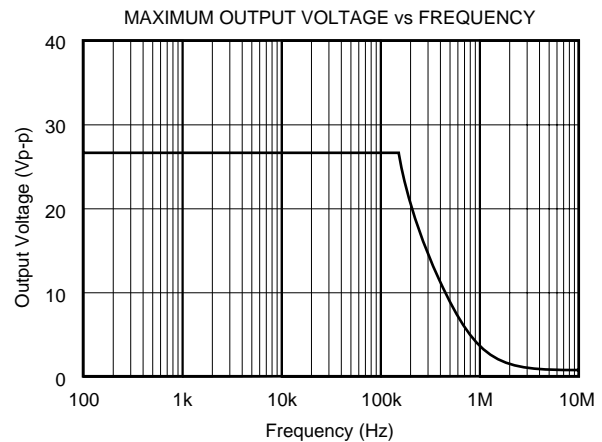
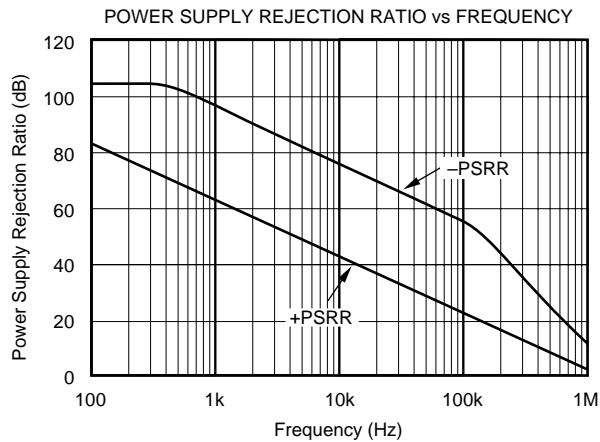
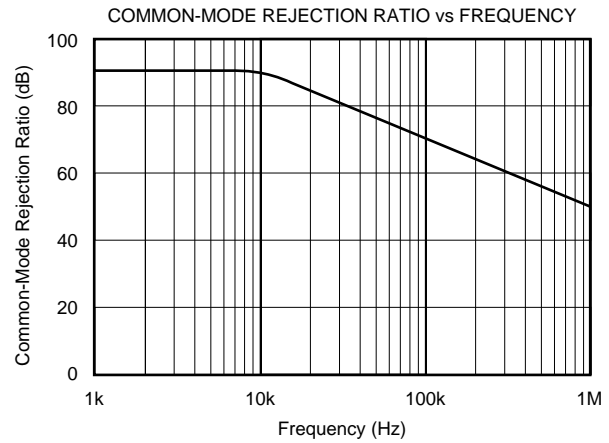
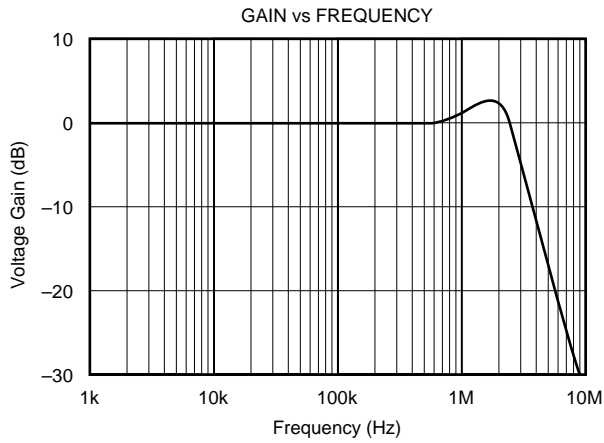
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
INA154U	SO-8 Surface-Mount	182	-40°C to +85°C	INA154U	INA154U	Rails
"	"	"	"	"	INA154U/2K5	Tape and Reel
INA154UA	SO-8 Surface-Mount	182	-40°C to +85°C	INA154UA	INA154UA	Rails
"	"	"	"	"	INA154UA/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA154U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

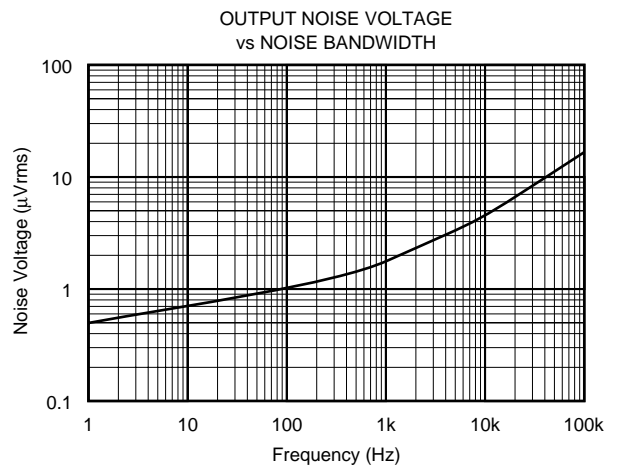
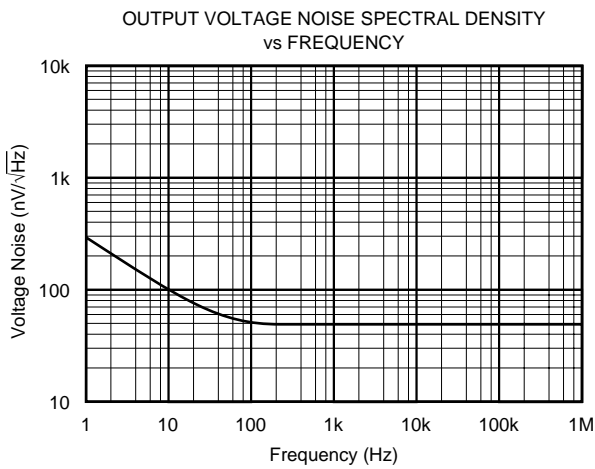
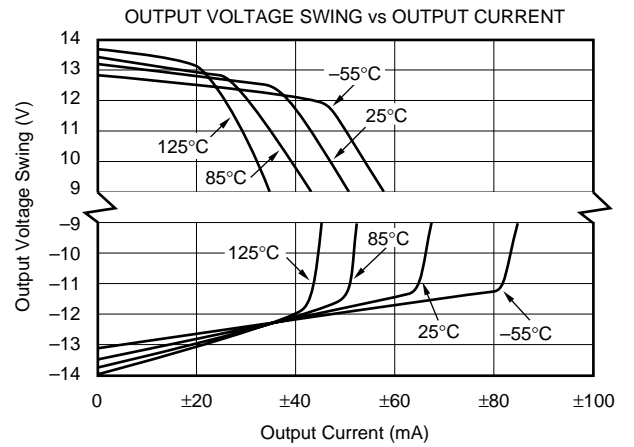
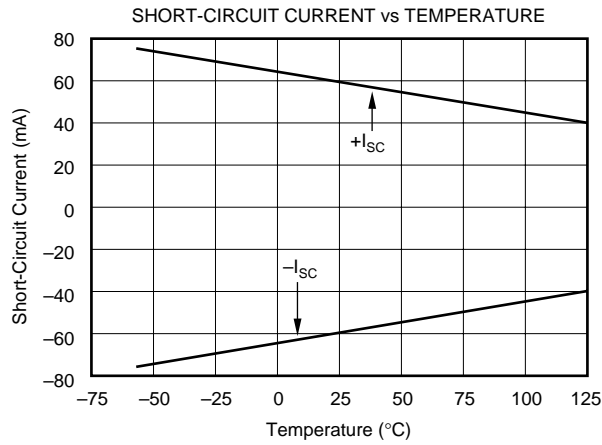
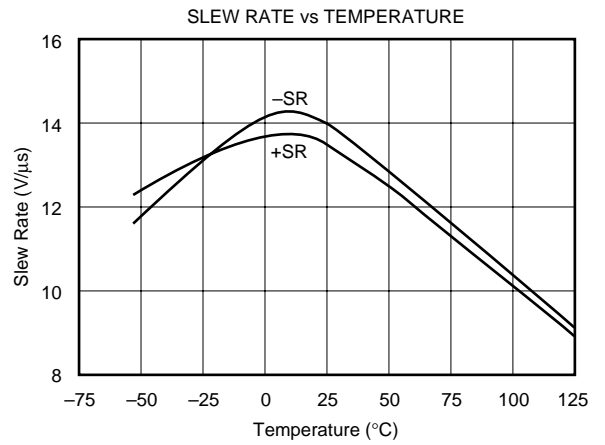
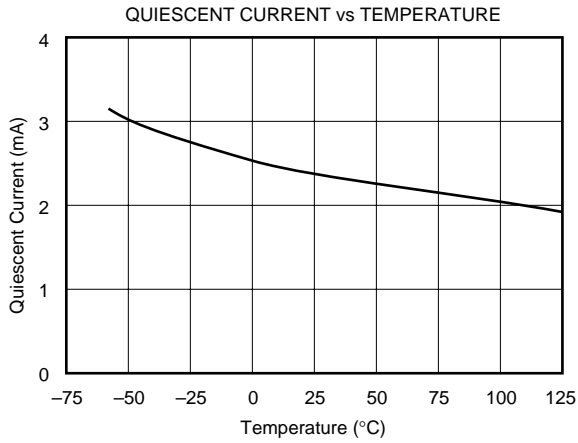
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$, unless otherwise noted.



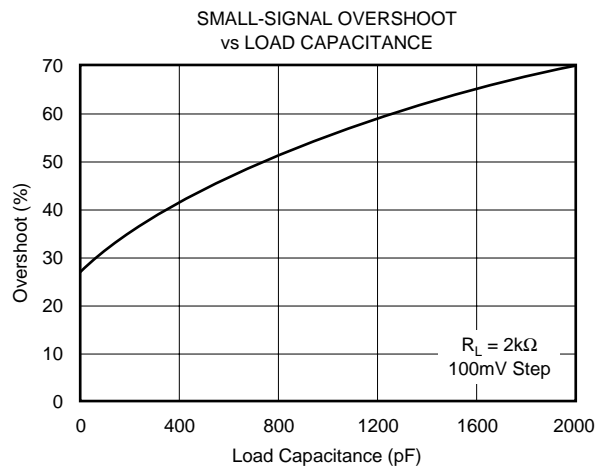
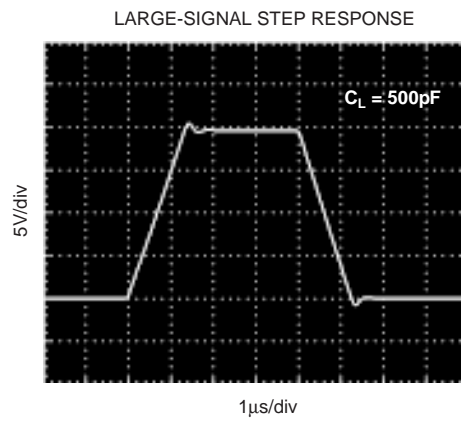
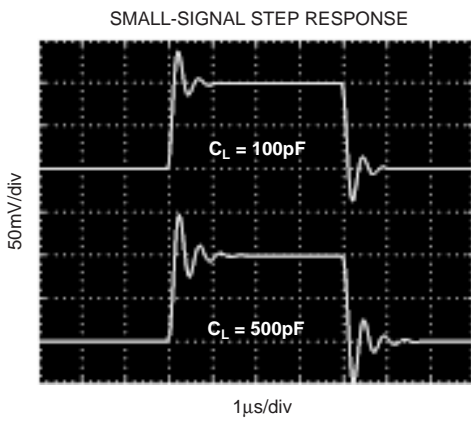
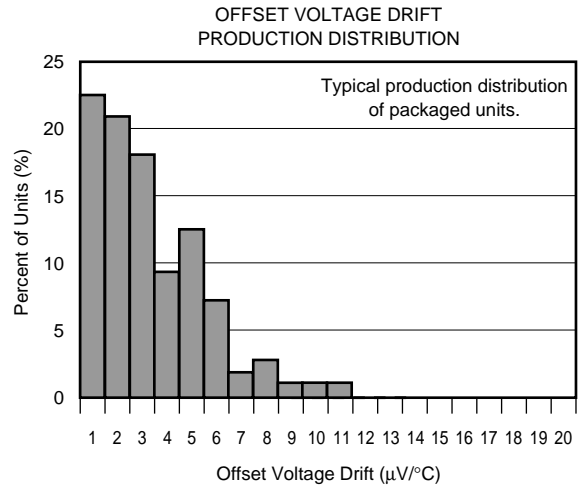
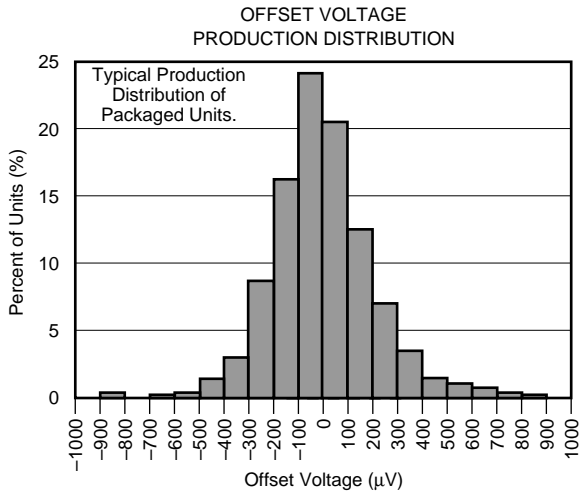
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA154. Decoupling capacitors are strongly recommended in applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 1.

As shown in Figure 1, the output is referred to the reference terminal (pin 1). A voltage applied to this pin will be summed with output signal. The differential input signal is connected to pins 2 and 3. The source impedances connected to the pinouts must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB (a 10Ω mismatch degrades CMR to 74dB). If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. The resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

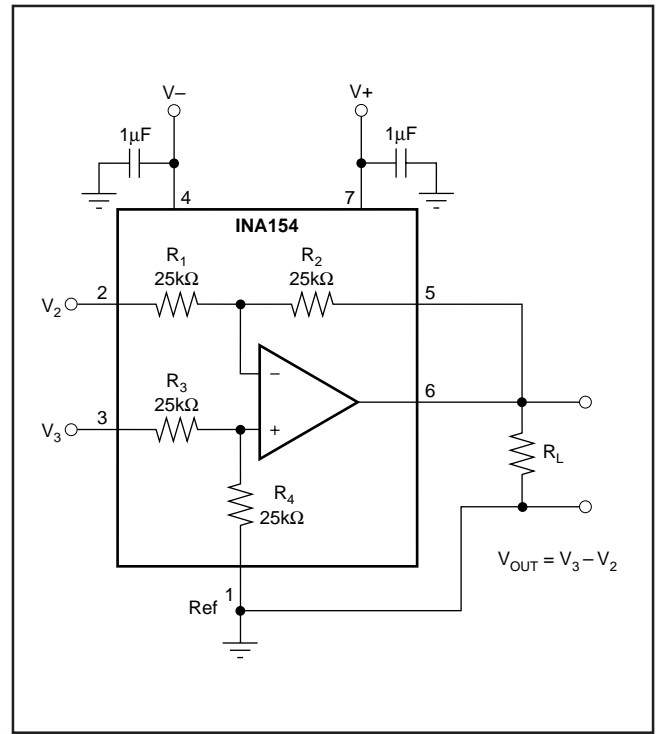


FIGURE 1. Basic Power Supply and Signal Connections.

OPERATING VOLTAGE

The INA154 operates from ±4V to ±18V supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Performance Curves.

INPUT VOLTAGE RANGE

The INA154 can accurately measure differential signals that are beyond the positive or negative power supply rails. The linear common-mode range extends from $2 \cdot (V+) - 5V$ to $2 \cdot (V-) + 5V$. See the Typical Performance Curve, “Input Common-Mode Range vs Output Voltage.”

OFFSET VOLTAGE TRIM

The INA154 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

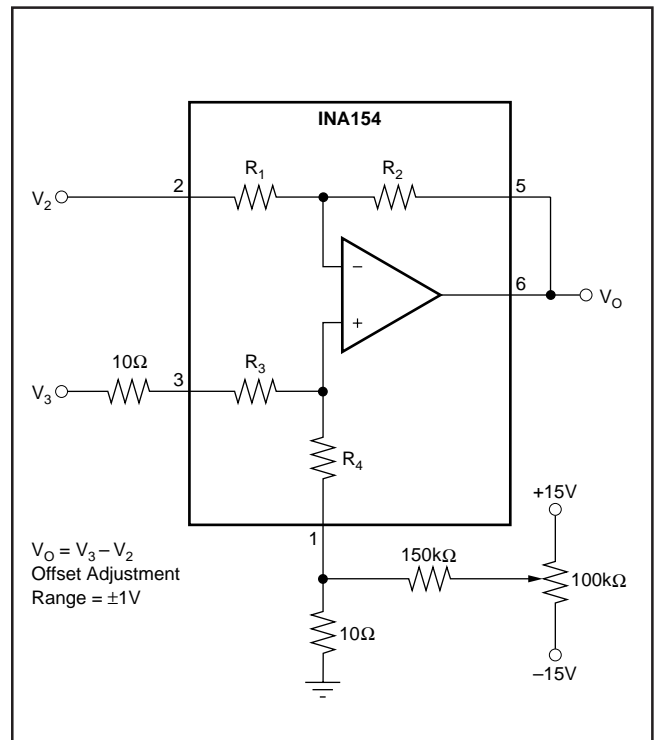


FIGURE 2. Offset Adjustment.

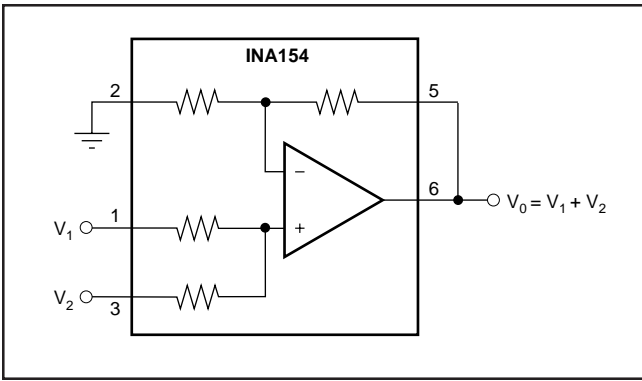


FIGURE 3. Precision Summing Amplifier.

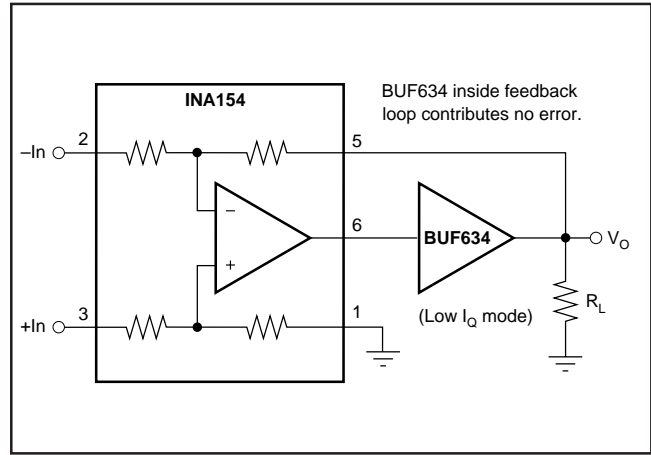


FIGURE 5. Boosting Output Current.

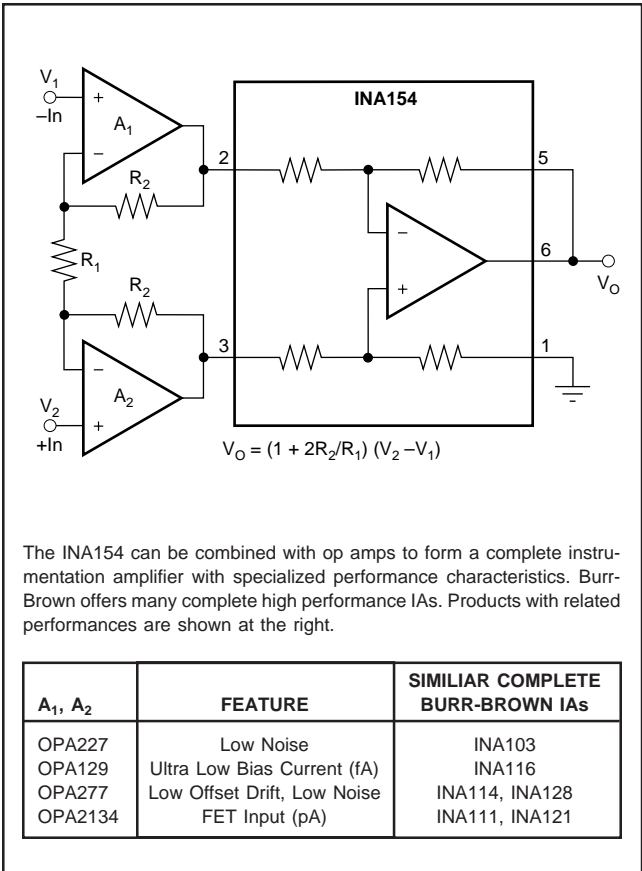


FIGURE 4. Precision Instrumentation Amplifier.

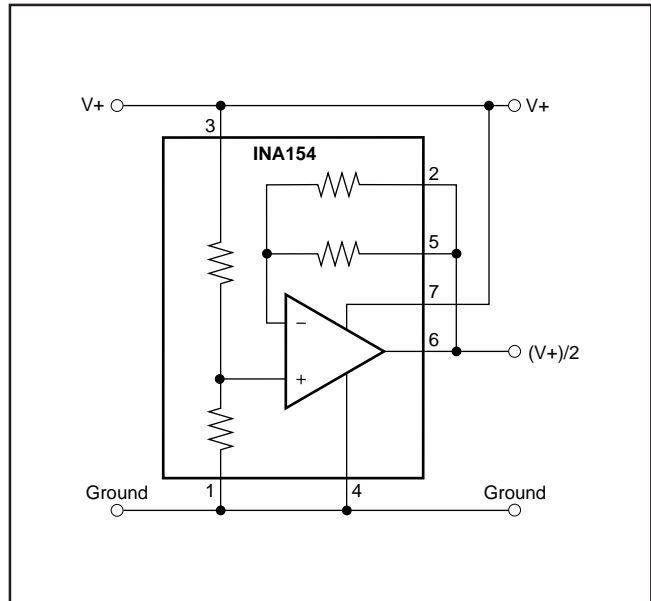


FIGURE 6. Pseudoground Generator.

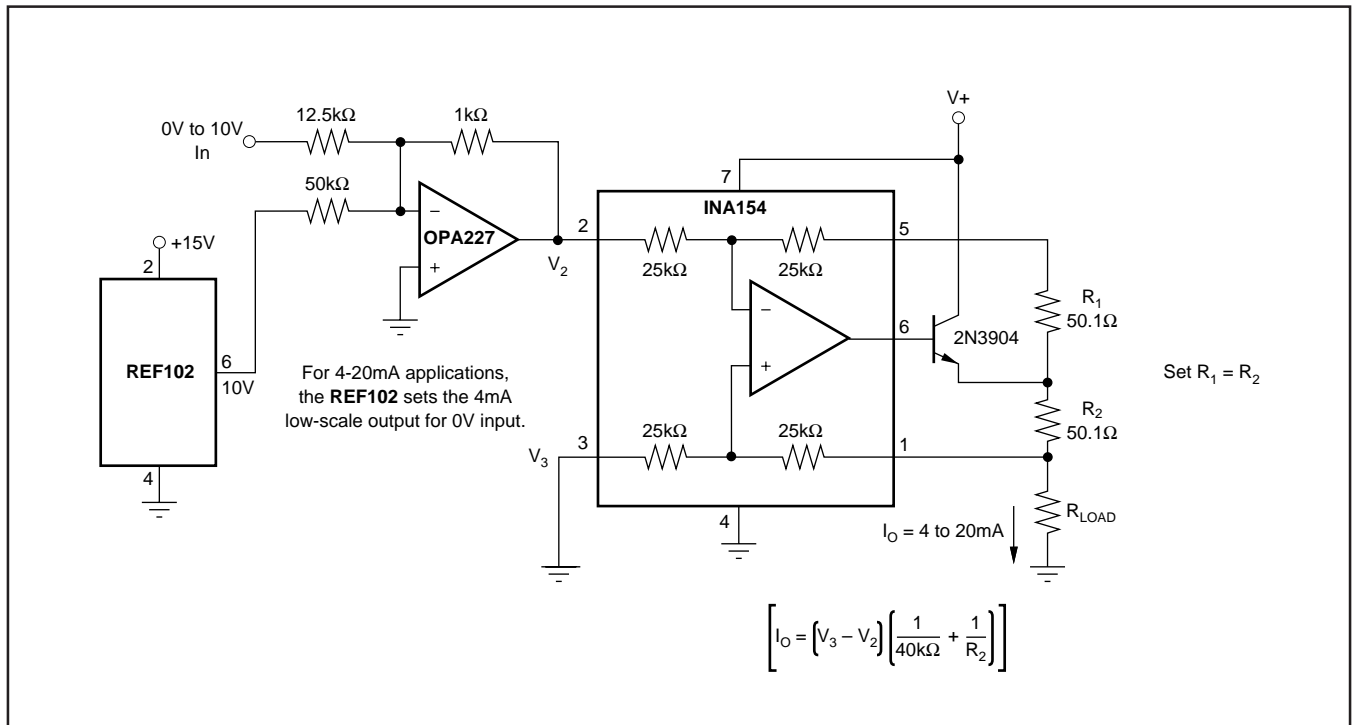


FIGURE 7. Precision Voltage-to-Current Conversion.

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- $\pm 10V$ Precision Voltage Reference
- $\pm 5V$ Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision $G = 2$ Amplifier (see INA157)
- Precision $G = 1/2$ Amplifier (see INA157)
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low I_{OUT}
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ± 1 Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA154U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 154U	Samples
INA154U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 154U	Samples
INA154UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 154U A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA154U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA154U/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA154U	D	SOIC	8	75	506.6	8	3940	4.32
INA154UA	D	SOIC	8	75	506.6	8	3940	4.32

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