LM321 Low Power Single Operational Amplifier

1 Features

- (V_{CC} = 5 V, T_A = 25°C. Typical values unless specified.)
- Gain-Bandwidth Product 1 MHz
- Low Supply Current 430 µA
- Low Input Bias Current 45 nA
- Wide Supply Voltage Range 3 V to 32 V
- Stable With High Capacitive Loads
- Single Version of LM324

2 Applications

- Chargers
- Power Supplies
- Industrial: Controls, Instruments
- Desktops
- Communications Infrastructure

3 Description

The LM321 brings performance and economy to low power systems. With a high unity gain frequency and a specified 0.4-V/µs slew rate, the quiescent current is only 430-µA/amplifier (5 V). The input common mode range includes ground and therefore the device is able to operate in single supply applications as well as in dual supply applications. It is also capable of comfortably driving large capacitive loads.

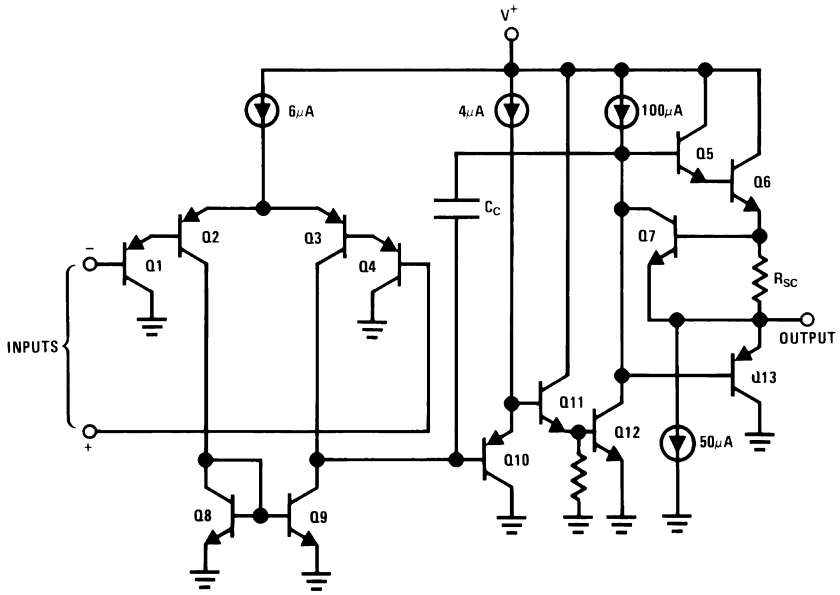
The LM321 is available in the SOT-23 package. Overall the LM321 is a low power, wide supply range performance operational amplifier that can be designed into a wide range of applications at an economical price without sacrificing valuable board space.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM321	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C — **Page**

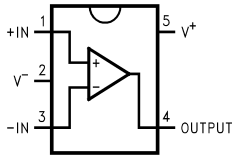
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (March 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 13

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	1	I	Noninverting input
V–	2	—	Negative (lowest) power supply
–IN	3	I	Inverting input
OUTPUT	4	O	Output
V+	5	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings (1)

	MIN	MAX	UNIT
Differential Input Voltage	±Supply Voltage		
Input Current (V_{IN} < −0.3 V) (2)		50	mA
Supply Voltage (V^+ - V^-)		32	V
Input Voltage	−0.3	32	V
Output Short Circuit to GND, V^+ ≤ 15 V and T_A = 25°C (3)	Continuous		
Junction Temperature (4)		150	°C
Mounting Temperature: Lead temperature (Soldering, 10 sec)		260	°C
Mounting Temperature: Infrared (10 sec)		215	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the operational amplifer to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.36V (at 25°C).
(3) Short circuits from the output V+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.
(4) The maximum power dissipation is a function of TJ(MAX), θJA , and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±300	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature Range	−40	85	°C
Supply Voltage	3	30	V

6.4 Thermal Information

THERMAL METRIC(1)		LM321 DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, all limits specified for at T_A = 25°C; V^+ = 5 V, V^- = 0 V, V_O = 1.4 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage				(1)2	7	mV
			(1), –40°C ≤ T_J ≤ 85°C			9	
I_{OS}	Input Offset Current				5	50	nA
			–40°C ≤ T_J ≤ 85°C			150	
I_B	Input Bias Current (2)				45	250	nA
			–40°C ≤ T_J ≤ 85°C			500	
V_{CM}	Input Common-Mode Voltage Range		V^+ = 30 V (3), for CMRR > = 50dB	0		V^+ - 1.5	V
			V^+ = 30 V (3), for CMRR > = 50dB, –40°C ≤ T_J ≤ 85°C			V^+ - 2	
A_V	Large Signal Voltage Gain		(V^+ = 15 V, R_L = 2kΩ, V_O = 1.4 V to 11.4 V)	25	100		V/mV
			(V^+ = 15 V, R_L = 2kΩ, V_O = 1.4 V to 11.4 V), –40°C ≤ T_J ≤ 85°C	15			
PSRR	Power Supply Rejection Ratio		R_S ≤ 10kΩ, V^+ ≤ 5 V to 30 V	65	100		dB
CMRR	Common Mode Rejection Ratio		R_S ≤ 10kΩ	65	85		dB
V_O	Output Swing	V_{OH}	V^+ = 30 V, R_L = 2kΩ, –40°C ≤ T_J ≤ 85°C	26			V
			V^+ = 30 V, R_L = 10kΩ, –40°C ≤ T_J ≤ 85°C	27	28		
		V_{OL}	V^+ = 5 V, R_L = 10kΩ, –40°C ≤ T_J ≤ 85°C		5	20	mV
I_S	Supply Current, No Load		V^+ = 5 V		0.430	1.15	mA
			V^+ = 5 V, –40°C ≤ T_J ≤ 85°C		0.7	1.2	
			V^+ = 30 V		0.660	2.85	
			V^+ = 30 V, –40°C ≤ T_J ≤ 85°C		1.5	3	
I_{SOURCE}	Output Current Sourcing		V_{ID} = +1 V, V^+ = 15 V, V_O = 2 V	20	40		mA
			V_{ID} = +1 V, V^+ = 15 V, V_O = 2 V, –40°C ≤ T_J ≤ 85°C	10	20		
I_{SINK}	Output Current Sinking		V_{ID} = −1 V, V^+ = 15 V, V_O = 2 V	10	20		mA
			V_{ID} = −1 V, V^+ = 15 V, V_O = 2 V, –40°C ≤ T_J ≤ 85°C	5	8		
			V_{ID} = −1 V, V^+ = 15 V, V_O = 0.2 V	12	100		µA

(1) VO ≅ 1.4 V, RS = 0Ω with V+ from 5 V to 30 V; and over the full input common-mode range (0 V to V+ - 1.5 V) at 25°C.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(3) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V+ - 1.5 V at 25°C, but either or both inputs can go to +32 V without damage, independent of the magnitude of V+.

Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for at T_A = 25°C; V^+ = 5 V, V^- = 0 V, V_O = 1.4 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_O	Output Short Circuit to Ground (4)	V^+ = 15 V		40	85	mA
SR	Slew Rate	V^+ = 15 V, R_L = 2kΩ, V_{IN} = 0.5 to 3 V, C_L = 100pF, Unity Gain		0.4		V/µs
GBW	Gain Bandwidth Product	V^+ = 30 V, f = 100kHz, V_{IN} = 10 mV, R_L =2kΩ, C_L = 100 pF		1		MHz
φm	Phase Margin			60		degrees
THD	Total Harmonic Distortion	f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_O = $2V_{PP}$, C_L = 100 pF, V^+ = 30 V		0.015%		
e_n	Equivalent Input Noise Voltage	f = 1kHz, R_S = 100Ω, V^+ = 30 V		40		nV/√Hz

(4) Short circuits from the output V+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

6.6 Typical Characteristics

Unless otherwise specified, V_S = 5 V, single supply, T_A = 25°C.

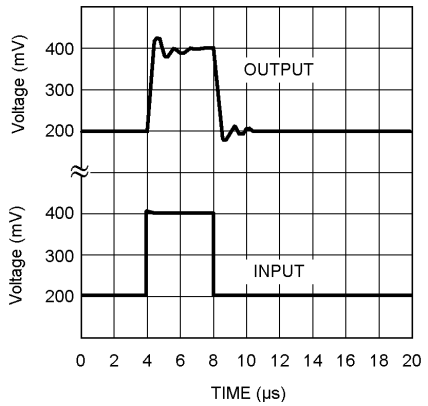


Figure 1. Small Signal Pulse Response

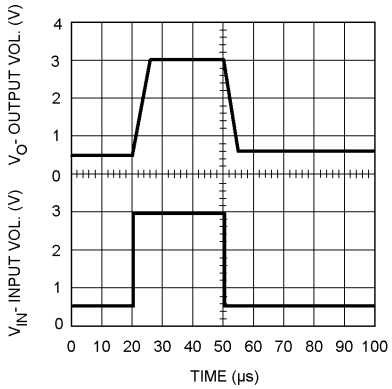


Figure 2. Large Signal Pulse Response

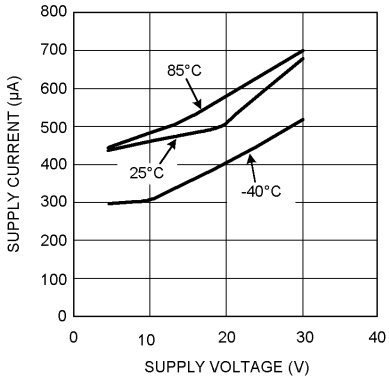


Figure 3. Supply Current vs. Supply Voltage

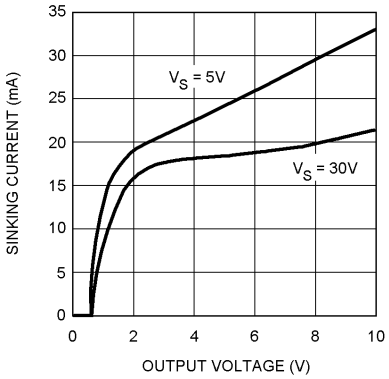


Figure 4. Sinking Current vs Output Voltage

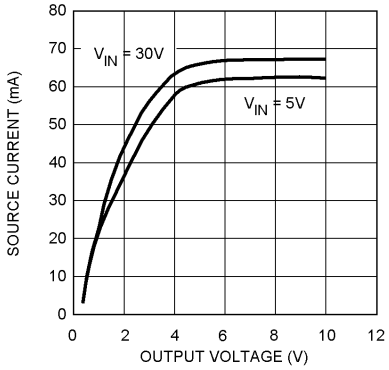


Figure 5. Source Current vs. Output Voltage

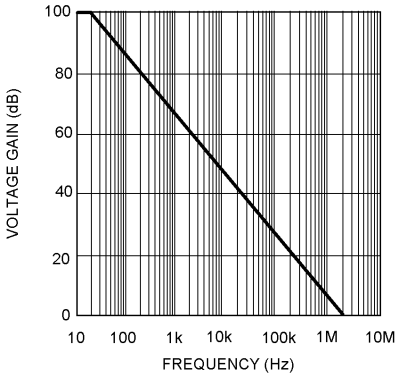


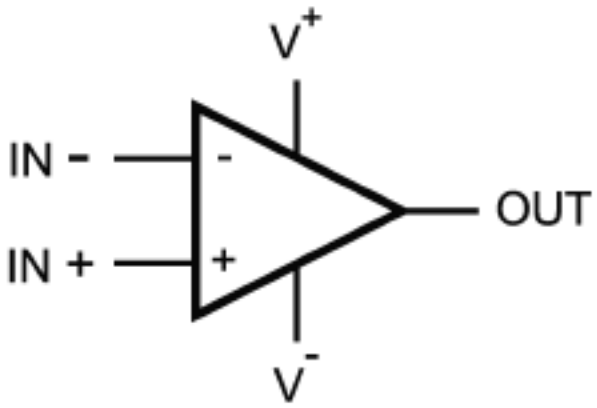
Figure 6. Open Loop Frequency Response

7 Detailed Description

7.1 Overview

The LM321 operational amplifer can operate with a single or dual power supply voltage, has true-differential inputs, and remains in the linear mode with an input common-mode voltage of 0 VDC. This amplifier operates over a wide range of power supply voltages, with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 3 V. Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 VDC (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

7.2 Functional Block Diagram



7.3 Feature Description

To reduce the power supply drain, the amplifier has a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sinks large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and to reduce distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if large load capacitance must be driven by the amplifier.

The bias network of the LM321 establishes a supply current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures than a standard IC operational amplifer.

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the LM321 series extends from 300 mV below ground to 32 V for normal operation. The typical performance in this range is summarized in Table 1:

Table 1. Typical Performance Range (Vs = 5 V)

PARAMETER	MIN	TYP	MAX	UNIT
Input voltage range	–0.3		32	V
Offset voltage		2	7	mV
Offset voltage drift (T_A = –40°C to 85°C)			9	µV/°C
CMRR	65	85		dB
PSRR	65	100		dB
Gain bandwidth product (GBP)		1		MHz
Slew rate		0.4		V/µs
Phase margin		60		°
Equivalent input noise voltage		40		nV/$\sqrt{Hz}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM321 operational amplifer can operate with a single or dual power supply voltage, has true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. This amplifier operates over a wide range of power supply voltages, with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 3 V.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C).An input clamp diode with a resistor to the IC input terminal can be used.

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For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and to reduce distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if large load capacitance must be driven by the amplifier.

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Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures than a standard IC operational amplifer.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard operational amplifer circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

8.2 Typical Applications

8.2.1 Noninverting DC Gain (0-V Input = 0-V Output)

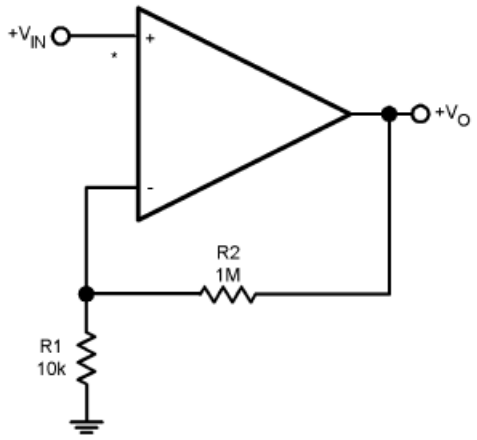


Figure 7. Non-Inverting DC Gain Schematic (0-V Input = 0-V Output)

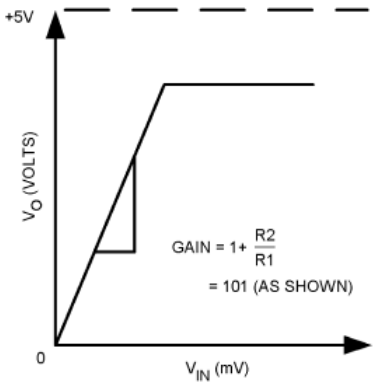
8.2.1.1 Design Requirements

- Supply voltage (up to 32 V)
- Phase margin: 60°

8.2.1.2 Detailed Design Procedure

- Connect 1-MΩ feedback resistor between the output and the inverting terminal of the amplifier.
- Connect 10-kΩ resistor between the inverting terminal and ground. Place the resistor as close to the inverting pin as possible.
- Connect power supply and input voltages.

8.2.1.3 Application Curve



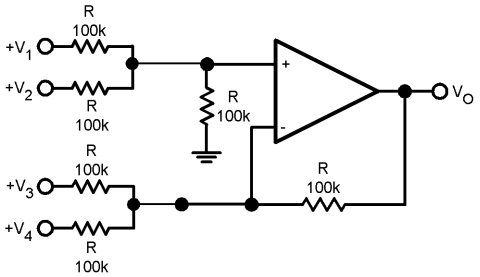
* R not needed due to temperature independent

Figure 8. Gain of the Noninverting Amplifier

Typical Applications (continued)

8.2.2 DC Summing Amplifier ($V_{IN's} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 7. The circuit gives an inverted output which is equal to the weighted algebraic sum of all four inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor. The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.



Where: $V_0 = V_1 + V_2 - V_3 - V_4$, $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Figure 9. DC Summing Amplifier Schematic ($V_{IN's} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)

8.2.3 Amplitude Modulator Circuit

The modulator circuit is shown in Figure 10. PWM signal is used to switch the MOSFET. When the MOSFET is on, the circuit acts as an inverting amplifier with gain 1. When The MOSFET is off, the inverting and non-inverting signals cancel each other out. Therefore, the output switches from –VIN to GND at the carrier frequency.

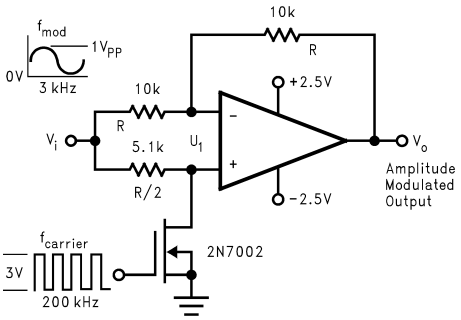
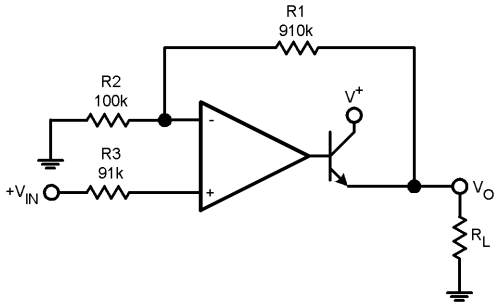


Figure 10. Amplitude Modulator Circuit Schematic

Typical Applications (continued)

8.2.4 Power Amplifier

Power amplifier application circuit is shown in Figure 11. Voltage gain is set by R1 and R2. The output of the amplifier is connected to the base of BJT which amplifies the current. Current gain is set by β, current gain of a BJT. The resulting output provides high power to the load. Differential voltage supplies are necessary.



V_0 = 0 V_{DC} for V_{IN} = 0 V_{DC}, A_V = 10

Figure 11. Power Amplifier Schematic

8.2.5 LED Driver

LM321 operating as an LED driver is shown in Figure 12. The output of the amplifier sets the current through the diode. The voltage across the LED is assumed constant.

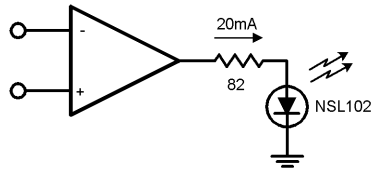


Figure 12. LED Driver Schematic

8.2.6 Fixed Current Sources

Operational amplifier can be used to provide fixed current source to multiple loads. The output voltage of the amplifier is connected to bases of bipolar transistors. The feedback is provided from the drain of a BJT to the inverting terminal of the amplifier. Currents in the second and later BJTs are set by the ratio of R1 and R2.

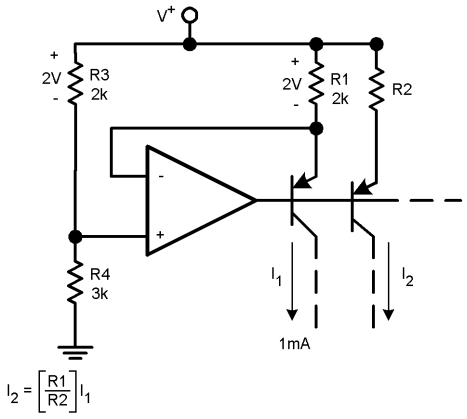


Figure 13. Fixed Current Sources Schematic

Typical Applications (continued)

8.2.7 Lamp Driver

Similar to the LED driver, LM321 can be used as a lamp driver. The output of the amplifier is to be connected to the base of a bipolar transistor which will drive β*output current of the amplifier through the lamp.

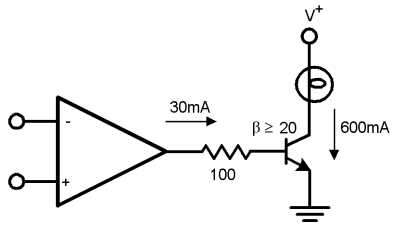


Figure 14. Lamp Driver Schematic

9 Power Supply Recommendations

The LM321 is specified for operation up to 32 V; many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*. Place 0.1-µF bypass capacitors close to the power-supply terminals to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifer itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 15, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

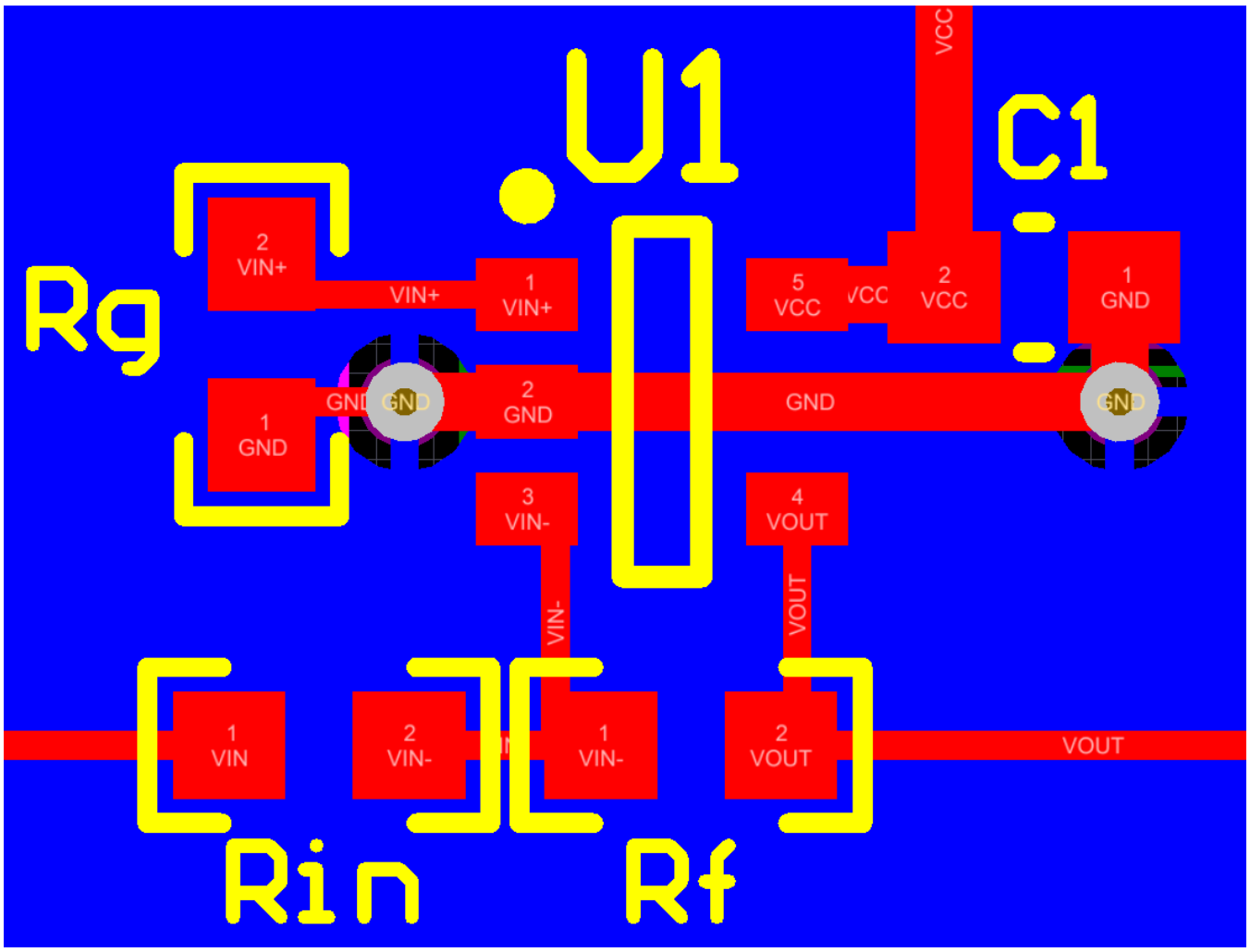


Figure 15. PCB Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM321MF	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A63A	
LM321MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A63A	Samples
LM321MFX	LIFEBUY	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A63A	
LM321MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A63A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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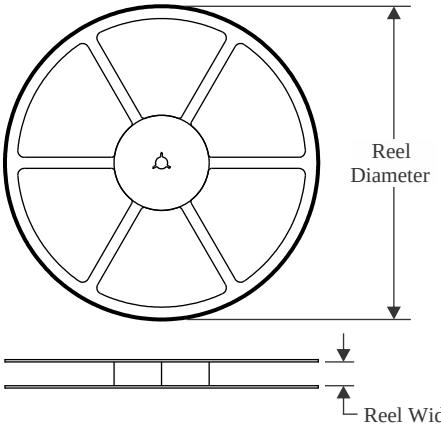
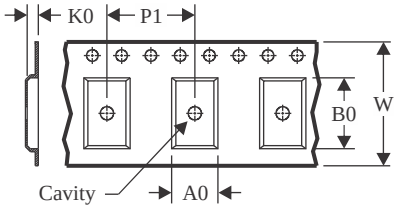
TAPE AND REEL INFORMATION

REEL DIMENSIONS

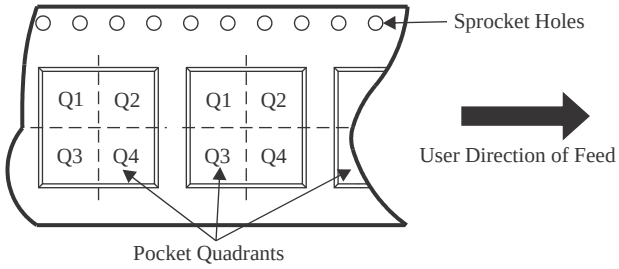


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

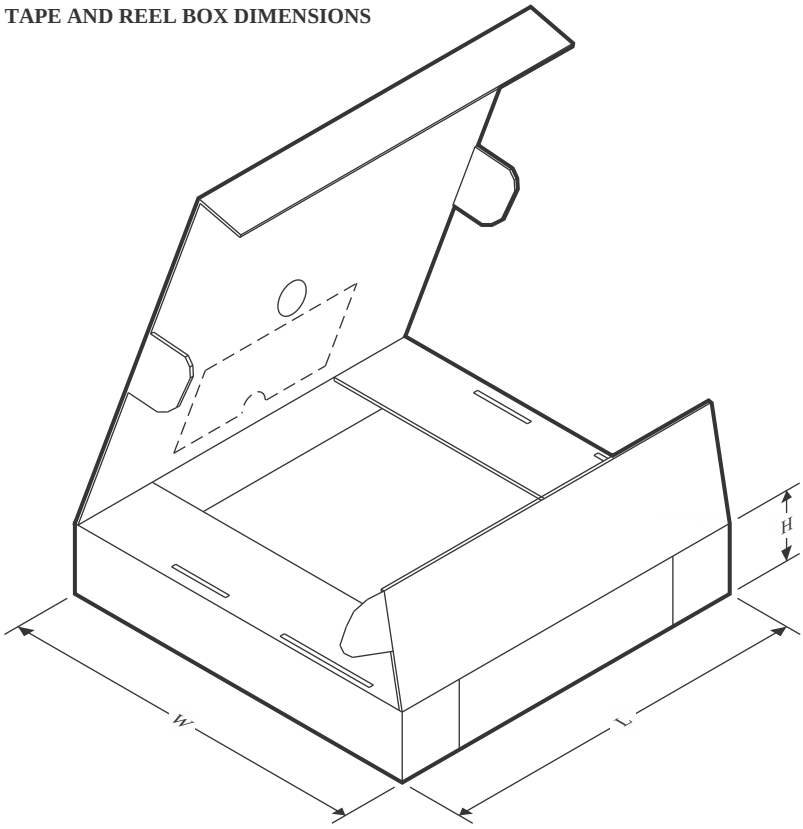
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM321MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MF/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

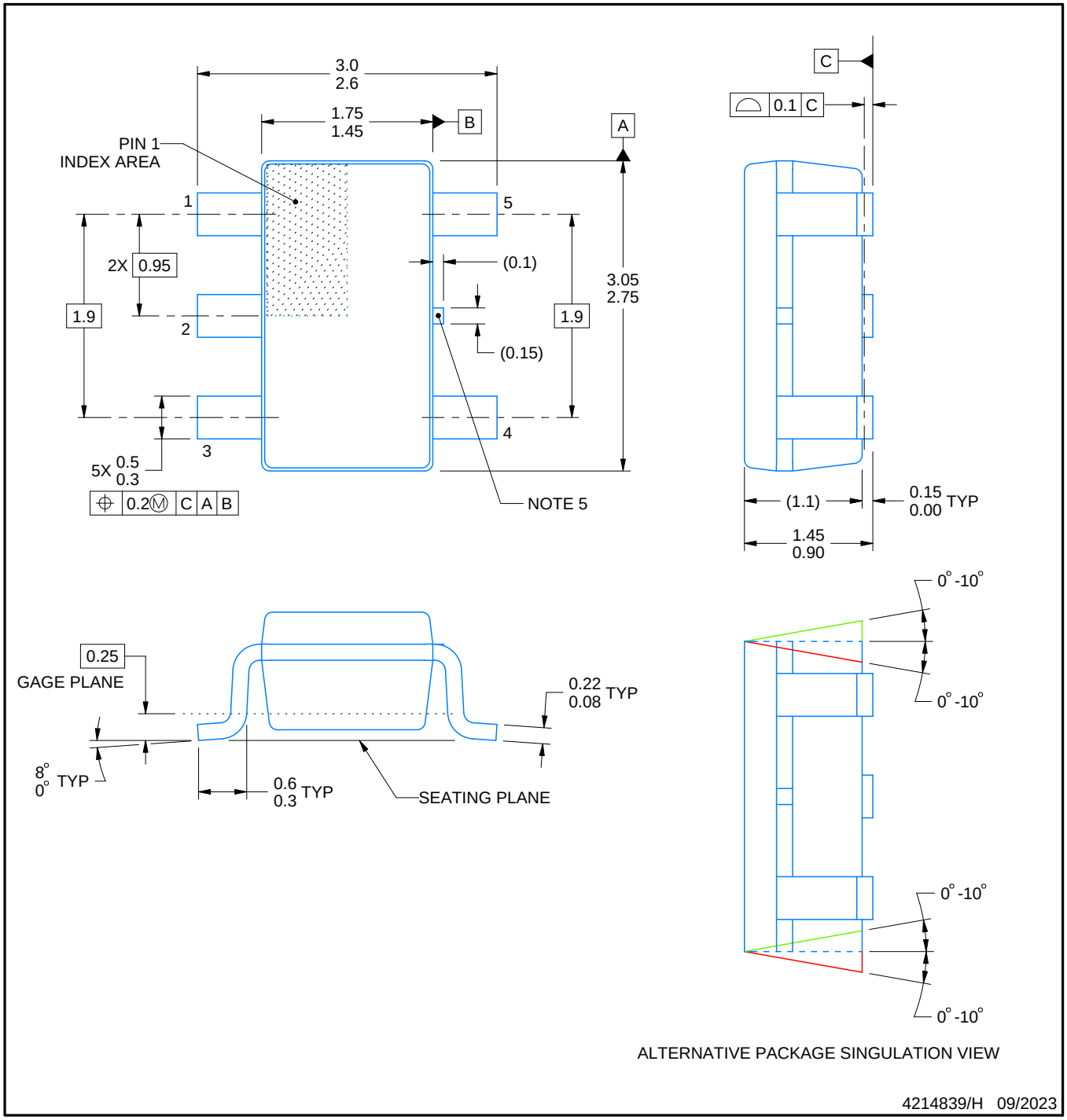
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM321MF	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM321MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM321MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM321MFX	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM321MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM321MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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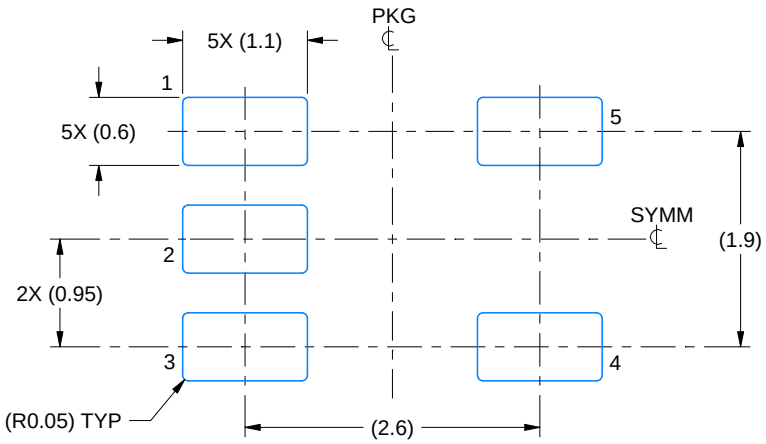
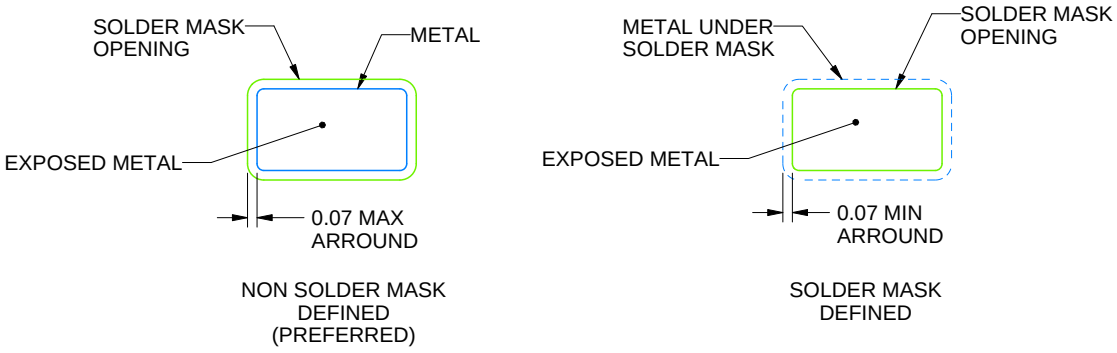
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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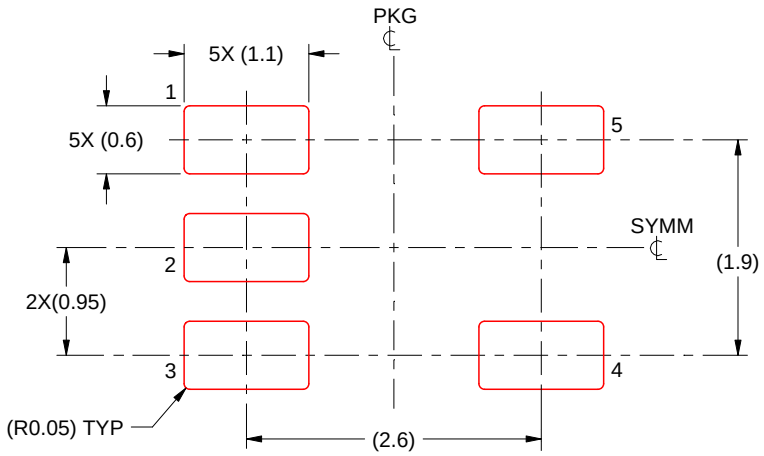
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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