10-W STEREO CLASS-D AUDIO POWER AMPLIFIER

Check for Samples: TPA3110L

FEATURES

- **10-W/ch into 8-Ω Loads at 10% THD+N From a 13-V Supply**
- **90% Efficient Class-D Operation Eliminates Need for Heat Sinks**
- **Wide Supply Voltage Range Allows Operation from 8 V to 26 V**
- **SpeakerGuard ™ Speaker Protection Includes Adjustable Power Limiter plus DC Protection**
- **Flow Through Pin Out Facilitates Easy Board Layout**
- **Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto Recovery Option**
- **Excellent THD+N / Pop-Free Performance**
- **Four Selectable, Fixed Gain Settings**
- **Differential Inputs**

APPLICATIONS

- **Televisions**
- **Consumer Audio Equipment**

DESCRIPTION

The TPA3110L is a 10-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers.

The TPA3110L can drive stereo speakers as low as 4Ω. The high efficiency of the TPA3110L, 90%, eliminates the need for an external heat sink when playing music.

The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

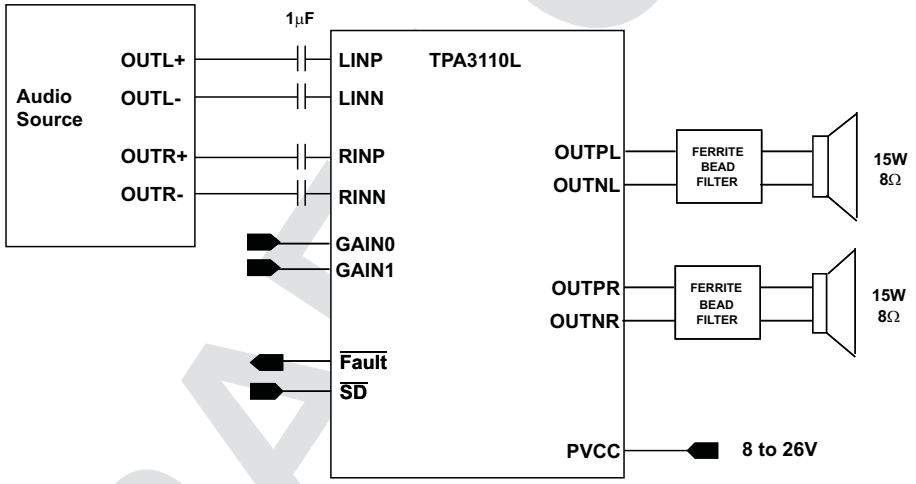


Figure 1. TPA3110L Simplified Application Schematic

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V to 30 V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$	–0.3 V to V_{CC} + 0.3 V
		RINN, RINP, LINN, LINP	–0.3 V to 6.3 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range(2)		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
R_L	Minimum Load Resistance	BTL: PVCC > 15 V	4.8
		BTL: PVCC ≤ 15 V	3.2
ESD	Electrostatic discharge	Human body model (3) (all pins)	±2 kV
		Charged-device model (4) (all pins)	±500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The TPA3110L incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.
(3) In accordance with JEDEC Standard 22, Test Method A114-B.
(4) In accordance with JEDEC Standard 22, Test Method C101-A

THERMAL INFORMATION

THERMAL METRIC(1)		TPA3110L PWP 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance		°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance		
θ_{JB}	Junction-to-board thermal resistance		
ψ_{JT}	Junction-to-top characterization parameter		
ψ_{JB}	Junction-to-board characterization parameter		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$=100k, V_{CC}=26V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 2V, V_{CC} = 18 V		50	µA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 0.8 V, V_{CC} = 18 V		5	µA
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 24V			32	50	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 24V			250	400	µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		400		mΩ
			Low side		400		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{on}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 100µA		6.4	6.9	7.4	V

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 12V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 12V			200		µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		400		mΩ
			Low side		400		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2mA		6.4	6.9	7.4	V

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

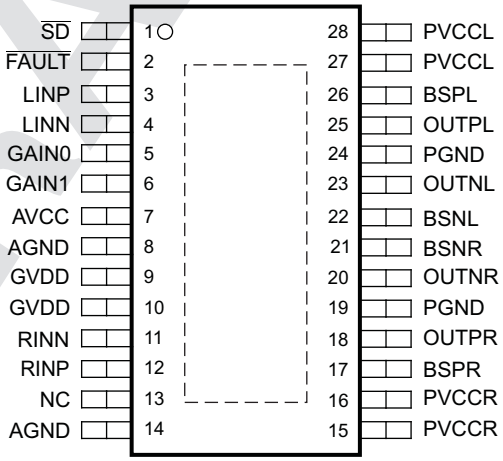
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, V_{CC} = 16 V		15		W
THD+N	Total harmonic distortion + noise	V_{CC} = 16 V, f = 1 kHz, P_O = 7.5 W (half-power)		0.1		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz; V_{CC} = 13 V		10		W
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half-power)		0.06		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

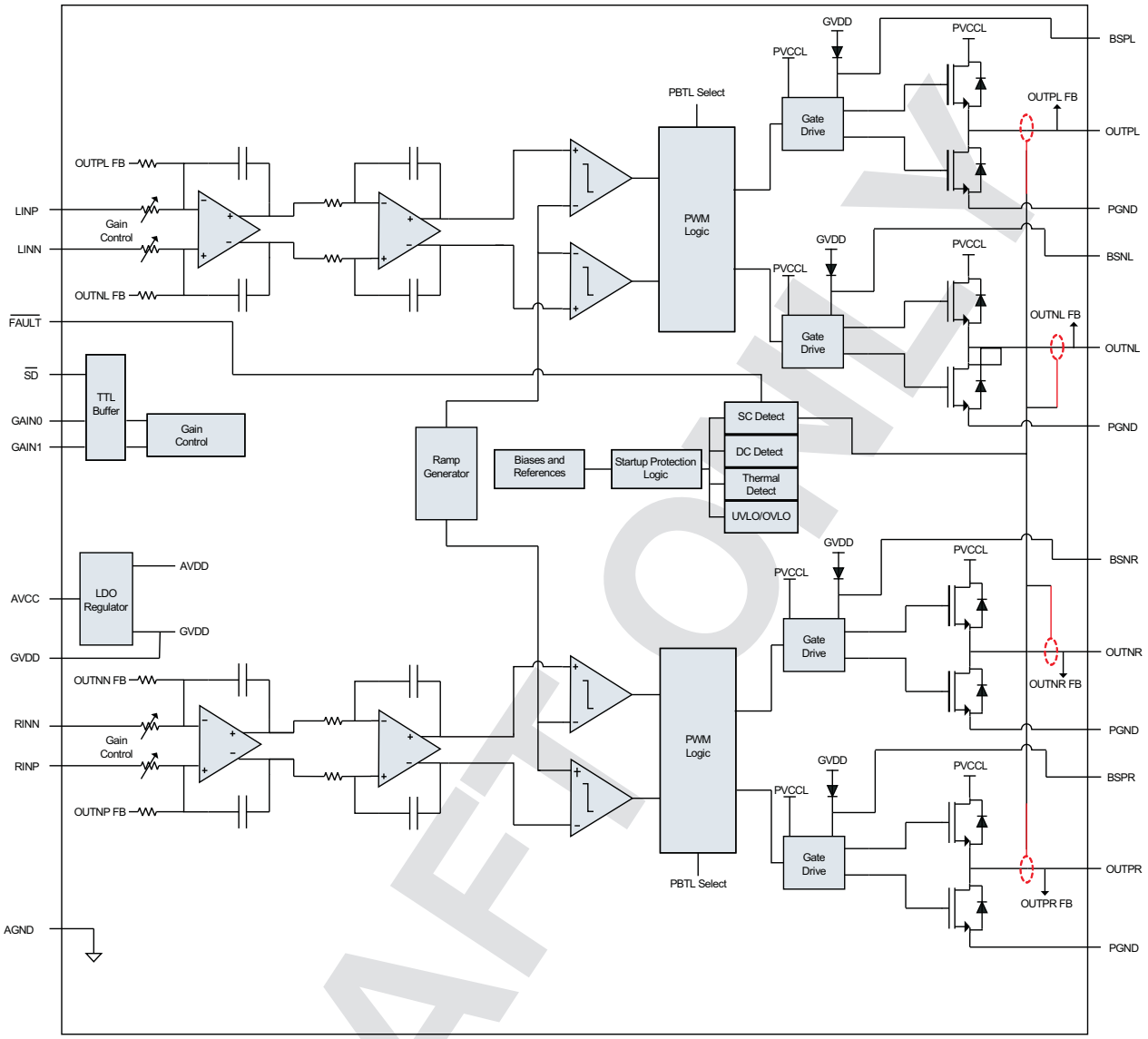
PWP (TSSOP) PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O/P	DESCRIPTION
NAME	NO.		
$\overline{SD}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, short circuit faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel. Biased at 3V.
LINN	4	I	Negative audio input for left channel. Biased at 3V.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply
AGND	8, 14		Analog signal ground. Connect to the thermal pad.
GVDD	9, 10	O	High-side FET gate drive supply. Nominal voltage is 7V. Also should be used as supply for PLIMIT function
RINN	11	I	Negative audio input for right channel. Biased at 3V.
RINP	12	I	Positive audio input for right channel. Biased at 3V.
NC	13		Not connected
PVCCR	15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCR	16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19		Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24		Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCL	28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110L EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

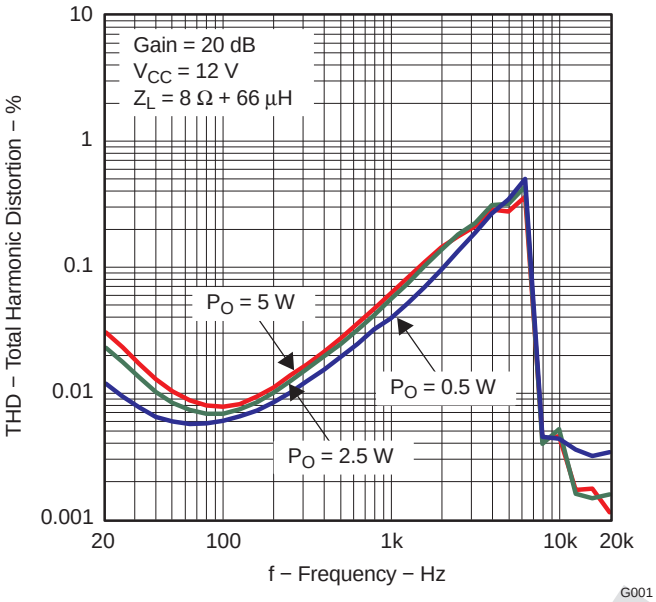


Figure 2.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

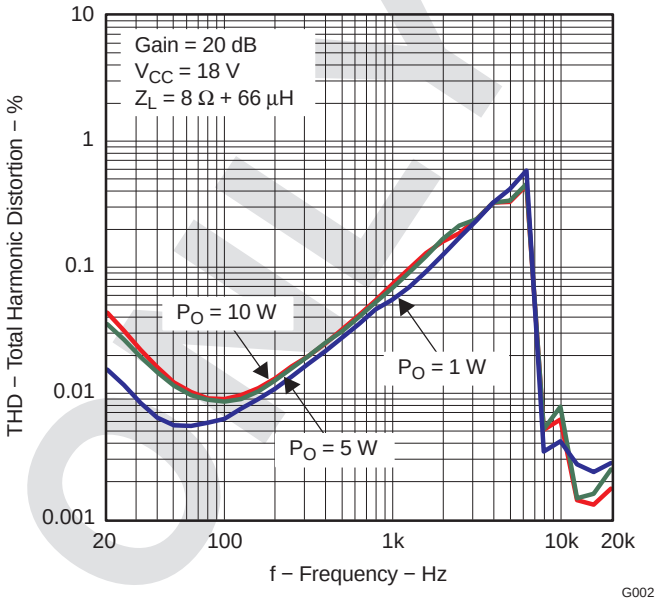


Figure 3.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

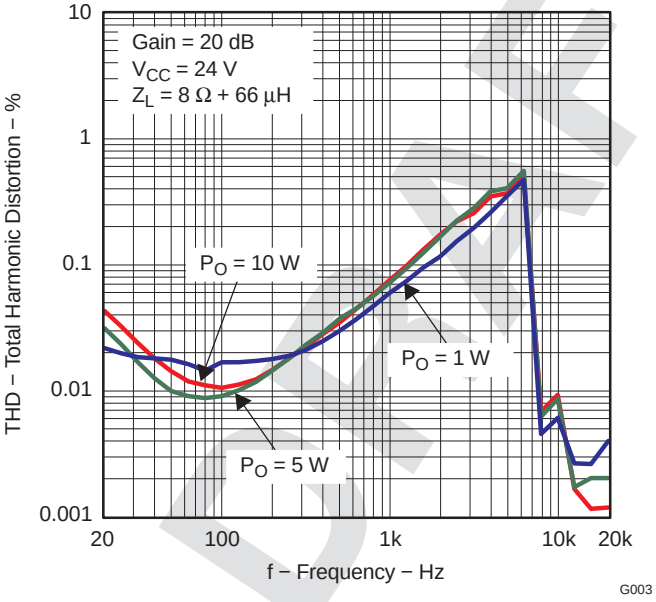


Figure 4.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

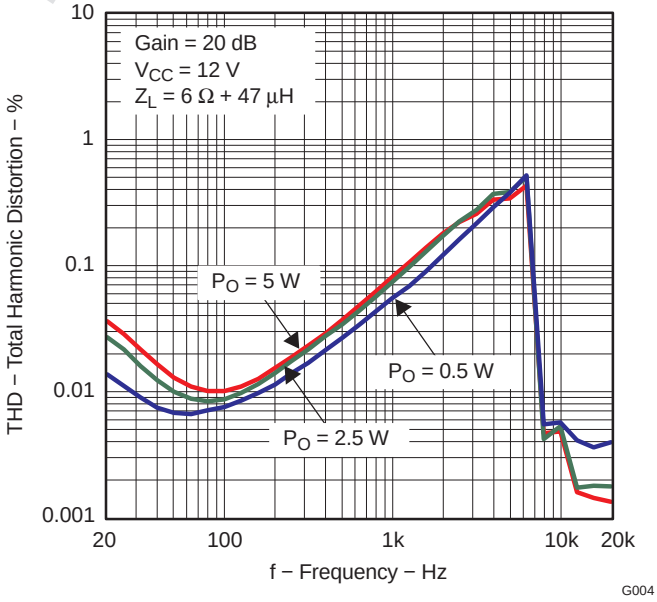


Figure 5.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110L EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

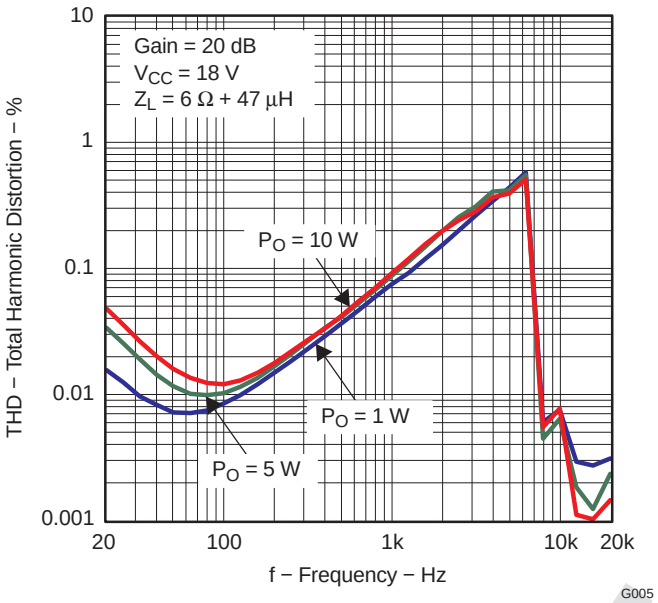


Figure 6.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

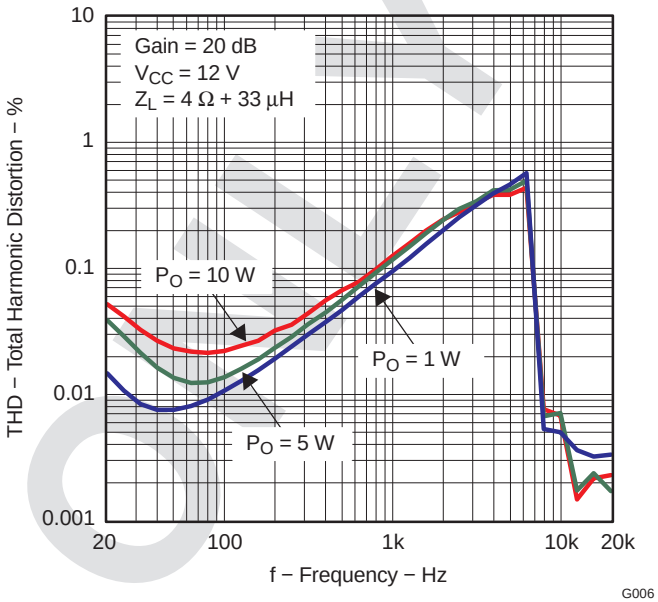


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

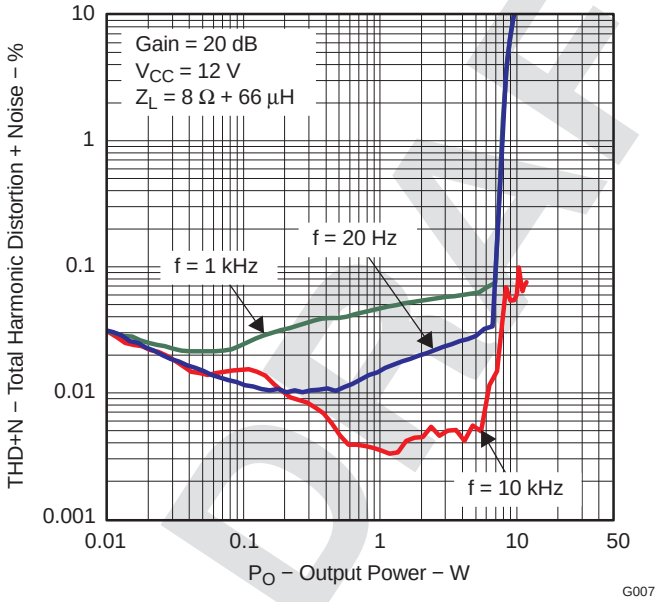


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

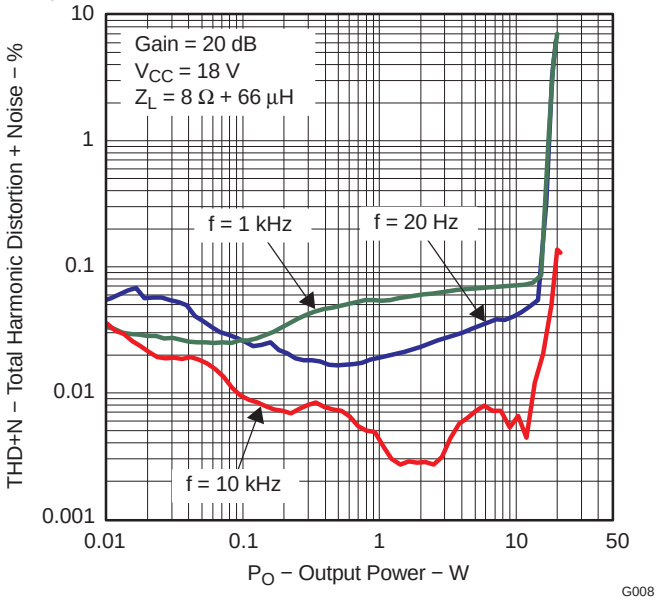


Figure 9.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110L EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

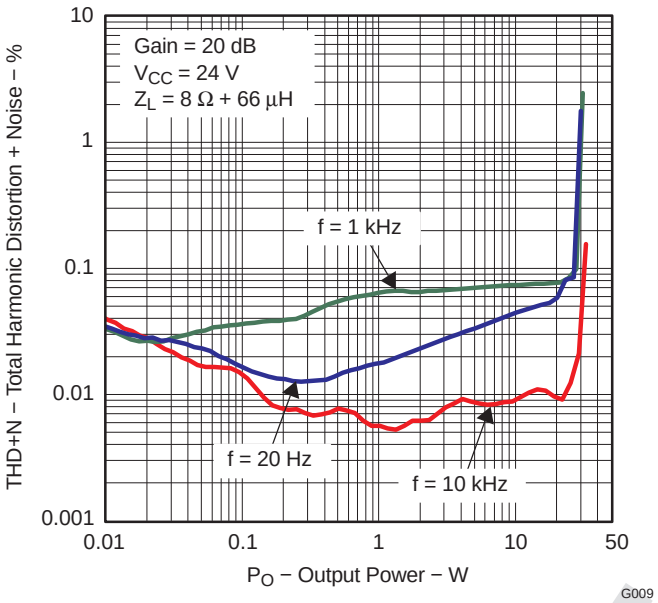


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

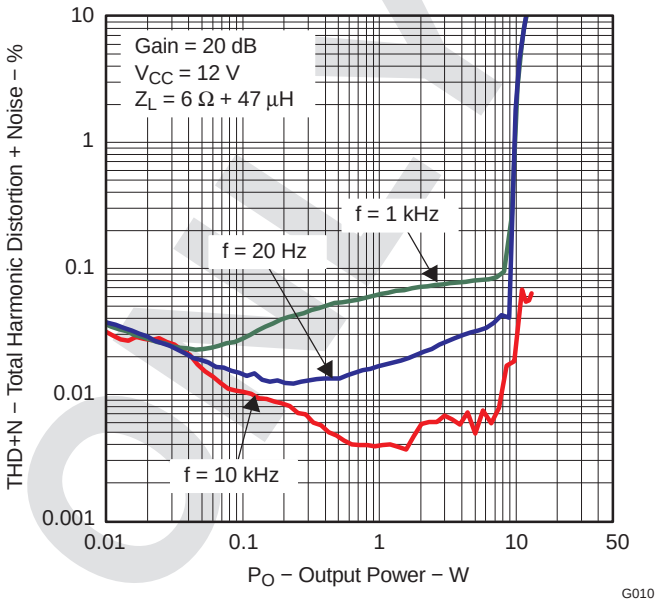


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

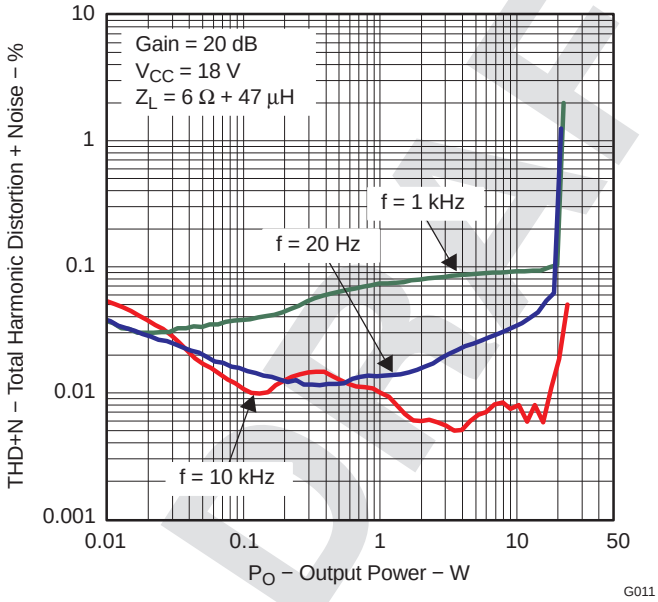


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

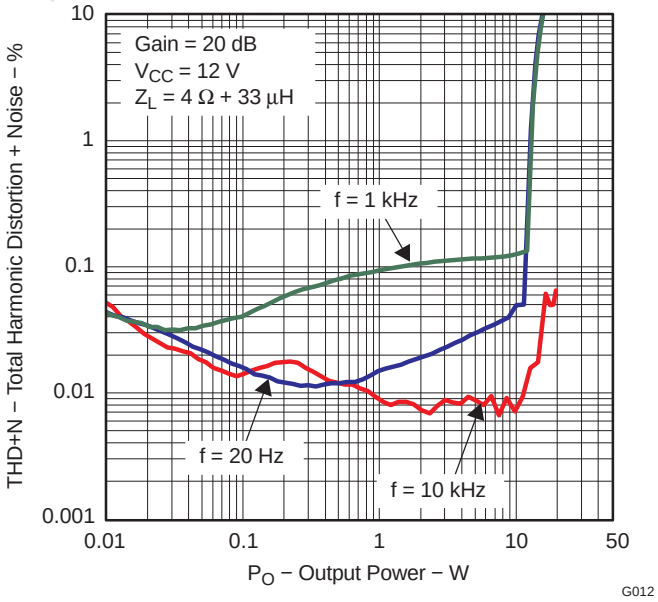


Figure 13.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110L EVM which is available at ti.com.)

GAIN/PHASE vs FREQUENCY (BTL)

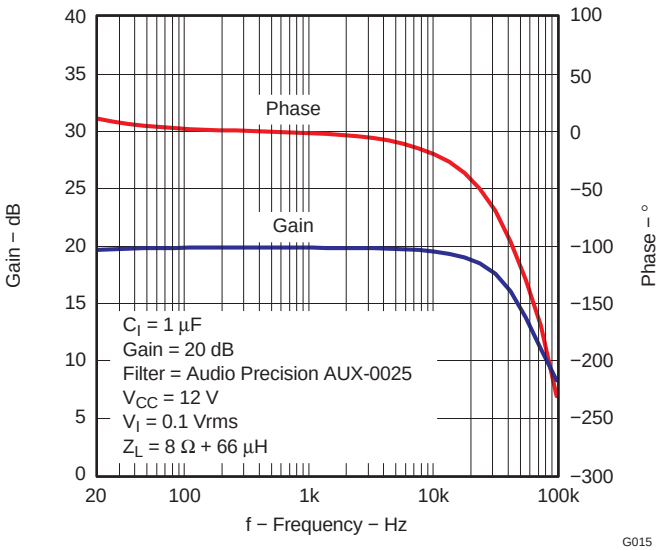
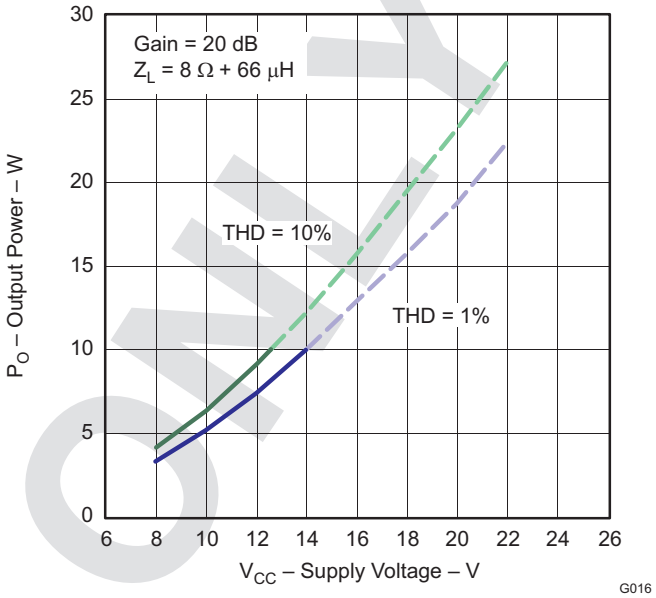


Figure 14.

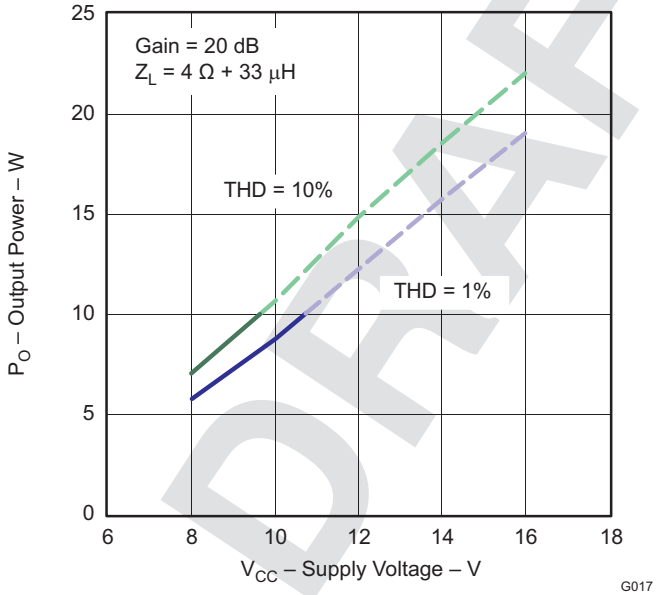
OUTPUT POWER vs SUPPLY VOLTAGE (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 15.

OUTPUT POWER vs SUPPLY VOLTAGE (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 16.

EFFICIENCY vs OUTPUT POWER (BTL)

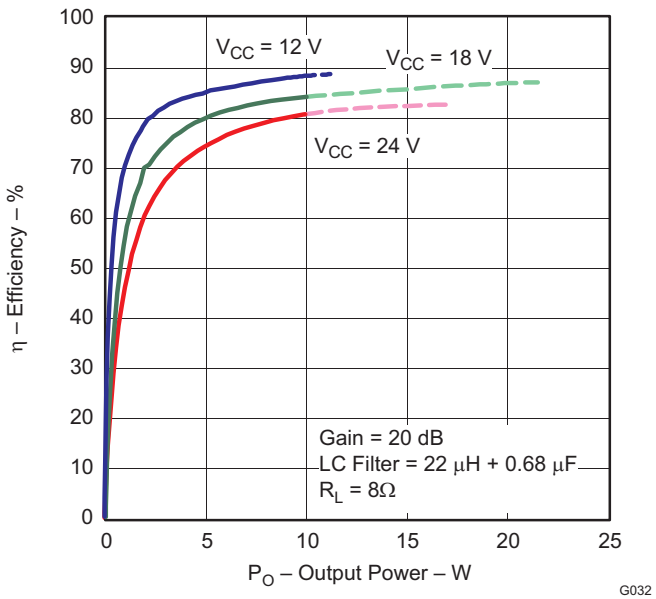


Figure 17.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110L EVM which is available at ti.com.)

EFFICIENCY vs OUTPUT POWER (BTL)

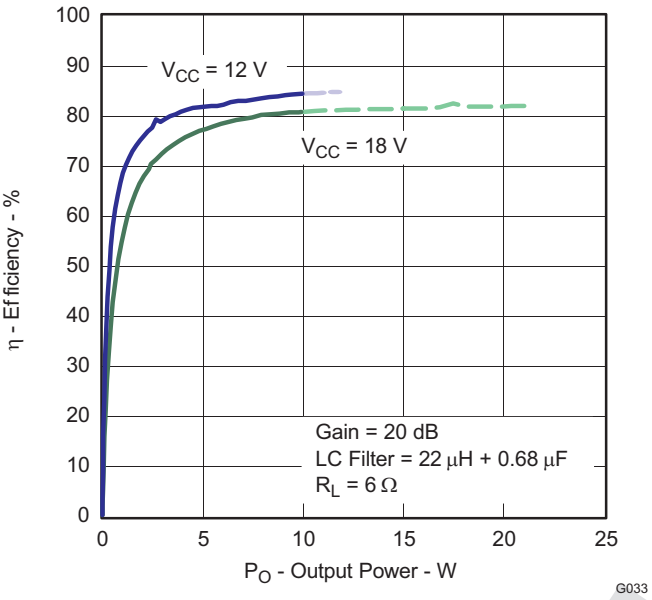


Figure 18.

EFFICIENCY vs OUTPUT POWER (BTL)

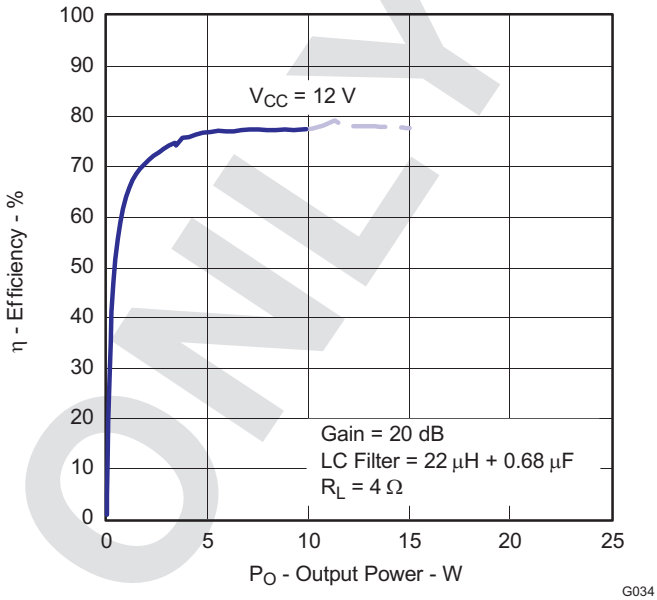
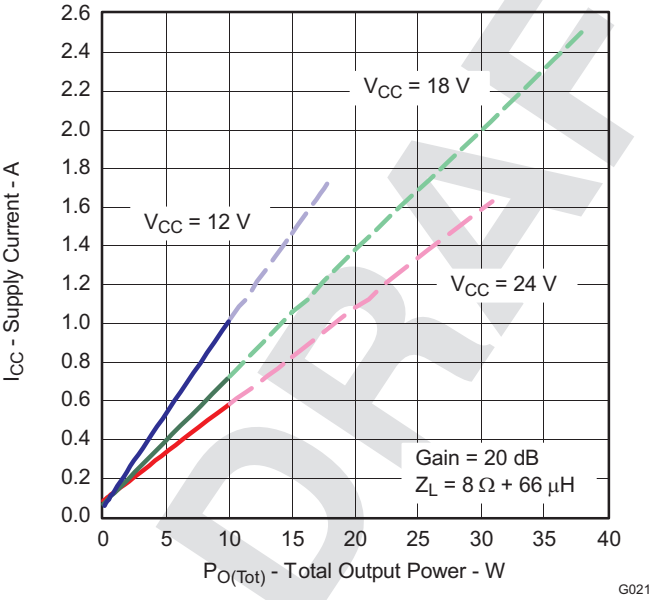


Figure 19.

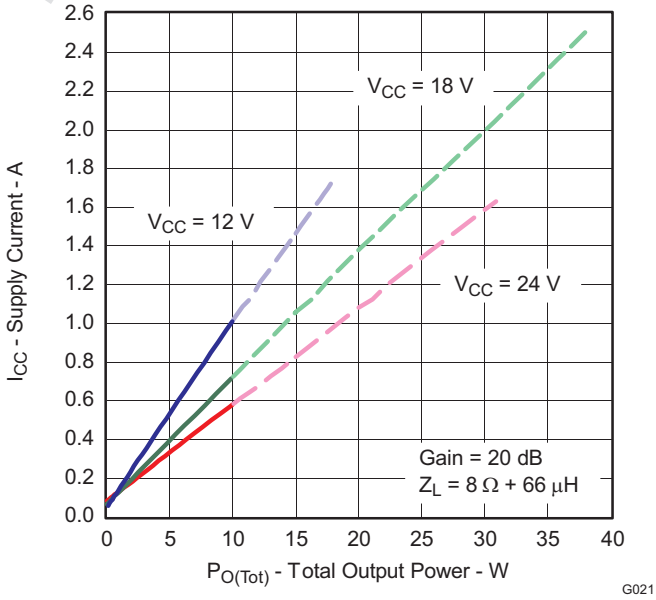
SUPPLY CURRENT vs TOTAL OUTPUT POWER (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 20.

SUPPLY CURRENT vs TOTAL OUTPUT POWER (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 21.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110L EVM which is available at ti.com.)

CROSSTALK vs FREQUENCY (BTL)

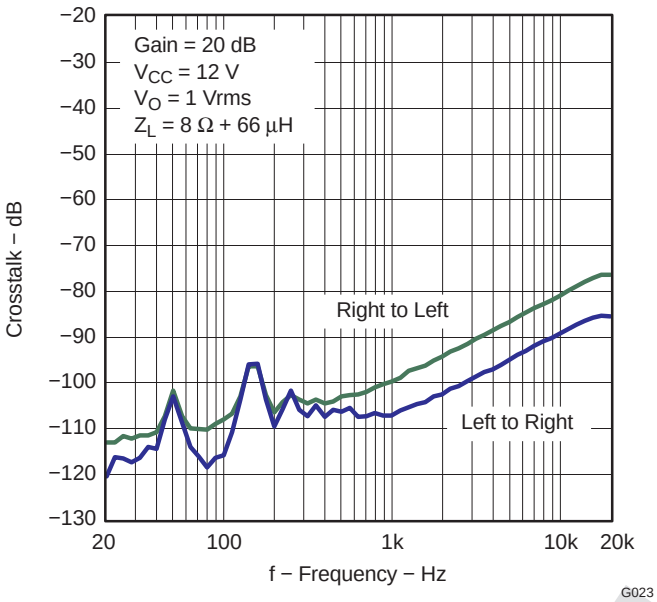


Figure 22.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY (BTL)

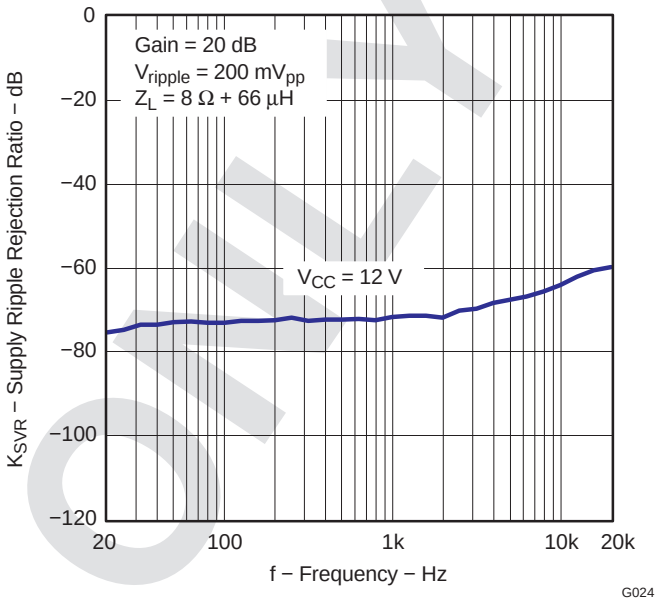


Figure 23.

DEVICE INFORMATION

Gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3110L is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the TPA3110L. At the lower gain settings, the input impedance could increase as high as 72 kΩ.

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

$\overline{SD}$ OPERATION

The TPA3110L employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

PLIMIT

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1μF capacitor from pin 10 to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{1}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P

P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 2. PLIMIT Typical Operation

Test Conditions ()	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V_{P-P})
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	6.97	36.1 (thermally limited)	43
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	2.94	15 (thermally limited)	25.2
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	2.34	10	20
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	1.62	5	14
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	6.97	12.1 (thermally limited)	27.7
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	3.00	10	23
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.86	5	14.8
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	6.97	10.55 (thermally limited)	23.5
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.76	5	15

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1μF capacitor to ground at this pin.

DC Detect

TPA3110D2 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling SD will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, +57%, -43%) for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum differential input voltages required to trigger the DC detect are show in table 2. The inputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 3. DC Detect Threshold

AV(dB)	Vin (mV, differential)
20	112
26	56
32	28
36	17

SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

TPA3110L has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULT pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the short-circuit protection latch.

THERMAL PROTECTION

Thermal protection on the TPA3110L prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ terminal.

APPLICATION INFORMATION

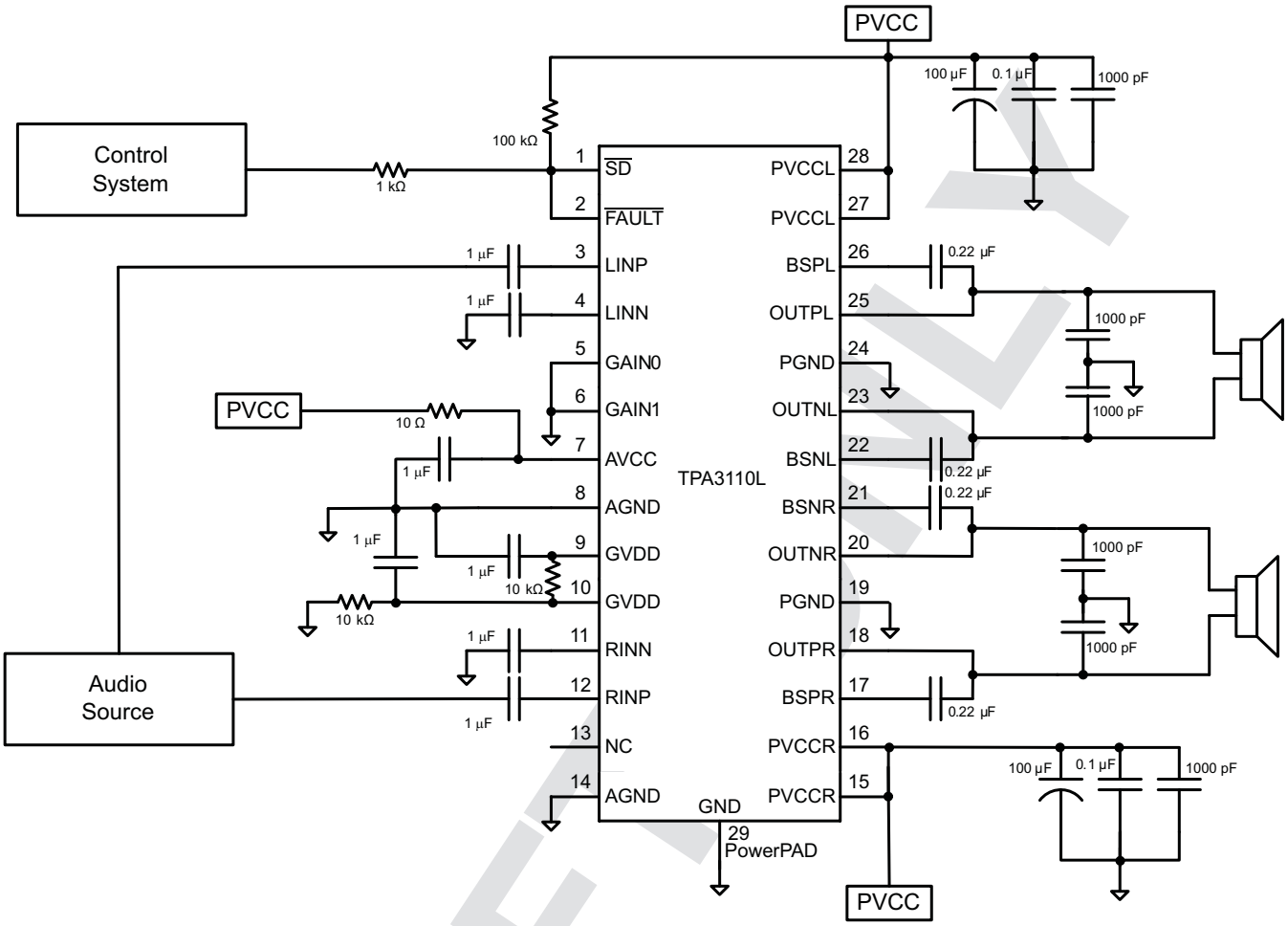


Figure 24. Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs

TPA3110L Modulation Scheme

The TPA3110L uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

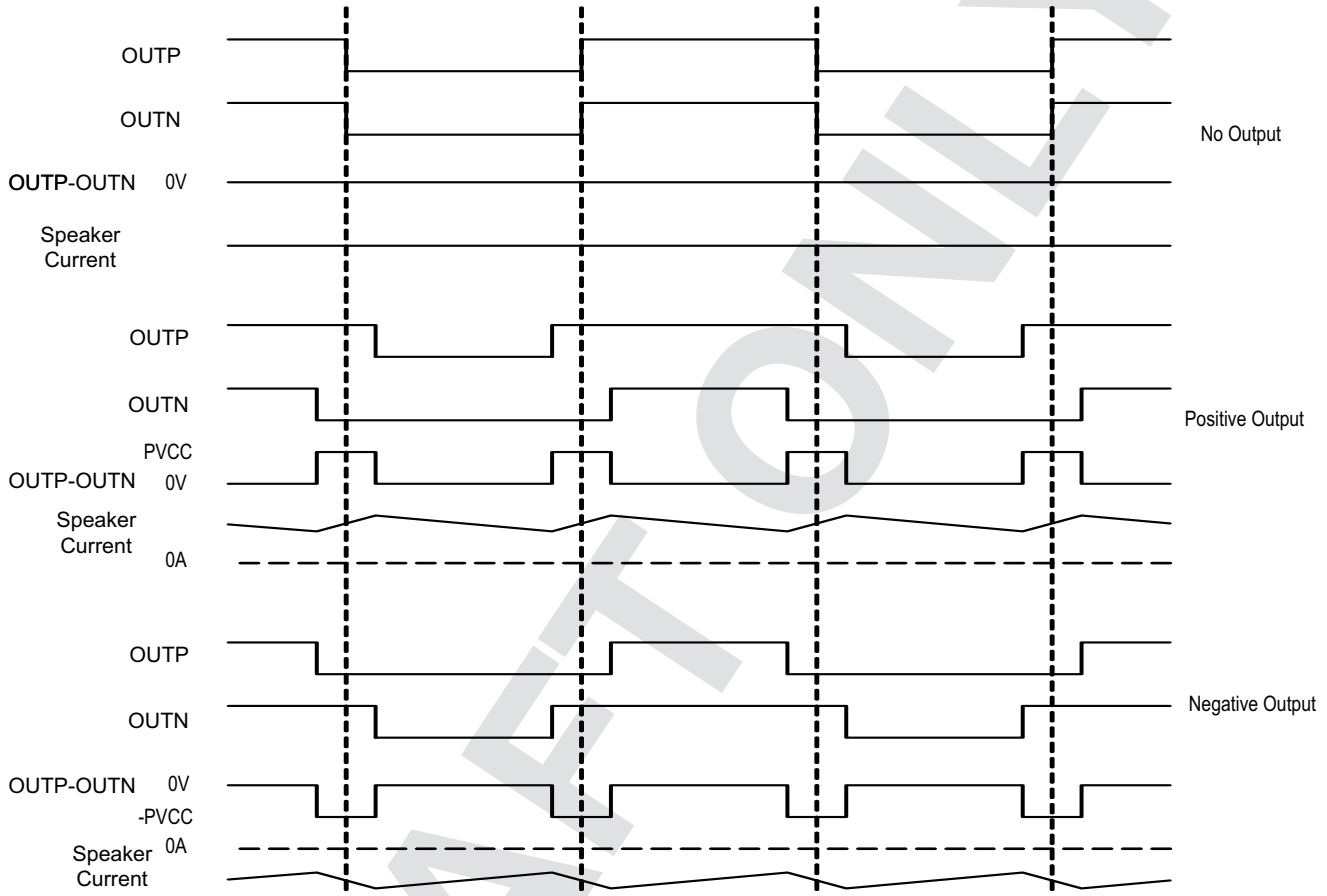


Figure 25. The TPA3110L Output Voltage and Current Waveforms Into an Inductive Load

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

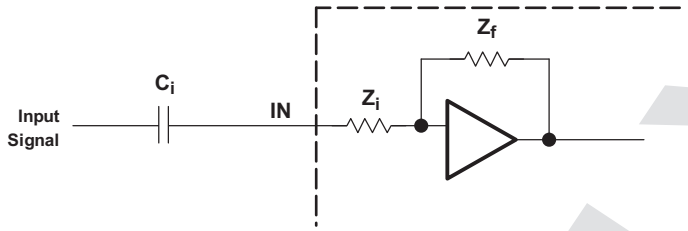
The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3110L modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.



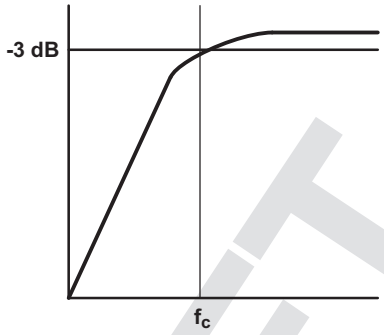
The -3-dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad (2)$$

INPUT CAPACITOR, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (3)$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (4)$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

POWER SUPPLY DECOUPLING, C_S

The TPA3110L is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220 μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 μF or larger capacitor should be placed on each PVCC terminal. A 10 μF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

BSN and BSP CAPACITORS

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 μF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22 μF capacitor must be connected from OUTPx to BSPx, and one 0.22 μF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 1.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL INPUTS

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3110L with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3110L with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

The TPA3110L can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3110L on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1µF and 1µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 7) decoupling capacitor should be grounded to analog ground (AGND). The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3110L.
- Output filter—The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3110L Evaluation Module (TPA3110LEVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

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