

ESDS31x Data-Line Surge and ESD Protection Diode Array

1 Features

- IEC 61000-4-2 ESD protection:
 - ±30kV Contact Discharge
 - ±30kV Air Gap Discharge
- IEC 61000-4-4 EFT protection:
 - 80A (5/50ns)
- IEC 61000-4-5 surge protection:
 - 25A (8/20µs)
- IO capacitance:
 - 4.5pF (typical)
- DC breakdown voltage: 5.5V (minimum)
- Ultra low leakage current: 5nA (typical)
- Supports high speed interfaces up to 5Gbps
- Industrial temperature range: –40°C to +125°C
- Easy flow-through routing package (ESDS312)

2 Applications

- End equipment:
 - [Ethernet switches](#)
 - [Access points](#)
 - [Gateways](#)
 - [Printers](#)
 - [DVR and NVR](#)
- Interfaces:
 - Ethernet™ 10/100/1000Mbps
 - USB™ 2.0
 - GPIO

3 Description

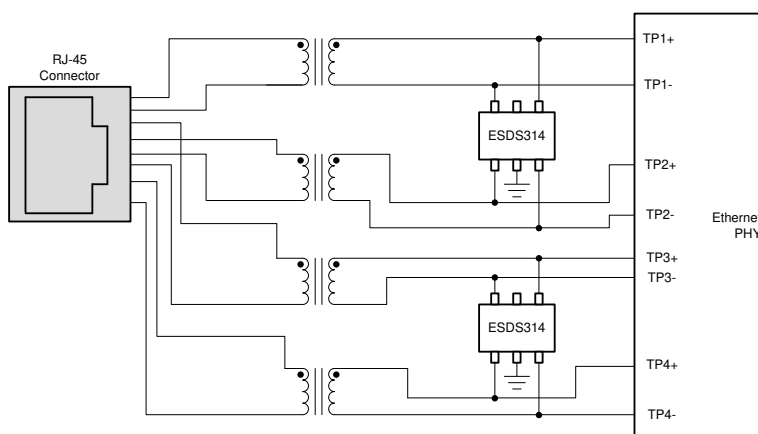
The ESDS31x devices are unidirectional TVS ESD protection diode array for Ethernet, USB and general purpose data line surge protection up to 25A (8/20µs). The ESDS31x devices are rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

The devices feature a 4.5pF IO capacitance per channel making the device an excellent choice for protecting high-speed interfaces such as Ethernet 10/100/1000, USB 2.0 and GPIO. The low dynamic resistance and low clamping voltage provides system level protection against transient events.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE ⁽¹⁾
ESDS311	1 Channel	DYF (SOD323, 2)
ESDS312	2 Channels	DBV (SOT-23, 5)
ESDS314	4 Channels	DBV (SOT-23, 5)

(1) For more information, [Section 10](#)



Typical Application Schematic



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4 Pin Configuration and Functions

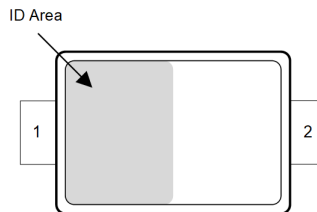


Figure 4-1. ESDS311 DYF, 2-Pin SOD323 (Top View)

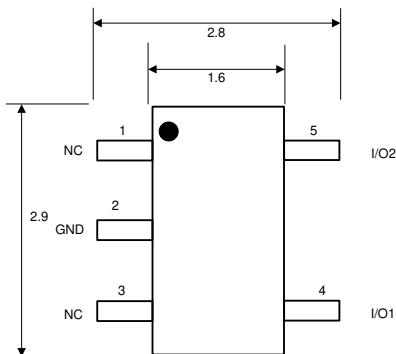


Figure 4-2. ESDS312 DBV Package, 5-Pin SOT23 (Top View)

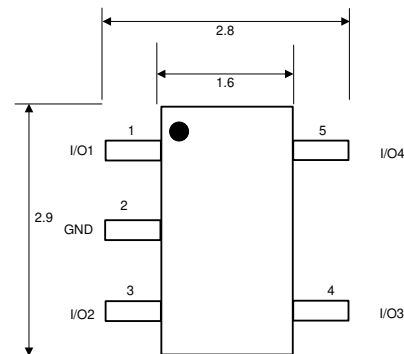


Figure 4-3. ESDS314 DBV Package, 5-Pin SOT23 (Top View)

Table 4-1. Pin Functions for ESDS311

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
I/O	1	I/O	Surge/ESD protected channels. Connect to the lines being protected.
GND	2	GND	Ground. Connect to ground.

Table 4-2. Pin Functions for ESDS312

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
I/O1	4	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	5		
GND	2	GND	Ground. Connect to ground.
NC	1	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	3		

Table 4-3. Pin Functions for ESDS314

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
I/O1	1	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	3		
I/O3	4		
I/O4	5		
GND	2	GND	Ground. Connect to ground

(1) I = input, O = output, NC = no connection, and GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
IEC 61000-4-4 Electrical Fast Transient	Peak Power at 25 °C		80	A
IEC 61000-4-5 Surge (t _p 8/20µs)	Peak Power at 25 °C		170	W
	Peak Current at 25 °C		25	A
T _A	Operating free-air temperature	-40	125	°C
T _{stg}	Storage temperature	-65	155	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - JEDEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all-pins ⁽¹⁾	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	0		3.6	V
T _A	Operating Free Air Temperature	-40		125	°C

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESDS311	ESDS312	ESDS314	UNIT
		DYF (SOD323)	DBV (SOT-23)	DBV (SOT-23)	
		2 PINS	5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	739.2	163.9	127.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	287.7	113.4	78.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	605.5	76.9	43.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	118.4	59.8	24.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	591.1	76.8	43.7	°C/W

5.5 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		ESDS311	ESDS312	ESDS314	UNIT
		DYF (SOD323)	DBV (SOT-23)	DBV (SOT-23)	
		2 PINS	5 PINS	5 PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics

At T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	Device	MIN	TYP	MAX	UNIT	
V _{RWM}	Reverse stand-off voltage	I _{IO} < 500nA, across operating temperature range				3.6	V	
I _{LEAKAGE}	Leakage current at 3.6V	V _{IO} = 3.6V, Any IO pin to GND			5	50	nA	
V _{BRF}	Breakdown voltage, IO to GND ⁽¹⁾	I _{IO} = 1mA		4.5		7.5	V	
V _{FWD}	Forward Voltage, GND to IO	I _{IO} = 1mA			0.8		V	
V _{HOLD}	Holding Voltage, IO to GND ⁽²⁾	I _{IO} = 1mA			5		V	
V _{CLAMP}	Surge Clamping voltage, t _p = 8/20μs	I _{PP} = 1A, Any IO pin to GND	ESDS312/314		5		V	
V _{CLAMP}		I _{PP} = 12A, Any IO pin to GND	ESDS311		6.3		V	
V _{CLAMP}			ESDS312/314		5.6			
V _{CLAMP}		I _{PP} = 25A, Any IO pin to GND	ESDS311		7.7		V	
V _{CLAMP}			ESDS312/314		6.5			
V _{CLAMP}		I _{PP} = 1A, GND to any IO pin	ESDS312/314		1		V	
V _{CLAMP}			I _{PP} = 12A, GND to any IO pin	ESDS311		3		V
V _{CLAMP}				ESDS312/314		2.1		
V _{CLAMP}		I _{PP} = 25A, GND to any IO pin	ESDS311		4.9		V	
V _{CLAMP}			ESDS312/314		3.6			
V _{CLAMP}	I _{PP} = 16A, Any IO pin to GND		ESDS311		6.5			V
V _{CLAMP}		ESDS312/314		5.5				
V _{CLAMP}	TLP Clamping Voltage, t _p = 100ns	I _{PP} = 16A, GND to any IO pin	ESDS311		3.4		V	
V _{CLAMP}			ESDS312/314		2.2			
C _{LINE}	Line capacitance, Any IO to GND	V _{IO} = 0V, V _{p-p} = 30mV, f = 1MHz			4.5	5.5	pF	
ΔC _{LINE}	Variation of line capacitance	C _{LINE1} - C _{LINE2} , V _{IO} = 0V, V _{p-p} = 30mV, f = 1MHz	ESDS312/314		0.05	0.1	pF	
C _{CROSS}	Line-to-line capacitance	V _{IO} = 0V, V _{rms} = 30mV, f = 1MHz	ESDS312/314		2.25	2.75	pF	

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1mA is applied, after the device has successfully latched into the snapback state.

5.7 Typical Characteristics

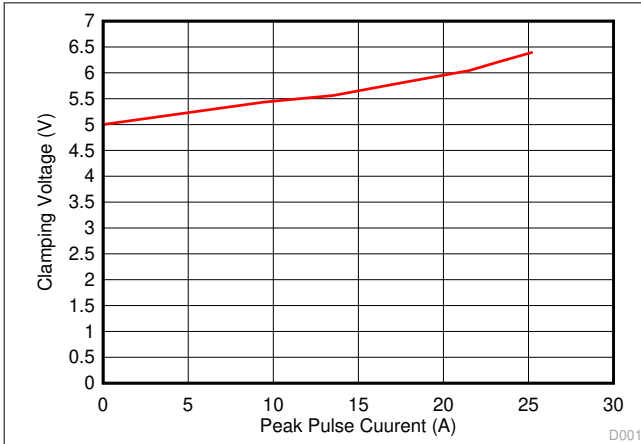


Figure 5-1. Clamping Voltage vs. Peak Pulse Current ($t_p = 8/20\mu s$), Any IO Pin to GND

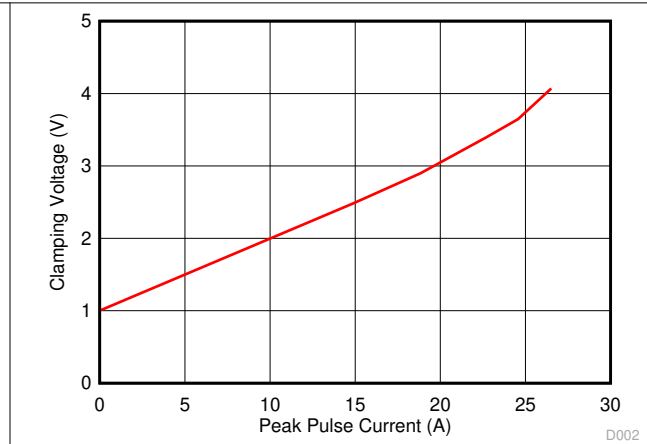


Figure 5-2. Clamping Voltage vs. Peak Pulse Current ($t_p = 8/20\mu s$), GND to Any IO Pin

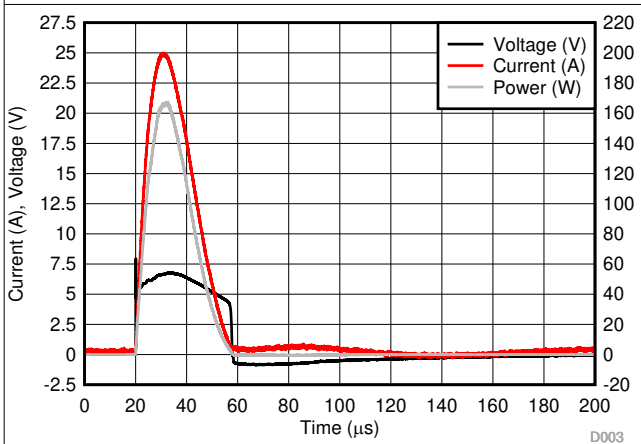


Figure 5-3. Surge Current, Clamping Voltage and Power Curve ($t_p = 8/20\mu s$), Any IO Pin to GND

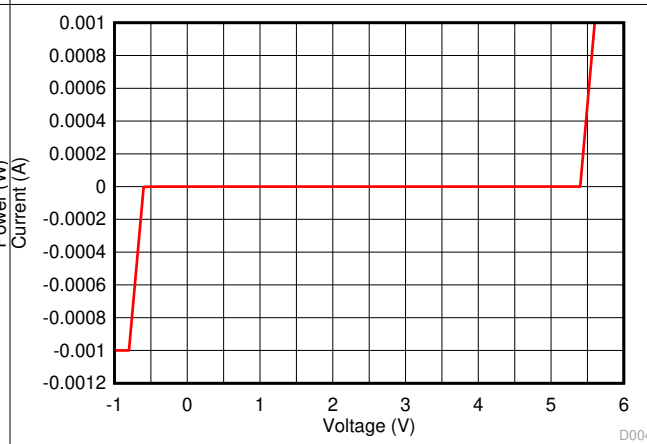


Figure 5-4. DC I-V Curve

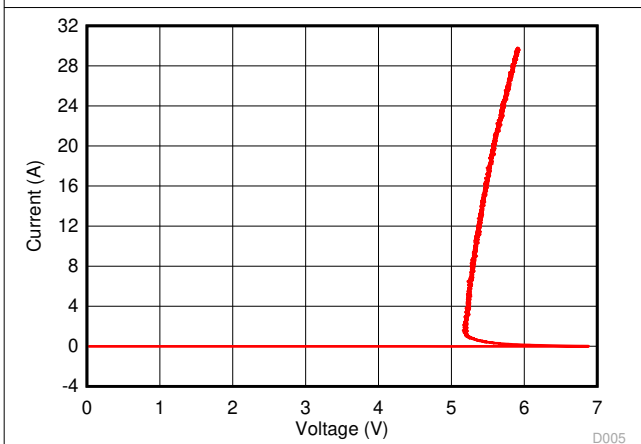


Figure 5-5. TLP I-V Curve, IO to GND, $t_p = 100ns$

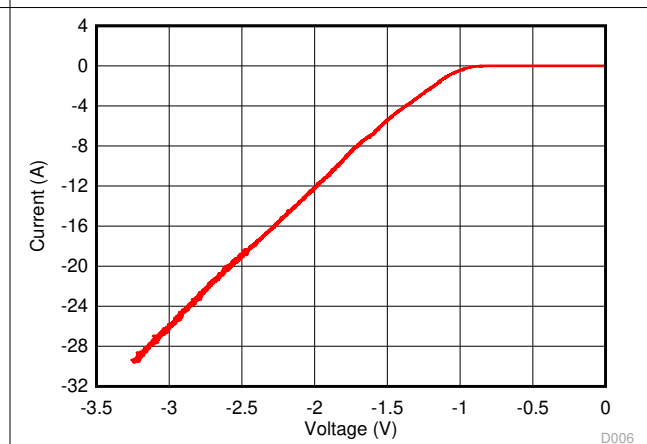
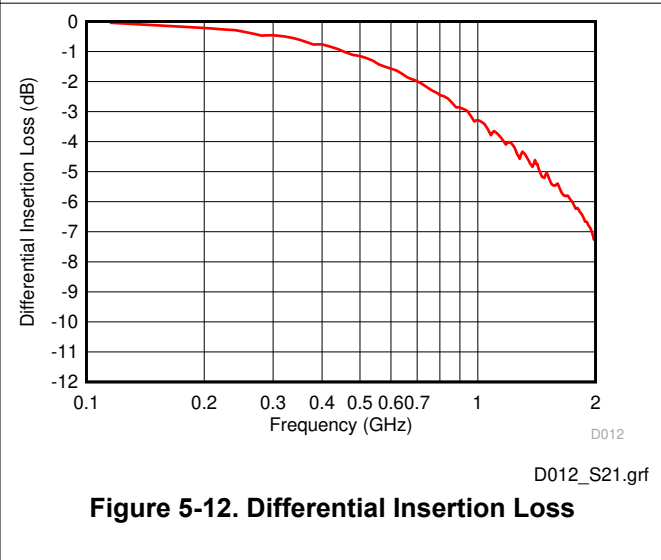
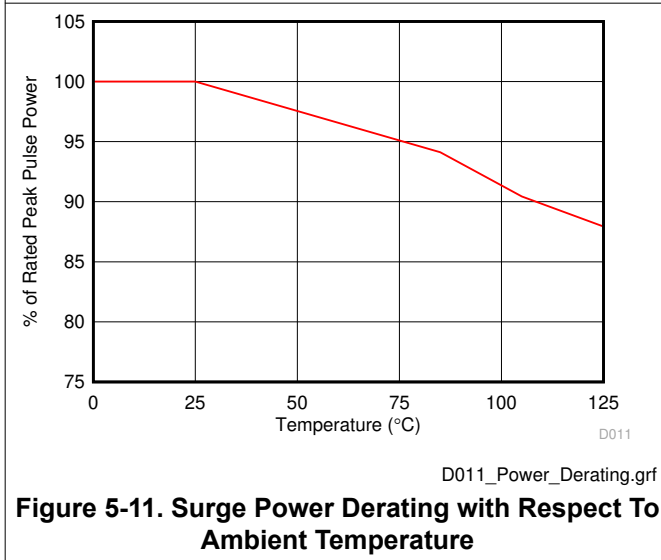
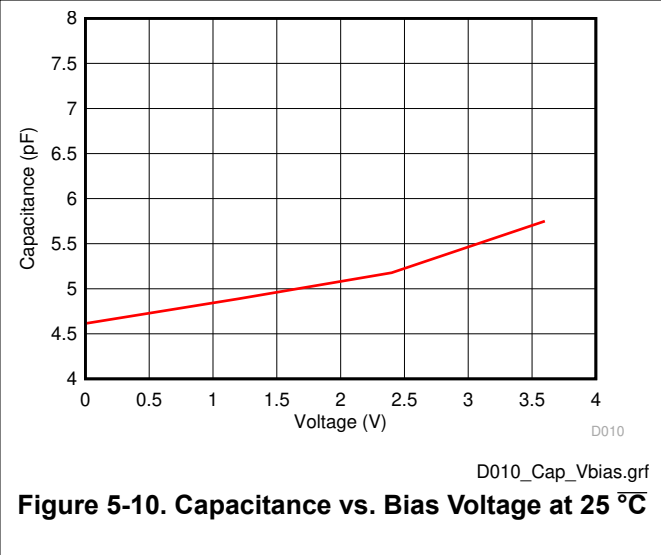
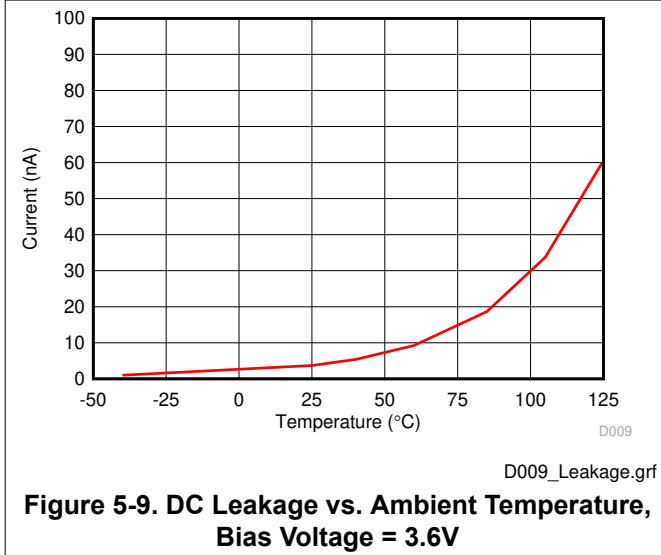
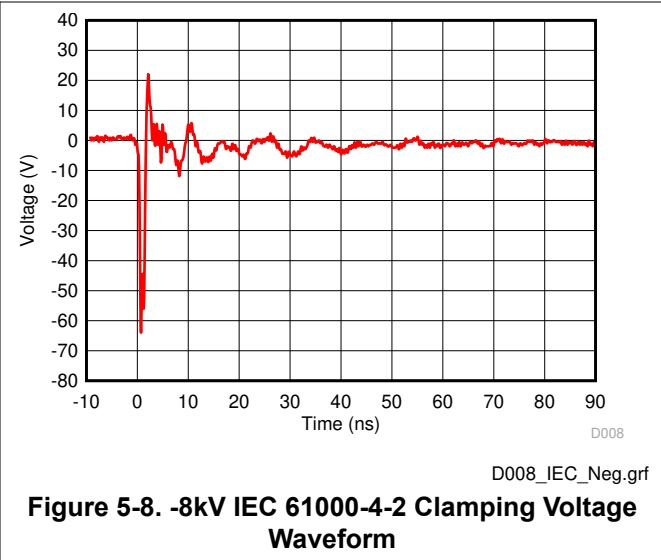
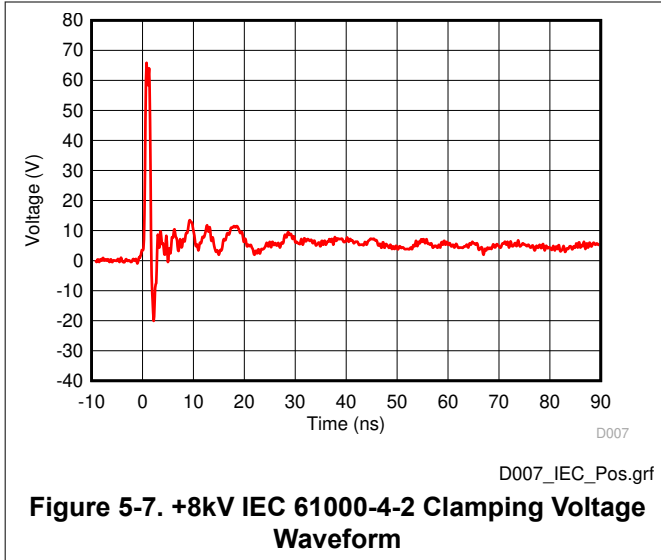


Figure 5-6. TLP I-V Curve, IO to GND Negative, $t_p = 100ns$

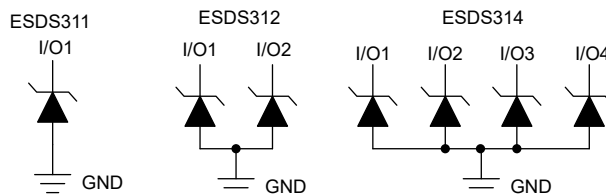


6 Detailed Description

6.1 Overview

The ESDS31x devices are unidirectional ESD Protection Diodes with a low capacitance. These devices can dissipate high surge currents up to 25A (8/20 μ s) and ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The low capacitance makes this device an excellent choice for protecting high-speed signal interfaces such as Ethernet 10/100/1000Mbps and general purpose high speed data lines.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 IEC 61000-4-4 EFT Protection

The I/O pins of ESDS311, ESDS312, and ESDS314 can withstand surge events (IEC 61000-4-5, 8/20 μ s waveform) up to 25A and 170W. These devices also provide ESD protection up to ± 30 kV contact and ± 30 kV air gap per IEC 61000-4-2 standard. The I/O pins can withstand an electrical fast transient (EFT) burst of up to 80A (IEC 61000-4-4 5/50ns waveform, 4kV with 50 Ω impedance). The capacitance between each I/O pin to ground is 4.5pF (typical) and 5.5pF (maximum). This device supports data rates up to 1Gbps.

The reverse DC breakdown voltage of each I/O pin is a minimum of 4.5V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 3.6V. The I/O pins feature an ultra-low leakage current of 100nA (maximum) with a bias of 3.6V. This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

6.4 Device Functional Modes

The ESDS31x devices are a passive integrated circuit that triggers when voltages are above V_{BRF} or below 0.7V. During ESD events, voltages as high as ± 30 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESDS31x (usually within a few nano-seconds) the devices reverts to passive.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESDS31x devices are a diode type TVS which is used to provide a path to ground for dissipating surge and ESD events on high-speed signal lines between a human interface connector and a system. As the current from surge or ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

7.2 Typical Application

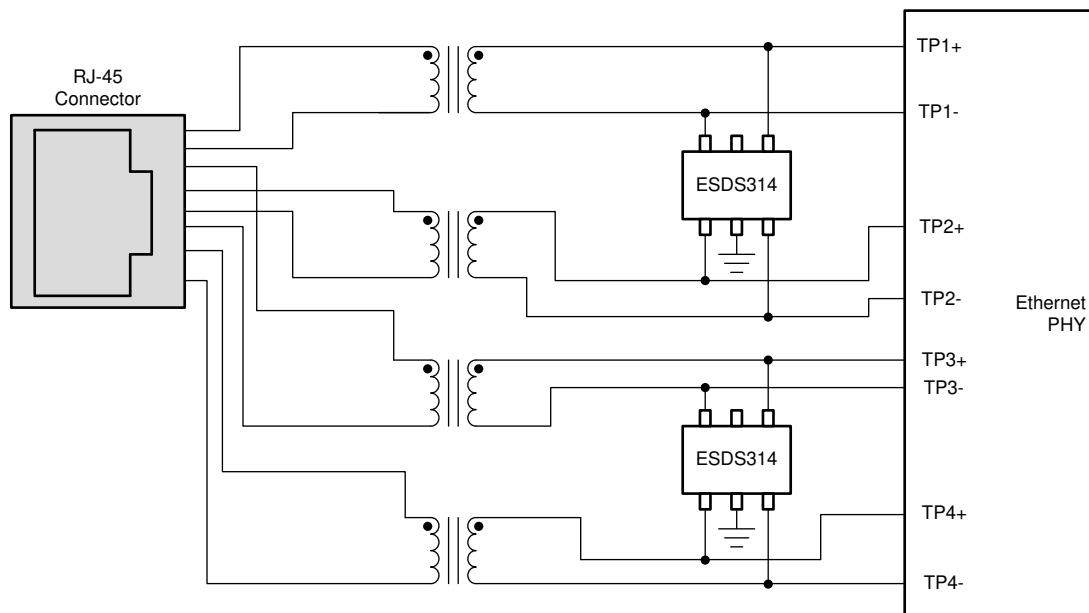


Figure 7-1. ESDS314 Protecting the Ethernet 1Gbps Interface

7.2.1 Design Requirements

A typical operation for the ESDS314 would be protecting a high speed dataline similar to one shown in [Figure 7-1](#). In this example, the ESDS314 is protecting an Ethernet PHY's data lines that has a nominal operating voltage of 3.6V. Many of the Ethernet interfaces that connect to long cables require protection against $\pm 1kV$ surge test through a 42Ω coupling resistor and a $0.5\mu F$ capacitor, equaling roughly 24A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition, this input voltage will rise to hundreds of volts for multiple microseconds, harming the device.

For Ethernet 1000Base-T (1Gbps), application design parameters listed in [Table 7-1](#) are known.

Table 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on differential data line pairs	0 to 3.6V
Operating frequency	125MHz

7.2.2 Detailed Design Procedure

7.2.2.1 Signal Range

The ESDS314 has 4 identical surge protection channels with each channel supporting a signal range of 0 to 3.6V. The device will work well with any Ethernet PHY that drives the single ended voltage on the data line up to a 3.6V.

7.2.2.2 Operating Frequency

The ESDS314 has a capacitance of 4.5pF (typical) and can support the 125MHz operation of Ethernet 1000Base-T application

7.2.3 Application Curves

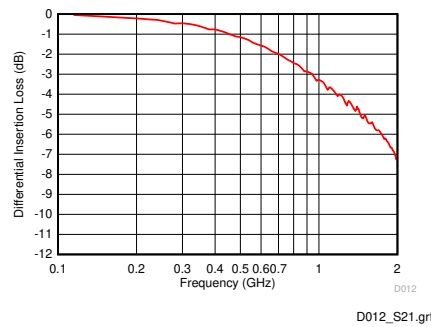


Figure 7-2. Differential Insertion Loss vs. Frequency

7.3 Power Supply Recommendations

The ESDS314, ESDS312 devices are passive ESD devices and there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

7.4.2 Layout Example

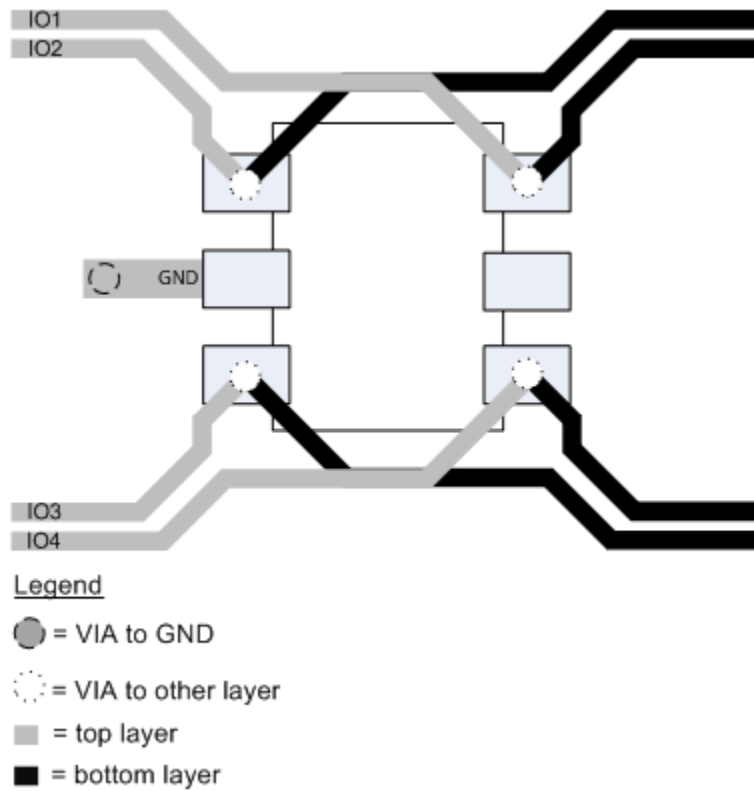


Figure 7-3. Layout Example for 4-channel Device

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

Ethernet™ is a trademark of Xerox Corporation.

USB™ is a trademark of USB Implementers Forum.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2018) to Revision C (February 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Added the ESDS311 device to the data sheet..... 1

Changes from Revision A (July 2018) to Revision B (September 2018) **Page**

- Changed from Advanced Information to Production Data 1

Changes from Revision * (May 2018) to Revision A (July 2018)	Page
• Changed from Product Preview to Advance Information.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESDS311DYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	370F	Samples
ESDS312DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1R4B	Samples
ESDS314DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1R2B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS311DYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
ESDS312DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
ESDS314DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS311DYFR	SOT	DYF	2	3000	210.0	200.0	42.0
ESDS312DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
ESDS314DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

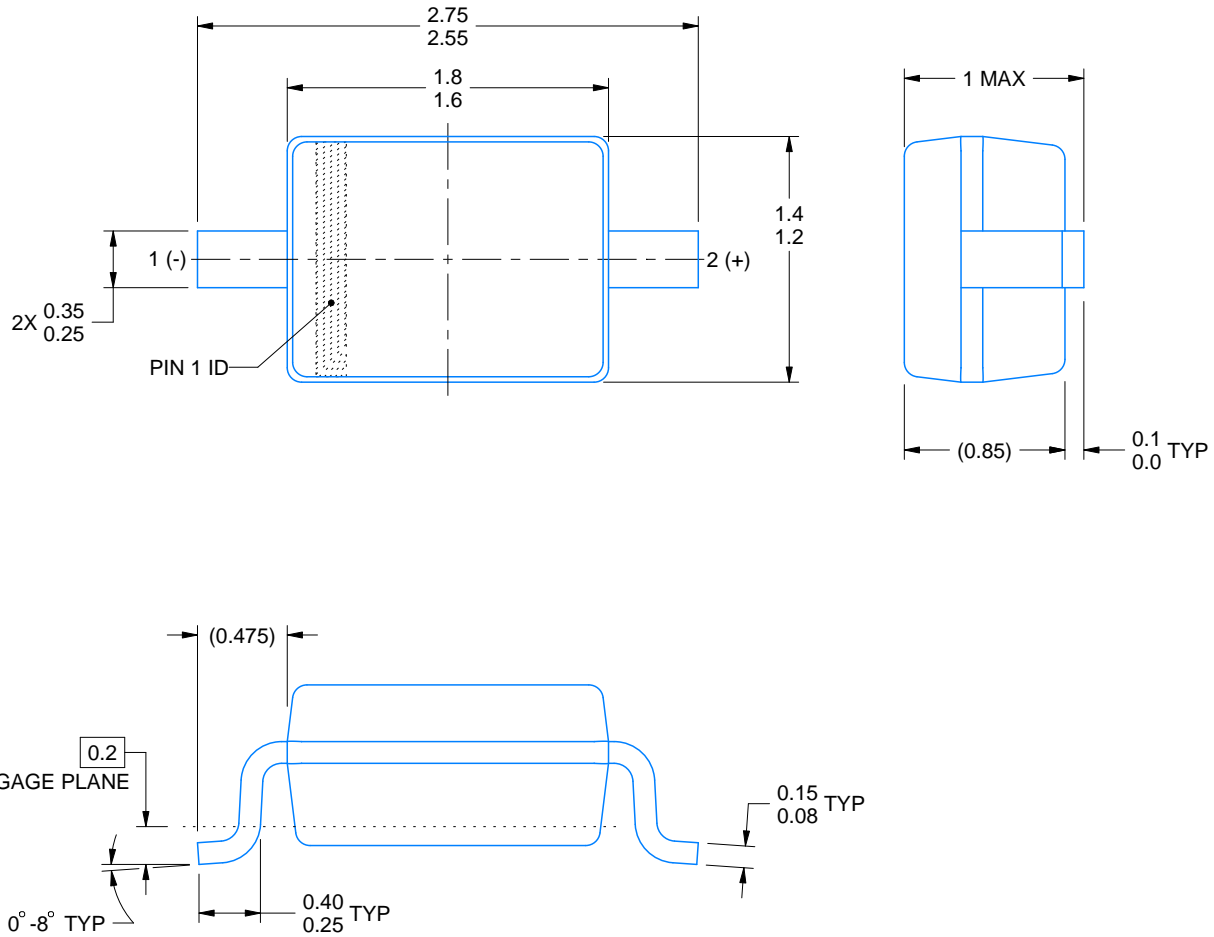
DYF0002A



PACKAGE OUTLINE

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

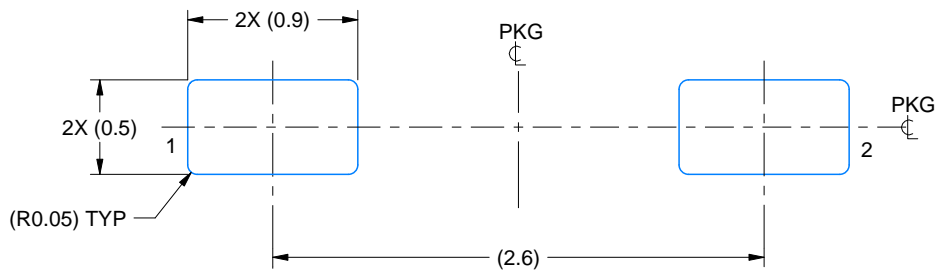
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

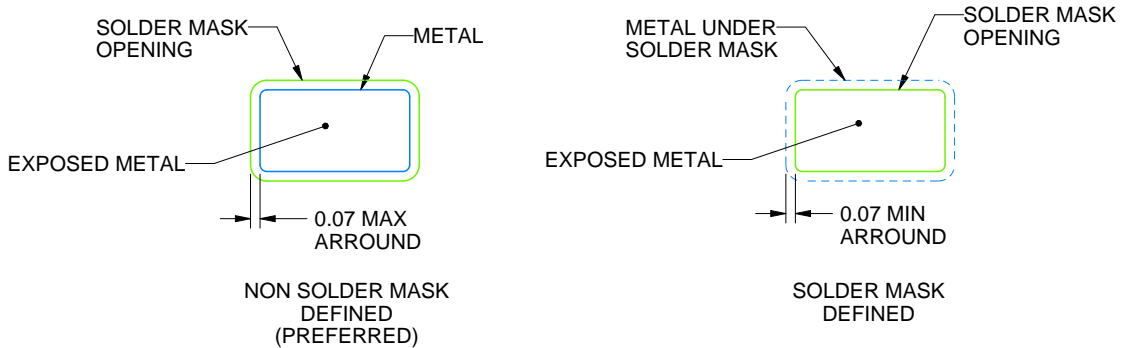
DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

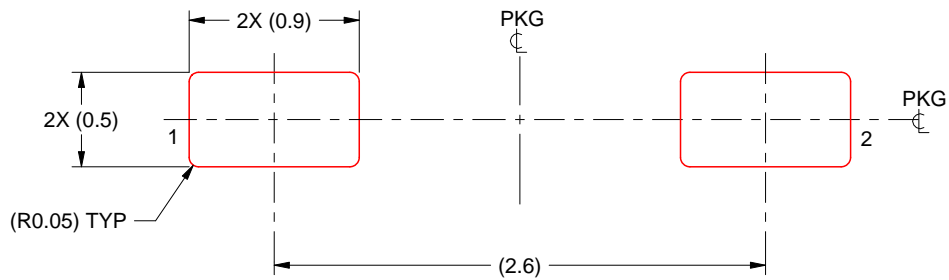
- 3. Publication IPC-7351 may have alternate designs.
- 4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR

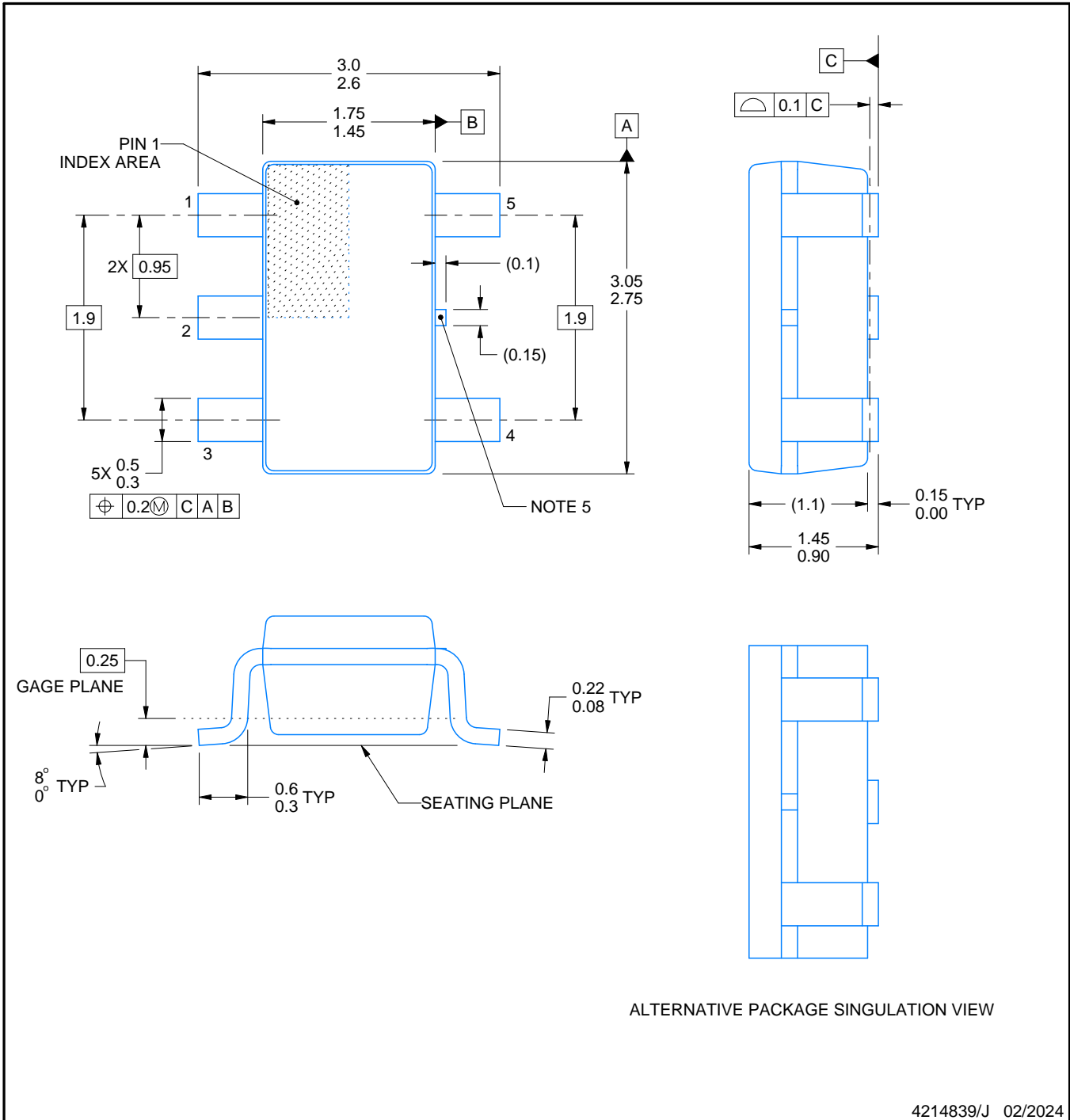


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

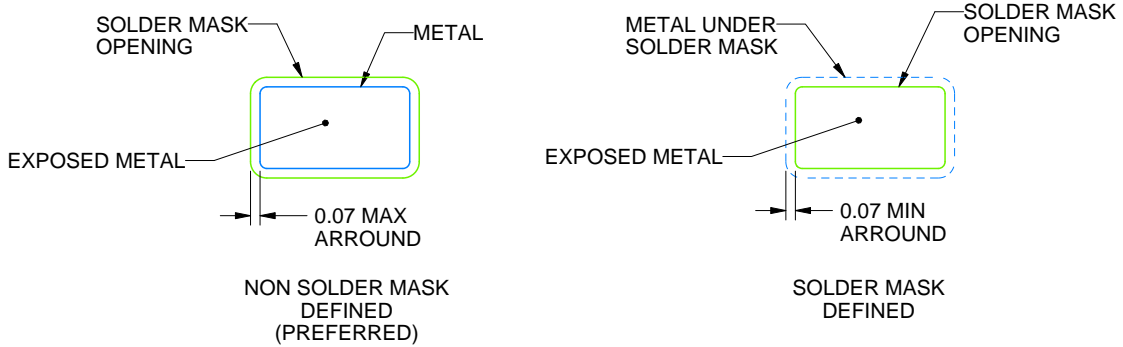
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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