CSD19537Q3 100-V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Lead free terminal plating
- RoHS compliant
- Halogen free
- SON 3.3-mm × 3.3-mm plastic package

2 Applications

- Primary Side Isolated Converters
- Motor Control

3 Description

This 100-V, 12.1-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

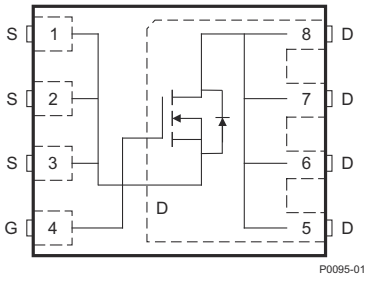


Figure 3-1. Top View

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10 V)	16		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.9		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V	13.8	mΩ
		V_{GS} = 10 V	12.1	mΩ
$V_{GS(th)}$	Threshold Voltage	3		V

Ordering Information[1]

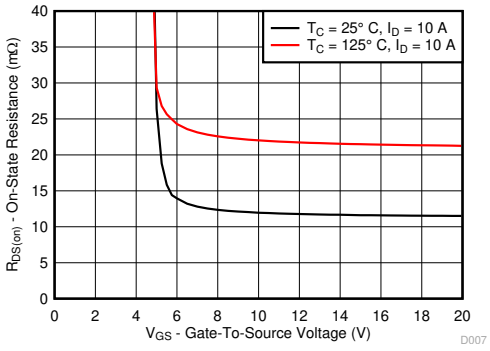
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD19537Q3	13-Inch Reel	2500	SON 3.3- x 3.3-mm Plastic Package	Tape and Reel
CSD19537Q3T	13-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

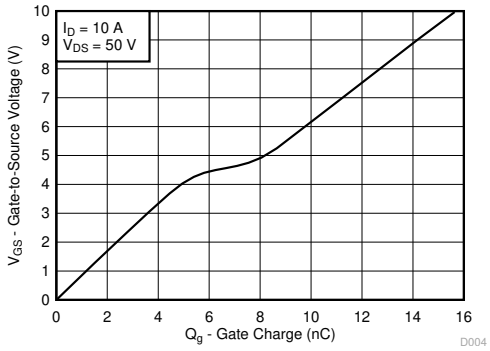
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	50	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	53	A
	Continuous Drain Current [1]	9.7	A
I_{DM}	Pulsed Drain Current [2]	219	A
P_D	Power Dissipation [1]	2.8	W
	Power Dissipation, T_C = 25°C	83	W
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 33 A, L = 0.1 mH, R_G = 25 Ω	55	mJ

(1) Typical $R_{\theta JA}$ = 45°C/W on a 1-in², 2-oz Cu pad on a 0.06-in thick FR4 PCB.
(2) Max $R_{\theta JC}$ = 1.5°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Revision History

Changes from Revision A (May 2016) to Revision B (November 2022) **Page**

- Corrected legend on Figure 5-11 4

Changes from Revision * (August 2015) to Revision A (May 2016) **Page**

- Corrected typo in X axis legend on Figure 5-11 4

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

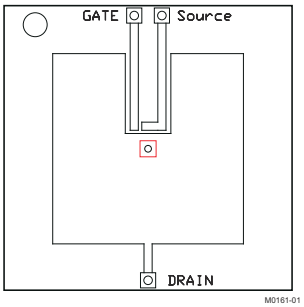
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 80 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.6	3	3.6	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V, I_D = 10 A		13.8	16.6	mΩ
		V_{GS} = 10 V, I_D = 10 A		12.1	14.5	mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 10 A		45		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz		1290	1680	pF
C_{oss}	Output capacitance			251	326	pF
C_{rss}	Reverse transfer capacitance			13.3	17.3	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 50 V, I_D = 10 A		16	21	nC
Q_{gd}	Gate charge gate-to-drain			2.9		nC
Q_{gs}	Gate charge gate-to-source			5.5		nC
$Q_{g(th)}$	Gate charge at V_{th}			3.8		nC
Q_{oss}	Output charge	V_{DS} = 50 V, V_{GS} = 0 V		44		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 10 A, R_G = 0 Ω		5		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turn off delay time			10		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 10 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50 V, I_F = 10 A, di/dt = 300 A/µs		134		nC
t_{rr}	Reverse recovery time			36		ns

5.2 Thermal Information

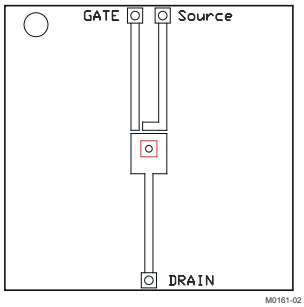
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (1)			1.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance, Note 1 and Note 2 (1) (2)			55	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 160°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

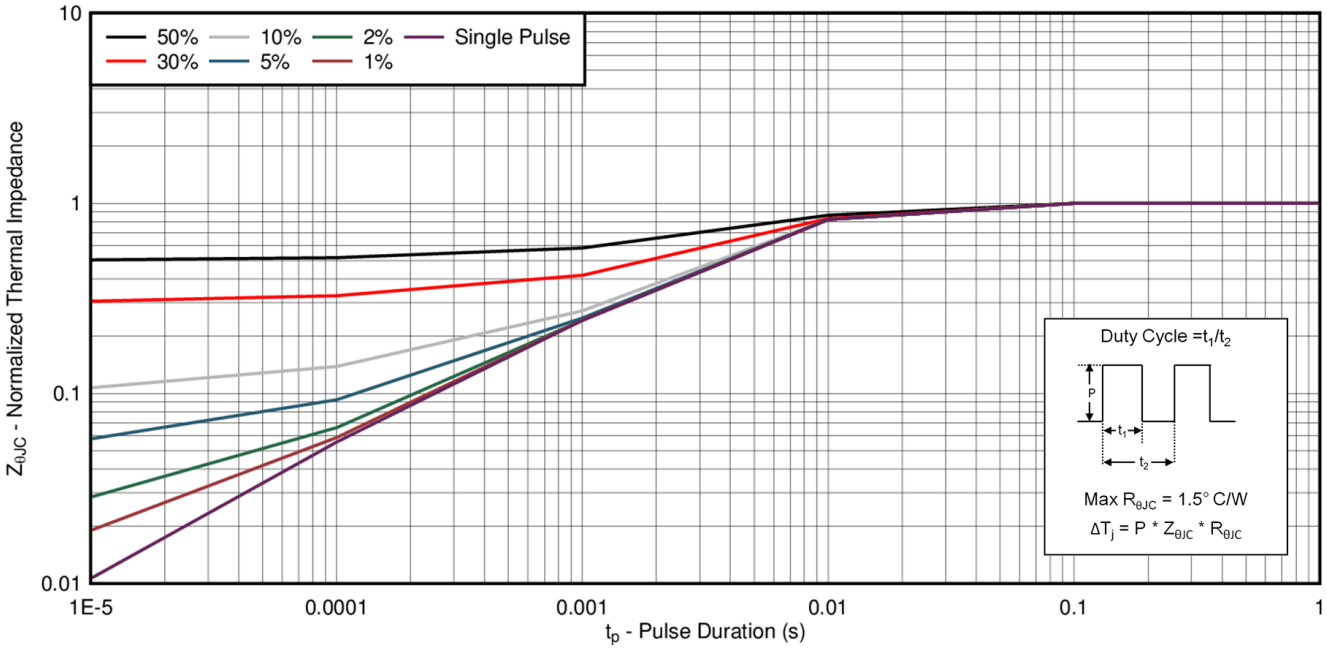


Figure 5-1. Transient Thermal Impedance

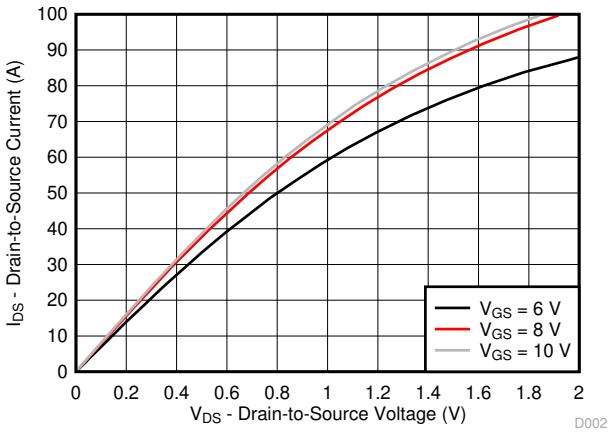
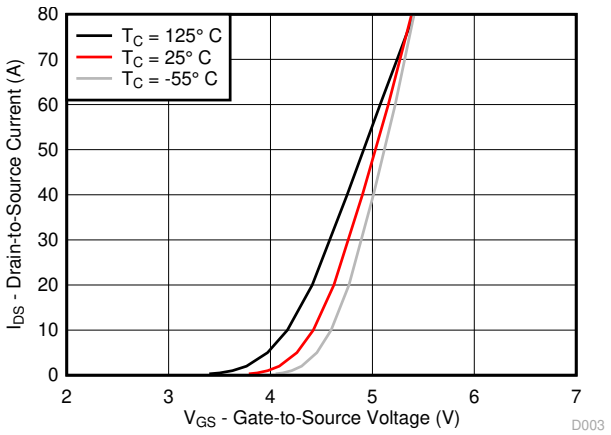
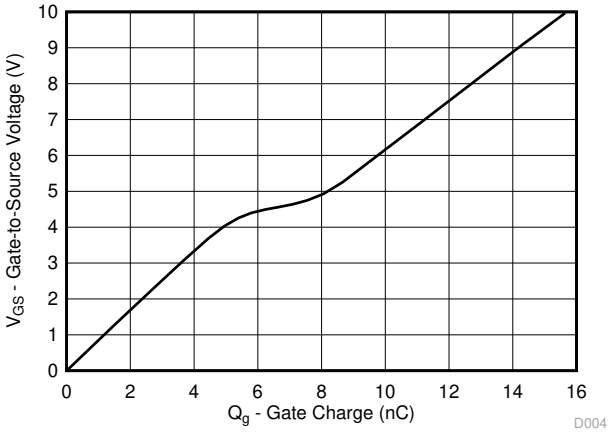


Figure 5-2. Saturation Characteristics



V_{DS} = 5 V

Figure 5-3. Transfer Characteristics



I_D = 10 A V_{DS} = 50 V

Figure 5-4. Gate Charge

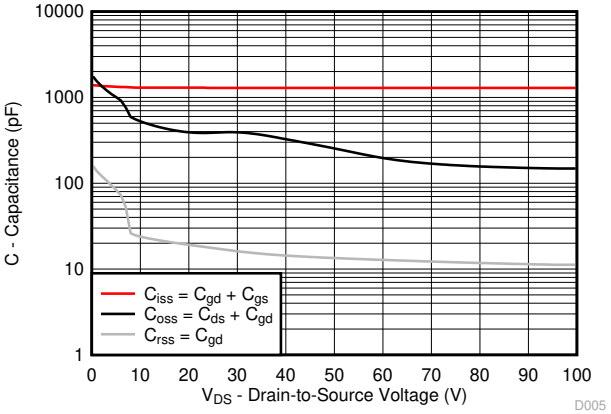
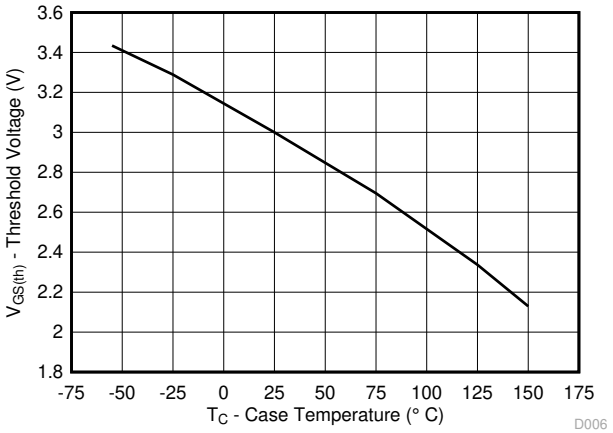


Figure 5-5. Capacitance



I_D = 250 µA

Figure 5-6. Threshold Voltage vs Temperature

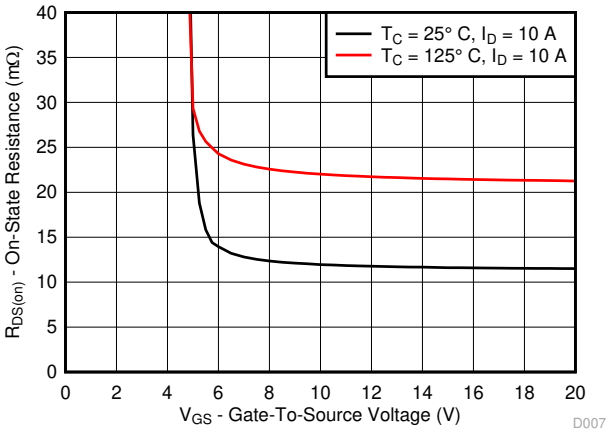
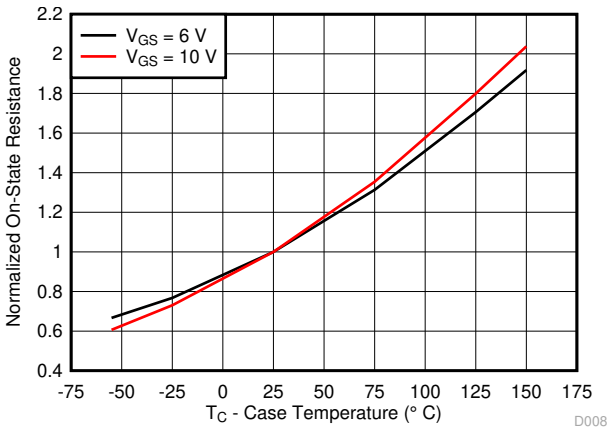


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 10 A

Figure 5-8. Normalized On-State Resistance vs Temperature

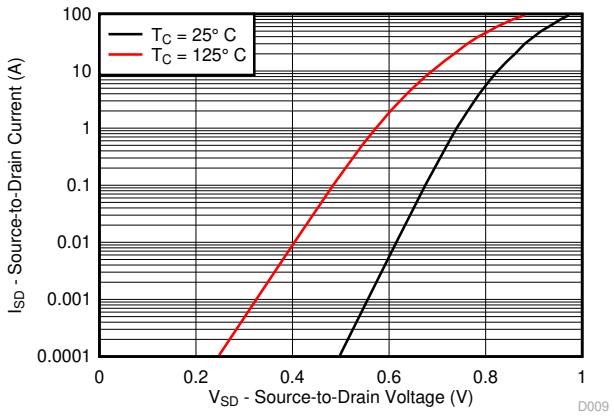
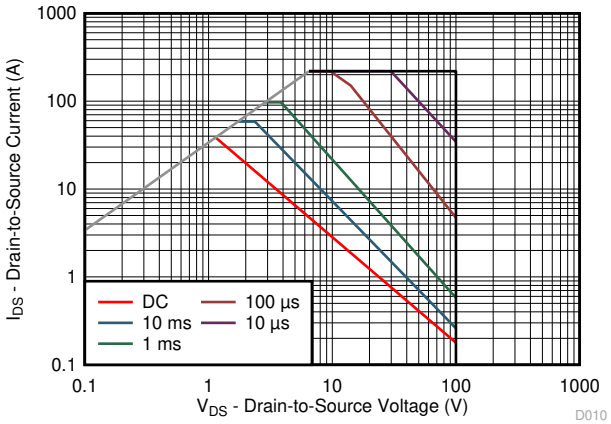


Figure 5-9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JC}$ = 1.5°C/W

Figure 5-10. Maximum Safe Operating Area

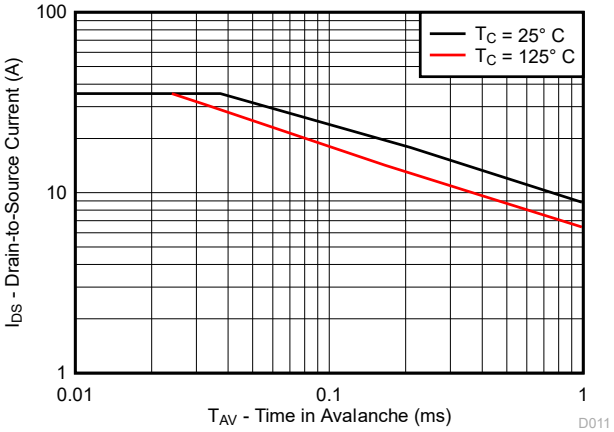


Figure 5-11. Single Pulse Unclamped Inductive Switching

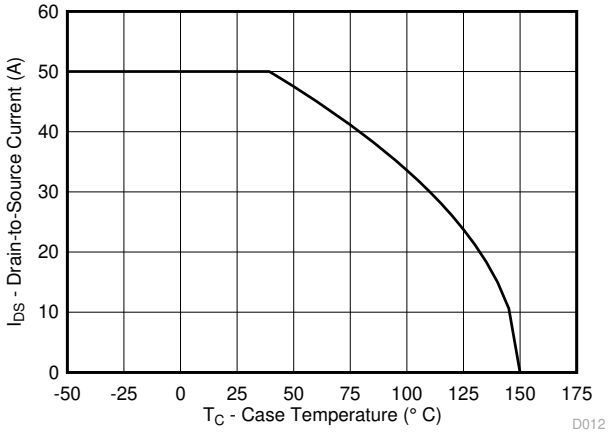


Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET™ is a trademark of Texas Instruments.
E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

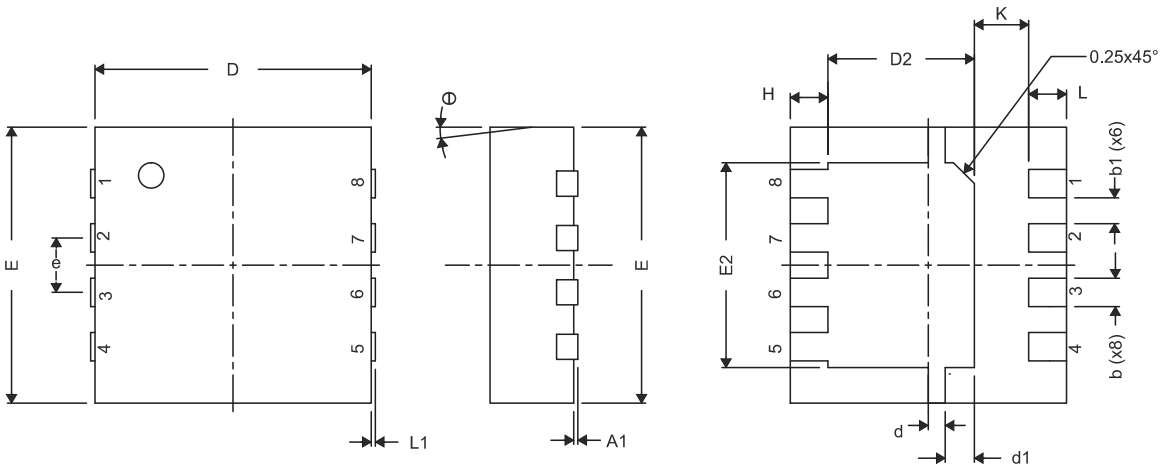
6.4 Glossary

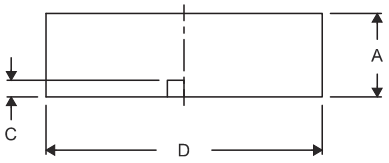
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

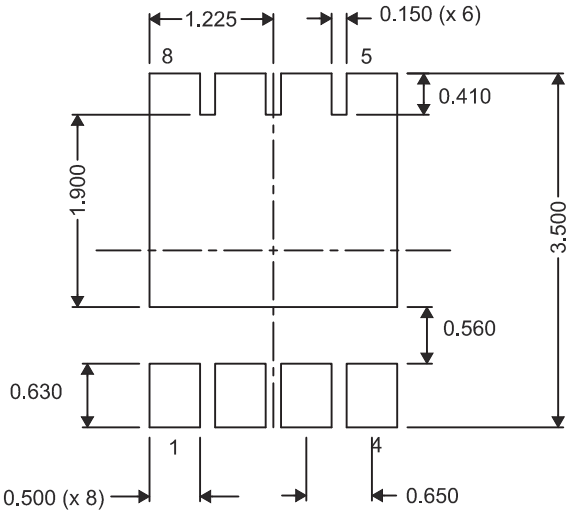
7.1 Q3 Package Dimensions





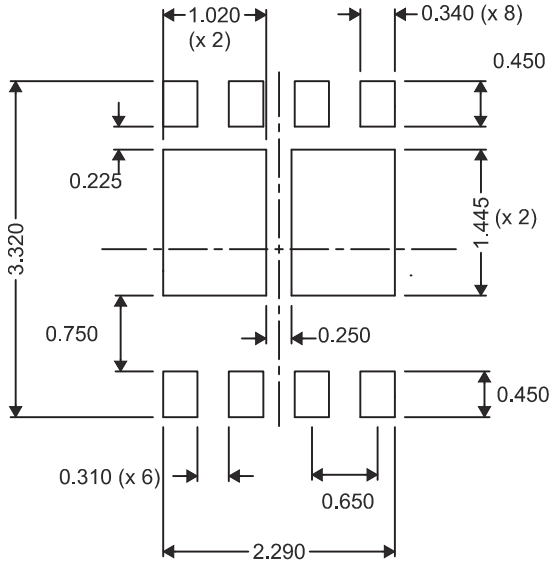
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310 NOM			0.012 NOM	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 TYP			0.026 TYP	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 TYP			0.026 TYP	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



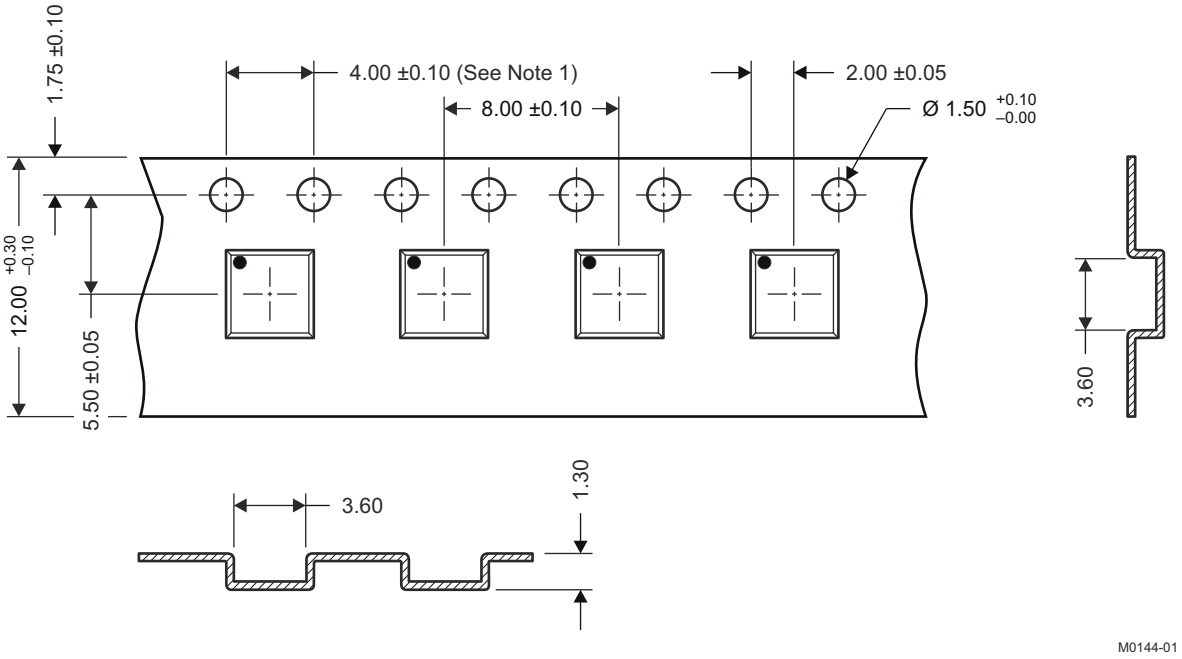
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19537Q3	ACTIVE	VSON-CLIP	DQG	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537	Samples
CSD19537Q3T	ACTIVE	VSON-CLIP	DQG	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

单击下面可查看定价，库存，交付和生命周期等信息

>>TI(德州仪器)