SN74LVC1G17-Q1 Single Schmitt-Trigger Buffer

1 Features

- Qualified for Automotive Applications
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Max t_{pd} of 8 ns at 3.3 V
- Low power consumption, 20-μA Max I_{CC}
- ±24-mA Output drive at 3.3 V
- I_{off} Supports live insertion, partial-power-down mode, and back-drive protection
- ESD protection exceeds JEDEC JS-001
  - 2000-V Human-body model
  - 1000-V Charged-device model

2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- MP3 player/recorder
- Personal digital assistant (PDA)
- Power: Telecom/server AC/DC supply: single controller: analog and digital
- Solid state drive (SSD): client and enterprise
- TV: LCD/Digital and high-definition (HDTV)
- Tablet: Enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

3 Description

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G17-Q1 device contains one buffer and performs the Boolean function Y = A.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

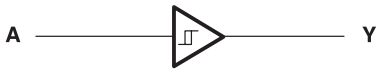
The SN74LVC1G17-Q1 is available in a variety of packages.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G17-Q1	SOT-23 (5)	2.9 mm × 1.6 mm
	SC-70 (5)	2.0 mm × 1.25 mm
	SON (6)	1.45 mm × 1.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2019) to Revision C — **Page**

- Corrected clerical errors introduced in Revision B: Features included incorrect values ... 1
- Changed to automotive ESD table format ... 4
- Corrected clerical errors introduced in Revision B: Electrical Characteristics values returned to Revision A values ... 6
- Corrected clerical errors introduced in Revision B: Switching Characteristics values returned to Revision A values ... 6
- Deleted inaccurate typical characteristics plot for operation across temperature. ... 7
- Deleted unnecessary parameter measurement information for 15 pF load (unused). ... 8

Changes from Revision A (April 2008) to Revision B — **Page**

- Added *Applications*. ... 1
- Added *Device Information* table. ... 1
- Removed Ordering Information table. ... 3
- Added DRY package to graphic figures and Pin Functions table ... 3
- Added Pin Functions table. ... 3
- Added ESD Ratings table. ... 4
- Added Thermal Information table. ... 5
- Added Typical Characteristics. ... 7
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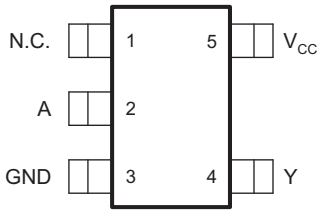
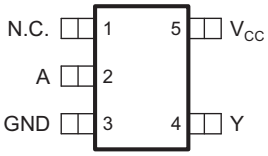
- Added Layout section. ... 11
- Added *Device and Documentation Support* section ... 12
- Added *Mechanical, Packaging, and Orderable Information* section ... 12

5 Pin Configuration and Functions

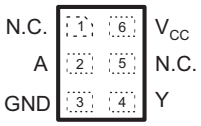
DBV Package
5-Pin SOT-23
Top View



DCK Package
5-Pin SC-70
Top View



DRY Package
6-Pin SON
Transparent Top View



(1) N.C. - No internal connection

See mechanical drawings for at the end of the data sheet for dimensions

Pin Functions

PIN			DESCRIPTION
NAME	DBV, DCK	DRY	
NC	1	1, 5	Not connected
A	2	2	Input
GND	3	3	Ground
Y	4	4	Output
V_{CC}	5	6	Power terminal

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G17-Q1			UNIT
		DBV	DCK	DRY	
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	280	608	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164	66	432	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	67	446	°C/W
ψ_{JT}	Junction-to-top characterization parameter	44	2	191	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62	66	442	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	198	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+} (Positive-going input threshold voltage)		1.65 V	0.64		1.25	V
		2.3 V	1		1.68	
		3 V	1.36		2.04	
		4.5 V	2.07		2.86	
		5.5 V	2.53		3.43	
V_{T-} (Negative-going input threshold voltage)		1.65 V	0.23		0.71	V
		2.3 V	0.44		1.05	
		3 V	0.77		1.35	
		4.5 V	1.22		2.09	
		5.5 V	1.73		2.52	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.26		0.74	V
		2.3 V	0.33		0.92	
		3 V	0.4		0.99	
		4.5 V	0.45		1.28	
		5.5 V	0.56		1.32	
V_{OH}	I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –4 mA	1.65 V	1.2			
	I_{OH} = –8 mA	2.3 V	1.9			
	I_{OH} = –16 mA	3 V	2.4			
	I_{OH} = –24 mA		2.3			
	I_{OH} = –32 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45	
	I_{OL} = 8 mA	2.3 V			0.4	
	I_{OL} = 16 mA	3 V			0.5	
	I_{OL} = 24 mA				0.7	
	I_{OL} = 32 mA	4.5 V			0.7	
I_I A input	V_I = 5.5 V or GND	0 to 5.5 V			±10	µA
I_{off}	V_I or V_O = 5.5 V	0			±25	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			20	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_I	V_I = V_{CC} or GND	3.3 V		4.5		pF

6.6 Switching Characteristics AC Limit

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.8	14	1	9	1.5	8	0.7	7	ns

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	20	21	22	26	pF

6.8 Typical Characteristics

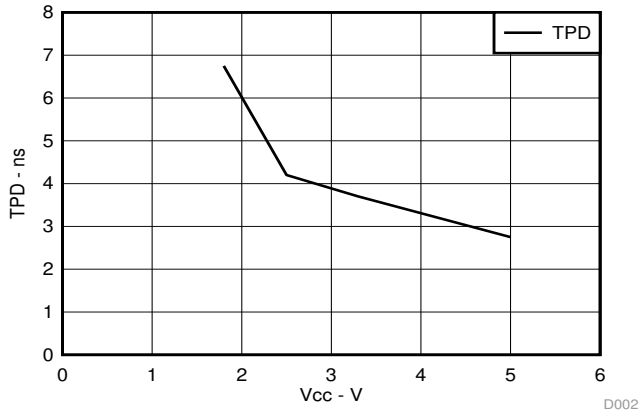
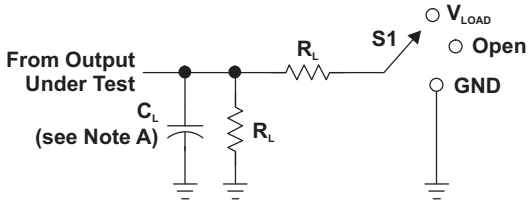


Figure 1. Across Vcc at 25°C

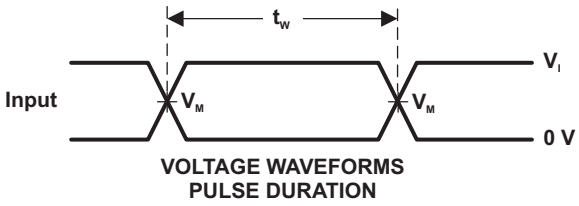
7 Parameter Measurement Information



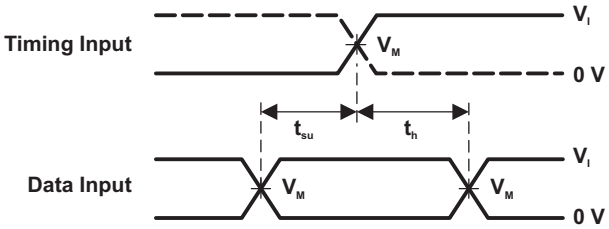
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

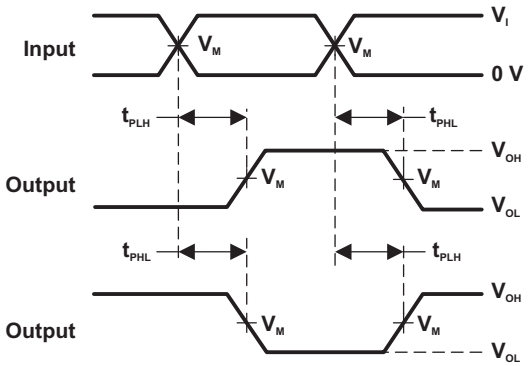
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



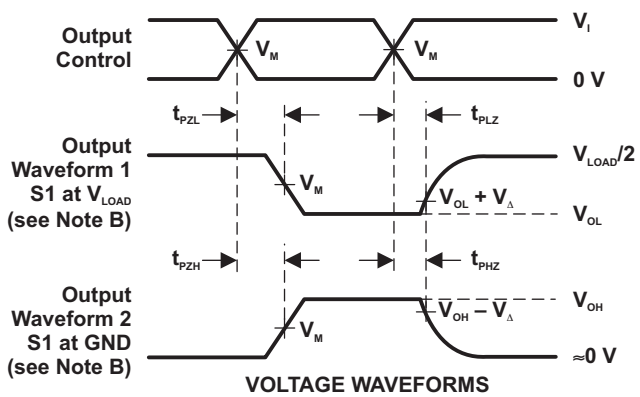
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

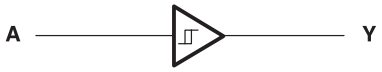
8 Detailed Description

8.1 Overview

The SN74LVC1G17-Q1 device contains one Schmitt trigger buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of Schmitt action, it will have different input threshold levels for a positive-going (V_{T+}) and negative-going (V_{T-}) signals .

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range.
  - Operates From 1.65 V to 5.5 V.
- Allows Down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G17-Q1 is a high-drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC}.

9.2 Typical Application

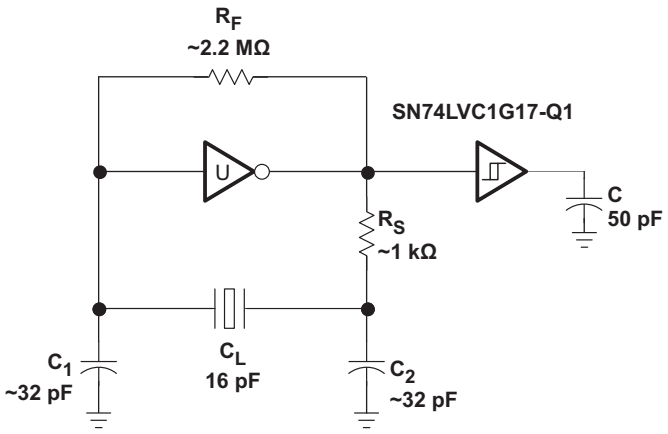


Figure 3. SN74LVC1G17-Q1 Typical Application

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the
   - *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the
   - *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the
   - *Recommended Operating Conditions* table at any valid V_{CC} .
2. Recommend Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the
   - *Absolute Max Ratings* table.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curves

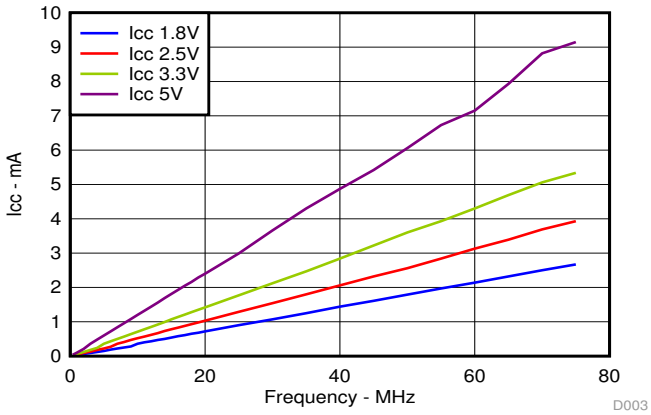


Figure 4. ICC vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

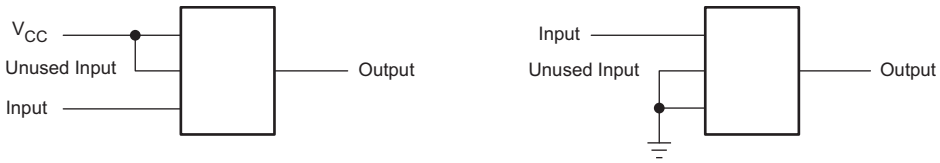
Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-μF capacitor is recommended and if there are multiple Vcc pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G17QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17O	Samples
SN74LVC1G17QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C7J, C7O)	Samples
SN74LVC1G17QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G17-Q1 :

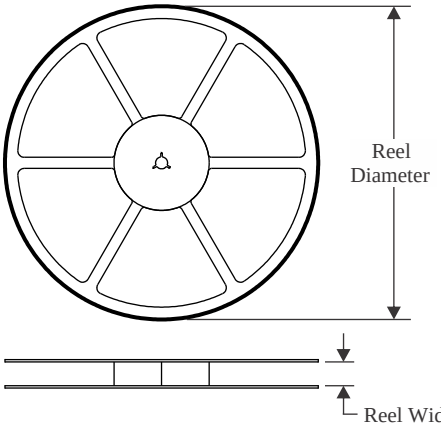
- Catalog : SN74LVC1G17
- Enhanced Product : SN74LVC1G17-EP

NOTE: Qualified Version Definitions:

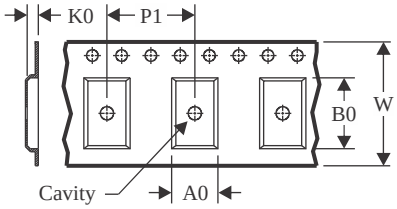
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

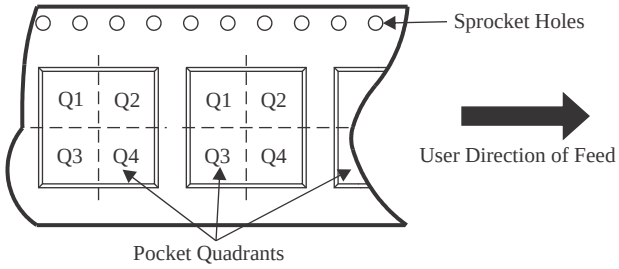


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

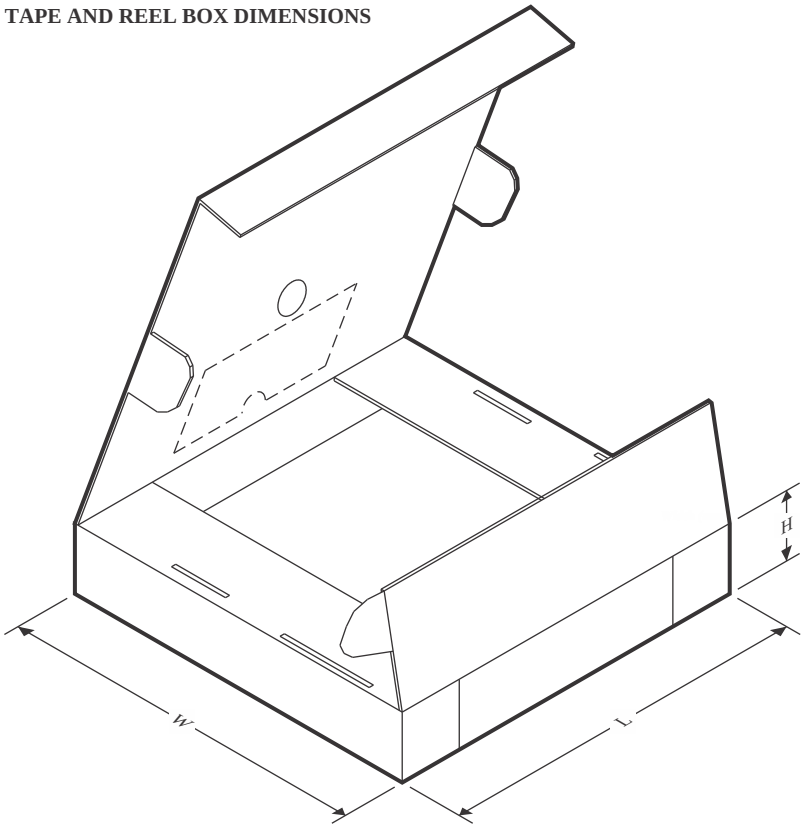
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G17QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74LVC1G17QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G17QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G17QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

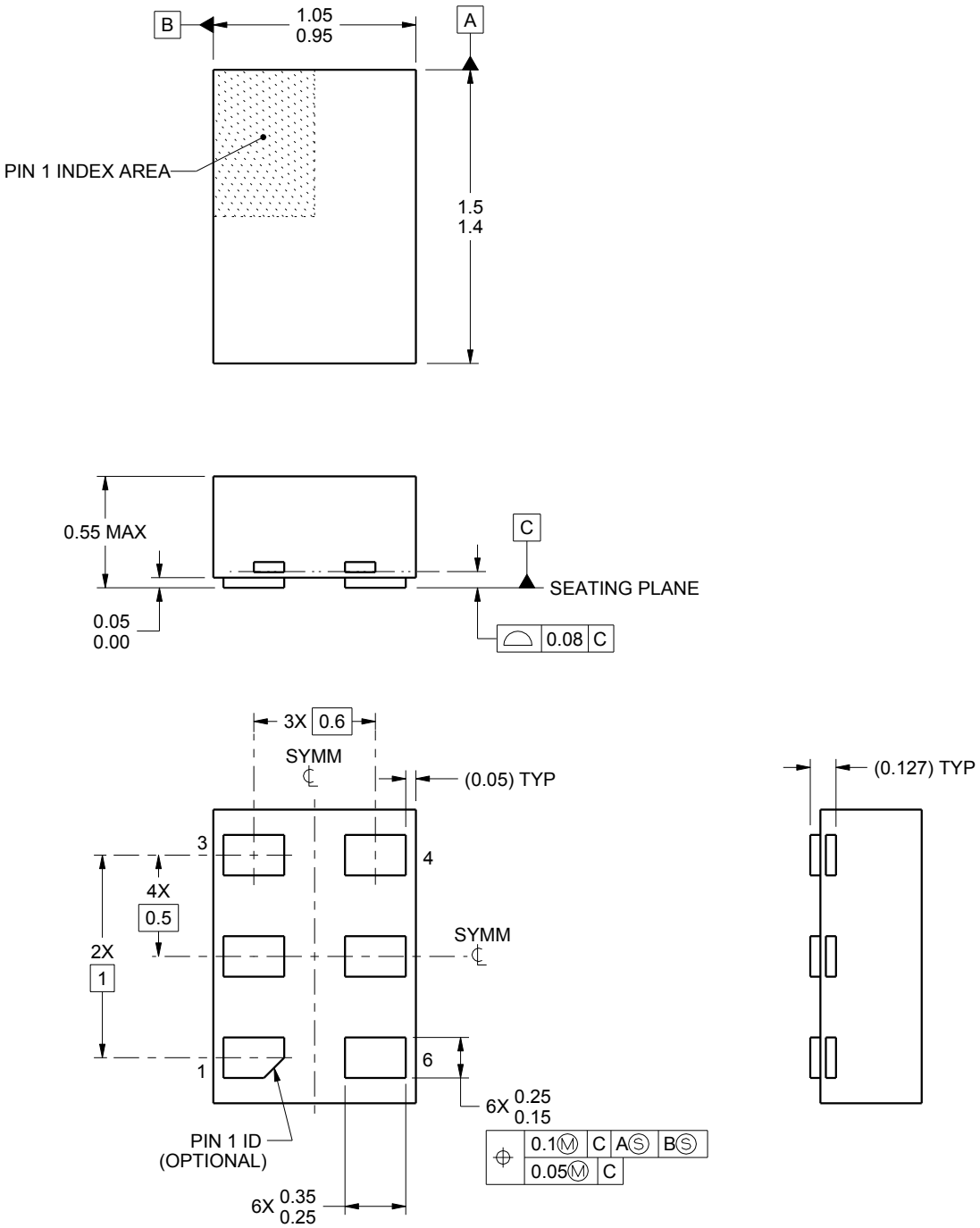
4207181/G

PACKAGE OUTLINE

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

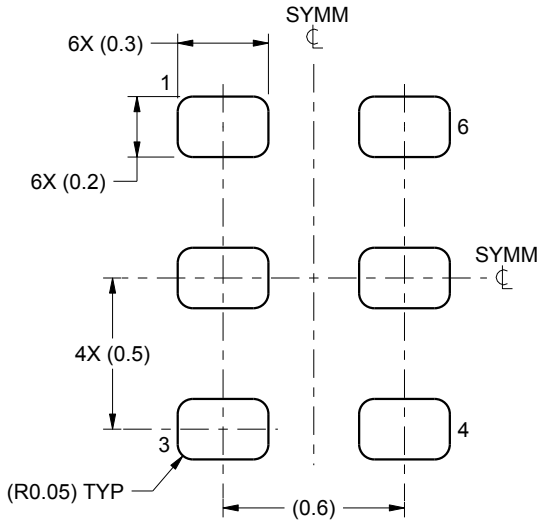
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

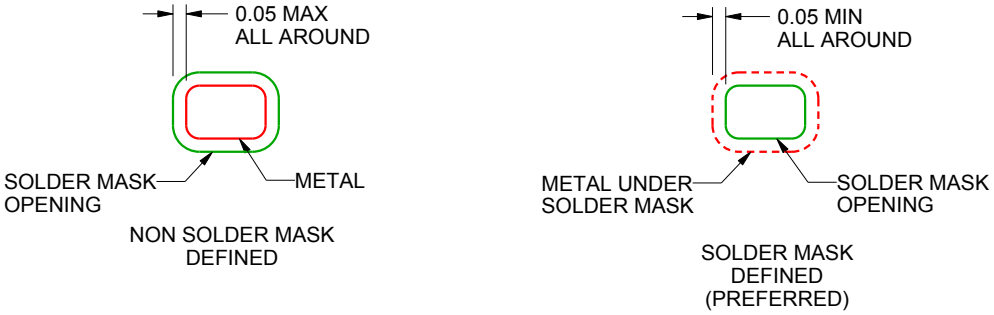
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

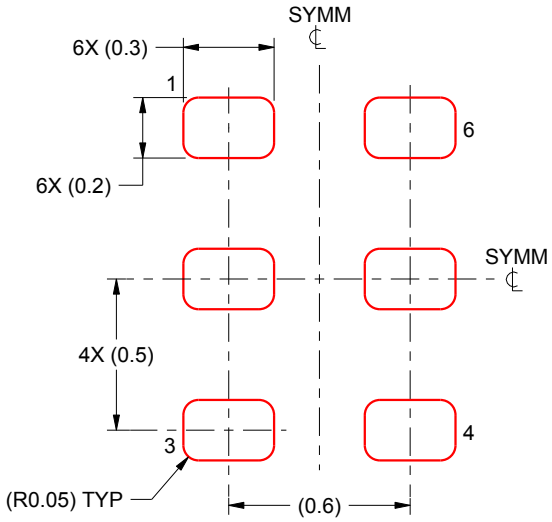
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

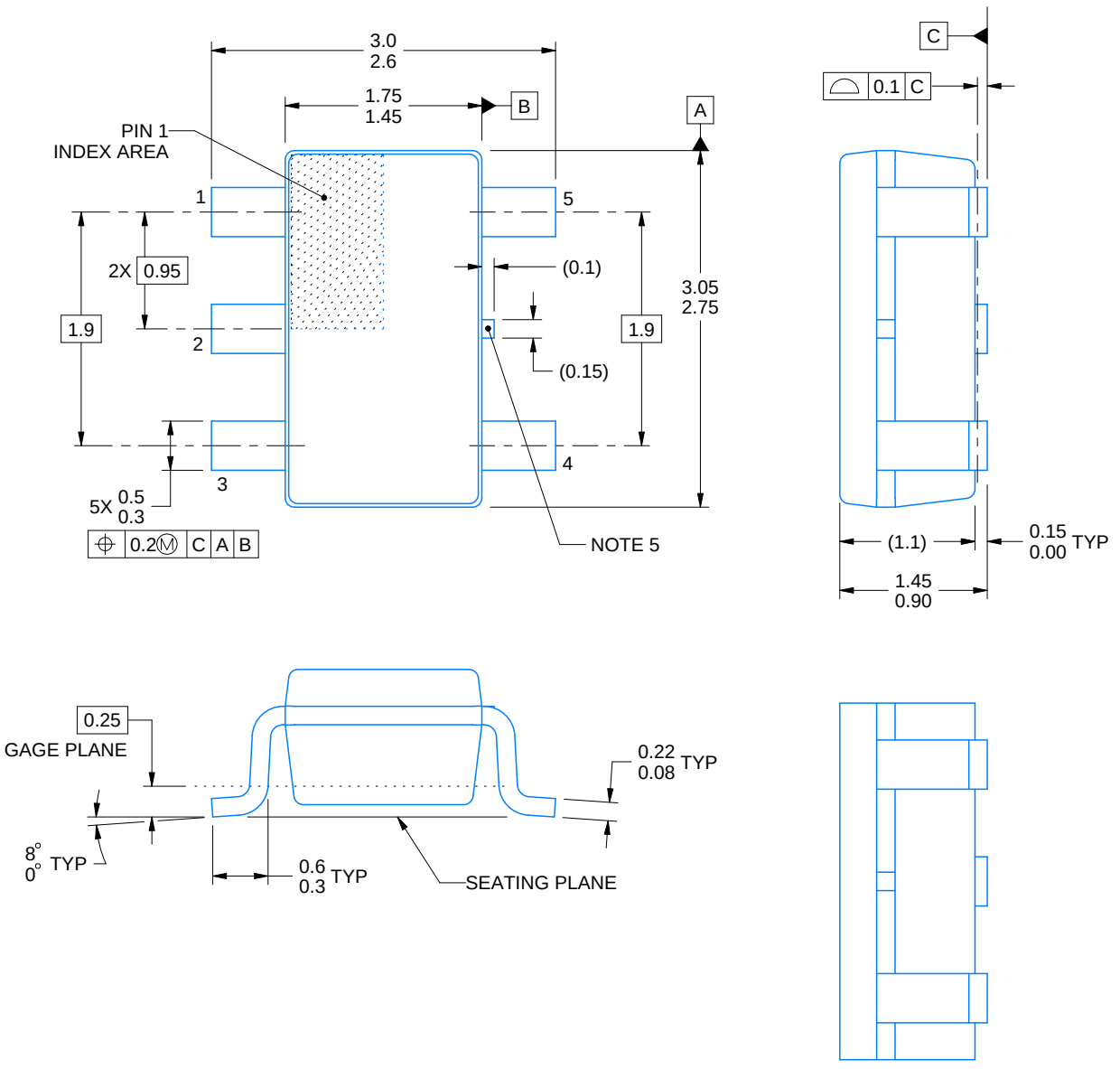
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

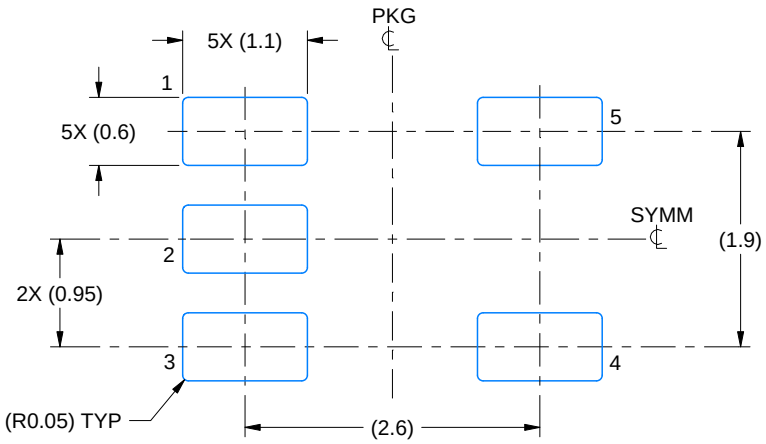


ALTERNATIVE PACKAGE SINGULATION VIEW

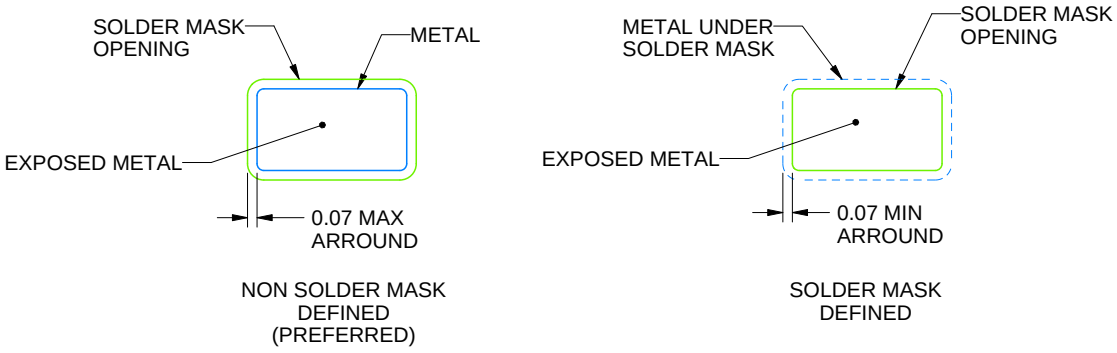
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

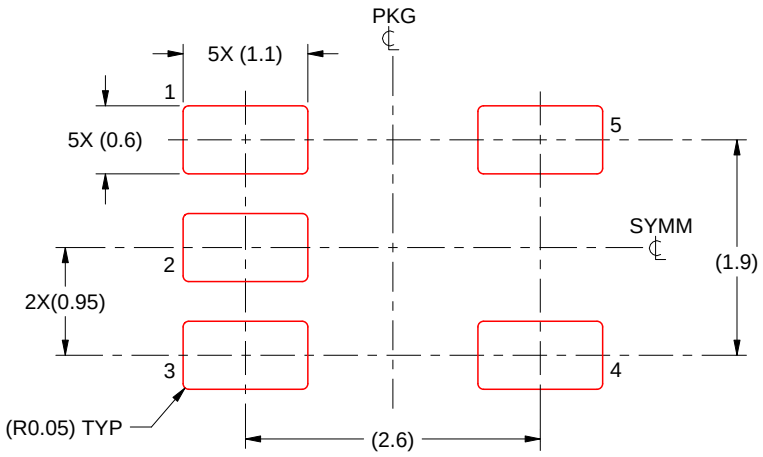


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

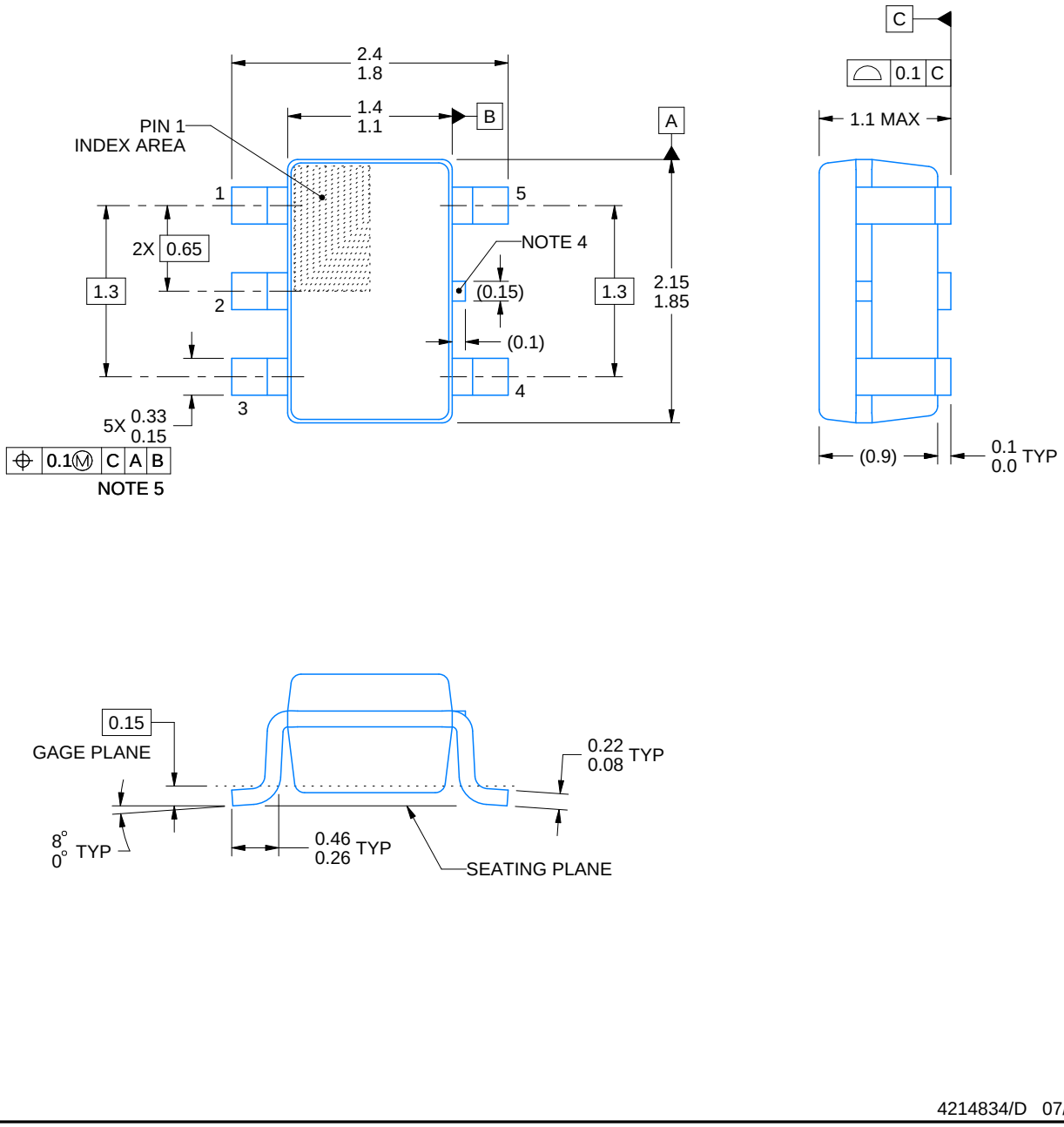
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

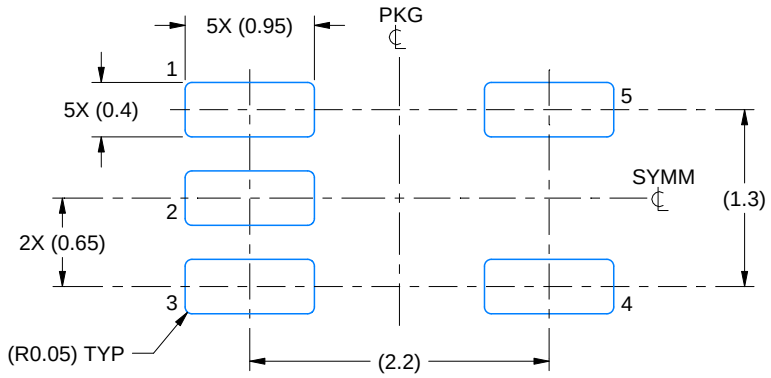
SMALL OUTLINE TRANSISTOR



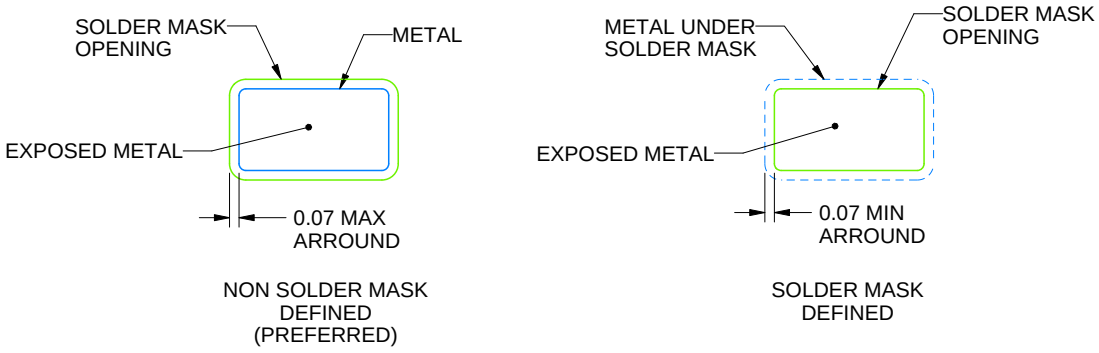
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

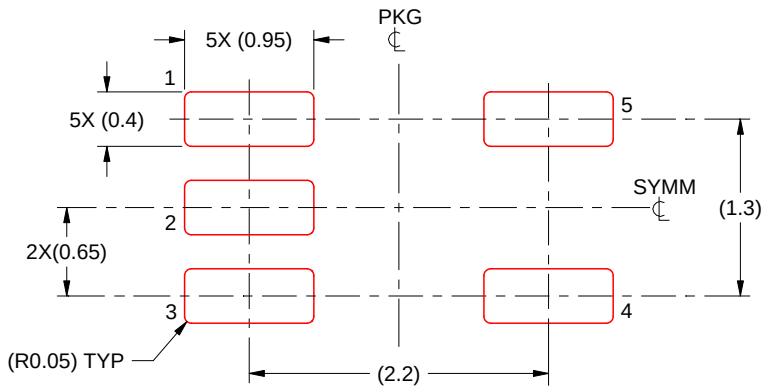


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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