# TPS370x-xx 具有电源故障检测功能的处理器监控电路

## 1 特性

- 具有 200ms 固定延时时间的上电复位发生器（无需外部电容器）
- 精密电源电压监控器：2.5V、3V、3.3V 和 5V
- 与 MAX705 至 MAX708 系列引脚对引脚兼容
- 集成看门狗时间（仅限 TPS3705-xx）
- 用于电源故障或低电池电量警告的电压监控器
- 50μA 最大电源电流
- 8 引脚 MSOP 和 8 引脚 SOIC 封装
- 温度范围：−40°C 至 85°C（TPS3705-33 为 −40°C 至 125°C）

## 2 应用

- 使用 DSP、微控制器或微处理器的设计
- 工业设备
- 可编程控制
- 汽车系统
- 便携式或电池供电类设备
- 智能仪表
- 无线通信系统
- 笔记本电脑或台式机

## 3 说明

TPS370x-xx 系列微处理器电源电压监控器主要为 DSP 以及基于其他处理器的系统提供电路初始化和时序监控。

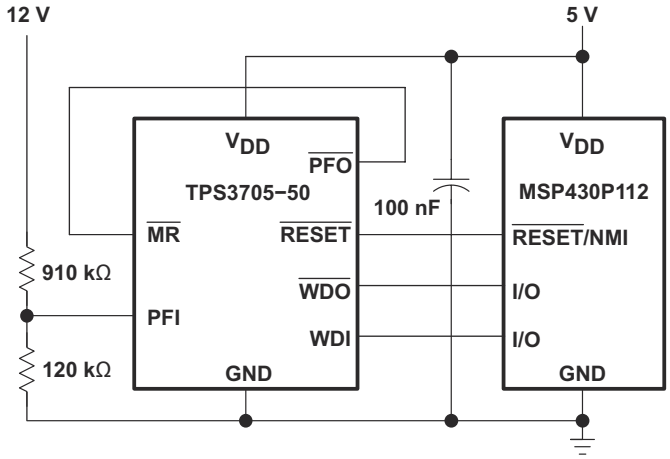
上电期间，如果电源电压 $V_{DD}$ 大于 1.1V，$\overline{RESET}$ 就会生效。因此，只要 $V_{DD}$ 保持在阈值电压 $V_{IT+}$ 以下，电源电压监控器就会监测 $V_{DD}$，并使 $\overline{RESET}$ 保持有效状态。当电源电压降到阈值电压 $V_{IT-}$ 以下时，输出再次变为有效状态（低电平）。无需外部组件。该系列中的所有器件均具有一个通过内部分压器设定的固定检测阈值电压 $V_{IT-}$。

该产品系列专为 2.5V、3V、3.3V 以及 5V 电源电压而设计。这些电路采用 8 引脚 MSOP 或标准 SOIC 封装。TPS370x-xx 器件的额定工作温度范围为 -40°C 至 85°C。

**器件信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS3705-xx、TPS3707-xx | MSOP- PowerPAD™ (8) | 3.00mm × 3.00mm |
| | SOIC (8) | 3.90mm x 4.90mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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**MSP430 典型应用**

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。



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# Table of Contents



## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision E (July 2017) to Revision F (October 2020) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |
| • Updated Device Comparison Table by adding -40°C to 125°C for TPS3705-33D | 3 |
| • Updated Absolute Maximum Ratings table to include Operating Temperature of -40°C to 125°C for TPS3705-33D | 5 |
| • Added TPS3705-33 Electrical Table | 8 |
| • Added histograms | 11 |

| Changes from Revision D (May 2016) to Revision E (July 2017) | Page |
|---|---|
| • 更新了 *器件信息* 表中的封装尺寸 | 1 |

| Changes from Revision C (December 2005) to Revision D (May 2016) | Page |
|---|---|
| • 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 | 1 |


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## 5 Device Comparison Table

| $T_A$ | THRESHOLD VOLTAGE | PACKAGED DEVICES | | MARKING DGN PACKAGE | CHIP FORM (Y) |
|---|---|---|---|---|---|
| | | SMALL OUTLINE (D) | POWER-PAD µ-SMALL OUTLINE (DGN) | | |
| – 40°C to 85°C | 2.63 V | TPS3705−30D | TPS3705−30DGN | TIAAT | TPS3705-30Y |
| | 4.55 V | TPS3705−50D | TPS3705−50DGN | TIAAV | TPS3705−50Y |
| | 2.25 V | TPS3707−25D | TPS3707−25DGN | TIAAW | TPS3707−25Y |
| | 2.63 V | TPS3707−30D | TPS3707−30DGN | TIAAX | TPS3707−30Y |
| | 2.93 V | TPS3707−33D | TPS3707−33DGN | TIAAY | TPS3707−33Y |
| | 4.55 V | TPS3707−50D | TPS3707−50DGN | TIAAZ | TPS3707−50Y |
| – 40°C to 125°C | 2.93 V | TPS3705−33D | TPS3705−33DGN | TIAAU | TPS3705−33Y |

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# 6 Pin Configuration and Functions

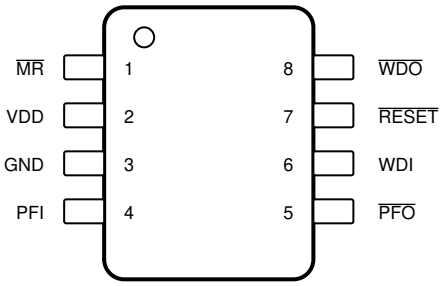


图 6-1. TPS3705-xx D Package 8-Pin SOIC Top View

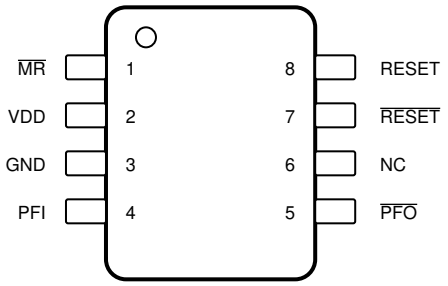


图 6-2. TPS3707-xx D Package 8-Pin SOIC Top View

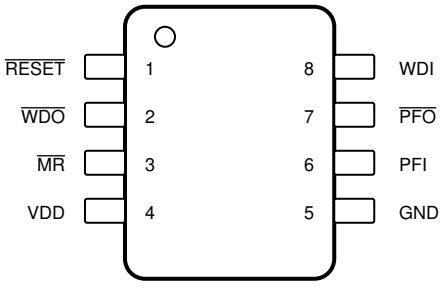


图 6-3. TPS3705-xx DGN Package 8-Pin MSOP-PowerPAD Top View

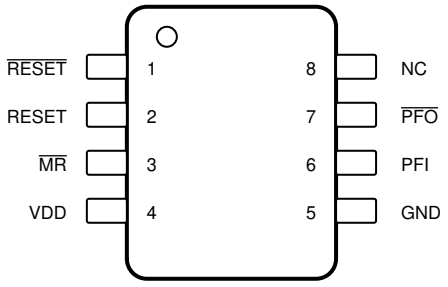


图 6-4. TPS3707-xx DGN Package 8-Pin MSOP-PowerPAD Top View

## 6.1 Pin Functions

| PIN | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | TPS3705-xx | | TPS3707-xx | | | |
| | SOIC | MSOP-PowerPAD | SOIC | MSOP-PowerPAD | | |
| GND | 3 | 5 | 3 | 5 | — | Ground |
| $\overline{MR}$ | 1 | 3 | 1 | 3 | I | Manual reset |
| NC | — | — | 6 | 8 | — | No internal connection |
| PFI | 4 | 6 | 4 | 6 | I | Power-fail comparator input |
| $\overline{PFO}$ | 5 | 7 | 5 | 7 | O | Power-fail comparator output |
| $\overline{RESET}$ | 7 | 1 | 7 | 1 | O | Active-low reset output |
| RESET | — | — | 8 | 2 | O | Active-high reset output |
| $V_{DD}$ | 2 | 4 | 2 | 4 | — | Supply voltage |
| WDI | 6 | 8 | — | — | I | Watchdog timer input |
| $\overline{WDO}$ | 8 | 2 | — | — | O | Watchdog timer output |


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{DD}$ (2) | | 7 | V |
| PFI voltage range, $V_{PFI}$ | – 0.3 | $V_{DD}$ + 0.3 | V |
| All other pins(2) | – 0.3 | 7 | V |
| Maximum low output current, $I_{OL}$ | | 5 | mA |
| Maximum high output current, $I_{OH}$ | | – 5 | mA |
| Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) | | ±20 | mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) | | ±20 | mA |
| Continuous total power dissipation | See # 7.9 | | |
| Soldering temperature | | 260 | °C |
| Operating temperature, $T_A$ | – 40 | 85 | °C |
| Operating temperature, $T_A$ for TPS3705-33 only | – 40 | 125 | °C |
| Storage temperature, $T_{stg}$ | – 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2 | | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{DD}$ + 0.3 | V |
| $V_{IH}$ | High-level input voltage | 0.7 × $V_{DD}$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.3 × $V_{DD}$ | V |
| $\Delta t/\Delta V$ | Input transition rise and fall rate at $\overline{MR}$ or WDI | | | 100 | ns/V |
| $T_A$ | Operating free-air temperature | – 40 | | 85 | °C |
| $T_A$ | Operating free-air temperature for TPS3705-33 only | – 40 | | 125 | °C |

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## 7.4 Thermal Information

| THERMAL METRIC[1] | | TPS3705-xx | TPS3707-xx | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DGN (MSOP-PowerPAD) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 118.2 | 66.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 64.4 | 62.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 58.5 | 45.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 15.8 | 7.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 57.9 | 44.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | 18.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | TPS370x-xx, $V_{DD}$ = 1.1 V, $I_{OH}$ = –4 µA | 0.8 | | | V |
| | | TPS3707-25, TPS370x-30, TPS370x-33, $V_{DD}$ = $V_{IT+}$ + 0.2 V, $I_{OH}$ = –500 µA | 0.7 × $V_{DD}$ | | | |
| | | TPS370x-50, $V_{DD}$ = $V_{IT+}$ + 0.2 V, $I_{OH}$ = –800 µA | $V_{DD}$ – 1.5 | | | |
| | | TPS370x-xx, $V_{DD}$ = 6 V, $I_{OH}$ = –800 µA | $V_{DD}$ – 1.5 | | | |
| $V_{OL}$ | Low-level output voltage | TPS3707-25, TPS370x-30, TPS370x-33, $V_{DD}$ = $V_{IT+}$ + 0.2 V, $I_{OL}$ = 1 mA | | | 0.3 | V |
| | | TPS370x-50, $V_{DD}$ = $V_{IT+}$ + 0.2 V, $I_{OL}$ = 2.5 mA | | | 0.4 | |
| | | TPS370x-xx, $V_{DD}$ = 6 V, $I_{OL}$ = 3 mA | | | 0.4 | |
| | Power-up reset voltage[1] | $V_{DD}$ ⩾ 1.1 V, $I_{OL}$ = 50 µA | | | 0.3 | V |
| $V_{IT-}$ | Negative-going input threshold voltage[2] | TPS3707-25, $T_A$ = 0°C to 85°C | 2.2 | 2.25 | 2.3 | V |
| | | TPS370x-30, $T_A$ = 0°C to 85°C | 2.57 | 2.63 | 2.68 | |
| | | TPS370x-33, $T_A$ = 0°C to 85°C | 2.87 | 2.93 | 2.98 | |
| | | TPS370x-50, $T_A$ = 0°C to 85°C | 4.45 | 4.55 | 4.63 | |
| | | TPS3707-25, $T_A$ = –40°C to 85°C | 2.2 | 2.25 | 2.32 | |
| | | TPS370x-30, $T_A$ = –40°C to 85°C | 2.57 | 2.63 | 2.7 | |
| | | TPS370x-33, $T_A$ = –40°C to 85°C | 2.87 | 2.93 | 3 | |
| | | TPS370x-50, $T_A$ = –40°C to 85°C | 4.45 | 4.55 | 4.65 | |
| | Negative-going input threshold voltage, PFI[2] | TPS370x-xx, $V_{DD}$ ⩾ 2 V, $T_A$ = –40°C to 85°C | 1.2 | 1.25 | 1.3 | |
| $V_{hys}$ | Hysteresis, $V_{DD}$ | TPS3707-25 | | 40 | | mV |
| | | TPS370x-30 | | 50 | | |
| | | TPS370x-33 | | 50 | | |
| | | TPS370x-50 | | 70 | | |
| | Hysteresis, PFI | TPS370x-xx | | 10 | | |
| $I_{IH(AV)}$ | Average high-level input current, WDI | WDI = $V_{DD}$ = 6 V, time average (dc = 88%) | | 100 | 150 | µA |
| $I_{IL(AV)}$ | Average low-level input current, WDI | WDI = 0 V, $V_{DD}$ = 6 V, time average (dc = 12%) | | –15 | –20 | µA |
| $I_{IH}$ | High-level input current, WDI | WDI = $V_{DD}$ = 6 V | | 120 | 170 | µA |
| | High-level input current, $\overline{MR}$ | $\overline{MR}$ = 0.7 × $V_{DD}$, $V_{DD}$ = 6 V | | –130 | –180 | |
| $I_{IL}$ | Low-level input current, WDI | WDI = 0 V, $V_{DD}$ = 6 V | | –120 | –170 | µA |
| | Low-level input current, $\overline{MR}$ | $\overline{MR}$ = 0 V, $V_{DD}$ = 6 V | | –430 | –600 | |
| $I_I$ | Input current, PFI | $V_{DD}$ = 6 V, 0 V ⩽ $V_I$ ⩽ $V_{DD}$ | –1 | 0 | 1 | µA |
| $I_{DD}$ | Supply current | TPS3705-xx, $V_{DD}$ = 2 V to 6 V, $\overline{MR}$ = $V_{DD}$, $\overline{MR}$, WDI and outputs unconnected | | 30 | 50 | µA |
| | | TPS3707-xx, $V_{DD}$ = 2 V to 6 V, $\overline{MR}$ = $V_{DD}$, $\overline{MR}$, WDI and outputs unconnected | | 20 | 50 | |
| $C_i$ | Input capacitance | $V_I$ = 0 V to $V_{DD}$ | | 5 | | pF |

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active, $t_{r,VDD}$ ⩾ 15 µs/V
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals

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## 7.6 Electrical Characteristics for TPS3705-33 Only

over operating free-air temperature range -40 to 125C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{DD}$ = 1.1 V, $I_{OH}$ = –4 µA | 0.8 | | | V |
| | | $V_{DD}$ = $V_{IT+}$ + 0.2 V, $I_{OH}$ = –500 µA | 0.7 × $V_{DD}$ | | | |
| | | $V_{DD}$ = 6 V, $I_{OH}$ = –800 µA | $V_{DD}$ – 1.5 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$ = $V_{IT+}$ + 0.2 V, $I_{OL}$ = 1 mA | | | 0.3 | V |
| | | $V_{DD}$ = 6 V, $I_{OL}$ = 3 mA | | | 0.4 | |
| | Power-up reset voltage(1) | $V_{DD}$ ⩾ 1.1 V, $I_{OL}$ = 50 µA | | | 0.3 | V |
| $V_{IT-}$ | Negative-going input threshold voltag | $T_A$ = 0°C to 125°C | 2.87 | 2.93 | 3 | V |
| | | $T_A$ = –40°C to 125°C | 2.87 | 2.93 | 3.02 | |
| | Negative-going input threshold voltage, PFI(2) | $V_{DD}$ ⩾ 2 V | 1.2 | 1.25 | 1.3 | |
| $V_{hys}$ | Hysteresis, $V_{DD}$ | | | 50 | | mV |
| | Hysteresis, PFI | | | 10 | | |
| $I_{IH(AV)}$ | Average high-level input current, WDI | WDI = $V_{DD}$ = 6 V, time average (dc = 88%) | | 100 | 150 | µA |
| $I_{IL(AV)}$ | Average low-level input current, WDI | WDI = 0 V, $V_{DD}$ = 6 V, time average (dc = 12%) | | –15 | –20 | µA |
| $I_{IH}$ | High-level input current, WDI | WDI = $V_{DD}$ = 6 V | | 120 | 170 | µA |
| | High-level input current, $\overline{MR}$ | $\overline{MR}$ = 0.7 × $V_{DD}$, $V_{DD}$ = 6 V | | –130 | –180 | |
| $I_{IL}$ | Low-level input current, WDI | WDI = 0 V, $V_{DD}$ = 6 V | | –120 | –170 | µA |
| | Low-level input current, $\overline{MR}$ | $\overline{MR}$ = 0 V, $V_{DD}$ = 6 V | | –430 | –600 | |
| $I_I$ | Input current, PFI | $V_{DD}$ = 6 V, 0 V ⩽ $V_I$ ⩽ $V_{DD}$ | –1 | 0 | 1 | µA |
| $I_{DD}$ | Supply current | $V_{DD}$ = 2 V to 6 V, $\overline{MR}$ = $V_{DD}$, $\overline{MR}$, WDI and outputs unconnected | | 30 | 50 | µA |
| $C_i$ | Input capacitance | $V_I$ = 0 V to $V_{DD}$ | | 5 | | pF |

## 7.7 Timing Requirements

at $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_w$ | Pulse width | At $V_{DD}$, $V_{DD}$ = $V_{IT+}$ + 0.2 V, $V_{DD}$ = $V_{IT-}$ – 0.2 V | 6 | | | µs |
| | | At $\overline{MR}$ and WDI, $V_{DD}$ ⩾ $V_{IT+}$ + 0.2 V, $V_{IL}$ = 0.3 × $V_{DD}$, $V_{IH}$ = 0.7 × $V_{DD}$ | 100 | | | ns |


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## 7.8 Switching Characteristics

at $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{t(out)}$ | Watchdog time out | $V_{DD} \geqslant V_{IT+}$ + 0.2 V, see 图 7-1 | 1.1 | 1.6 | 2.3 | s |
| $t_d$ | Delay time | $V_{DD} \geqslant V_{IT+}$ + 0.2 V, see 图 7-1 | 140 | 200 | 280 | ms |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $\overline{MR}$ to $\overline{RESET}$ delay, $V_{DD} \geqslant V_{IT+}$ + 0.2 V, $V_{IL}$ = 0.3 × $V_{DD}$, $V_{IH}$ = 0.7 × $V_{DD}$ | | 50 | 250 | ns |
| $t_{PLH}$ | Propagation (delay) time, low-to-high-level output | $\overline{MR}$ to RESET delay (TPS3707-xx only) $V_{DD} \geqslant V_{IT+}$ + 0.2 V, $V_{IL}$ = 0.3 × $V_{DD}$, $V_{IH}$ = 0.7 × $V_{DD}$ | | 50 | 250 | ns |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $V_{DD}$ to $\overline{RESET}$ delay | | 3 | 5 | µs |
| $t_{PLH}$ | Propagation (delay) time, low-to-high-level output | $V_{DD}$ to RESET delay (TPS3707-xx only) | | 3 | 5 | µs |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | PFI to $\overline{PFO}$ delay, $V_{DD}$ = 2 V to 6 V | | 0.5 | 1 | µs |
| $t_{PLH}$ | Propagation (delay) time, low-to-high-level output | PFI to $\overline{PFO}$ delay, $V_{DD}$ = 2 V to 6 V | | 0.5 | 1 | µs |

## 7.9 Dissipation Ratings

| PACKAGE | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| DGN | 2.14 W | 17.1 mW/°C | 1.37 W | 1.11 W |
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |

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## 7.10 Timing Diagram

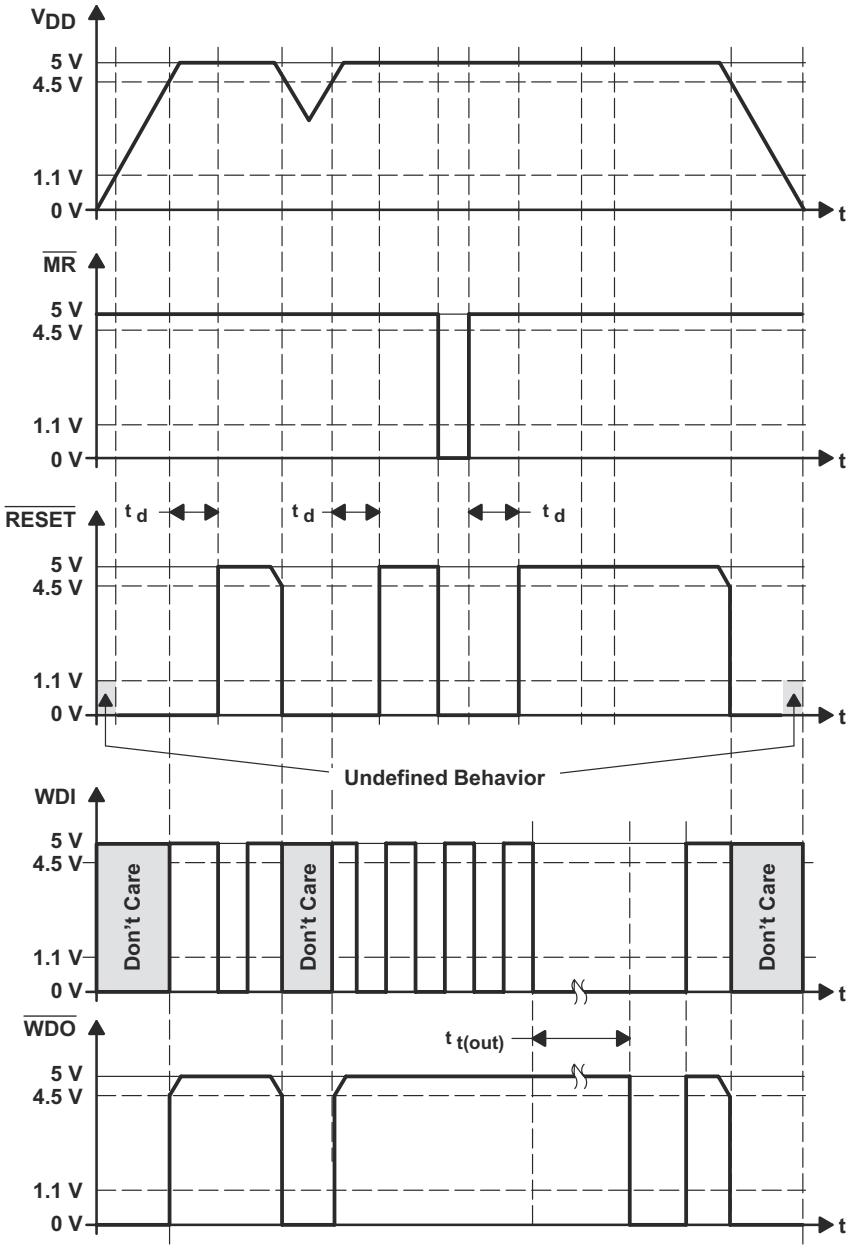


图 7-1. Timing Diagrams


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## 7.11 Typical Characteristics

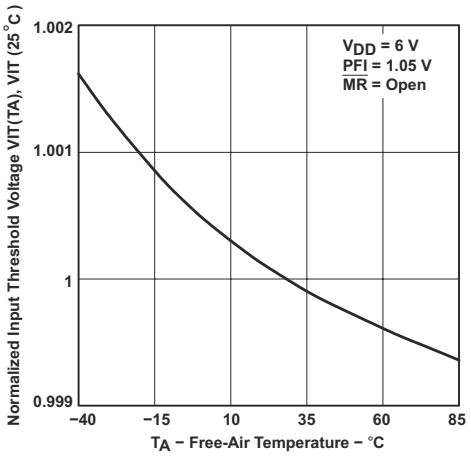


图 7-2. Normalized Input Threshold Voltage vs Free-Air Temperature at $V_{DD}$

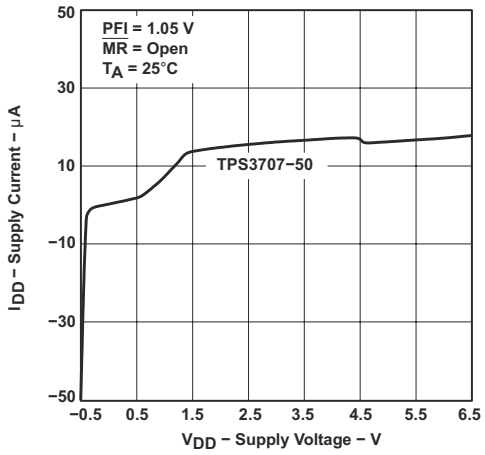


图 7-3. Supply Current vs Supply Voltage

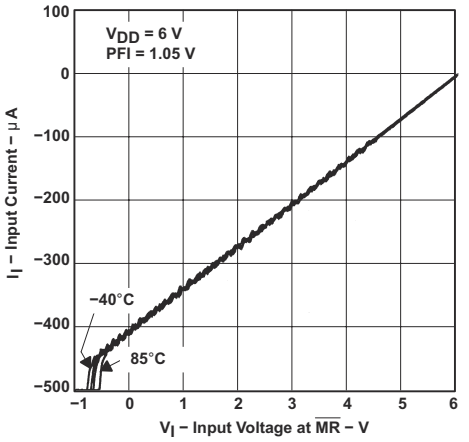


图 7-4. Input Current vs Input Voltage at $\overline{MR}$

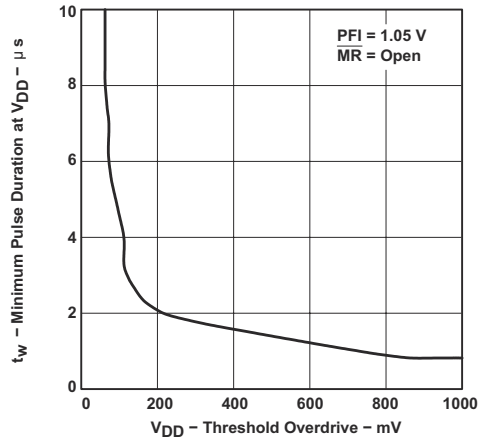


图 7-5. Minimum Pulse Duration at $V_{DD}$ vs $V_{DD}$ Threshold Overdrive

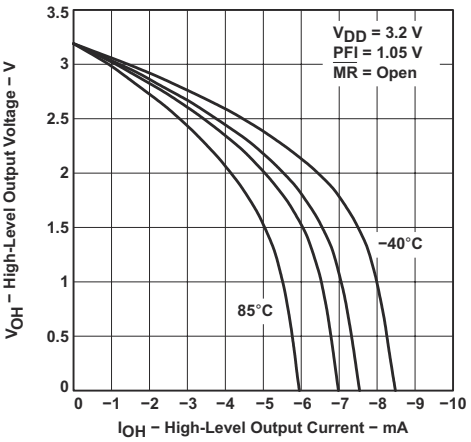


图 7-6. High-Level Output Voltage vs High-Level Output Current

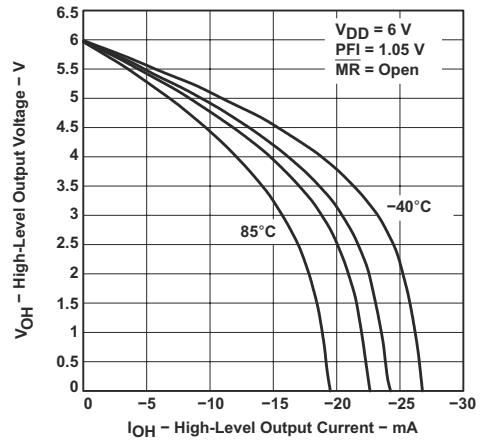


图 7-7. High-Level Output Voltage vs High-Level Output Current

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## 7.11 Typical Characteristics (continued)

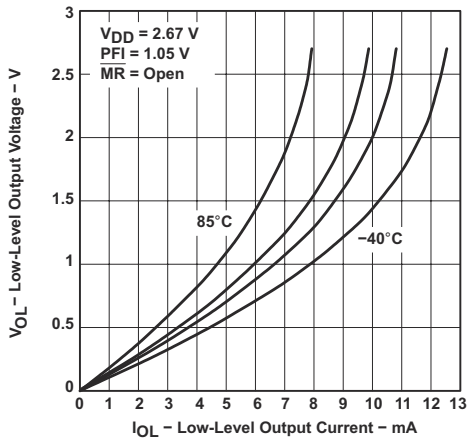


图 7-8. Low-Level Output Voltage vs Low-Level Output Current

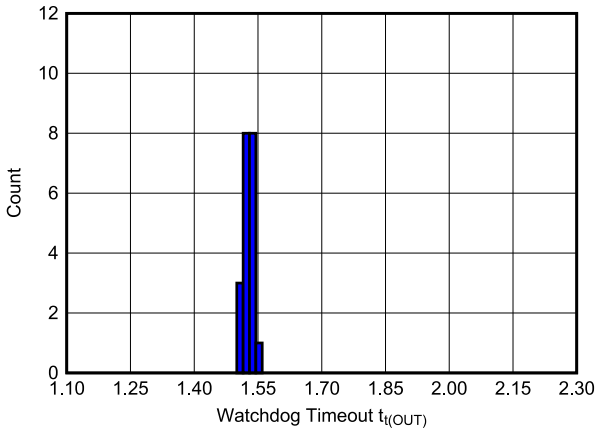


图 7-9. Watchdog Timeout Histogram for TSP3705-33 Devices at -40°C (Unit Count = 20)

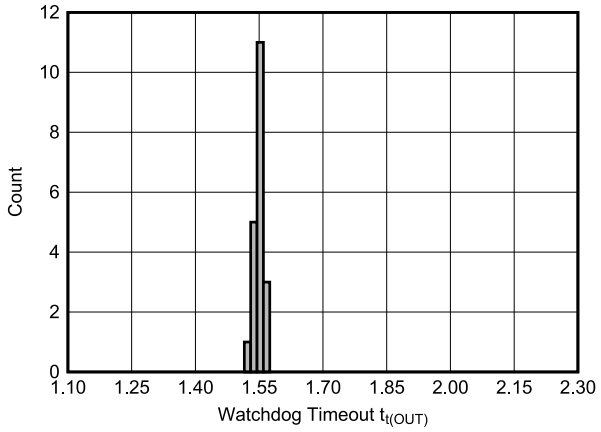


图 7-10. Watchdog Timeout Histogram for TSP3705-33 Devices at 25°C (Unit Count = 20)

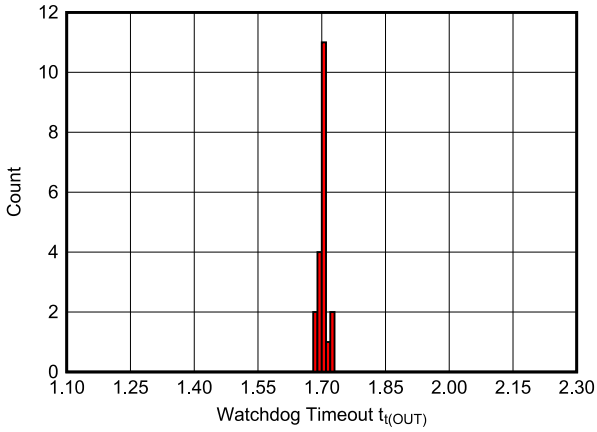


图 7-11. Watchdog Timeout Histogram for TSP3705-33 Devices at 125°C (Unit Count = 20)

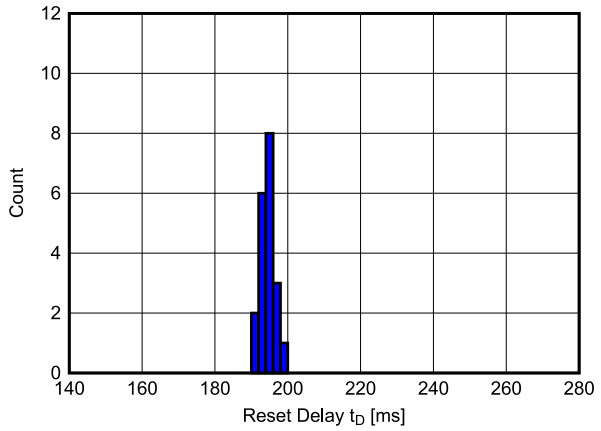


图 7-12. Reset Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)

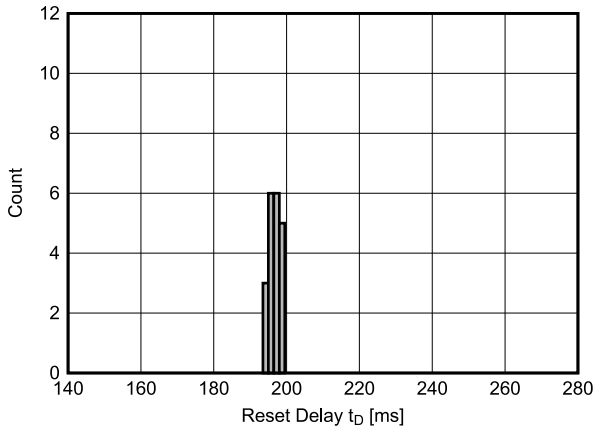


图 7-13. Reset Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)


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## 7.11 Typical Characteristics (continued)

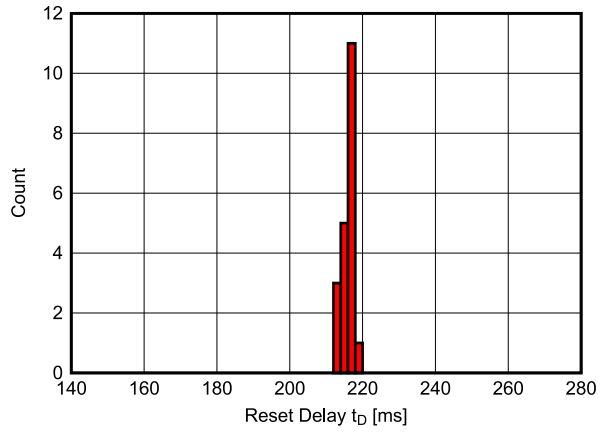


**图 7-14. Reset Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)**

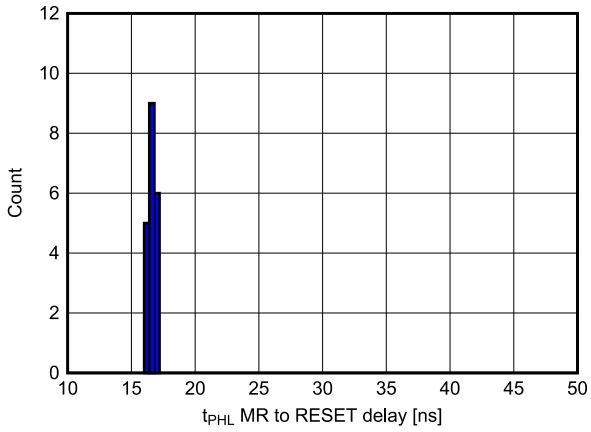


**图 7-15. $\overline{MR}$ to $\overline{RESET}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)**

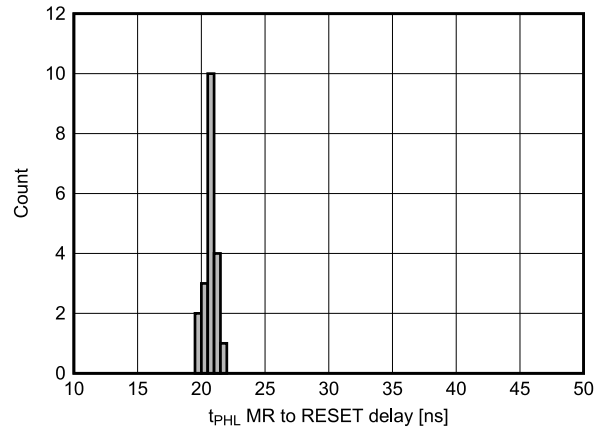


**图 7-16. $\overline{MR}$ to $\overline{RESET}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)**

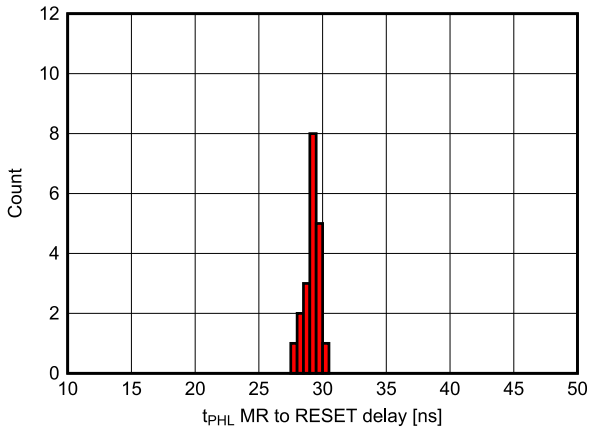


**图 7-17. $\overline{MR}$ to $\overline{RESET}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)**

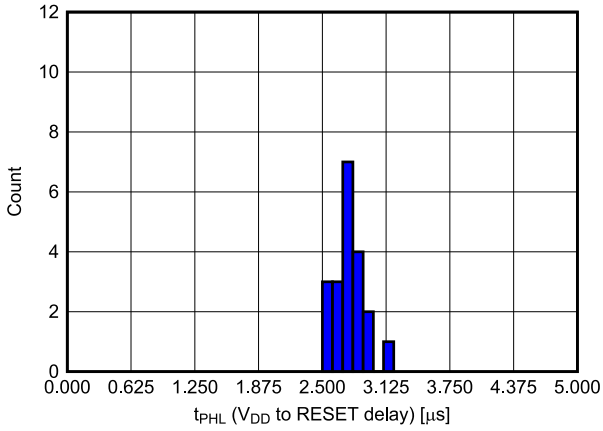


**图 7-18. $V_{DD}$ to $\overline{RESET}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)**

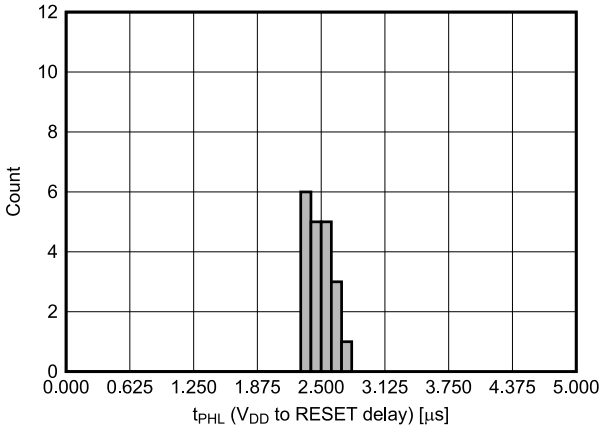


**图 7-19. $V_{DD}$ to $\overline{RESET}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)**


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## 7.11 Typical Characteristics (continued)

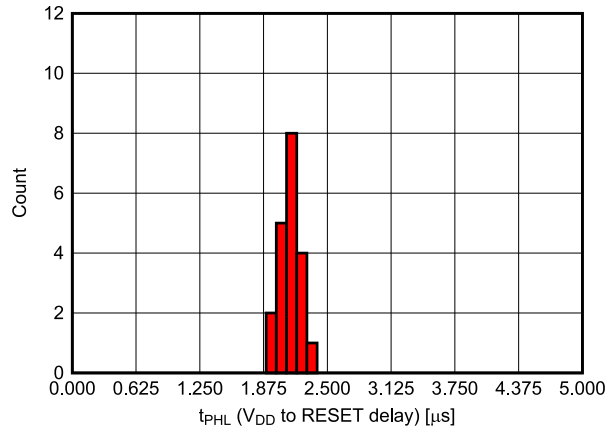


**图 7-20. $V_{DD}$ to $\overline{RESET}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)**

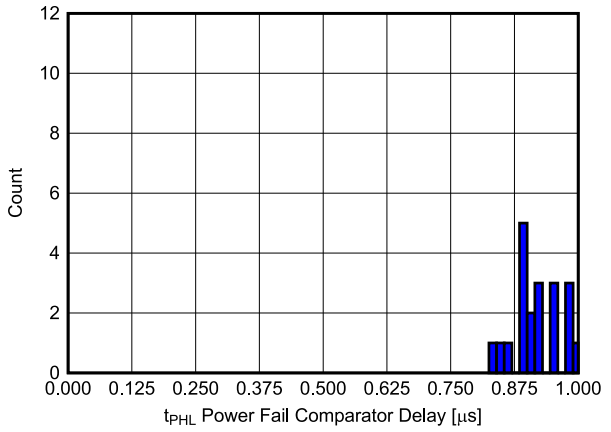


**图 7-21. PFI to $\overline{PFO}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)**

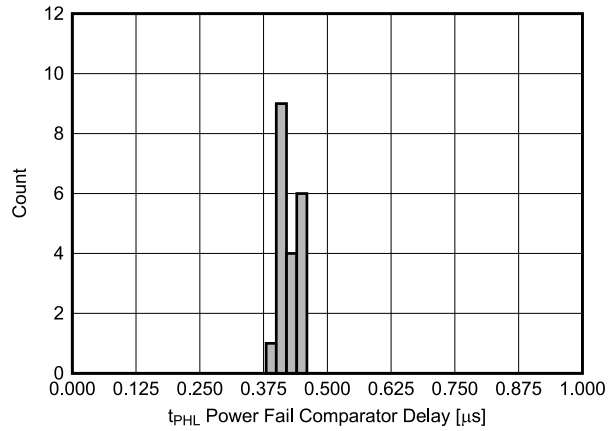


**图 7-22. PFI to $\overline{PFO}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)**

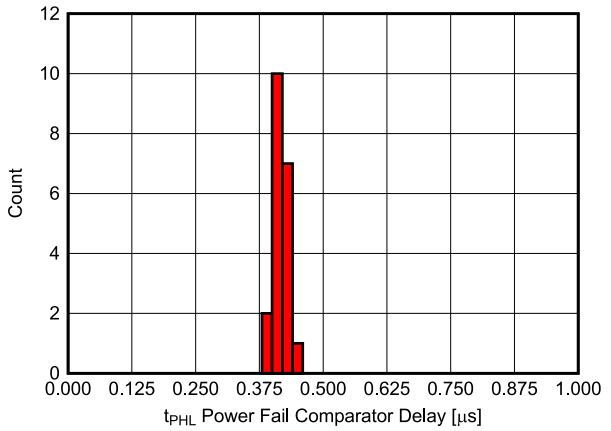


**图 7-23. PFI to $\overline{PFO}$ ($t_{PHL}$) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)**

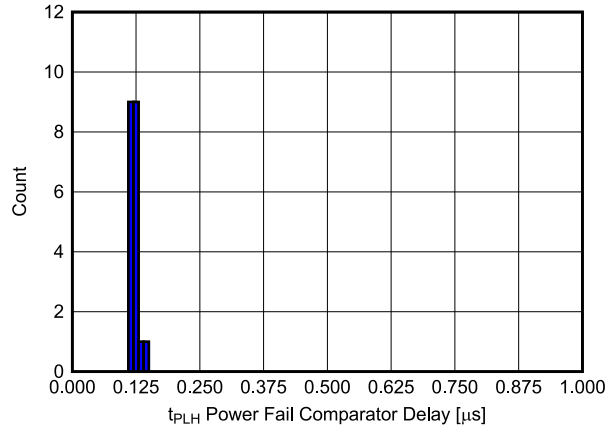


**图 7-24. PFI to $\overline{PFO}$ ($t_{PLH}$) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)**

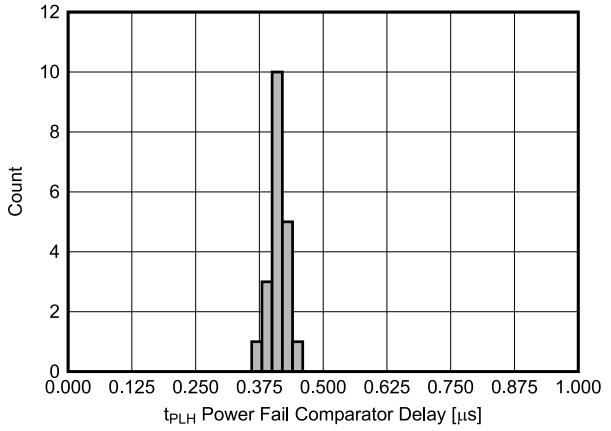


**图 7-25. PFI to $\overline{PFO}$ ($t_{PLH}$) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)**


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## 7.11 Typical Characteristics (continued)

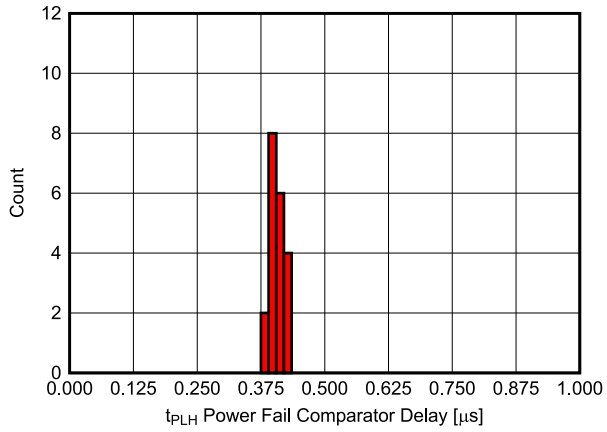


**图 7-26. PFI to $\overline{PFO}$ ($t_{PLH}$) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)**


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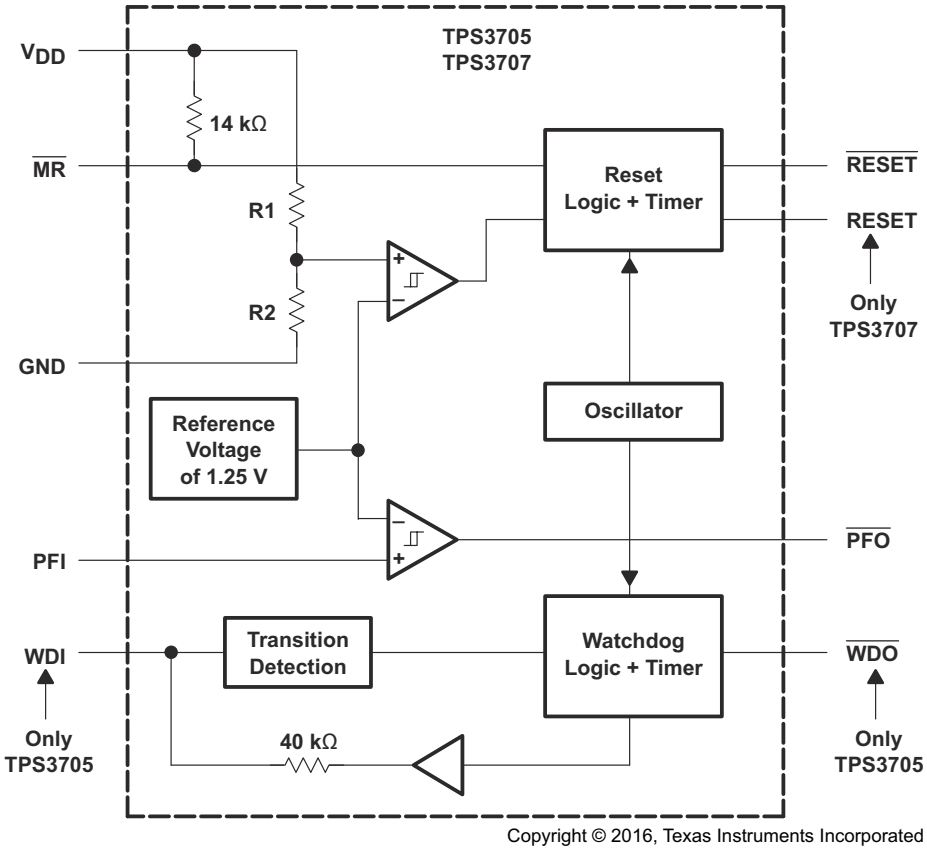
# 8 Detailed Description

## 8.1 Overview

The TPS370x-xx family of supervisors feature an integrated reference and comparator for $V_{DD}$ supervision, an additional power-fail supervisor, and a manual reset input. The TPS3705-xx devices feature a watchdog timer, where the TPS3707-xx devices feature a complimentary RESET output.

## 8.2 Functional Block Diagram

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## 8.3 Feature Description

### 8.3.1 Manual Reset Input

The TPS370x-xx devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active.

### 8.3.2 Power-Fail Comparator

The TPS370x-xx family integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

### 8.3.3 Watchdog Timer

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the timeout interval, $t_{t(out)}$ = 1.6 s, $\overline{WDO}$ becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the watchdog function, but include a high-level output RESET.


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## 8.4 Device Functional Modes

### 8.4.1 $V_{DD}$ < 1.1 V

When $V_{DD}$ is less than 1.1 V, the status of the outputs cannot be determined.

### 8.4.2 1.1 V < $V_{DD}$ ⩽ 2 V

When $V_{DD}$ is greater than 1.1 V but less than 2 V, the output states are valid. However, the specifications in 节 7.5 do not apply.

### 8.4.3 2 V < $V_{DD}$ < 6 V

When $V_{DD}$ is greater than 2 V but less than 6 V, the device is within the recommended operating conditions (see 节 7.3). See 表 8-1, 表 8-2, and 表 8-3 for corresponding truth tables.

**表 8-1. TPS3705 Truth Table**

| $\overline{MR}$ | $V_{DD} > V_{IT}$ | $\overline{RESET}$ | TYPICAL DELAY |
|---|---|---|---|
| H → L | 1 | H → L | 30 ns |
| L → H | 1 | L → H | 200 ms |
| H | 1 → 0 | H → L | 3 µs |
| H | 0 → 1 | L → H | 200 ms |

**表 8-2. TPS3707 Truth Table**

| $\overline{MR}$ | $V_{DD} > V_{IT}$ | $\overline{RESET}$ | RESET | TYPICAL DELAY |
|---|---|---|---|---|
| H → L | 1 | H → L | L → H | 30 ns |
| L → H | 1 | L → H | H → L | 200 ms |
| H | 1 → 0 | H → L | L → H | 3 µs |
| H | 0 → 1 | L → H | H → L | 200 ms |

**表 8-3. TPS370x Truth Table**

| PFI > $V_{IT}$ | $\overline{PFO}$ | TYPICAL DELAY |
|---|---|---|
| 0 → 1 | L → H | 0.5 µs |
| 1 → 0 | H → L | 0.5 µs |

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# 9 Application and Implementation

**备注**

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

The TPS370x-xx family of devices offers several options for power monitoring. The TPS3705-xx offers a watchdog supervisor, $V_{DD}$ rail monitoring, and a power-fail interrupt monitor. The TPS3707-xx offers $V_{DD}$ rail monitoring with complimentary outputs and a power-fail interrupt monitor.

## 9.2 Typical Application

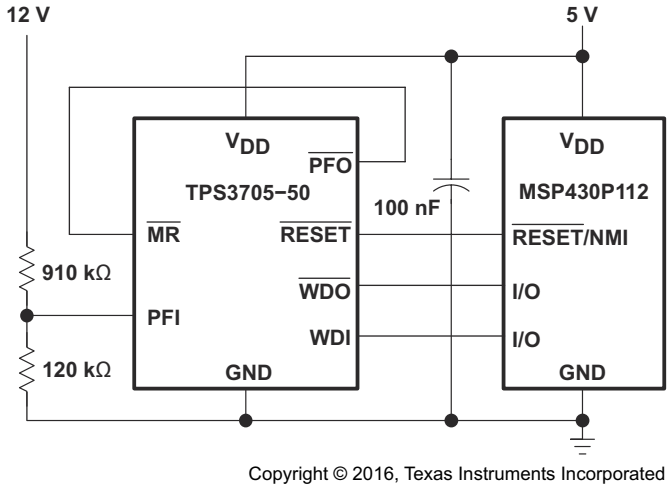


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**图 9-1. Typical MSP430 Application**

### 9.2.1 Design Requirements

表 9-1 lists the required design parameters for 图 9-1.

**表 9-1. Application Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Monitored voltage 1 | 5 V |
| Monitored voltage 2 | 12 V |

### 9.2.2 Detailed Design Procedure

To create two voltage monitoring rails, the PFI input can be used along with the MR pin to create a single output. The 5-V monitor is created by selecting a 5-V device option, giving threshold of 4.55 V. The PFI input is configured to any adjustable rail with a voltage divider. Use 方程式 1 to select resistors.

$$V_{TH} = \frac{R_1 + R_2}{R_2} \times V_{IT-} = \frac{910\,k + 120\,k}{120\,k} \times 1.25 = 10.73\ V \quad (1)$$


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### 9.2.3 Application Curves

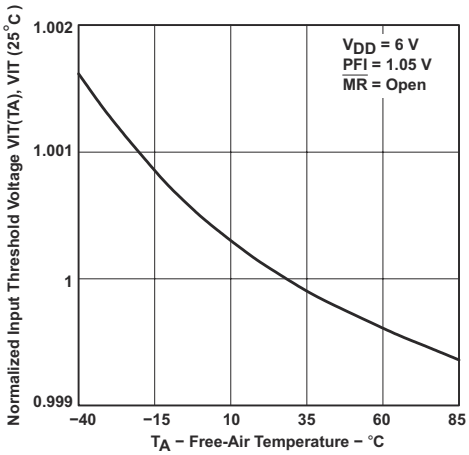


图 9-2. Normalized Input Threshold Voltage vs Free-Air Temperature at $V_{DD}$

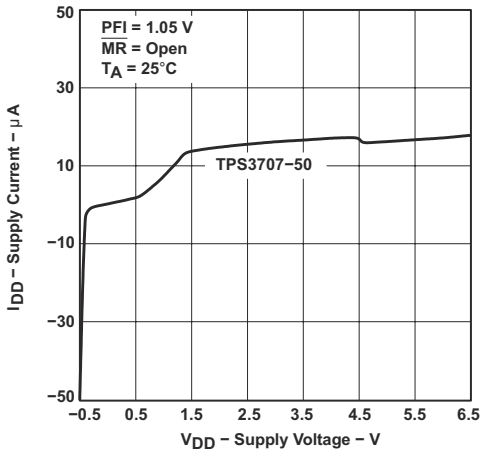


图 9-3. Supply Current vs Supply Voltage


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## 10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 2 V to 6 V.


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# 11 Layout

## 11.1 Layout Guidelines

Place a 0.1-µF decoupling capacitor as close to the device as possible.

If a resistor divider is used, place the resistors as close to the device as possible to minimize noise coupling.

## 11.2 Layout Example

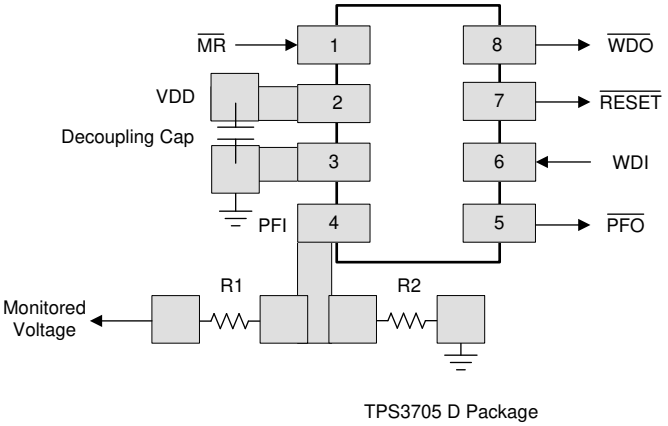


**图 11-1. TPS3705 Layout**


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# 12 Device and Documentation Support

## 12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.3 Trademarks

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## 12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3705-30D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70530 | Samples |
| TPS3705-30DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAT | Samples |
| TPS3705-30DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70530 | Samples |
| TPS3705-33D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 70533 | Samples |
| TPS3705-33DG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 70533 | Samples |
| TPS3705-33DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAU | Samples |
| TPS3705-33DGNR | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAU | Samples |
| TPS3705-33DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 70533 | Samples |
| TPS3705-50D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70550 | Samples |
| TPS3705-50DG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70550 | Samples |
| TPS3705-50DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAV | Samples |
| TPS3705-50DGNG4 | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAV | Samples |
| TPS3705-50DGNR | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAV | Samples |
| TPS3705-50DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70550 | Samples |
| TPS3705-50DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70550 | Samples |
| TPS3707-25D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70725 | Samples |
| TPS3707-25DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAW | Samples |
| TPS3707-25DGNR | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAW | Samples |
| TPS3707-25DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70725 | Samples |
| TPS3707-30D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70730 | Samples |



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| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3707-30DG4 | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70730 | |
| TPS3707-30DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAX | Samples |
| TPS3707-30DGNR | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAX | Samples |
| TPS3707-30DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70730 | Samples |
| TPS3707-33D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70733 | Samples |
| TPS3707-33DG4 | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70733 | |
| TPS3707-33DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAY | Samples |
| TPS3707-33DGNG4 | LIFEBUY | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAY | |
| TPS3707-33DGNR | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAY | Samples |
| TPS3707-33DGNRG4 | LIFEBUY | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAY | |
| TPS3707-33DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70733 | Samples |
| TPS3707-50D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70750 | Samples |
| TPS3707-50DGN | ACTIVE | HVSSOP | DGN | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAZ | Samples |
| TPS3707-50DGNR | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAZ | Samples |
| TPS3707-50DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 70750 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.



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**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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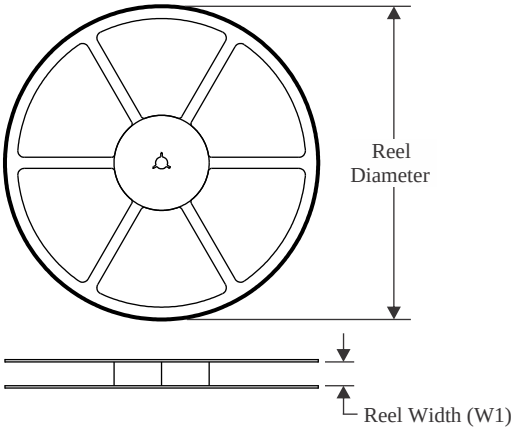
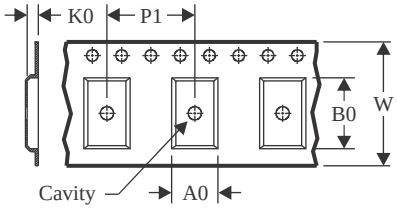
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

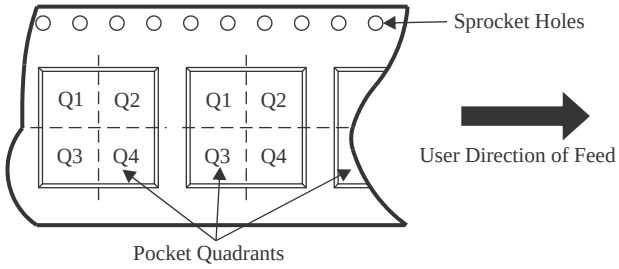



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3705-30DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3705-33DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3705-33DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3705-50DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3705-50DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3707-25DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3707-25DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3707-30DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3707-30DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3707-33DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3707-33DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3707-50DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3707-50DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |



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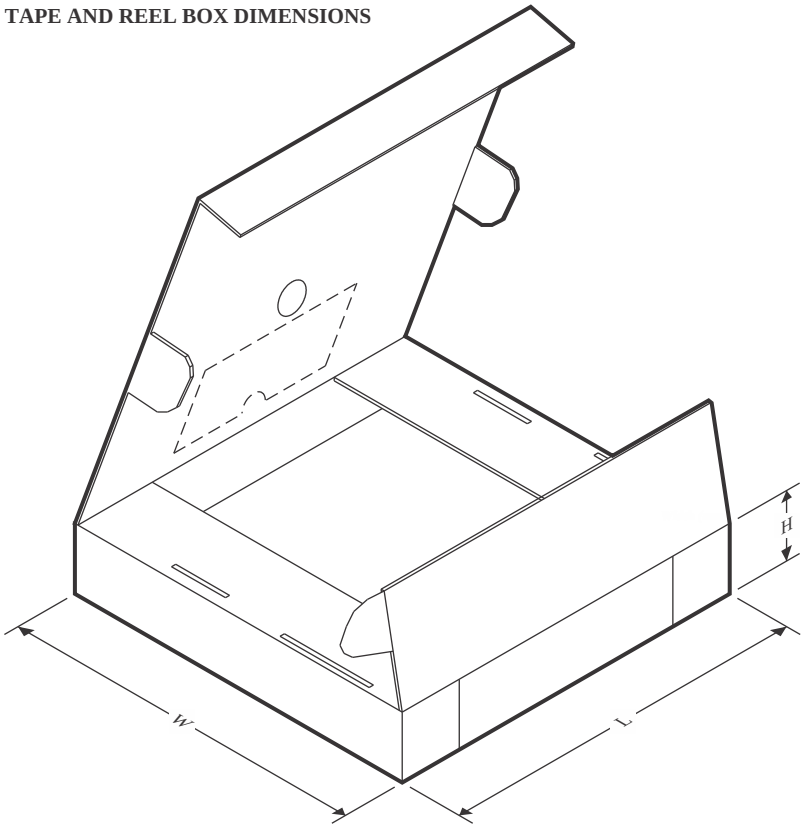
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3705-30DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3705-33DGNR | HVSSOP | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3705-33DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3705-50DGNR | HVSSOP | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3705-50DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3707-25DGNR | HVSSOP | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3707-25DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3707-30DGNR | HVSSOP | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3707-30DR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TPS3707-33DGNR | HVSSOP | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3707-33DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3707-50DGNR | HVSSOP | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3707-50DR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |



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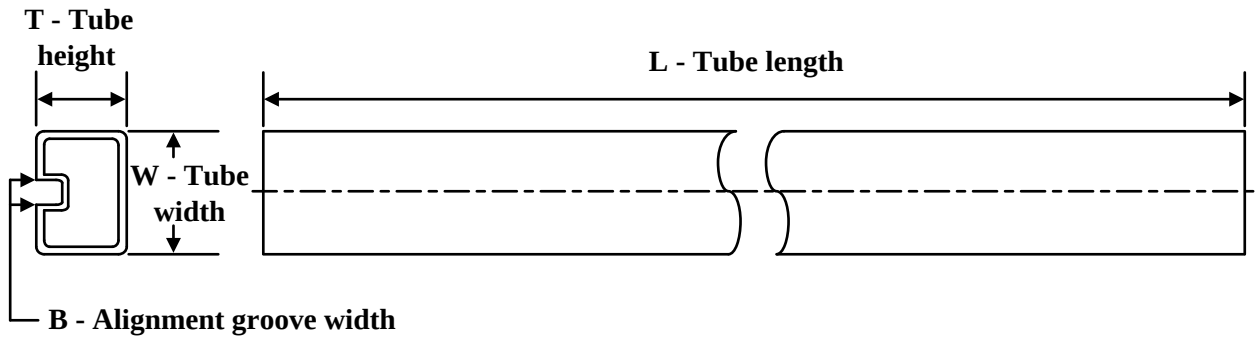
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS3705-30D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3705-30D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TPS3705-33D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3705-33DG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3705-50D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3705-50DG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3707-25D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3707-30D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3707-30D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TPS3707-30DG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TPS3707-30DG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3707-33D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3707-33DG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS3707-50D | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |



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# GENERIC PACKAGE VIEW

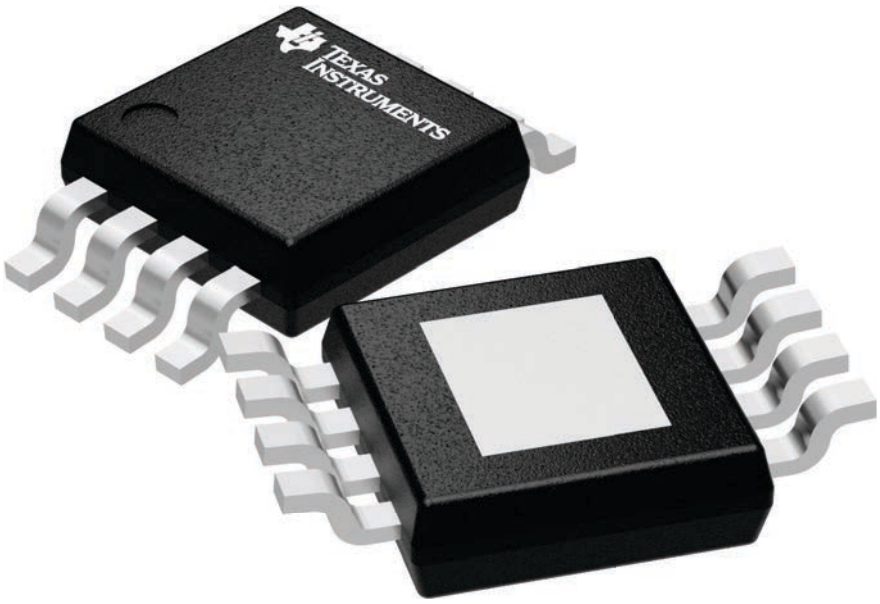
## DGN 8

## PowerPAD VSSOP - 1.1 mm max height

**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225482/A

TEXAS INSTRUMENTS

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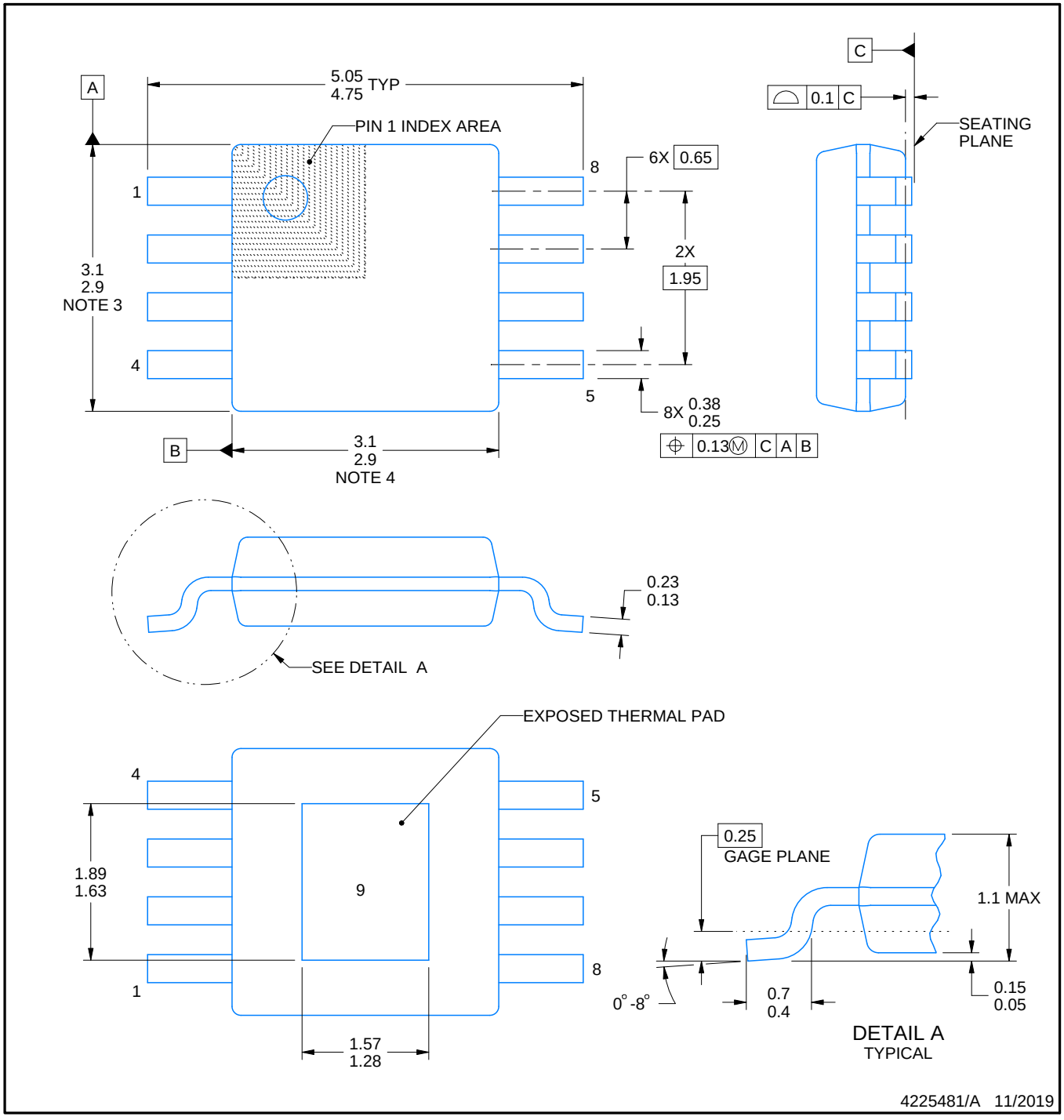
# PACKAGE OUTLINE

## DGN0008D

## PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

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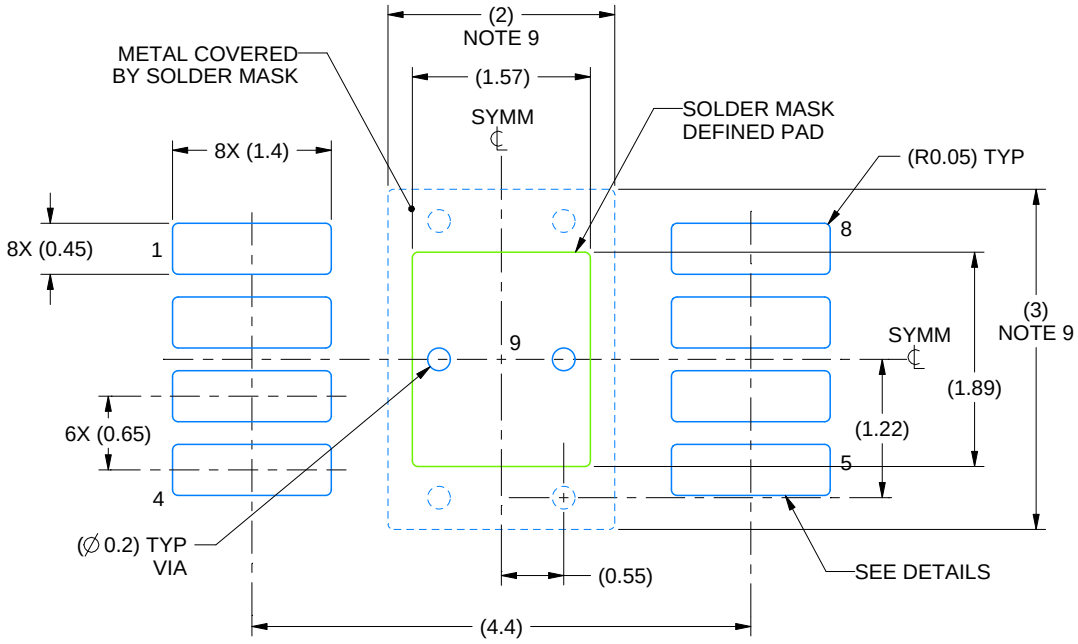
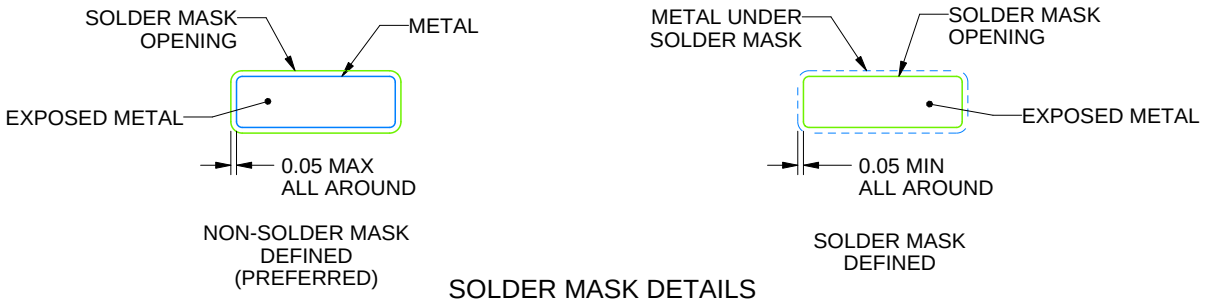



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

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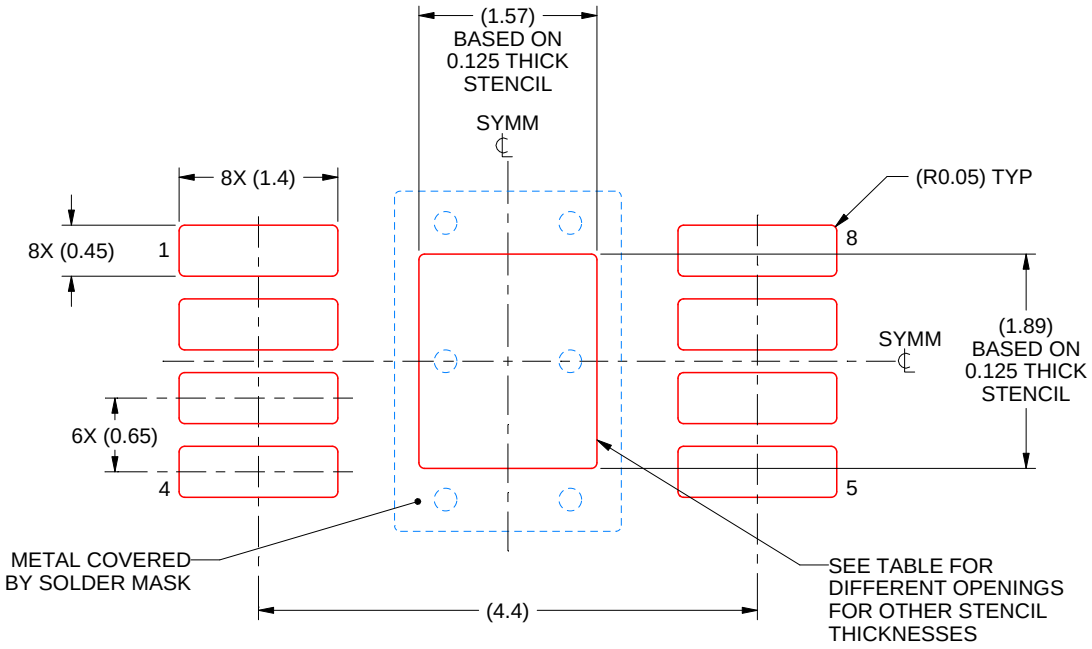
# EXAMPLE STENCIL DESIGN

## DGN0008D

## PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.76 X 2.11 |
| 0.125 | 1.57 X 1.89 (SHOWN) |
| 0.15 | 1.43 X 1.73 |
| 0.175 | 1.33 X 1.60 |

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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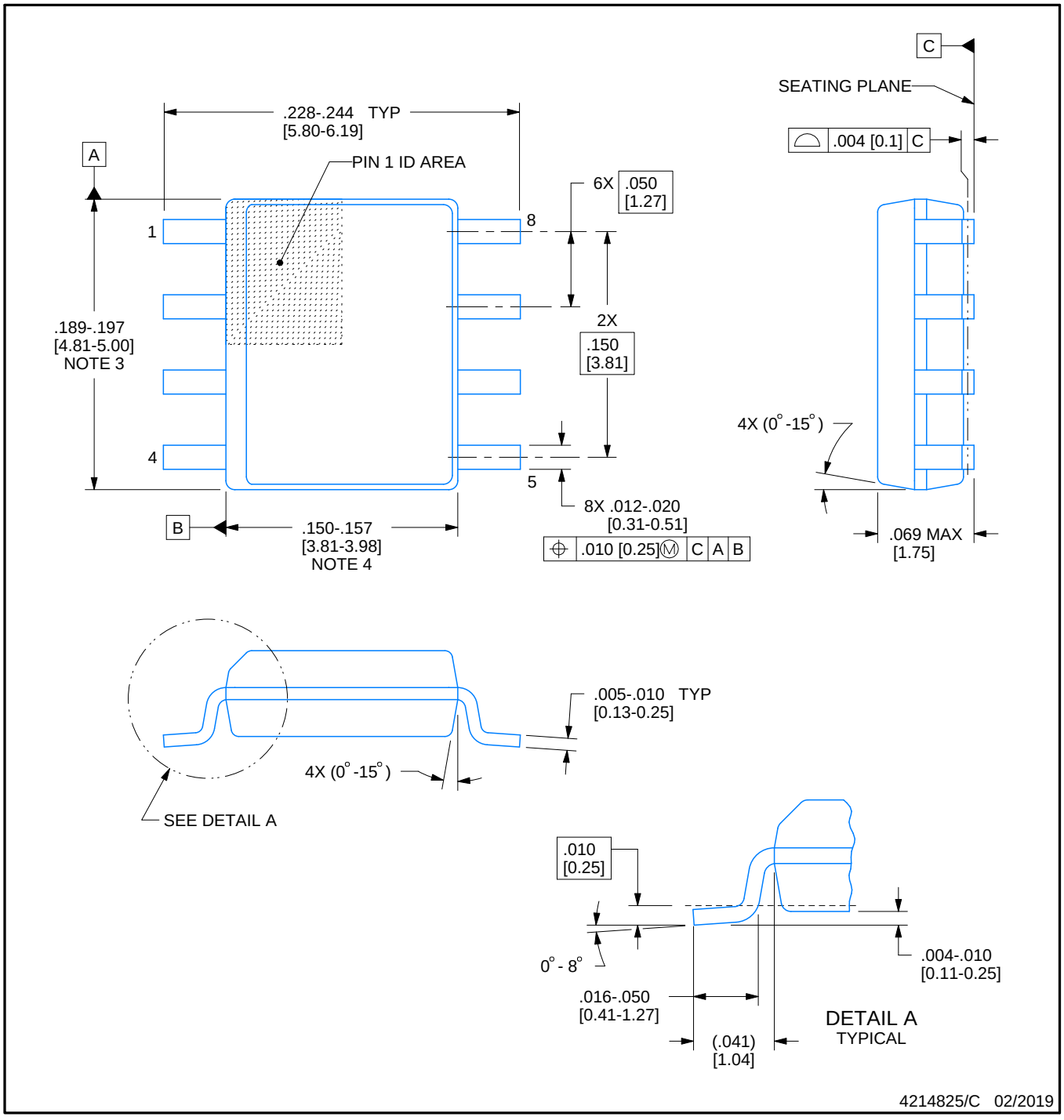
# PACKAGE OUTLINE

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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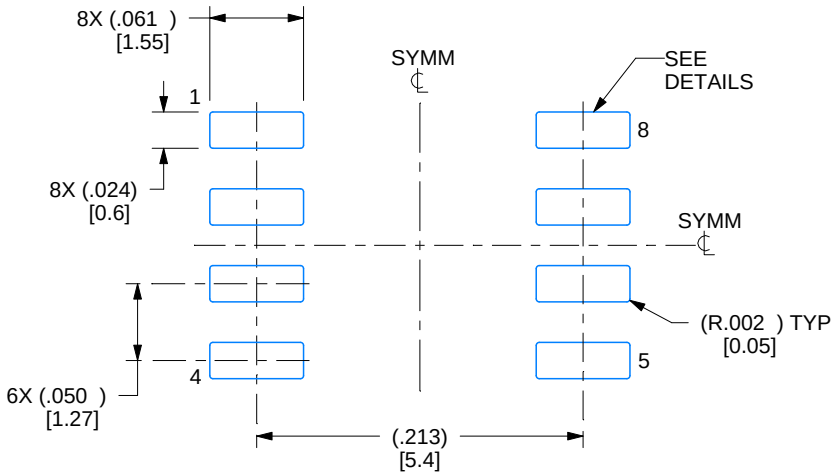
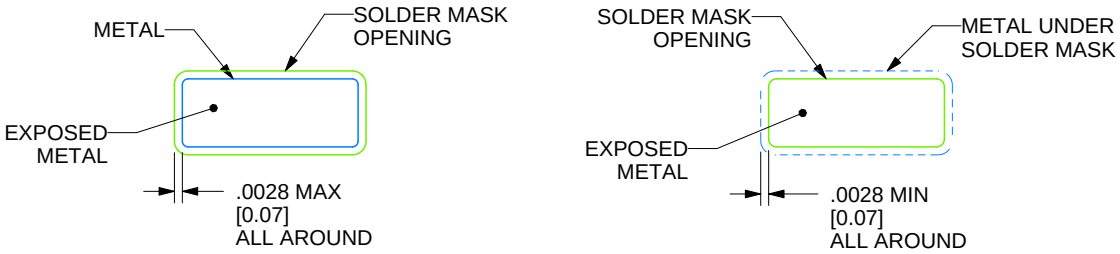



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.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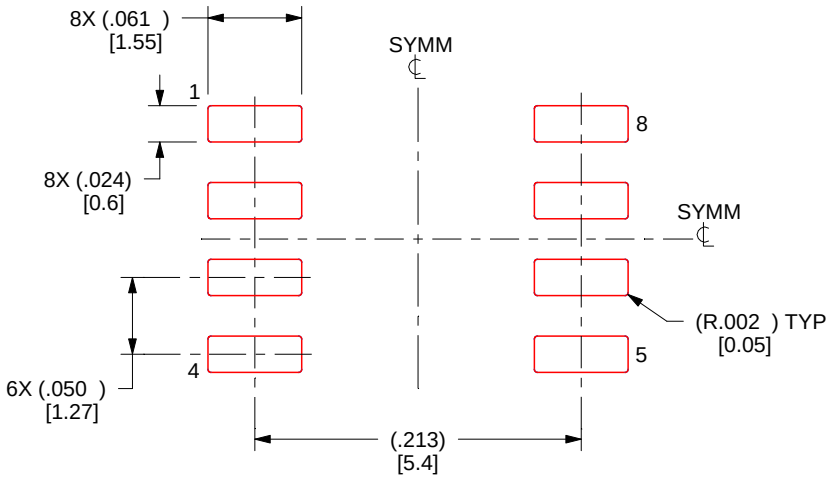
# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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