

## SNx4HC244 具有三态输出的八路缓冲器和线路驱动器

### 1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流输出可驱动多达 15 个 LSTTL 负载
- 三态输出驱动总线或缓冲存储器地址寄存器
- 低功耗： $I_{CC}$ ，80  $\mu$ A (最大值)
- $t_{pd}$  典型值 = 11ns
- $\pm 6$ mA 输出驱动 (电压为 5V 时)
- 低输入电流，最大值为 1 $\mu$ A
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数进行的测试。

### 2 应用

- 服务器
- 发光二极管 (LED) 显示屏
- 网络交换机
- 电信基础设施
- 电机驱动器
- I/O 扩展器

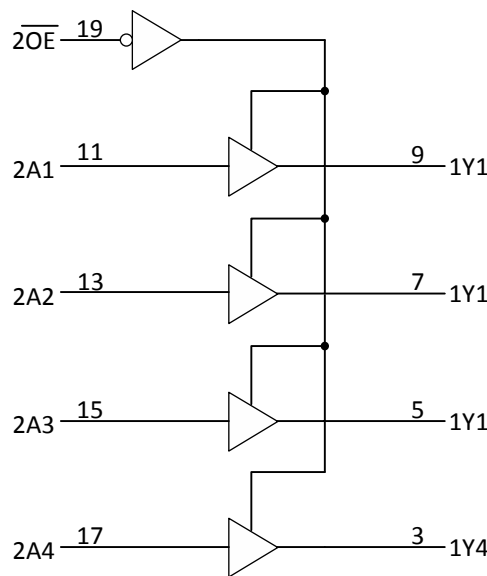
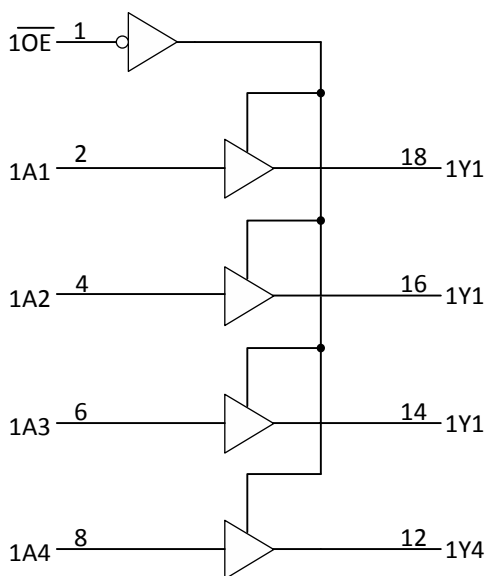
### 3 说明

SNx4HC244 八路缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。SNx4HC244 器件配备两个具有独立输出使能 ( $\overline{OE}$ ) 输入的 4 位缓冲器和驱动器。当  $\overline{OE}$  为低电平时，该器件将来自 A 输入的同相数据传递到 Y 输出。当  $\overline{OE}$  为高电平时，输出处于高阻态。

器件信息

器件型号	封装 (引脚) <sup>(1)</sup>	封装尺寸 (标称值)
SN54HC244	CDIP (20)	6.92mm × 24.38mm
	CFP (20)	6.92mm × 13.72mm
	LCCC (20)	8.89mm × 8.89mm
SN74HC244DB	SSOP (20)	5.30mm × 7.25mm
SN74HC244DW	SOIC (20)	7.50mm × 12.80mm
SN74HC244N	PDIP (20)	6.30mm × 25.40mm
SN74HC244NS	SOP (20)	5.30mm × 12.60mm
SN74HC244PW	TSSOP (20)	4.40mm × 6.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Copyright © 2016, Texas Instruments Incorporated

逻辑图 (正逻辑)



## Table of Contents

<b>1 特性</b> .....	1	8.1 Overview.....	12
<b>2 应用</b> .....	1	8.2 Functional Block Diagram.....	12
<b>3 说明</b> .....	1	8.3 Feature Description.....	12
<b>4 Revision History</b> .....	2	8.4 Device Functional Modes.....	12
<b>5 Pin Configuration and Functions</b> .....	3	<b>9 Application and Implementation</b> .....	13
Pin Functions.....	3	9.1 Application Information.....	13
<b>6 Specifications</b> .....	4	9.2 Typical Application.....	13
6.1 Absolute Maximum Ratings.....	4	<b>10 Power Supply Recommendations</b> .....	14
6.2 ESD Ratings.....	4	<b>11 Layout</b> .....	14
6.3 Recommended Operating Conditions.....	4	11.1 Layout Guidelines.....	14
6.4 Thermal Information.....	5	11.2 Layout Example.....	14
6.5 Electrical Characteristics.....	5	<b>12 Device and Documentation Support</b> .....	15
6.6 Electrical Characteristics - SN54HC244.....	5	12.1 Documentation Support.....	15
6.7 Electrical Characteristics - SN74HC244.....	6	12.2 接收文档更新通知.....	15
6.8 Switching Characteristics.....	6	12.3 支持资源.....	15
6.9 Switching Characteristics - $C_L = 50$ pF.....	8	12.4 Trademarks.....	15
6.10 Switching Characteristics - $C_L = 150$ pF.....	8	12.5 Electrostatic Discharge Caution.....	15
6.11 Typical Characteristic.....	9	12.6 术语表.....	15
<b>7 Parameter Measurement Information</b> .....	10	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	15
<b>8 Detailed Description</b> .....	12		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (May 2016) to Revision F (May 2022)	Page
• Junction-to-ambient thermal resistance values increased to match current function.....	5

Changes from Revision D (August 2003) to Revision E (May 2016)	Page
• 添加了 ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 向特性部分添加了“军用免责声明”.....	1
• 添加了应用部分.....	1
• 删除了“订购信息”表.....	1
• 添加了器件信息表.....	1

## 5 Pin Configuration and Functions

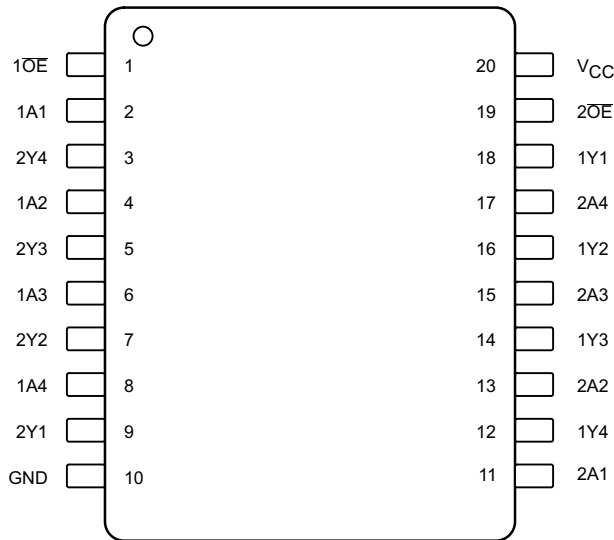


图 5-1. DB, DW, J, N, NS, PW, W Package 20-Pin SSOP, SOIC, CDIP, PDIP, SOP, TSSOP, or CFP Top View

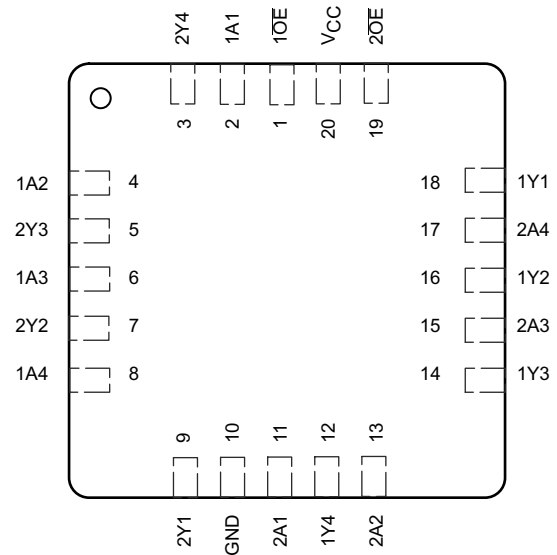


图 5-2. FK Package 20-Pin LCCC Top View

## Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	1 OE	I	Output Enable
2	1A1	I	Input
3	2Y4	O	Output
4	1A2	I	Input
5	2Y3	O	Output
6	1A3	I	Input
7	2Y2	O	Output
8	1A4	I	Input
9	2Y1	O	Output
10	GND	—	Ground
11	2A1	I	Input
12	1Y4	O	Output
13	2A2	I	Input
14	1Y3	O	Output
15	2A3	I	Input
16	1Y2	O	Output
17	2A4	I	Input
18	1Y1	O	Output
19	2 OE	I	Output Enable
20	V <sub>CC</sub>	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage range, $V_{CC}$	- 0.5	7	V
Input clamp current, $I_{IK}$	$V_I < 0$ or $V_I > V_{CC}$ <sup>(2)</sup>		±20 mA
Output clamp current, $I_{OK}$	$V_O < 0$ or $V_O > V_{CC}$ <sup>(2)</sup>		±20 mA
Continuous output current, $I_O$	$V_O = 0$ or $V_{CC}$		±35 mA
Continuous current through $V_{CC}$ or GND			±70 mA
Junction Temperature, $T_J$			150 °C
Storage temperature, $T_{stg}$	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

SN74HC244		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	2	5	6	V
$V_{IH}$ High-level input voltage	$V_{CC} = 2$ V	1.5		V
	$V_{CC} = 4.5$ V	3.15		
	$V_{CC} = 6$ V	4.2		
$V_{IL}$ Low-level input voltage	$V_{CC} = 2$ V		0.5	V
	$V_{CC} = 4.5$ V		1.35	
	$V_{CC} = 6$ V		1.8	
$V_I$ Input voltage	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	V
$\Delta t / \Delta v$ Input transition rise and fall time	$V_{CC} = 2$ V		1000	ns/V
	$V_{CC} = 4.5$ V		500	
	$V_{CC} = 6$ V		400	
$C_{pd}$ Power dissipation capacitance per buffer or driver (no load)		35		pF
$T_A$ Operating free-air temperature	SN54HC244	- 55	125	°C
	SN74HC244	- 40	85	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See the Texas Instruments application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 6.4 Thermal Information

THERMAL METRIC		SN74HC244					UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	122.7	84.6	113.4	131.8	°C/W
$R_{\theta JC (top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} = 2 \text{ V}$	1.9	1.998	V
			$V_{CC} = 4.5 \text{ V}$	4.4	4.499	
			$V_{CC} = 6 \text{ V}$	5.9	5.999	
		$I_{OH} = -6 \text{ mA}, V_{CC} = 4.5 \text{ V}$	3.98	4.3		
		$I_{OH} = -7.8 \text{ mA}, V_{CC} = 6 \text{ V}$	5.48	5.8		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	$V_{CC} = 2 \text{ V}$	0.002	0.1	V
			$V_{CC} = 4.5 \text{ V}$	0.001	0.1	
			$V_{CC} = 6 \text{ V}$	0.001	0.1	
		$I_{OL} = 6 \text{ mA}, V_{CC} = 4.5 \text{ V}$	0.17	0.26		
		$I_{OL} = 7.8 \text{ mA}, V_{CC} = 6 \text{ V}$	0.15	0.26		
$I_I$	$V_I = V_{CC}$ or 0, $V_{CC} = 6 \text{ V}$			$\pm 0.1$	$\pm 100$	nA
$I_{OZ}$	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or $V_{IL}$ , $V_{CC} = 6 \text{ V}$			$\pm 0.01$	$\pm 0.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$ , $V_{CC} = 6 \text{ V}$				8	$\mu\text{A}$
$C_i$	$V_{CC} = 2 \text{ V}$ to $6 \text{ V}$			3	10	pF

## 6.6 Electrical Characteristics - SN54HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} = 2 \text{ V}$	1.9		V
			$V_{CC} = 4.5 \text{ V}$	4.4		
			$V_{CC} = 6 \text{ V}$	5.9		
		$I_{OH} = -6 \text{ mA}, V_{CC} = 4.5 \text{ V}$	3.7			
		$I_{OH} = -7.8 \text{ mA}, V_{CC} = 6 \text{ V}$	5.2			

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu A$	$V_{CC} = 2 V$		0.1	V
			$V_{CC} = 4.5 V$		0.1	
			$V_{CC} = 6 V$		0.1	
		$I_{OL} = 6 mA, V_{CC} = 4.5 V$			0.4	
		$I_{OL} = 7.8 mA, V_{CC} = 6 V$			0.4	
$I_I$	$V_I = V_{CC}$ or 0, $V_{CC} = 6 V$				$\pm 1000$	nA
$I_{OZ}$	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or $V_{IL}$ , $V_{CC} = 6 V$				$\pm 10$	$\mu A$
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$ , $V_{CC} = 6 V$				160	$\mu A$
$C_i$	$V_{CC} = 2 V$ to $6 V$				10	pF

## 6.7 Electrical Characteristics - SN74HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu A$	$V_{CC} = 2 V$	1.9		V
			$V_{CC} = 4.5 V$	4.4		
			$V_{CC} = 6 V$	5.9		
		$I_{OH} = -6 mA, V_{CC} = 4.5 V$		3.84		
		$I_{OH} = -7.8 mA, V_{CC} = 6 V$	5.34			
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu A$	$V_{CC} = 2 V$		0.1	V
			$V_{CC} = 4.5 V$		0.1	
			$V_{CC} = 6 V$		0.1	
		$I_{OL} = 6 mA, V_{CC} = 4.5 V$			0.33	
		$I_{OL} = 7.8 mA, V_{CC} = 6 V$			0.33	
$I_I$	$V_I = V_{CC}$ or 0, $V_{CC} = 6 V$				$\pm 1000$	nA
$I_{OZ}$	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or $V_{IL}$ , $V_{CC} = 6 V$				$\pm 5$	$\mu A$
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$ , $V_{CC} = 6 V$				80	$\mu A$
$C_i$	$V_{CC} = 2 V$ to $6 V$				10	pF

## 6.8 Switching Characteristics

$T_A = 25^\circ C$  (unless otherwise noted; see [Figure 7-1](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd}$	From A (input) to Y (output)	$V_{CC} = 2 V$	$C_L = 50 pF$	40	115	ns
			$C_L = 150 pF$	56	165	
		$V_{CC} = 4.5 V$	$C_L = 50 pF$	13	23	
			$C_L = 150 pF$	18	33	
		$V_{CC} = 6 V$	$C_L = 50 pF$	11	20	
			$C_L = 150 pF$	15	28	
$t_{en}$	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 V$	$C_L = 50 pF$	75	150	ns
			$C_L = 150 pF$	100	200	
		$V_{CC} = 4.5 V$	$C_L = 50 pF$	15	30	
			$C_L = 150 pF$	20	40	
		$V_{CC} = 6 V$	$C_L = 50 pF$	13	26	
			$C_L = 150 pF$	17	34	

$T_A = 25^\circ\text{C}$  (unless otherwise noted; see [图 7-1](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{dis}$	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2\text{ V}$	$C_L = 50\text{ pF}$	75	150	ns
		$V_{CC} = 4.5\text{ V}$	$C_L = 50\text{ pF}$	15	30	
		$V_{CC} = 6\text{ V}$	$C_L = 50\text{ pF}$	13	26	
$t_t$	To Y (output)	$V_{CC} = 2\text{ V}$	$C_L = 50\text{ pF}$	28	60	ns
			$C_L = 150\text{ pF}$	45	210	
		$V_{CC} = 4.5\text{ V}$	$C_L = 50\text{ pF}$	8	12	
			$C_L = 150\text{ pF}$	17	42	
		$V_{CC} = 6\text{ V}$	$C_L = 50\text{ pF}$	6	10	
			$C_L = 150\text{ pF}$	13	36	

## 6.9 Switching Characteristics - $C_L = 50 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted; see [Figure 7-1](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd}$	From A (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		170	ns
			SN74HC244		145	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		34	
			SN74HC244		29	
		$V_{CC} = 6 \text{ V}$	SN54HC244		29	
			SN74HC244		25	
$t_{en}$	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		225	ns
			SN74HC244		190	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		45	
			SN74HC244		38	
		$V_{CC} = 6 \text{ V}$	SN54HC244		38	
			SN74HC244		32	
$t_{dis}$	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		225	ns
			SN74HC244		190	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		45	
			SN74HC244		38	
		$V_{CC} = 6 \text{ V}$	SN54HC244		38	
			SN74HC244		32	
$t_t$	To Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		90	ns
			SN74HC244		75	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		18	
			SN74HC244		15	
		$V_{CC} = 6 \text{ V}$	SN54HC244		15	
			SN74HC244		13	

## 6.10 Switching Characteristics - $C_L = 150 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted; see [Figure 7-1](#))

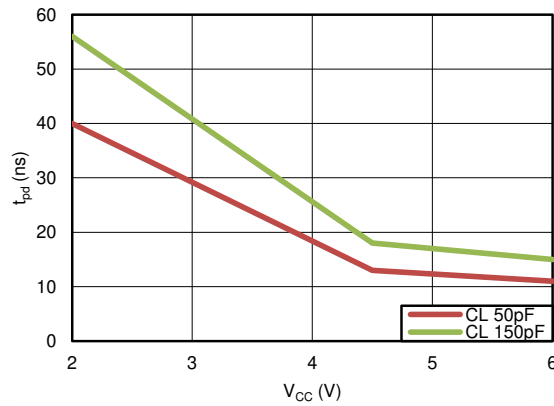
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd}$	From A (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		245	ns
			SN74HC244		210	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		49	
			SN74HC244		42	
		$V_{CC} = 6 \text{ V}$	SN54HC244		42	
			SN74HC244		35	
$t_{en}$	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		300	ns
			SN74HC244		250	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		60	
			SN74HC244		50	
		$V_{CC} = 6 \text{ V}$	SN54HC244		51	
			SN74HC244		43	



over recommended operating free-air temperature range (unless otherwise noted; see [图 7-1](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_t$	To Y (output)	$V_{CC} = 2\text{ V}$	SN54HC244		315	ns
			SN74HC244		265	
		$V_{CC} = 4.5\text{ V}$	SN54HC244		63	
			SN74HC244		53	
		$V_{CC} = 6\text{ V}$	SN54HC244		53	
			SN74HC244		45	

### 6.11 Typical Characteristic



**图 6-1. Propagation Delay**

## 7 Parameter Measurement Information

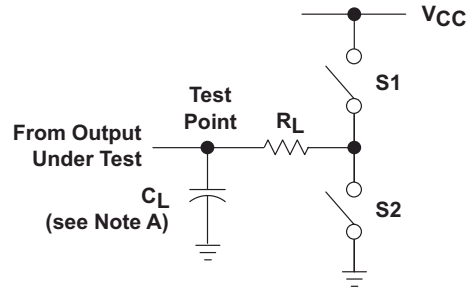


图 7-1. Load Circuit

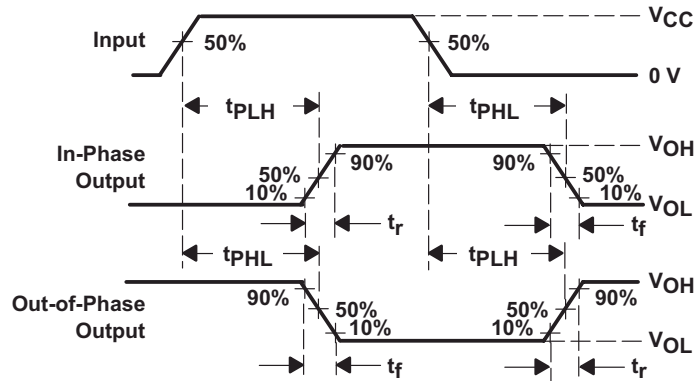


图 7-2. Propagation Delay and Output Transition Times

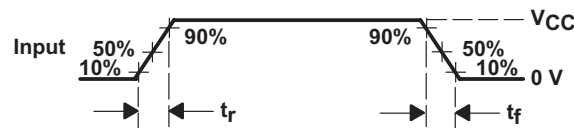


图 7-3. Input Rise and Fall Times

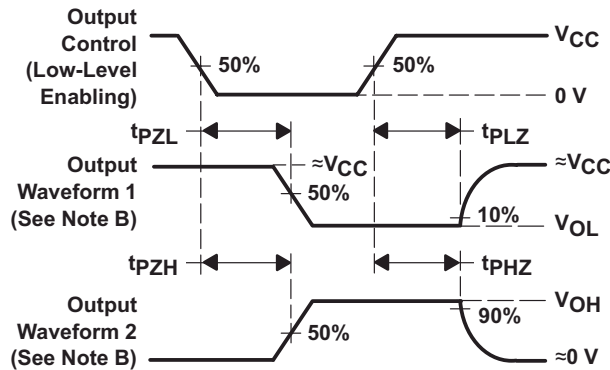


图 7-4. Enable and Disable Times for 3-State Outputs

备注

NOTE:

- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**表 7-1. Switching Information Table**

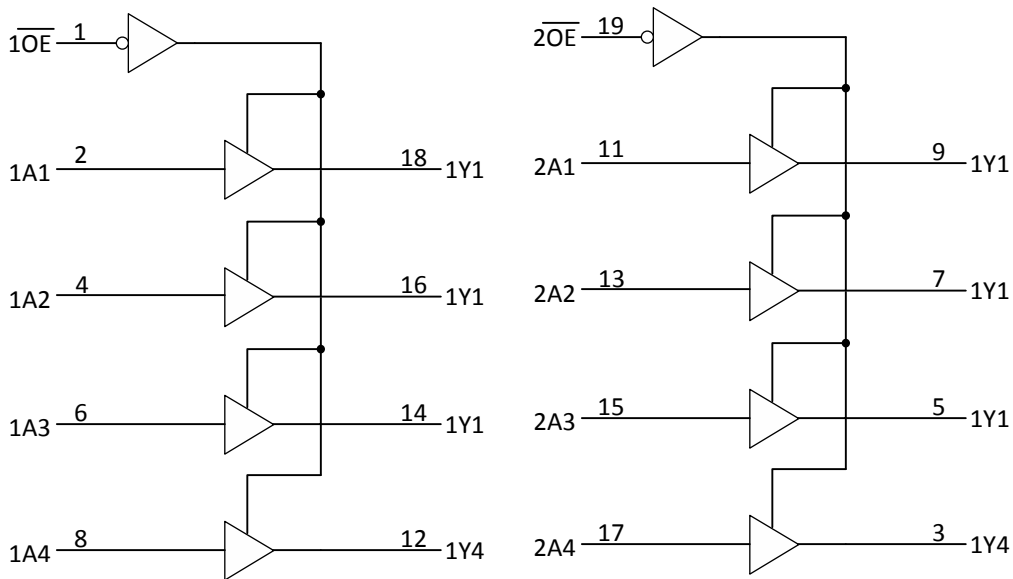
PARAMETER		RL	CL	S1	S2
$t_{en}$	$t_{PZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{PZL}$	1 k $\Omega$	50 pF or 150 pF	Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{PLZ}$	1 k $\Omega$	50 pF	Closed	Open
$t_{pd}$ or $t_t$		—	50 pF or 150 pF	Open	Open

## 8 Detailed Description

### 8.1 Overview

The SNx4HC244 device is organized as two 4-bit buffers and line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 8.3 Feature Description

The SNx4HC244 has a wide operating voltage of 2 V to 6 V. Inputs accept voltage levels up to  $V_{CC}$ . This device has a low power consumption of  $I_{CC}$  80  $\mu$ A (maximum). The SNx4HC244 device can drive  $\pm 6$  mA at  $V_{CC}$  of 5 V.

### 8.4 Device Functional Modes

表 8-1 lists the functions of the SNx4HC244.

表 8-1. Function Table  
(Each Buffer or Driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

## 9 Application and Implementation

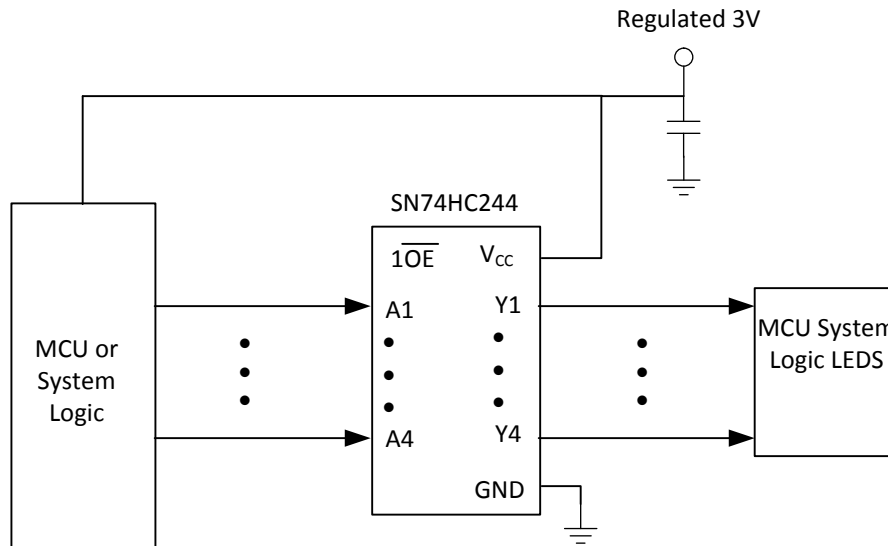
### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

SN74HC244 is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 9.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

图 9-1. SN74HC244 Application Schematic

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t / \Delta V$  in [§ 6.3](#).
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in [§ 6.3](#).
2. Recommend output conditions:
  - Load currents should not exceed  $I_O$  max per output and should not exceed the continuous current through  $V_{CC}$  or GND total current for the part. These limits are located in [§ 6.1](#).
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curve

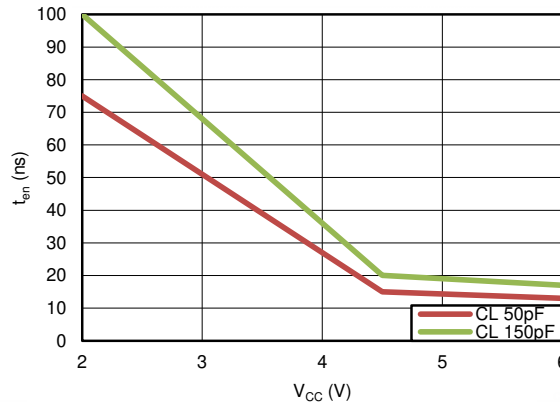


图 9-2. Enable Time

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [# 6.3](#).

Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor. If there are multiple V<sub>CC</sub> terminals, then TI recommends 0.01- μ F or 0.022- μ F capacitors for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input and gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [图 11-1](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient.

### 11.2 Layout Example

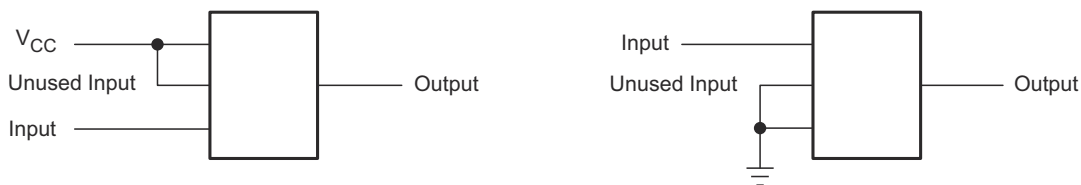


图 11-1. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Links

表 12-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC244	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HC244	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8409601VRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8409601VR A SNV54HC244J	Samples
5962-8409601VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8409601VS A SNV54HC244W	Samples
84096012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK	Samples
8409601RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409601RA SNJ54HC244J	Samples
8409601SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W	Samples
JM38510/65705B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65705B2A	Samples
JM38510/65705BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65705BRA	Samples
JM38510/65705BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65705BSA	Samples
M38510/65705B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65705B2A	Samples
M38510/65705BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65705BRA	Samples
M38510/65705BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65705BSA	Samples
SN54HC244J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC244J	Samples
SN74HC244APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244A	Samples
SN74HC244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC244DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	<a href="#">Samples</a>
SN74HC244N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC244N	<a href="#">Samples</a>
SN74HC244NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC244N	<a href="#">Samples</a>
SN74HC244NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	<a href="#">Samples</a>
SN74HC244NSRG4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	<a href="#">Samples</a>
SN74HC244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	<a href="#">Samples</a>
SN74HC244PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	<a href="#">Samples</a>
SN74HC244PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	<a href="#">Samples</a>
SN74HC244QDWRG4Q1	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		HC244Q	<a href="#">Samples</a>
SNJ54HC244FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK	<a href="#">Samples</a>
SNJ54HC244J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409601RA SNJ54HC244J	<a href="#">Samples</a>
SNJ54HC244W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC244, SN54HC244-SP, SN74HC244 :**

- Catalog : [SN74HC244](#), [SN54HC244](#)
- Automotive : [SN74HC244-Q1](#), [SN74HC244-Q1](#)
- Enhanced Product : [SN74HC244-EP](#), [SN74HC244-EP](#)
- Military : [SN54HC244](#)
- Space : [SN54HC244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC244DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244QDWRG4Q1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC244APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC244APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244DWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC244QDWRG4Q1	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8409601VSA	W	CFP	20	25	506.98	26.16	6220	NA
84096012A	FK	LCCC	20	1	506.98	12.06	2030	NA
8409601SA	W	CFP	20	1	506.98	26.16	6220	NA
JM38510/65705B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/65705BSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/65705B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/65705BSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74HC244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC244FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HC244W	W	CFP	20	1	506.98	26.16	6220	NA

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

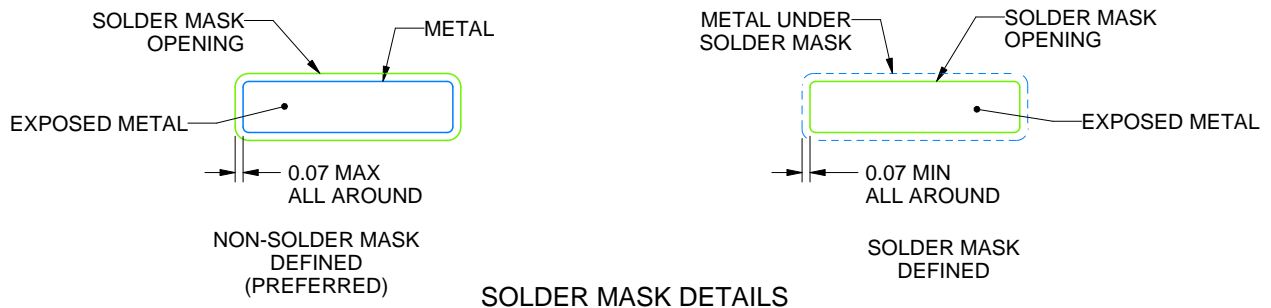
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

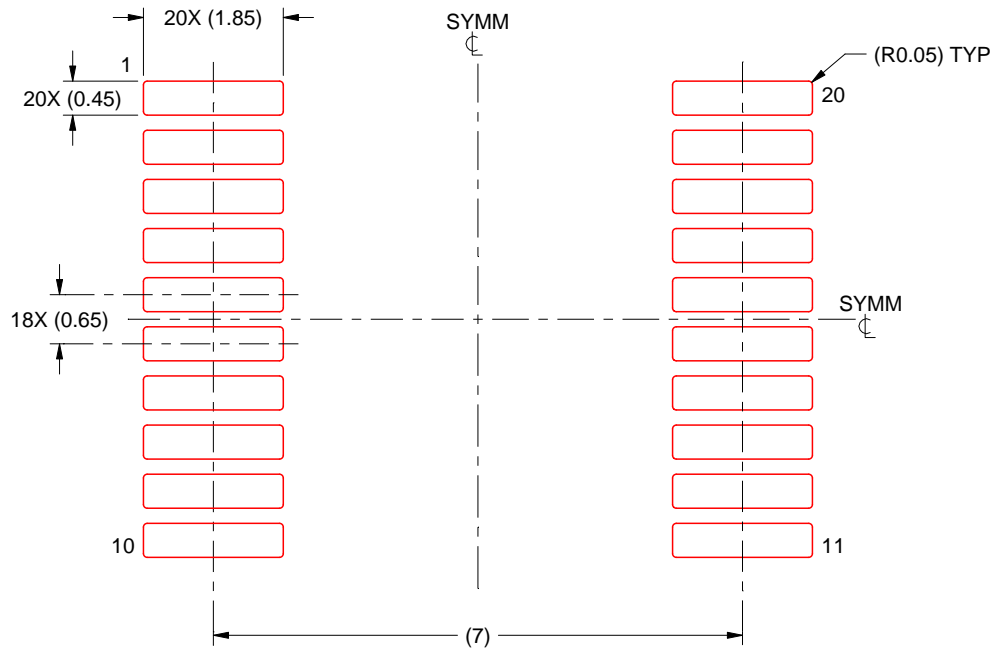


# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

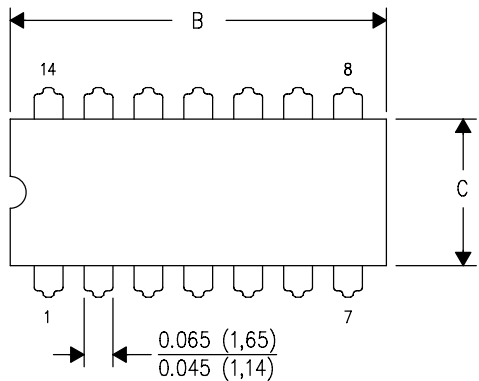
14-PINS SHOWN



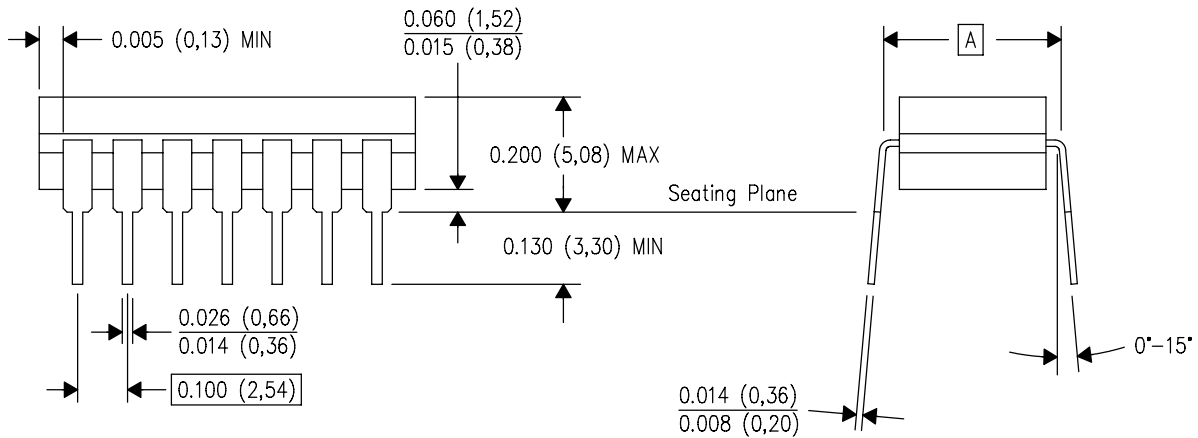
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

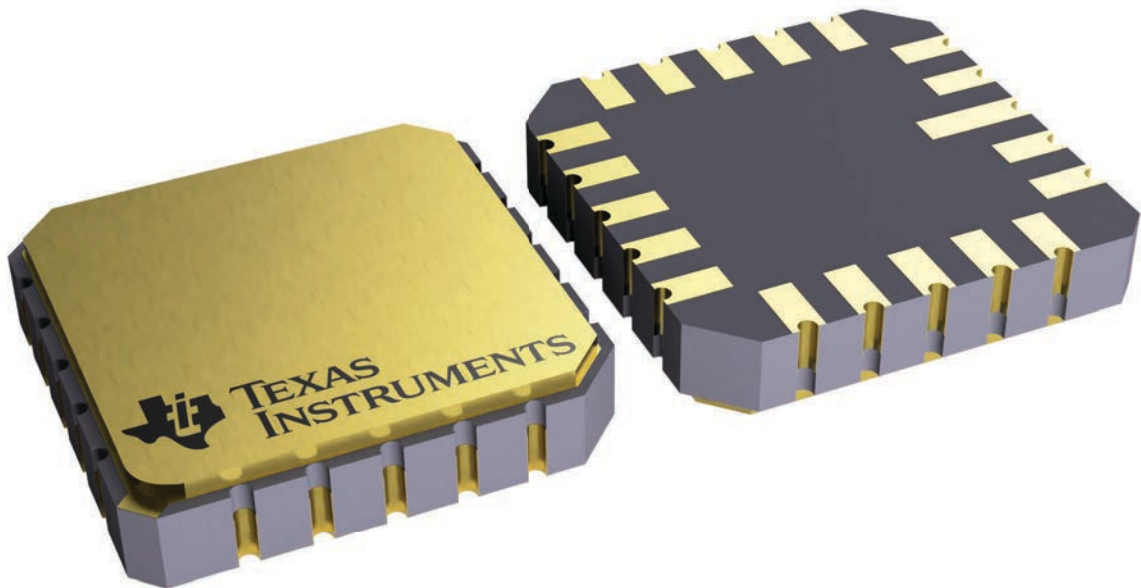
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

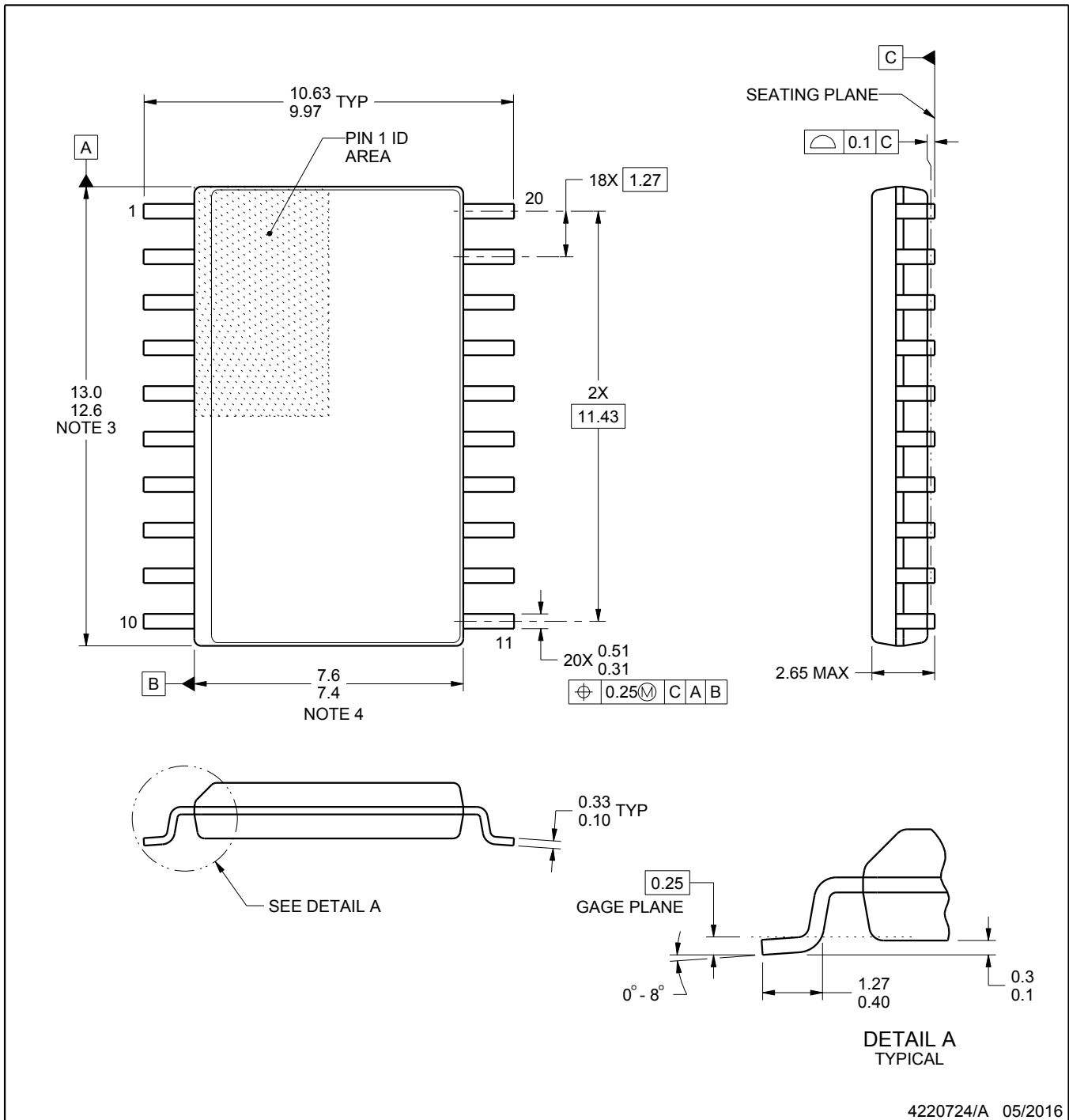
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

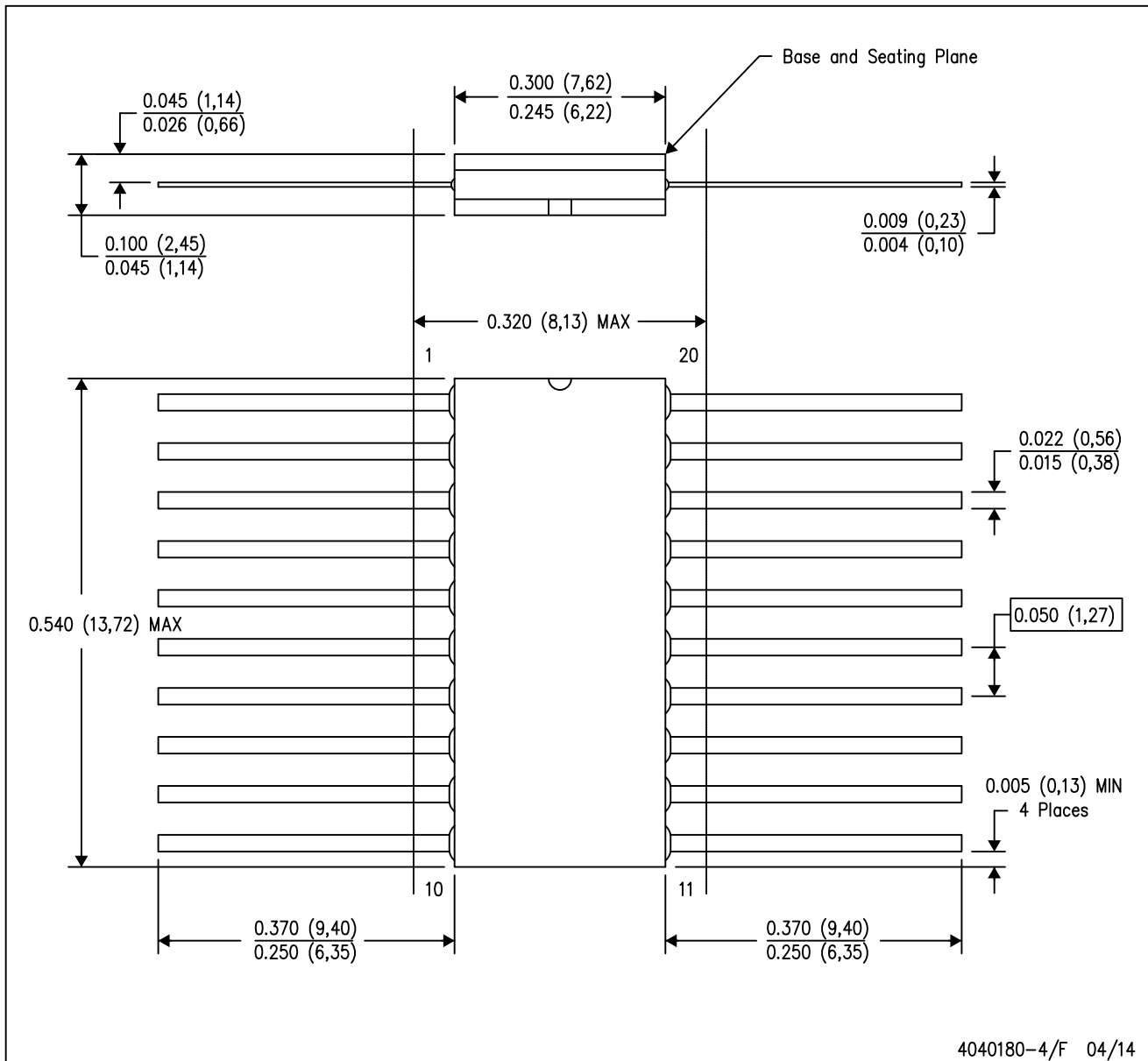
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

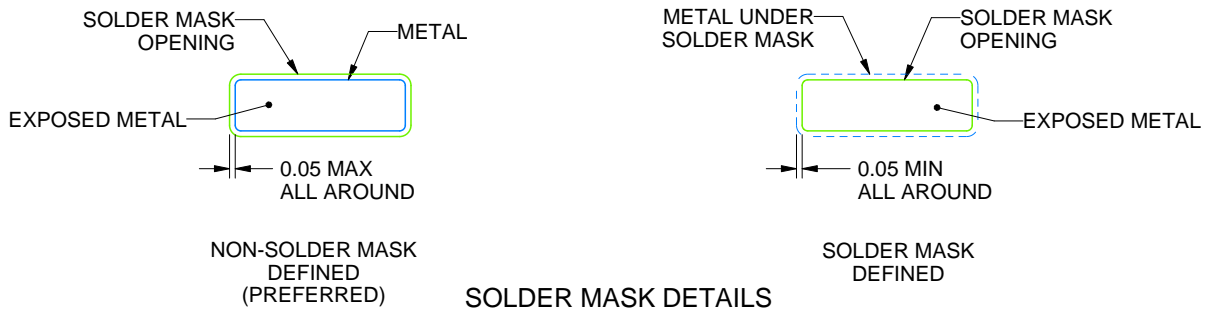
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司

单击下面可查看定价，库存，交付和生命周期等信息

[>>TI\(德州仪器\)](#)