LM5020 100V Current Mode PWM Controller

Check for Samples: LM5020

FEATURES

- **Internal Start-up Bias Regulator**
- **Error Amplifier**
- **Precision Voltage Reference**
- **Programmable Softstart**
- **1A Peak Gate Driver**
- **Maximum Duty Cycle Limiting (80% for LM5020-1 or 50% for LM5020-2)**
- **Programmable Line Under Voltage Lockout (UVLO) with Adjustable Hysteresis**
- **Cycle-by-Cycle Over-Current Protection**
- **Slope Compensation (LM5020-1)**
- **Programmable Oscillator Frequency with Synchronization Capability**
- **Current Sense Leading Edge Blanking**
- **Thermal Shutdown Protection**

APPLICATIONS

- **Telecommunication Power Converters**
- **Industrial Power Converters**
- **+42V Automotive Systems**

PACKAGES

- **VSSOP-10**
- **WSON-10 (4 mm x 4 mm)**

DESCRIPTION

The LM5020 high voltage pulse-width-modulation (PWM) controller contains all of the features needed to implement single ended primary power converter topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent line feed-forward. The LM5020 includes a high-voltage start-up regulator that operates over a wide input range up to 100V. The PWM controller is designed for high speed capability including an oscillator frequency range to 1MHz and total propagation delays less than 100ns. Additional features include an error amplifier, precision reference, line under-voltage lockout, cycle-by-cycle current limit, slope compensation, softstart, oscillator synchronization capability and thermal shutdown. The controller is available in both VSSOP-10 and WSON-10 packages.

Typical Application Circuit

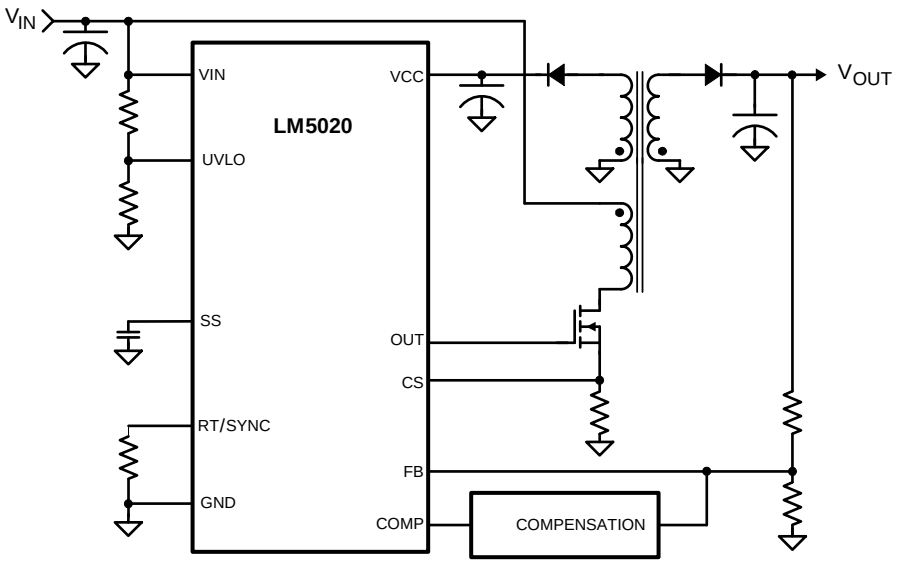


Figure 1. Non-Isolated Flyback Converter

Connection Diagram

Top View

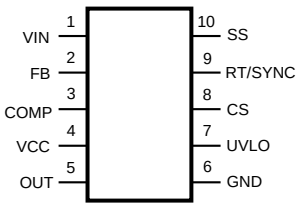


Figure 2. 10-Lead VSSOP, WSON

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	VIN	Source Input Voltage	Input to the start-up regulator. Input range is 13V to 100V.
2	FB	Feedback Signal	Inverting input of the internal error amplifier. The non-inverting input is internally connected to a 1.25V reference.
3	COMP	The output of the error amplifier and input to the Pulse Width Modulator	COMP pull-up is provided by an internal 5K resistor which may be used to bias an opto-coupler transistor.
4	VCC	Output of the internal high voltage series pass regulator. Regulated output voltage is 7.7V	If an auxiliary winding raises the voltage on this pin above the regulation set point, the internal series pass regulator will shut down, reducing the internal power dissipation.
5	OUT	Output of the PWM controller	Gate driver output with a 1A peak current capability.
6	GND	Ground return	
7	UVLO	Line Under-Voltage Shutdown	An external resistor divider from the power converter source voltage sets the shutdown levels. The threshold at this pin is 1.25V. Hysteresis is set by a switched internal 20µA current source.
8	CS	Current Sense input	Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5V the OUT pin switches low for cycle-by-cycle current limiting. CS is held low for 50ns after OUT switches high to blank leading edge current spikes.
9	RT / SYNC	Oscillator timing resistor pin and synchronization input	An external resistor connected from RT to GND sets the oscillator frequency. This pin also accepts synchronization pulses from an external clock.
10	SS	Softstart Input	An external capacitor and an internal 10µA current source set the soft-start ramp rate.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VIN to GND		-0.3V to 100V
VCC to GND		-0.3V to 16V
RT to GND		-0.3V to 5.5V
All other pins to GND		-0.3V to 7V
Power Dissipation		Internally Limited
ESD Rating[3]	Human Body Model	2kV
Storage Temperature		-65°C to +150°C
Junction Temperature		150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor.

Operating Ratings

VIN Voltage	13V to 90V
External Voltage applied to VCC	8V to 15V
Operating Junction Temperature	-40°C to +125°C

Electrical Characteristics

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: VIN = 48V, VCC = 10V, and RT = 31.6kΩ.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator						
V_{CC}Reg	V_{CC} Regulation	V_{CC} = Open	**7.4**	7.7	**8.0**	V
	V_{CC} Current Limit	See[2]	**15**	22		mA
I-V_{IN}	Startup Regulator Leakage	V_{IN} = 100V		150	**500**	µA
I_{IN}	Shutdown Current	V_{UVLO} = 0V, V_{CC} = open		250	**350**	µA
VCC Supply						
	V_{CC} UVLO (Rising)		**VccReg - 300mV**	VccReg - 100mV		V
	V_{CC} UVLO (Falling)		**5.3**	6.0	**6.7**	V
I_{CC}	Supply Current	Cload = 0		2	**3**	mA
Error Amplifier						
GBW	Gain Bandwidth			4		MHz
	DC Gain			75		dB
	Reference Voltage	FB = COMP	**1.225**	1.25	**1.275**	V
	COMP Sink Capability	FB = 1.5V COMP= 1V	**5**	17		mA
UVLO Pin						
	Shutdown Threshold		**1.225**	1.25	**1.275**	V
	Undervoltage Shutdown Hysteresis Current Source		**16**	20	**24**	µA
Current Limit						
	ILIM Delay to Output	CS step from 0 to 0.6V Time to onset of OUT Transition (90%)		30		ns
	Cycle by Cycle CS Threshold Voltage		**0.45**	0.5	**0.55**	V
	Leading Edge Blanking Time			50		ns

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).
(2) Device thermal limitations may limit usable range.

Electrical Characteristics (continued)

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: VIN = 48V, VCC = 10V, and RT = 31.6kΩ.(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	CS Sink Impedance (clocked)			35	**55**	Ω
Soft Start						
	Softstart Current Source		**7**	10	**13**	µA
	Softstart to COMP Offset		**0.35**	0.55	**0.75**	V
Oscillator						
	Frequency1 (RT = 31.6k)	See(3)	**175**	200	**225**	kHz
	Frequency2 (RT = 9.76k)	See(3)	**560**	630	**700**	kHz
	Sync threshold		**2.4**	3.2	**3.8**	V
PWM Comparator						
	Delay to Output	COMP set to 2V, CS stepped 0 to 0.4V, Time to onset of OUT transition low		25		ns
	Min Duty Cycle	COMP=0V			0	%
	Max Duty Cycle (-1 Device)		**75**	80	**85**	%
	Max Duty Cycle (-2 Device)			50		%
	COMP to PWM Comparator Gain			0.33		
	COMP Open Circuit Voltage		**4.3**	5.2	**6.1**	V
	COMP Short Circuit Current	COMP=0V	**0.6**	1.1	**1.5**	mA
Slope Compensation						
	Slope Comp Amplitude (LM5020-1 Device Only)	Delta increase at PWM Comparator to CS	**80**	105	**130**	mV
Output Section						
	Output High Saturation	Iout = 50mA, V_{CC} - V_{OUT}		0.25	**0.75**	V
	Output Low Saturation	I_{OUT} = 100mA, V_{OUT}		0.25	**0.75**	V
	Rise Time	Cload = 1nF		18		ns
	Fall Time	Cload = 1nF		15		ns
Thermal Shutdown						
Tsd	Thermal Shutdown Temp.			165		°C
	Thermal Shutdown Hysteresis			25		°C

(3) Specification applies to the oscillator frequency. The operational frequency of the LM5020-2 devices is divided by two.

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C.

V_{CC} and V_{IN} vs V_{IN}

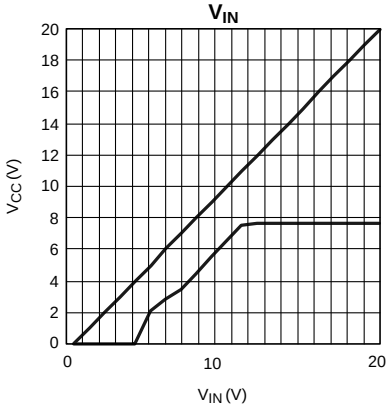


Figure 3.

V_{CC} vs I_{CC} (V_{IN} = 48V)

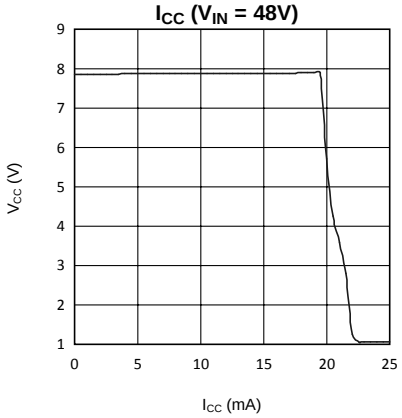


Figure 4.

Oscillator Frequency vs RT

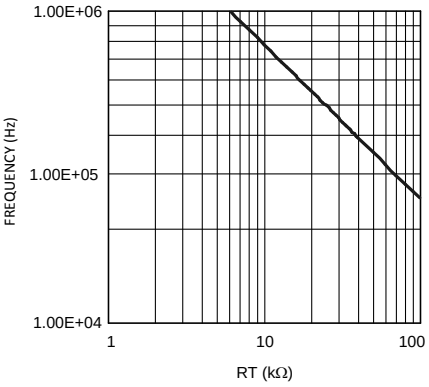


Figure 5.

Oscillator Frequency vs Temperature RT = 31.6kΩ

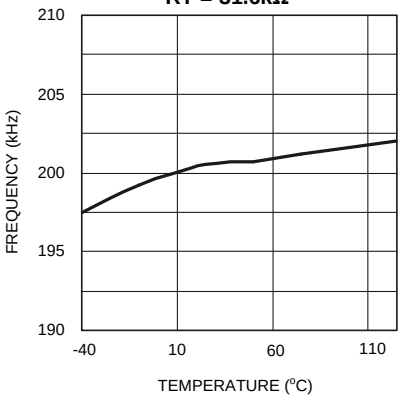


Figure 6.

Soft Start Current vs Temperature

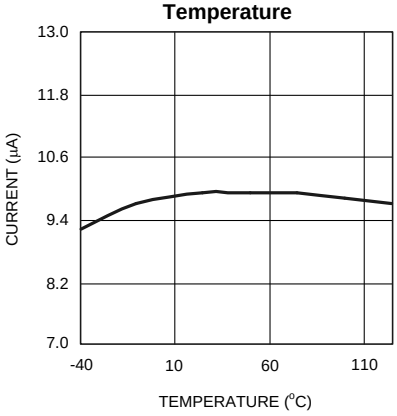


Figure 7.

Error Amp. Gain/Phase Plot

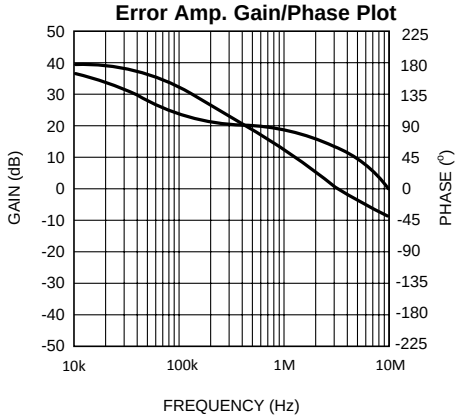
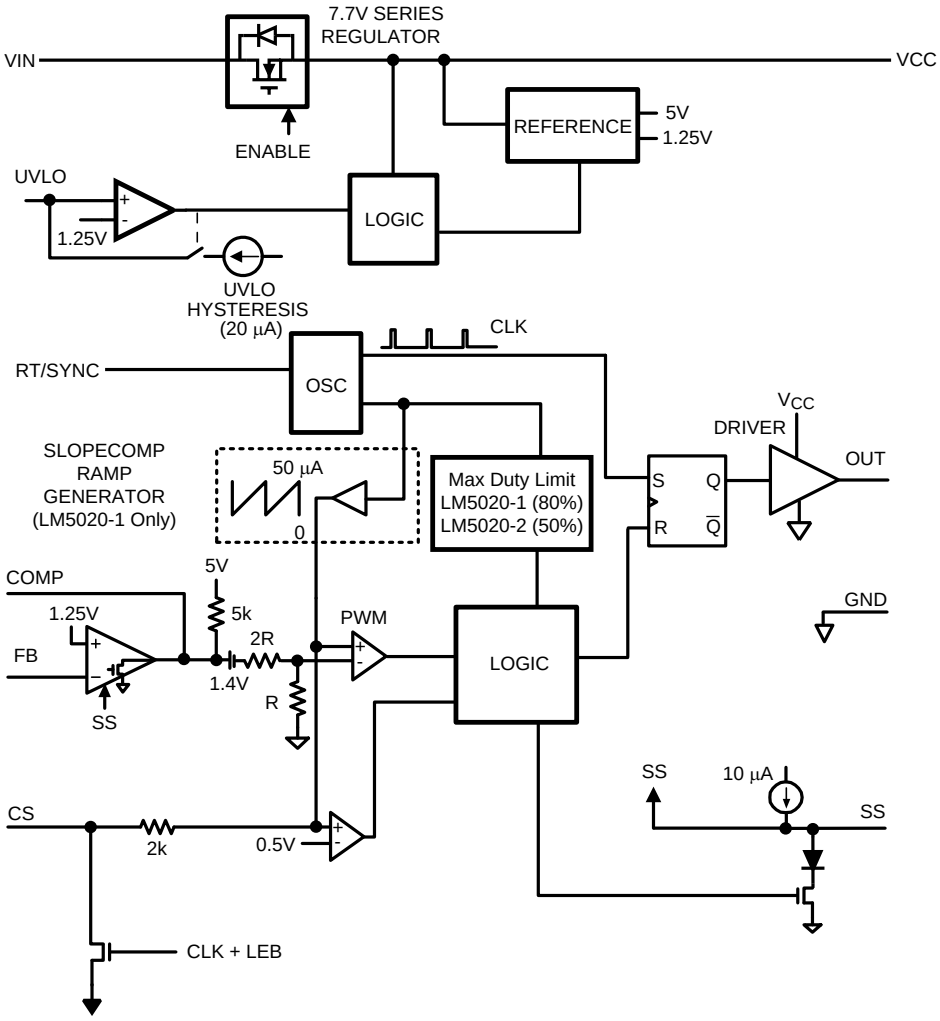


Figure 8.

Block Diagram



DETAILED OPERATING DESCRIPTION

The LM5020 High Voltage PWM controller contains all of the features needed to implement single ended primary power converter topologies. The LM5020 includes a high-voltage startup regulator that operates over a wide input range to 100V. The PWM controller is designed for high speed capability including an oscillator frequency range to 1MHz and total propagation delays less than 100ns. Additional features include an error amplifier, precision reference, line under-voltage lockout, cycle-by-cycle current limit, slope compensation, softstart, oscillator sync capability and thermal shutdown. The functional block diagram of the LM5020 is shown in Figure 1. The LM5020 is designed for current-mode control power converters, which require a single drive output, such as Flyback and Forward topologies. The LM5020 provides all of the advantages of current-mode control including line feed-forward, cycle-by-cycle current limiting and simplified loop compensation .

High Voltage Start-Up Regulator

The LM5020 contains an internal high voltage startup regulator, that allows the input pin (Vin) to be connected directly to line voltages as high as 100V. The regulator output is internally current limited to 15mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance range for the Vcc regulator is 0.1µF to 100µF. When the voltage on the V_{CC} pin reaches the regulation level of 7.7V, the controller output is enabled. The controller will remain enabled until V_{CC} falls below 6V.

In typical applications, a transformer auxiliary winding is connected through a diode to the V_{CC} pin. This winding should raise the V_{CC} voltage above 8V to shut off the internal startup regulator. Powering V_{CC} from an auxiliary winding improves conversion efficiency while reducing the power dissipated in the controller. The external V_{CC} capacitor must be selected such that the capacitor maintains the Vcc voltage greater than the V_{CC} UVLO falling threshold (6V) during the initial start-up. During a fault condition when the converter auxiliary winding is inactive, external current draw on the V_{CC} line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation capability of the controller.

An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the Vin pins together and feeding the external bias voltage (8-15V) to the two pins.

Line Under Voltage Detector

The LM5020 contains a line Under Voltage Lock Out (UVLO) circuit. An external set-point voltage divider from Vin to GND sets the operational range of the converter. The resistor divider must be designed such that the voltage at the UVLO pin is greater than 1.25V when Vin is in the desired operating range. If the under voltage threshold is not met, all functions of the controller are disabled and the controller remains in a low power standby state.

UVLO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. If an external transistor pulls the UVLO pin below the 1.25V threshold, the converter is disabled.

Error Amplifier

An internal high gain error amplifier is provided within the LM5020. The amplifier's non-inverting input is internally set to a fixed reference voltage of 1.25V. The inverting input is connected to the FB pin. In non-isolated applications, the power converter output is connected to the FB pin via voltage scaling resistors. Loop compensation components are connected between the COMP and FB pins. For most isolated applications the error amplifier function is implemented on the secondary side of the converter and the internal error amplifier is not used. The internal error amplifier is configured as an open drain output and can be disabled by connecting the FB pin to ground. An internal 5K pull-up resistor between a 5V reference and COMP can be used as the pull-up for an optocoupler in isolated applications.

Current Limit/Current Sense

The LM5020 provides a cycle-by-cycle over current protection function. Current limit is accomplished by an internal current sense comparator. If the voltage at the current sense comparator input exceeds 0.5V, the output is immediately terminated. A small RC filter, located near the controller, is recommended to filter noise from the current sense signal. The CS input has an internal MOSFET which discharges the CS pin capacitance at the conclusion of every cycle. The discharge device remains on an additional 50ns after the beginning of the new cycle to attenuate the leading edge spike on the current sense signal.

The LM5020 current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be located very close to the LM5020 and connected directly to the pins of the controller (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor and the current sense filter network. A sense resistor located in the source of the primary power MOSFET may be used for current sensing, but a low inductance resistor is required. When designing with a current sense resistor all of the noise sensitive low power ground connections should be connected together local to the controller and a single connection should be made to the high current power ground (sense resistor ground point).

Oscillator and Sync Capability

A single external resistor connected between the RT and GND pins sets the LM5020 oscillator frequency. Internal to the LM5020-2 device (50% duty cycle limited option) is an oscillator divide by two circuit. This divide by two circuit creates an exact 50% duty cycle pulse which is used internally to create a precise 50% duty cycle limit function. Because of this, the internal oscillator actually operates at twice the frequency of the output (OUT). For the LM5020-1 device the oscillator frequency and the operational output frequency are the same. To set a desired output operational frequency (F), the RT resistor can be calculated from:

LM5020-1:

$$RT = \frac{1}{F \times 158 \times 10^{-12}} \quad (1)$$

LM5020-2:

$$RT = \frac{1}{F \times 316 \times 10^{-12}} \quad (2)$$

The LM5020 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin through a 100pF capacitor. A peak voltage level greater than 3.7 Volts at the RT pin is required for detection of the sync pulse. The sync pulse width should be set between 15 to 150ns by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated at 2 Volts. The RT resistor should be located very close to the device and connected directly to the pins of the controller (RT and GND).

PWM Comparator / Slope Compensation

The PWM comparator compares the current ramp signal with the loop error voltage derived from the error amplifier output. The error amplifier output voltage at the COMP pin is offset by 1.4V and then further attenuated by a 3:1 resistor divider. The PWM comparator polarity is such that 0 Volts on the COMP pin will result in a zero duty cycle at the controller output. For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. The LM5020-1 integrates this slope compensation by summing a current ramp generated by the oscillator with the current sense signal. Additional slope compensation may be added by increasing the source impedance of the current sense signal. Since the LM5020-2 is not capable of duty cycles greater than 50%, there is no slope compensation feature in this device.

Soft Start

The softstart feature allows the power converter to gradually reach the initial steady state operating point, thereby reducing start-up stresses and current surges. At power on, after the V_{CC} and the line undervoltage lockout thresholds are satisfied, an internal 10µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and the duty cycle of the output pulses.

Gate Driver and Maximum Duty Cycle Limit

The LM5020 provides an internal gate driver (OUT), which can source and sink a peak current of 1 Amp. The LM5020 is available in two duty cycle limit options. The maximum output duty cycle is typically 80% for the LM5020-1 option and precisely equal to 50% for the LM5020-2 option. The maximum duty cycle function for the LM5020-2 is accomplished with an internal toggle flip-flop which ensures an accurate duty cycle limit. The internal oscillator frequency of the LM5020-2 is therefore twice the operating frequency of the PWM controller (OUT pin).

The 80% maximum duty cycle limit of the LM5020-1 is determined by the internal oscillator and varies more than the 50% limit of the LM5020-2. For the LM5020-1 the internal oscillator frequency and the operational frequency of the PWM controller are equal.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. This feature prevents catastrophic failures from accidental device overheating. When activated, typically at 165 degrees Celsius, the controller is forced into a low power standby state, disabling the output driver and the bias regulator. After the temperature is reduced (typical hysteresis = 25°C) the V_{CC} regulator is enabled and a softstart sequence initiated.

Typical Application Circuit: 36V - 75 V_{IN} and 3.3V, 4.5A OUT

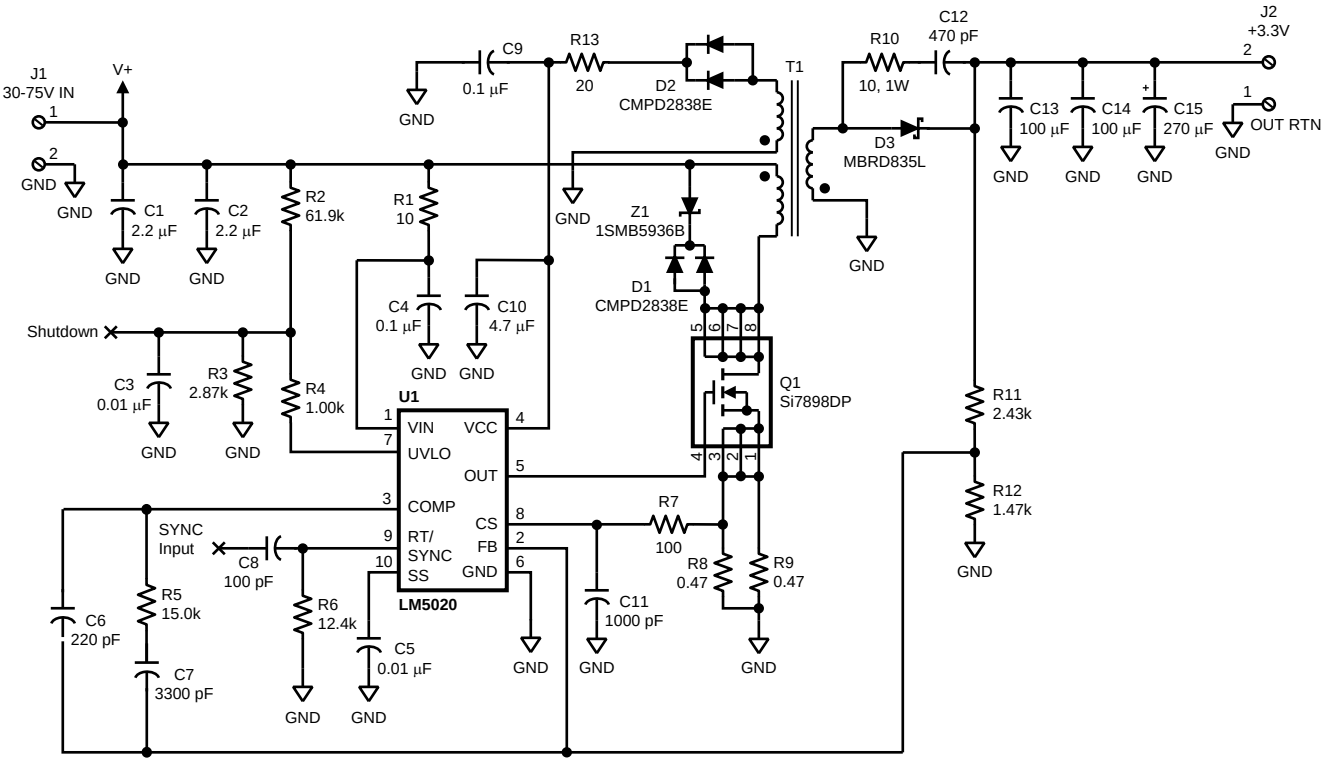


Table 1. Bill Of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2µF, 100V
C	2	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2µF, 100V
C	3	C2012X7R1H103K	CAPACITOR, CER, TDK	0.01µF, 50V
C	4	C3216X7R2A104K	CAPACITOR, CER, TDK	0.1µF, 100V
C	5	C2012X7R1H103K	CAPACITOR, CER, TDK	0.01µF, 50V
C	6	C2012C0G1H221J	CAPACITOR, CER, KEMET	220pF, 50V
C	7	C2012C0G1H332J	CAPACITOR, CER, TDK	3300pF, 50V
C	8	C2012C0G1H101J	CAPACITOR, CER, TDK	100pF, 50V
C	9	C2012X7R1H104K	CAPACITOR, CER, TDK	0.1µF, 50V
C	10	C3216X7R1C475K	CAPACITOR, CER, TDK	4.7µF, 16V
C	11	C2012C0G1H102J	CAPACITOR, CER, TDK	1000pF, 50V
C	12	C2012C0G1H471J	CAPACITOR, CER, TDK	470p, 50V
C	13	C4532X7S0G107M	CAPACITOR, CER, TDK	100µF, 4V
C	14	C4532X7S0G107M	CAPACITOR, CER, TDK	100µF, 4V
C	15	A700X277M0004AT	CAPACITOR, ALUM ORGANIC, KEMET	270µF, 4V
D	1	CMPD2838E-NSA	DIODE, SIGNAL, CENTRAL	
D	2	CMPD2838E-NSA	DIODE, SIGNAL, CENTRAL	
D	3	MBRD835L	DIODE, RECTIFIER, ON SEMICONDUCTOR	
J	1	MKDS 1/2-3.81	TERM BLK, MINI, 2 POS, PHOENIX CONTACT	
J	2	MKDS 1/2-3.81	TERM BLK, MINI, 2 POS, PHOENIX CONTACT	
Q	1	SI7898DP	FET, SILICONIX	150V, 85mΩ
R	1	CRCW120610R0F	RESISTOR	10
R	2	CRCW12066192F	RESISTOR	61.9kΩ
R	3	CRCW08052871F	RESISTOR	2.87kΩ
R	4	CRCW08051001F	RESISTOR	1.00kΩ
R	5	CRCW08051502F	RESISTOR	15.0kΩ
R	6	CRCW08051242F	RESISTOR	12.4kΩ
R	7	CRCW08051000F	RESISTOR	100
R	8	CRCW12060R47F	RESISTOR	0.47
R	9	CRCW12060R47F	RESISTOR	0.47
R	10	CRCW251210R0F	RESISTOR	10, 1W
R	11	CRCW08052431F	RESISTOR	2.43K
R	12	CRCW08051471F	RESISTOR	1.47K
R	13	CRCW080520R0F	RESISTOR	20
T	1	B0695-A COILCRAFT	TRANSFORMER, FLYBACK, EFD20 CORE	
T	1	PA0751 PULSE	TRANSFORMER, FLYBACK, EFD20 CORE	ALTERNATE
U	1	LM5020-2MM	CONTROLLER, SINGLE OUT, PWM, NATIONAL	
Z	1	1SMB5936B	DIODE, ZENER, SMB, 30V	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5020MM-1	NRND	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 125	SBLB	
LM5020MM-1/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SBLB	Samples
LM5020MM-2/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SBNB	Samples
LM5020MMX-1/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SBLB	Samples
LM5020MMX-2/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SBNB	Samples
LM5020SD-1/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5020-1	Samples
LM5020SD-2/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5020-2	Samples
LM5020SDX-1/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5020-1	Samples
LM5020SDX-2/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5020-2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

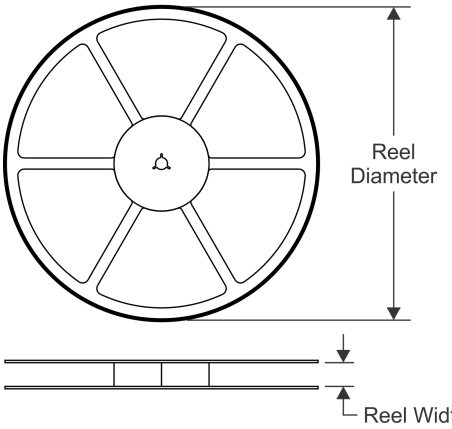
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

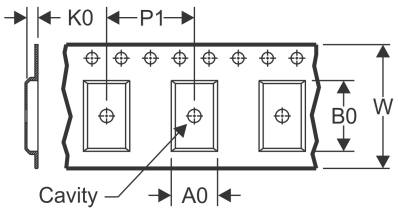
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

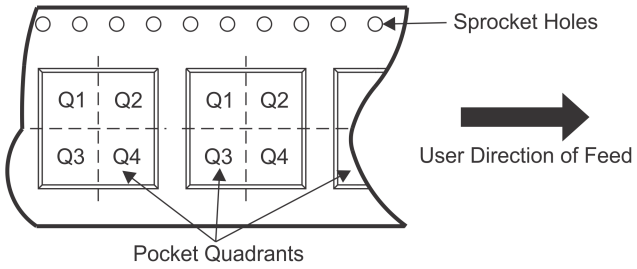


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

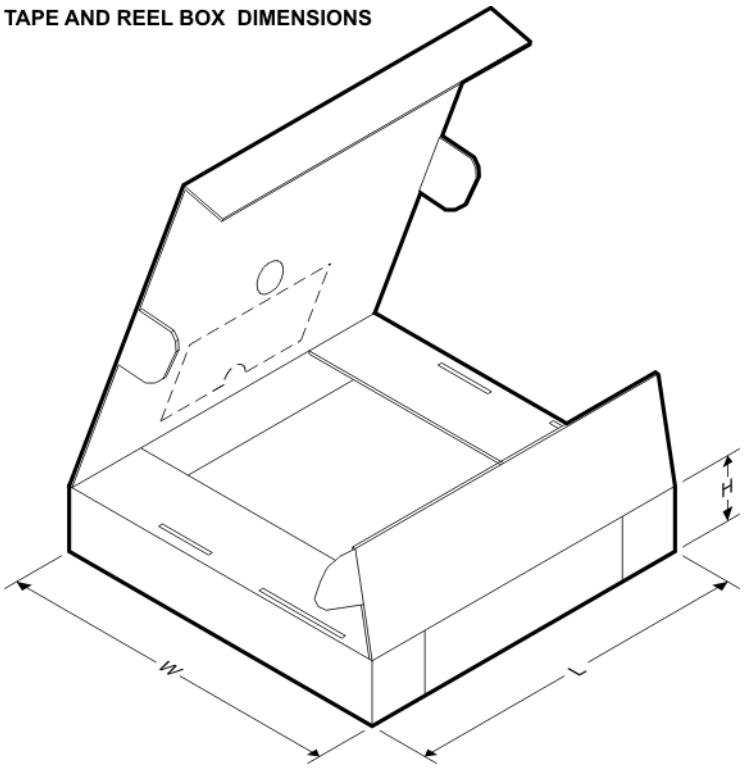
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5020MM-1	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5020MM-1/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5020MM-2/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5020MMX-1/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5020MMX-2/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5020SD-1/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5020SD-2/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5020SDX-1/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5020SDX-2/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

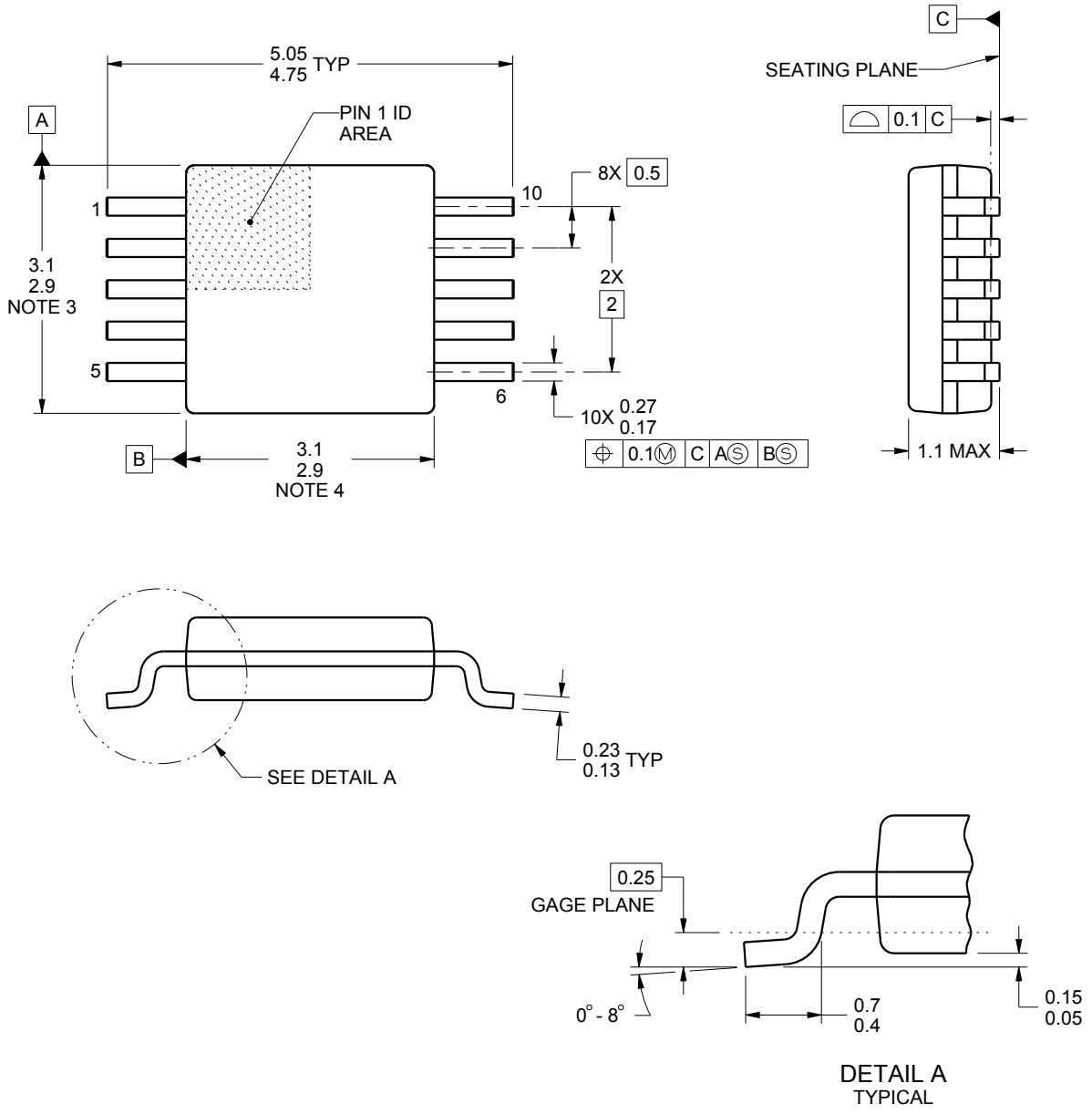
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5020MM-1	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5020MM-1/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5020MM-2/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5020MMX-1/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5020MMX-2/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5020SD-1/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5020SD-2/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5020SDX-1/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5020SDX-2/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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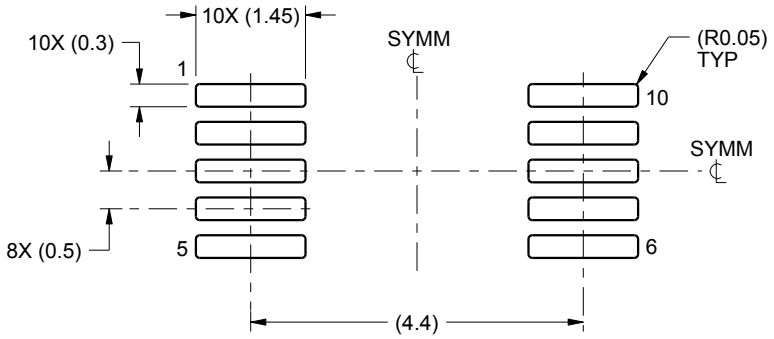
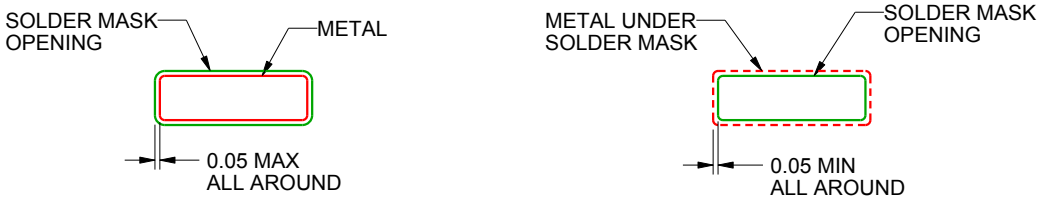
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

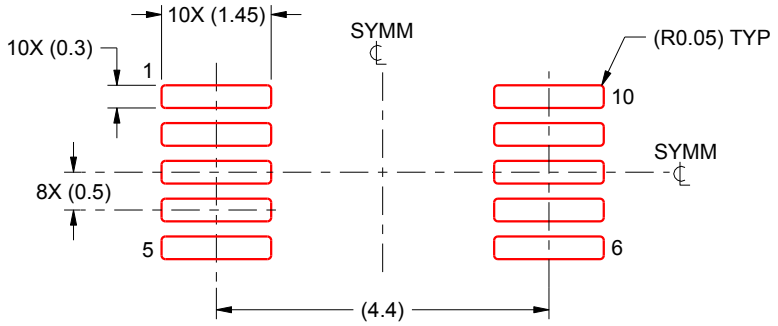


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



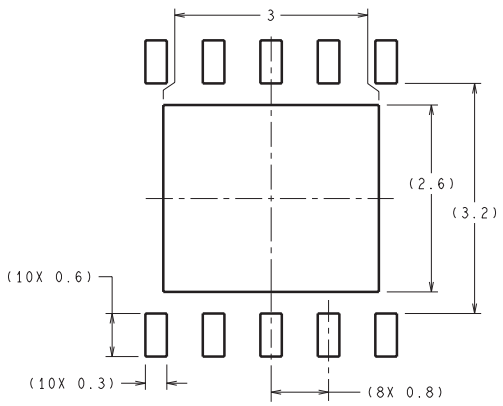
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

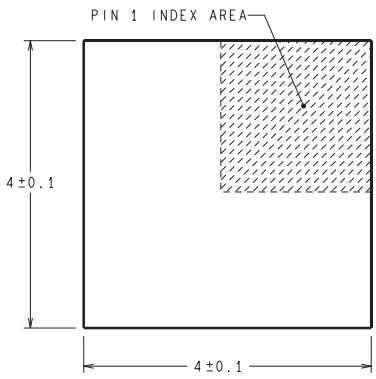
NOTES: (continued)

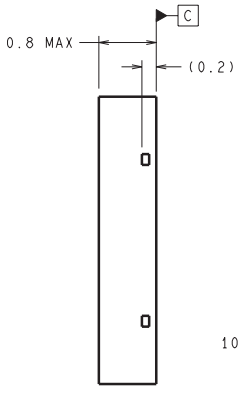
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

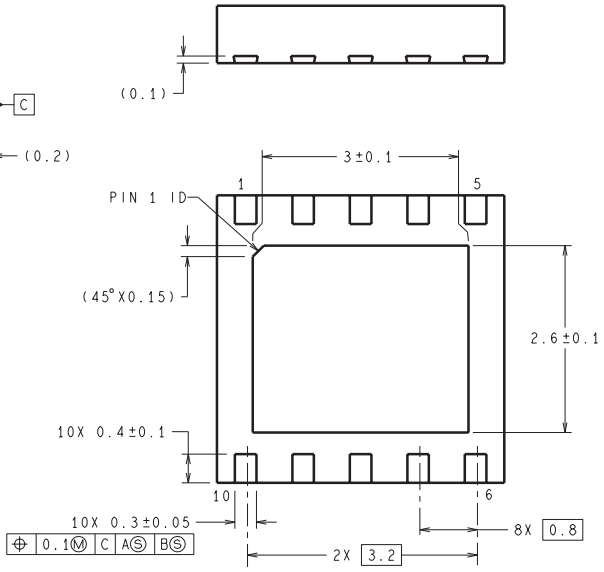
DPR0010A



RECOMMENDED LAND PATTERN







DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)

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