INA12x Precision, Low-Power Instrumentation Amplifiers

1 Features

- Low offset voltage: 50 µV, maximum
- Low drift: 0.5 µV/°C, maximum
- Low input bias current: 5 nA, maximum
- Low noise: 8 nV/√Hz, 0.2 µVpp
- High CMR: 120 dB, minimum
- Bandwidth: 1.3 MHz (G = 1)
- Inputs protected to ±40 V
- Wide supply range: ±2.25 V to ±18 V
- Low quiescent current: 700 µA
- Packages: 8-pin plastic DIP, SO-8

2 Applications

- Pressure transmitter
- Temperature transmitter
- Weigh scale
- Electrocardiogram (ECG)
- Analog input module
- Data acquisition (DAQ)

3 Description

The INA128 and INA129 (INA12x) are low-power, general-purpose instrumentation amplifiers that offer excellent accuracy. The versatile three op amp design and small size make these amplifiers an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation with a 50-kΩ resistor. The INA129 gain equation uses a 49.4-kΩ resistor to allow for drop-in replacements of comparable devices.

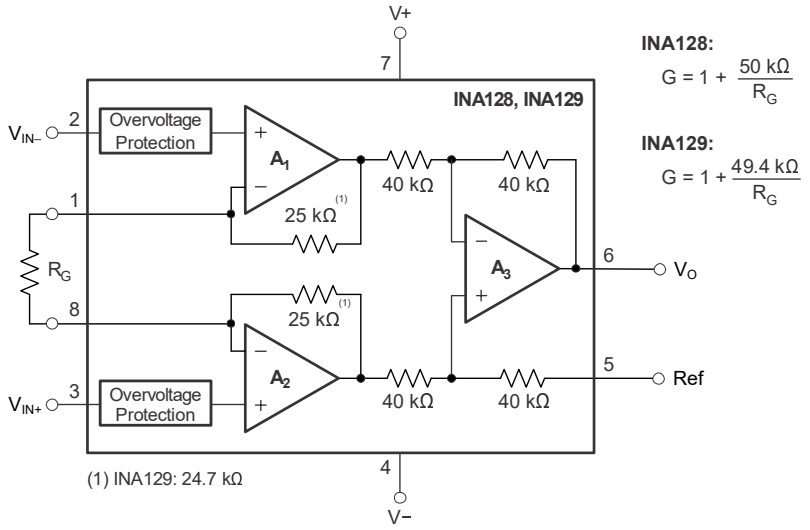
The INA12x are available in plastic DIP and surface-mount packages, specified for the –40°C to +85°C temperature range. The INA128 is also available in a dual configuration, the INA2128.

The upgraded INA828 offers a lower input bias current (0.6 nA, max) and lower noise (7 nV/√Hz) at the same quiescent current. See the *Device Comparison Table* for a selection of precision instrumentation amplifiers from Texas Instruments.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA128, INA129	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2019) to Revision F (May 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added bandwidth and noise specifications in *Features*	1
• Changed *Applications* to link to latest end-equipment solutions on ti.com	1
• Changed reference from INA819 to INA818 in *Device Comparison Table*	4
• Added single supply specification to *Absolute Maximum Ratings*	5
• Added note clarifying output short-circuit "to ground" in *Absolute Maximum Ratings* refers to short-circuit to V_S / 2	5
• Added single supply specification to *Recommended Operating Conditions*	5
• Changed input common-mode voltage range specification from V – 2 to (V–) + 2 in *Recommended Operating Conditions*	5
• Deleted INA128-HT and INA129-HT operating temperature specifications from *Recommended Operating Conditions*	5
• Added specified temperature range to *Recommended Operating Conditions*	5
• Added V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 to "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity	6
• Changed test condition for offset voltage drift specification in *Electrical Characteristics* from "T_A = T_{MIN} to T_{MAX}" to "T_A = –40°C to +85°C" for clarity	6
• Changed typical long-term stability specification from ±0.1±3/G µV/mo to ±0.2±3/G µV/mo in *Electrical Characteristics*	6
• Changed common-mode voltage specification from (V–) + 2 V minimum and (V+) – 2 V minimum across two rows to (V–) + 2 V minimum and (V+) – 2 V maximum across one row in *Electrical Characteristics*	6
• Deleted typical common-mode voltage specifications in *Electrical Characteristics*	6
• Added test condition of "R_S = 0 Ω" to safe input voltage specification in *Electrical Characteristics* for clarity	6
• Added test condition of "T_A = –40°C to +85°C" to input bias current drift specification in *Electrical Characteristics* for clarity	6
• Added test condition of "T_A = –40°C to +85°C" to input offset current drift specification in *Electrical Characteristics* for clarity	6
• Changed maximum gain error specification for INA128PA/UA and INA129PA/UA with G = 1 from ±0.01% to ±0.1% in *Electrical Characteristics*	6

- Added test condition of "T_A = –40°C to +85°C" for gain drift in *Electrical Characteristics* for clarity....6
- Changed parameter names from "Voltage - Positive" to "Positive output voltage swing" and from "Voltage - Negative" to "Negative output voltage swing" in *Electrical Characteristics* 6
- Deleted typical positive and negative output voltage swing specifications in *Electrical Characteristics* 6
- Added test condition of "Continuous to V_S / 2" to short-circuit current specification in *Electrical Characteristics* for clarity....6
- Changed typical bandwidth specification for G = 10 from 700 kHz to 640 kHz in *Electrical Characteristics* 6
- Changed typical slew rate specification from 4 V/µs to 1.2 V/µs in *Electrical Characteristics* 6
- Changed typical settling time specification for G = 1, G = 10, and G = 100 from 7 µs, 7 µs, and 9 µs respectively to 12 µs, 12 µs, and 12 µs, in *Electrical Characteristics* 6
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 6
- Changed Figures 7-1, 7-3, 7-4, 7-9, 7-10, 7-11, 7-16, 7-17, 7-20, 7-21....8
- Changed values discussed in *Input Common-Mode Range* from typical input common-mode voltage range values to maximum and minimum values....14
- Changed Figure 9-1 to fix missing text and include reference voltage....15
- Added more detailed guidance concerning REF pin in *Design Requirements* 15
- Changed Figures 9-6, 9-7....18
- Changed Figures 9-10 and 9-11 to fix missing text....19
- Added *Related Documentation* links to *Device and Documentation Support* 22

Changes from Revision D (January 2018) to Revision E (April 2019) **Page**

- Added information about the newer, upgraded INA828....1
- Added *Device Comparison Table* 4

Changes from Revision C (October 2015) to Revision D (January 2018) **Page**

- Added top navigator icon for TI Reference Design 1
- Changed "±0.5±0/G" to "±0.5±20/G" in MAX column of Offset voltage RTI vs temperature row of *Electrical Characteristics*....6

Changes from Revision B (February 2005) to Revision C (April 2015) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.... 1

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35-µV offset, 0.4-µV/°C V_{OS} drift, 8-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA821	35-µV offset, 0.4-µV/°C V_{OS} drift, 7-nV/√Hz noise, high-bandwidth, precision instrumentation amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-µV offset, 0.5-µV/°C V_{OS} drift, 7-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1-µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion	G = 0.2 V/V	N/A
PGA112	Precision programmable gain op amp with SPI	Digital programmable	N/A

6 Pin Configuration and Functions

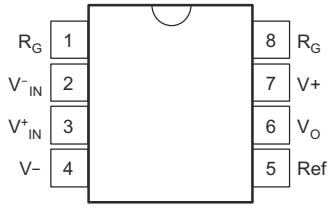


Figure 6-1. D (8-Pin SOIC) and P (8-Pin PDIP) Packages, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
REF	5	Input	Reference input. This pin must be driven by low impedance or connected to ground.
R_G	1,8	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
V–	4	Power	Negative supply
V+	7	Power	Positive supply
$V_{IN–}$	2	Input	Negative input
V_{IN+}	3	Input	Positive input
V_O	6	Output	Output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0 V		36	
	Analog input voltage			±40	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–40	125	°C
	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C
T_{stg}	Storage temperature		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±50	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
	Input common-mode voltage range for V_O = 0 V		(V–) + 2		(V+) – 2	V
T_A	Specified temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA12x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	11.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage (RTI)	1 ≤ G ≤ 10000	INA12xP, INA12xU			±10 ±100 / G	±50 ±500 / G	µV
			INA12xPA, INA12xUA			±25 ±100 / G	±125 ±1000 / G	
	Offset voltage drift (RTI)	T_A = –40°C to +85°C	INA12xP, INA12xU			±0.2 ±2 / G	±0.5 ±20 / G	µV/°C
			INA12xPA, INA12xUA			±0.2 ±5 / G	±1 ±20 / G	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±2.25 V to ±18 V	INA12xP, INA12xU			±0.2 ±20 / G	±1 ±100 / G	µV/V
			INA12xPA, INA12xUA				±2 ±200 / G	
	Long-term stability					±0.2 ±3 / G		µV/mo
	Input impedance	Differential				10 || 2		GΩ || pF
		Common-mode				100 || 9		
V_{CM}	Common-mode voltage(2)	V_O = 0 V			(V–) + 2		(V+) – 2	V
	Safe input voltage	R_S = 0 Ω					±40	V
CMRR	Common-mode rejection ratio	ΔR$_S$ = 1 kΩ, V_{CM} = ±13 V	G = 1	INA12xP, INA12xU	80	86		dB
				INA12xPA, INA12xUA	73			
			G = 10	INA12xP, INA12xU	100	106		
				INA12xPA, INA12xUA	93			
			G = 100	INA12xP, INA12xU	120	125		
				INA12xPA, INA12xUA	110			
			G = 1000	INA12xP, INA12xU	120	130		
				INA12xPA, INA12xUA	110			
INPUT BIAS CURRENT								
I_B	Input bias current	INA12xP, INA12xU				±2	±5	nA
		INA12xPA, INA12xUA					±10	
	Input bias current drift	T_A = –40°C to +85°C				±30		pA/°C
I_{OS}	Input offset current	INA12xP, INA12xU				±1	±5	nA
		INA12xPA, INA12xUA					±10	nA
	Input offset current drift	T_A = –40°C to +85°C				±30		pA/°C
NOISE								
e_N	Voltage noise (RTI)	G = 1000, R_S = 0 Ω	f = 10 Hz			10		nV/√Hz
			f = 100 Hz			8		
			f = 1 kHz			8		
			f_B = 0.1 Hz to 10 Hz			0.2		$µV_{PP}$
I_n	Current noise	f = 10 Hz				0.9		pA/√Hz
		f = 1 kHz				0.3		
		f_B = 0.1 Hz to 10 Hz				30		pA_{PP}

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
	Gain equation	INA128			1 + (50 kΩ / R_G)		V/V
		INA129			1 + (49.4 kΩ / R_G)		
G	Gain			1		10000	V/V
GE	Gain error	G = 1	INA12xP, INA12xU		±0.01	±0.024	%
			INA12xPA, INA12xUA			±0.1	
		G = 10	INA12xP, INA12xU		±0.02	±0.4	
			INA12xPA, INA12xUA			±0.5	
		G = 100	INA12xP, INA12xU		±0.05	±0.5	
			INA12xPA, INA12xUA			±0.7	
		G = 1000	INA12xP, INA12xU		±0.5	±1	
			INA12xPA, INA12xUA			±2	
	Gain drift[4]	T_A = –40°C to +85°C			±1	±10	ppm/°C
			50-kΩ or 49.4-kΩ resistance[3]		±25	±100	
	Gain nonlinearity[1]	G = 1, V_O = ±13.6 V	INA12xP, INA12xU		±0.0001	±0.001	% of FSR
			INA12xPA, INA12xUA			±0.002	
		G = 10	INA12xP, INA12xU		±0.0003	±0.002	
			INA12xPA, INA12xUA			±0.004	
		G = 100	INA12xP, INA12xU		±0.0005	±0.002	
			INA12xPA, INA12xUA			±0.004	
		G = 1000			±0.001		
OUTPUT							
	Positive output voltage swing			(V+) – 1.4			V
	Negative output voltage swing			(V–) + 1.4			V
C_L	Load capacitance	Stable operation			1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2			+6/–15		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 1			1.3		MHz
		G = 10			640		kHz
		G = 100			200		
		G = 1000			20		
SR	Slew rate	G = 5, V_O = ±10 V			1.2		V/µs
t_S	Settling time	To 0.01%	G = 1		12		µs
			G = 10		12		
			G = 100		12		
			G = 1000		80		
	Overload recovery	50% input overload			4		µs
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V			±700	±750	µA

(1) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%
(2) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(3) Temperature coefficient of the 50-kΩ or 49.4-kΩ term in the gain equation.
(4) Specified by wafer test.

7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

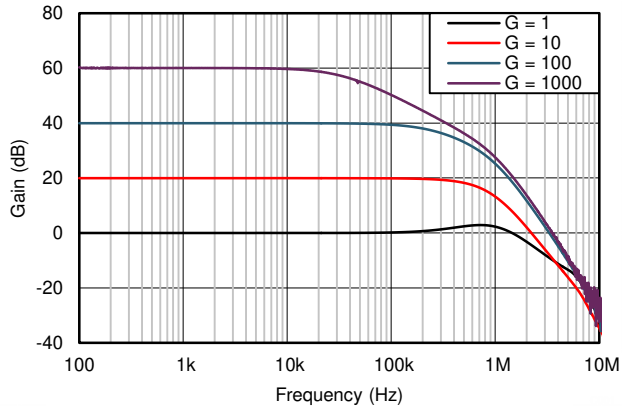


Figure 7-1. Gain vs Frequency

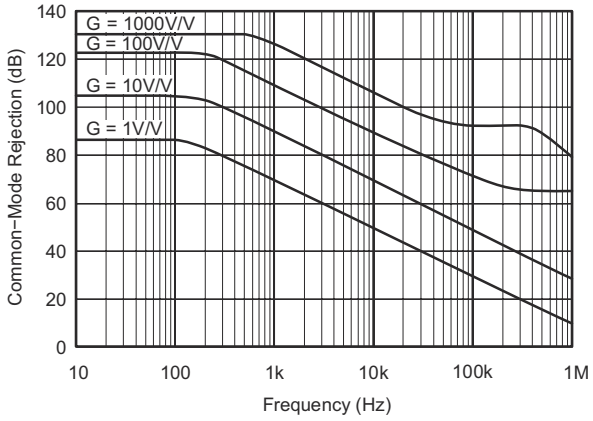


Figure 7-2. Common-Mode Rejection vs Frequency

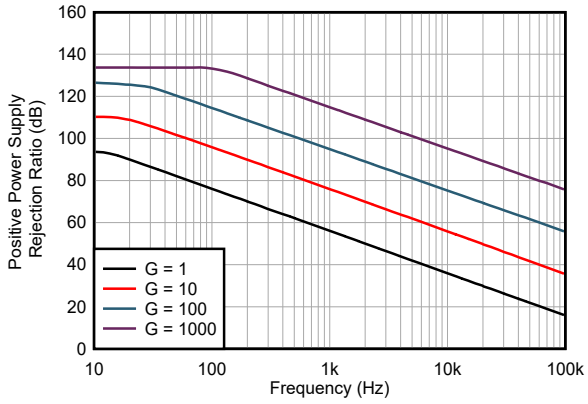


Figure 7-3. Positive Power Supply Rejection vs Frequency

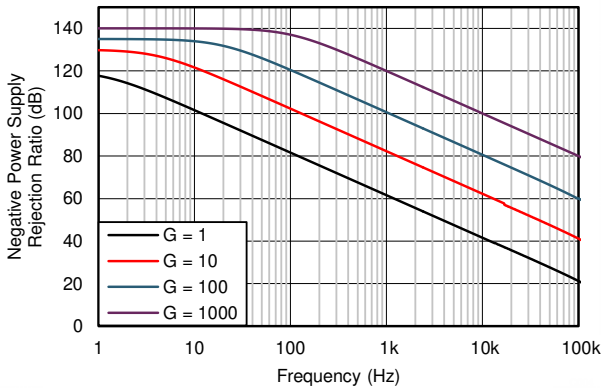
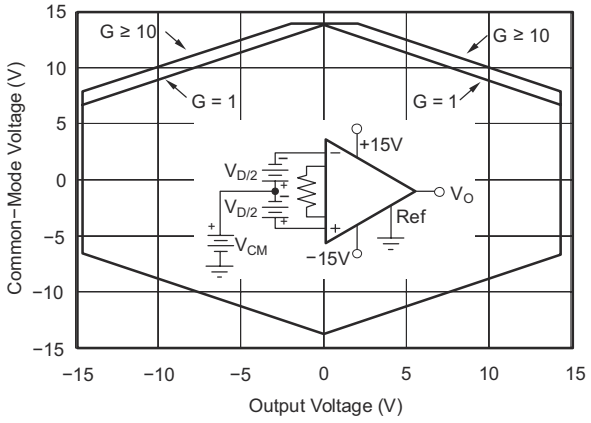
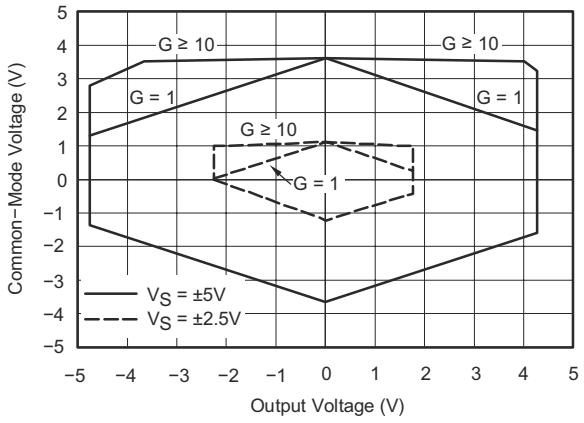


Figure 7-4. Negative Power Supply Rejection vs Frequency



V_S = ±15 V

Figure 7-5. Input Common-Mode Range vs Output Voltage



V_S = ±5 V, ±2.5 V

Figure 7-6. Input Common-Mode Range vs Output Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

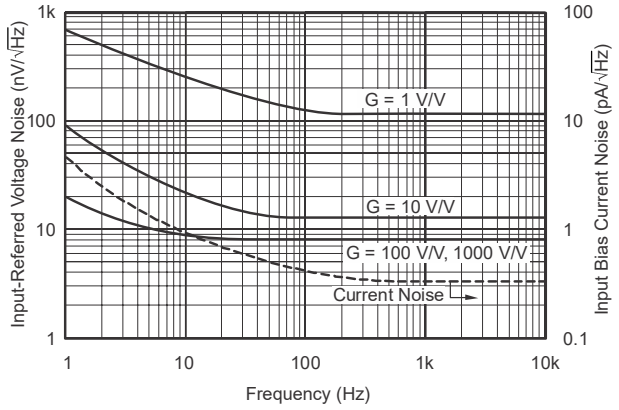


Figure 7-7. Input-Referred Noise vs Frequency

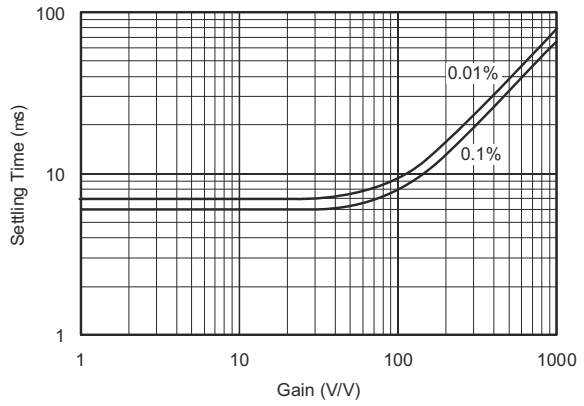


Figure 7-8. Settling Time vs Gain

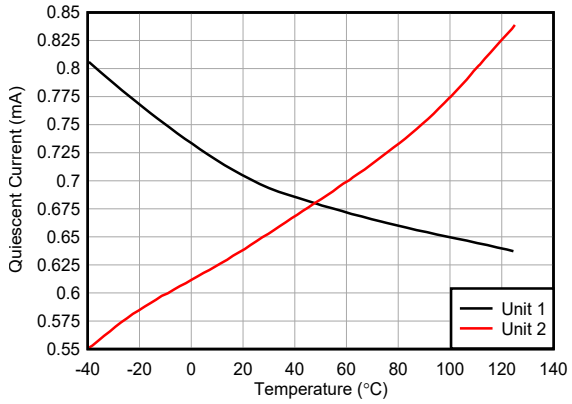


Figure 7-9. Quiescent Current vs Temperature

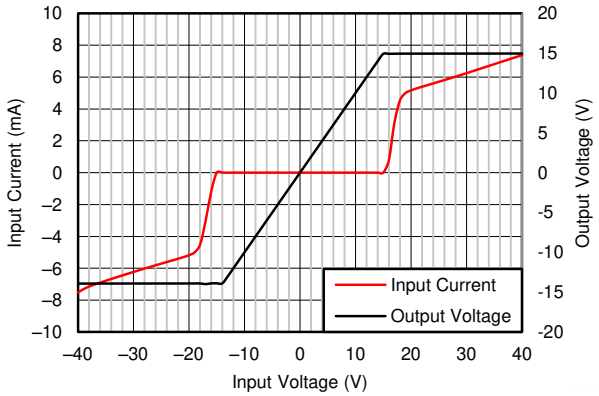


Figure 7-10. Input Overvoltage V/I Characteristics

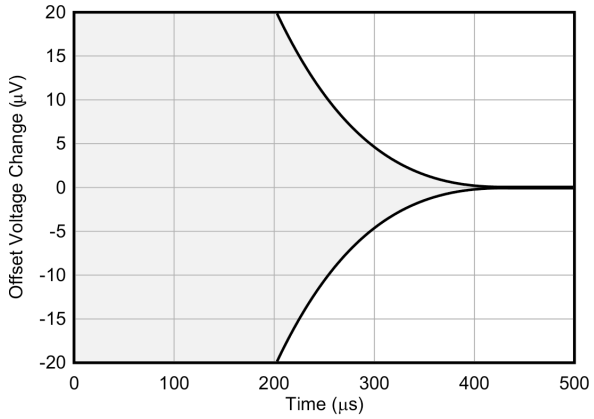


Figure 7-11. Input Offset Voltage Warm-Up

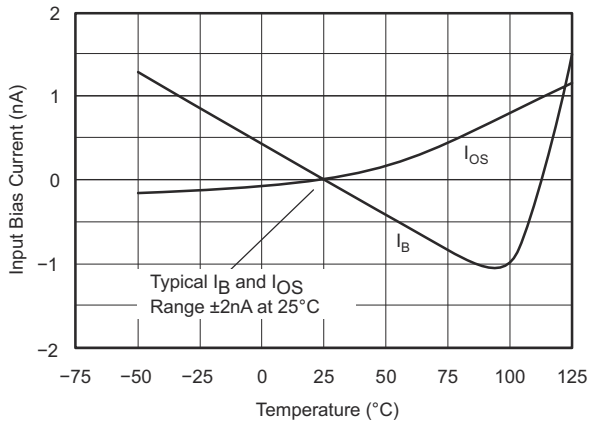


Figure 7-12. Input Bias Current vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

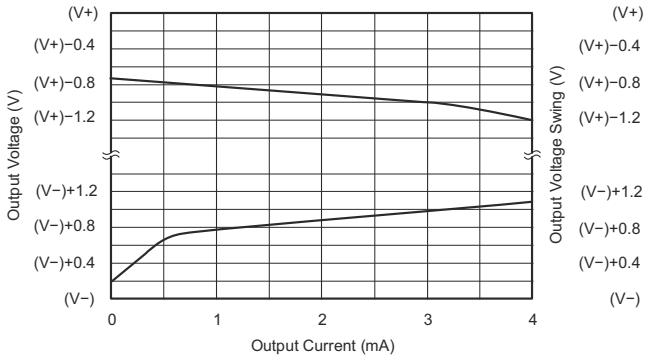


Figure 7-13. Output Voltage Swing vs Output Current

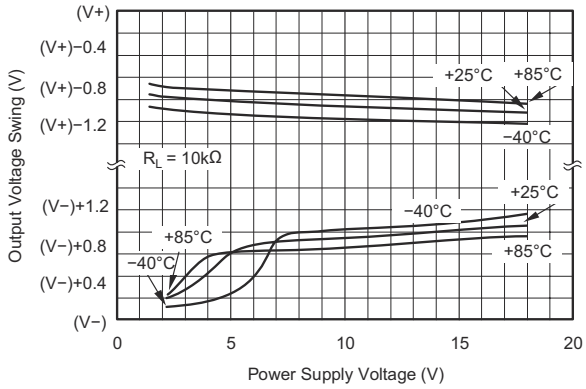


Figure 7-14. Output Voltage Swing vs Power Supply Voltage

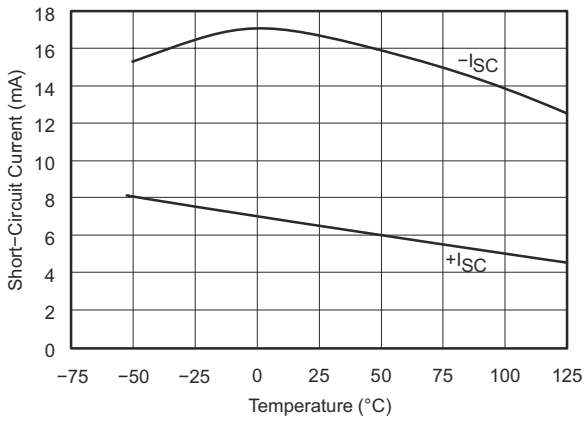


Figure 7-15. Short Circuit Output Current vs Temperature

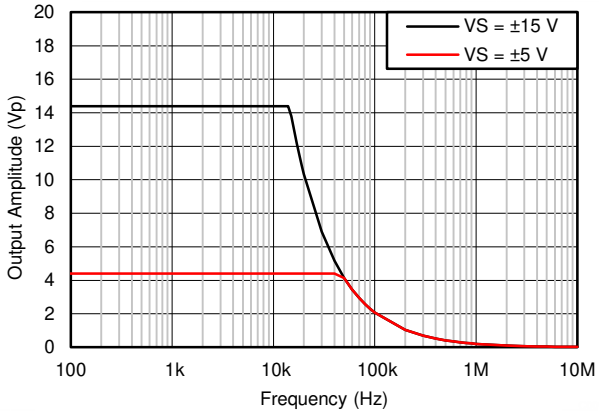


Figure 7-16. Maximum Output Voltage vs Frequency

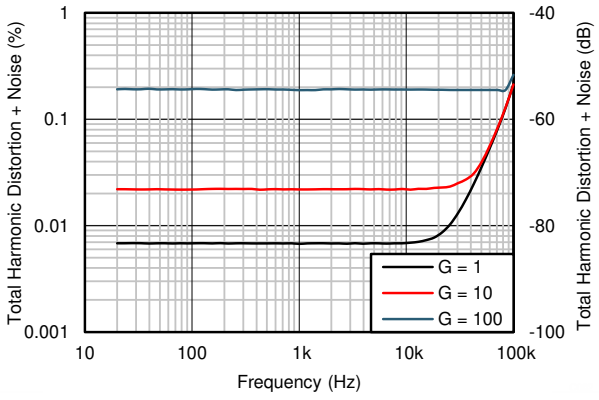


Figure 7-17. Total Harmonic Distortion + Noise vs Frequency

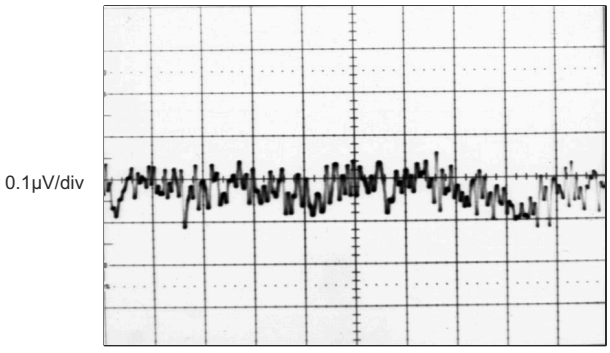
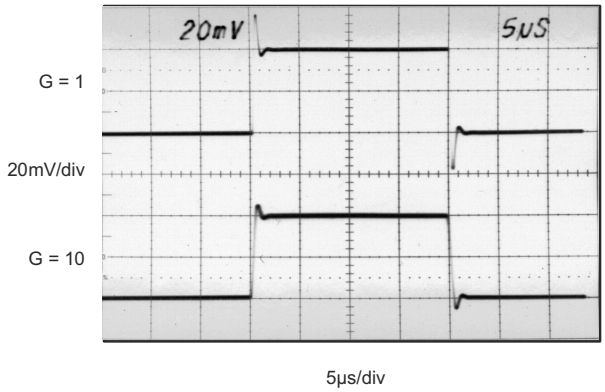


Figure 7-18. 0.1 to 10-Hz Input-Referred Voltage Noise

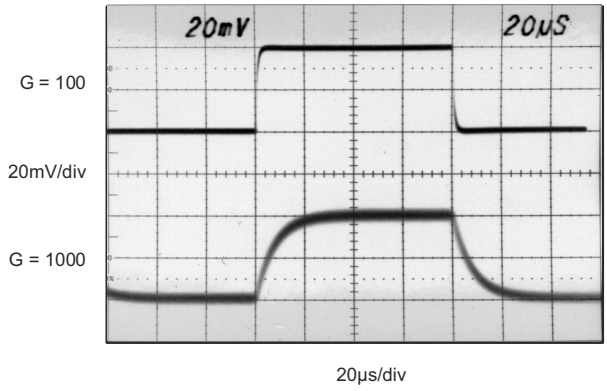
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)



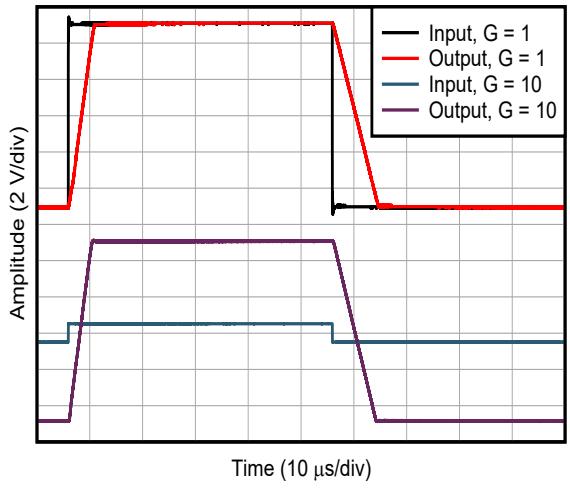
G = 1, 10

Figure 7-19. Small Signal



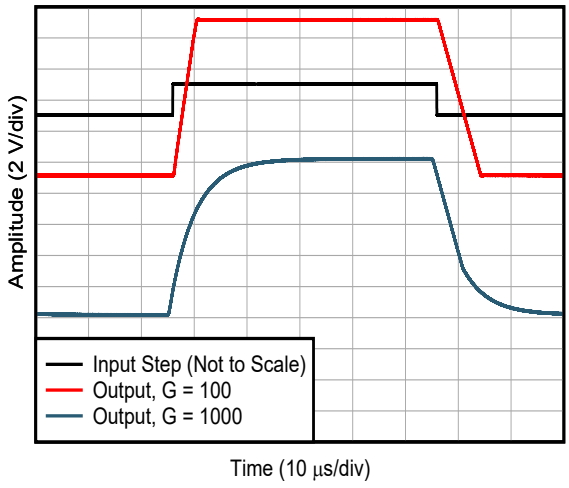
G = 100, 1000

Figure 7-20. Small Signal



G = 1, 10

Figure 7-21. Large Signal



G = 100, 1000

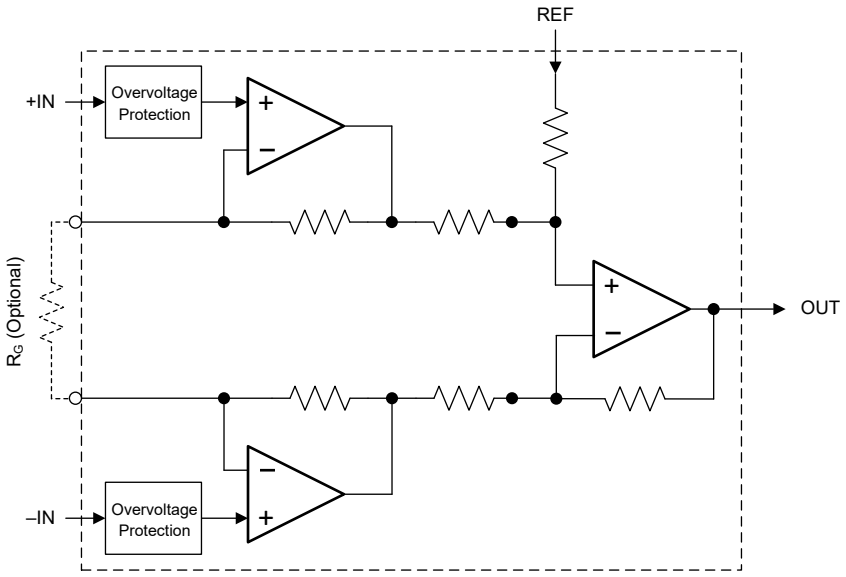
Figure 7-22. Large Signal

8 Detailed Description

8.1 Overview

The INA128 and INA129 (INA12x) instrumentation amplifiers are outfitted with an input protection circuit and input buffer amplifiers. These features eliminate the need for input impedance matching and make the amplifier an excellent choice for use in measurement and test equipment. Additional characteristics of the INA12x include a very-low dc offset, low drift, low noise, very-high open-loop gain, very-high common-mode rejection ratio, and very-high input impedances. The INA12x is used where great accuracy and stability of the circuit, both short and long term, are required.

8.2 Functional Block Diagram



8.3 Feature Description

The INA12x are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-op-amp design and small size make the amplifiers an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA12x are laser trimmed for very low offset voltage (25 µV typical) and high common-mode rejection (93 dB at G ≥ 100). These devices operate with power supplies as low as ±2.25 V, and a quiescent current of 2 mA, typically. The internal input protection can withstand up to ±40 V without damage, as shown in Figure 7-10.

8.3.1 Noise Performance

The INA12x provide very low noise in most applications. Low-frequency noise is approximately 0.2 μV_{PP} measured from 0.1 to 10 Hz (G ≥ 100). This feature provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

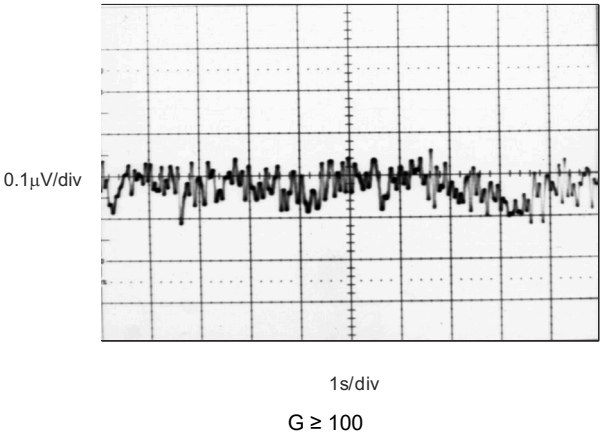


Figure 8-1. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

8.4 Device Functional Modes

The INA12x have a single functional mode and operate when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA12x is 36 V (±18 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA12x measure a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The high input-voltage protection circuit in conjunction with high input impedance make the INA12x an excellent choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

9.1.1 Input Common-Mode Range

The linear input voltage range of the INA12x input circuitry ranges from approximately 2 V less than the positive supply voltage to 2 V greater than the negative supply. A differential input voltage causes the output voltage to increase; however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on the supply voltage (see Figure 7-6).

Input overload can produce an output voltage that appears normal. For example, if an input-overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of A_3 is near 0 V even though both inputs are overloaded.

9.2 Typical Application

Figure 9-1 shows the basic connections required for operation of the INA12x. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 8 Ω in series with the REF pin causes a typical device to degrade to approximately 80 dB CMR (G = 1).

INA128: $G = 1 + \frac{50\ k\Omega}{R_G}$ **INA129:** $G = 1 + \frac{49.4\ k\Omega}{R_G}$

DESIRED GAIN (V/V)	INA128 R_G (Ω)	INA128 NEAREST 1% R_G (Ω)	INA129 R_G (Ω)	INA129 NEAREST 1% R_G (Ω)
1	NC	NC	NC	NC
2	50.00k	49.9k	49.4k	49.9k
5	12.50k	12.4k	12.35k	12.4k
10	5.556k	5.62k	5489	5.49k
20	2.632k	2.61k	2600	2.61k
50	1.02k	1.02k	1008	1k
100	505.1	511	499	499
200	251.3	249	248	249
500	100.2	100	99	100
1000	50.05	49.9	49.5	49.9
2000	25.01	24.9	24.7	24.9
5000	10.00	10	9.88	9.76
10000	5.001	4.99	4.94	4.87

NC: No Connection

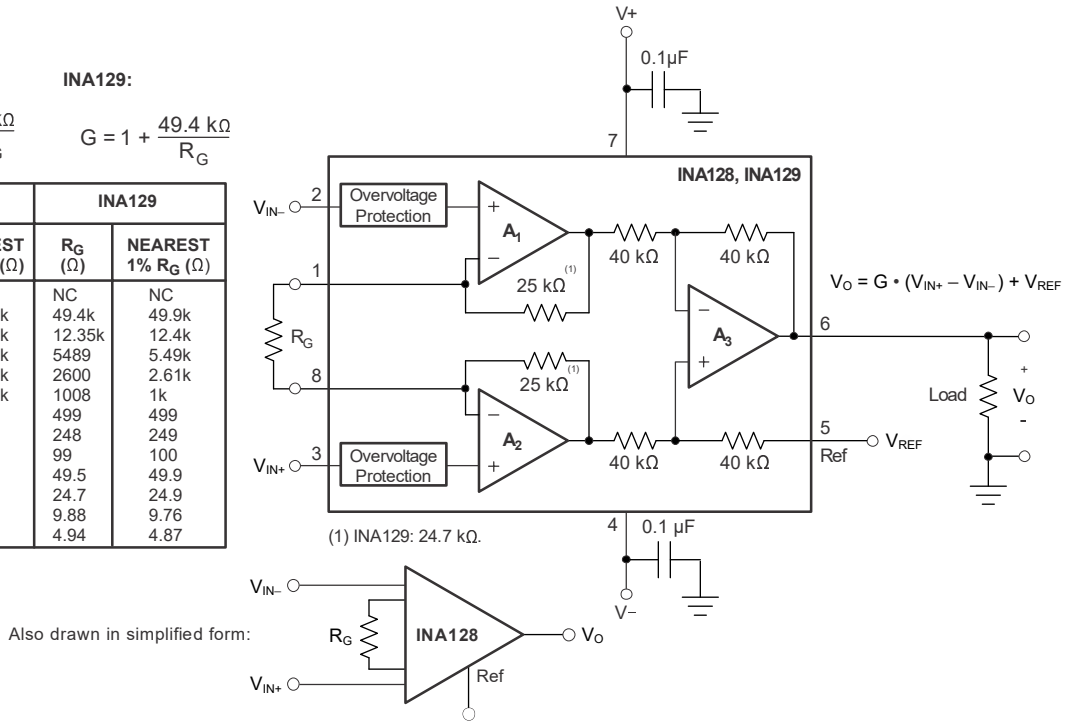


Figure 9-1. Basic Connections

9.2.1 Design Requirements

The devices are configured to monitor the input differential voltage when the input signal gain is set by the external resistor, R_G. The output signal is developed with respect to the voltage on the reference pin, REF. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground, as Figure 9-1 shows. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level shift the output so that the device can drive a single-supply ADC.

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider is used to generate a reference voltage, the voltage must be buffered by an op amp to avoid CMRR degradation.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

The gain (G) is set by connecting a single external resistor, R_G, between pins 1 and 8:

$$\text{INA128: } G = 1 + 50\ \text{k}\Omega / R_G \quad (1)$$

$$\text{INA129: } G = 1 + 49.4\ \text{k}\Omega / R_G \quad (2)$$

Commonly used gains and resistor values are shown in Figure 9-1.

The 50-kΩ term in Equation 1 and the 49.4-kΩ term in Equation 2 come from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate, absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications in the *Electrical Characteristics* table.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from Equation 1 and Equation 2. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

The typical performance curve in Figure 7-1 shows that despite low quiescent current, the INA12x achieve wide bandwidth even at high gain. This performance is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

9.2.2.3 Offset Trimming

The INA12x is laser trimmed for low-offset voltage and low offset voltage drift. Most applications require no external offset adjustment. Figure 9-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed with the output. The op-amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.

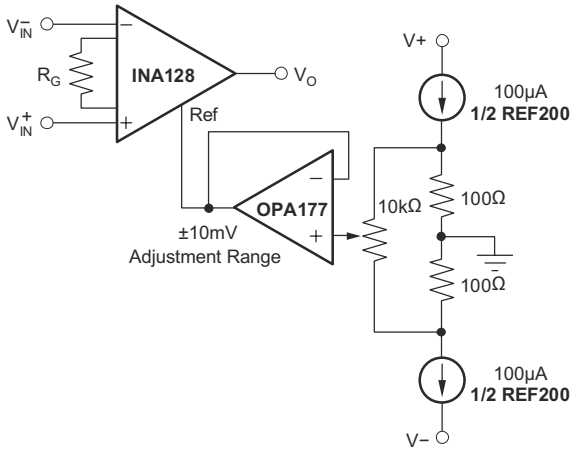


Figure 9-2. Optional Trimming of Output Offset Voltage

9.2.2.4 Input Bias Current Return Path

The input impedance of the INA12x is extremely high: approximately 10 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range, and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 9-3). With higher source impedance, use two equal resistors to provide a balanced input, with possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

For more details about why a valid input bias current return path is necessary, see the *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note.

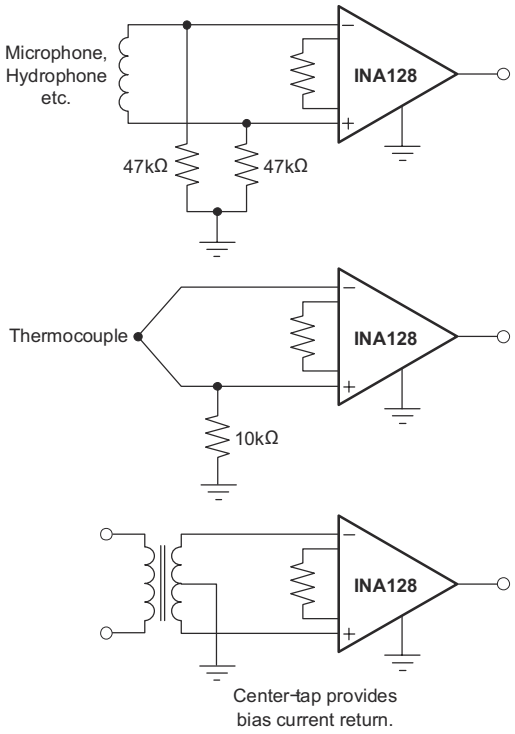
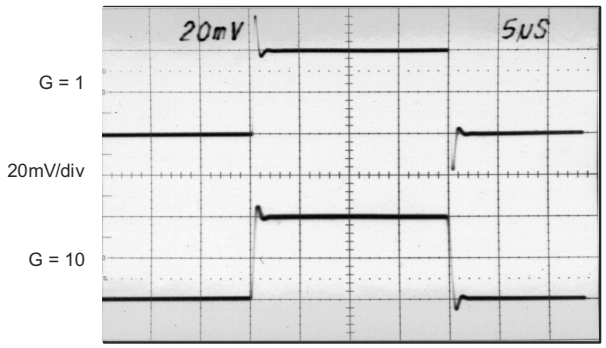


Figure 9-3. Providing an Input Common-Mode Current Path

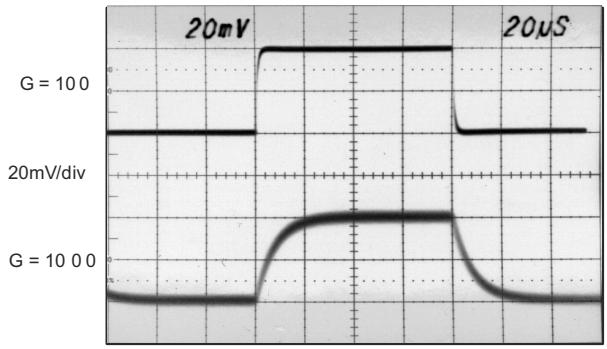
9.2.3 Application Curves



5µs/div

G = 1, 10

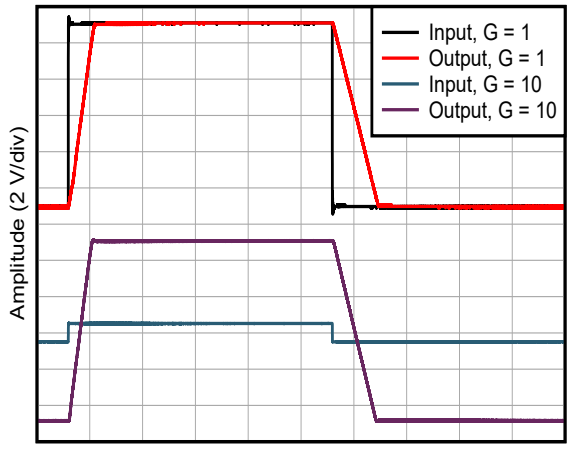
Figure 9-4. Small Signal



20µs/div

G = 100, 1000

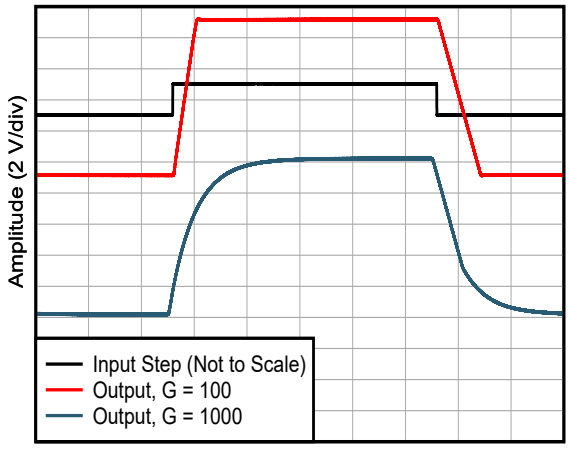
Figure 9-5. Small Signal



Time (10 µs/div)

G = 1, 10

Figure 9-6. Large Signal



Time (10 µs/div)

G = 100, 1000

Figure 9-7. Large Signal

9.3 System Examples

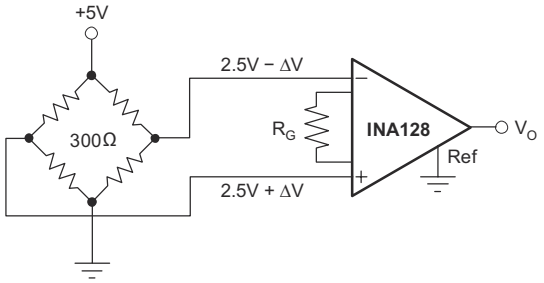


Figure 9-8. Bridge Amplifier

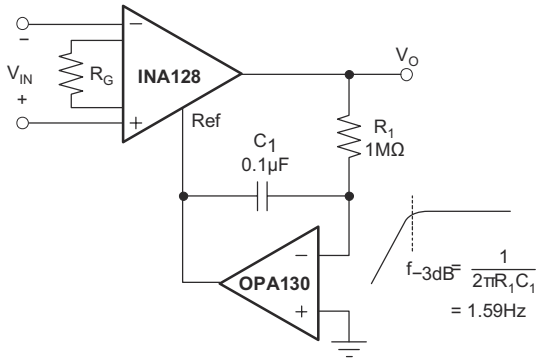
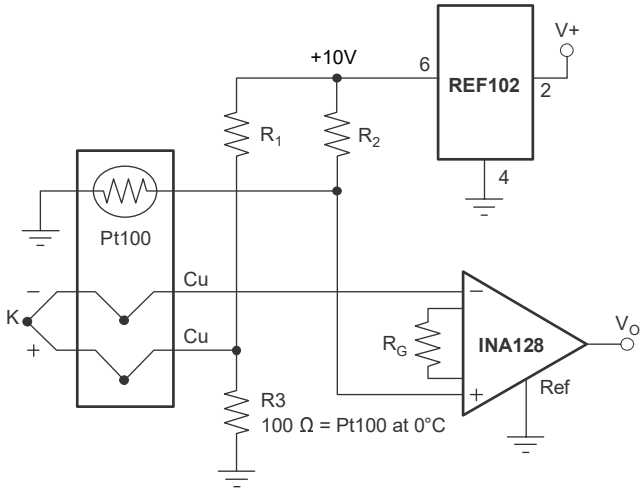
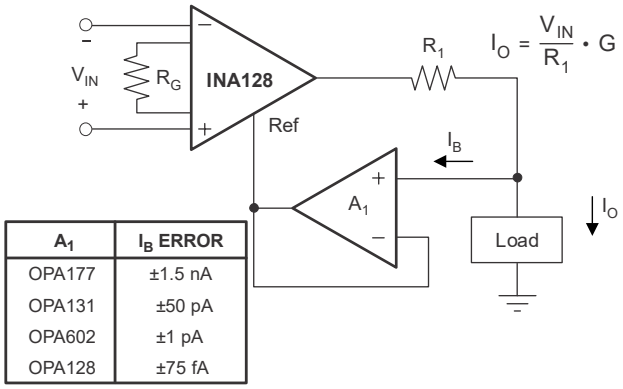


Figure 9-9. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFICIENT (µV/°C)	R1, R2
E	+ Chromel − Constantan	58.5	66.5 kΩ
J	+ Iron − Constantan	50.2	76.8 kΩ
K	+ Chromel − Alumel	39.4	97.6 kΩ
T	+ Copper − Constantan	38.0	102 kΩ

Figure 9-10. Thermocouple Amplifier With RTD Cold-Junction Compensation



A_1	I_B ERROR
OPA177	±1.5 nA
OPA131	±50 pA
OPA602	±1 pA
OPA128	±75 fA

Figure 9-11. Differential Voltage to Current Converter

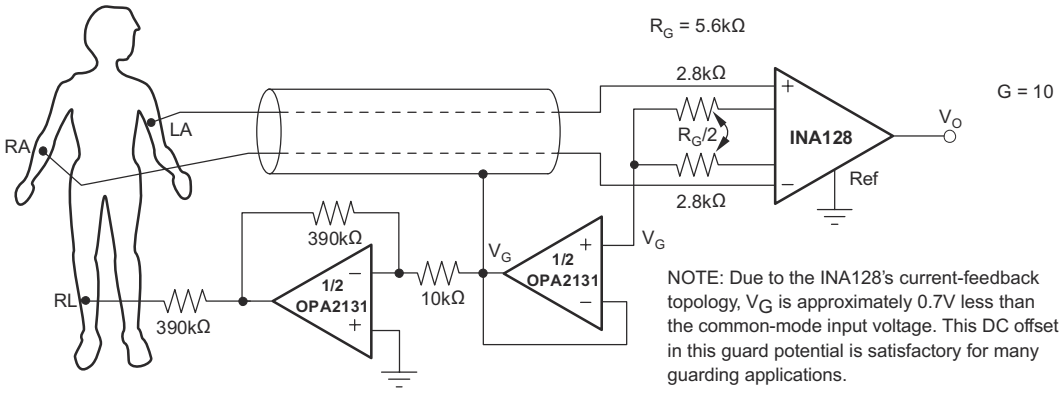


Figure 9-12. ECG Amplifier With Right-Leg Drive

10 Power Supply Recommendations

The minimum power supply voltage for INA12x is ±2.25 V and the maximum power supply voltage is ±18 V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance, ±15 V is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10.1 Low-Voltage Operation

The INA12x operate on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range; see *Section 7.6*.

Operation at very-low supply voltages requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. Figure 7-6 shows the range of linear operation for ±15-V, ±5-V, and ±2.5-V supplies.

11 Layout

11.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF to 1 µF. If necessary, add more decoupling capacitance to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x devices.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the devices.

11.2 Layout Example

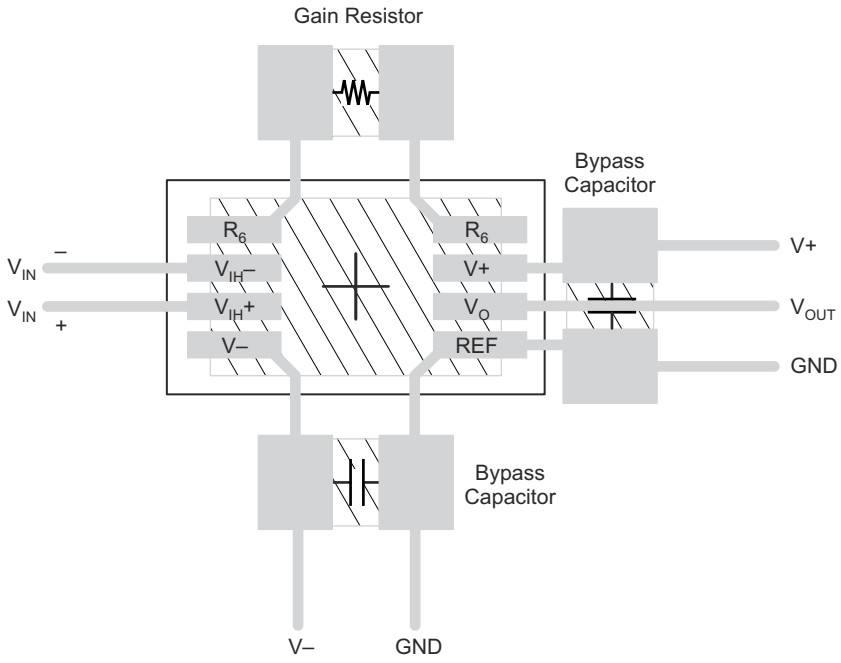


Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA128P	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P	
INA128PA	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P A	
INA128PG4	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P	
INA128U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 128U	Samples
INA128U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 128U	Samples
INA128U/2K5G4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI			Samples
INA128UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5G4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
INA128UAG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		Samples
INA128UG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	
INA129P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples
INA129PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P A	Samples
INA129PG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI			Samples
INA129U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 129U S	Samples
INA129U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 129U S	Samples
INA129UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										129U A	
INA129UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA128, INA129 :

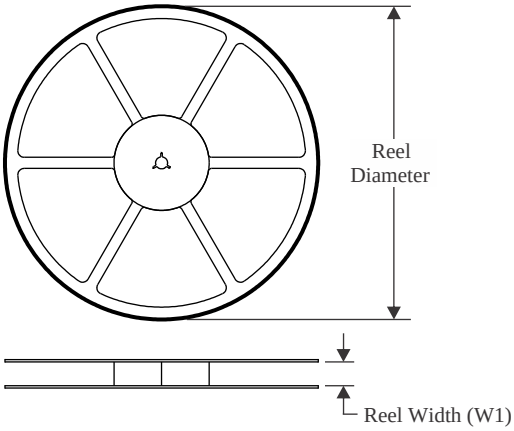
- Enhanced Product : INA129-EP

NOTE: Qualified Version Definitions:

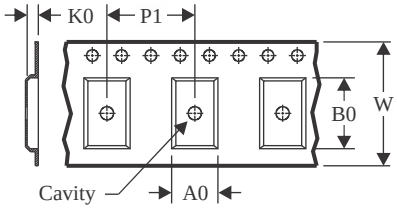
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

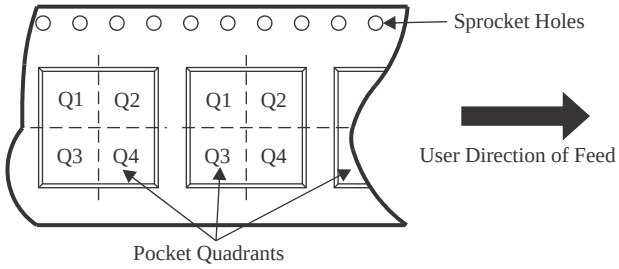


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

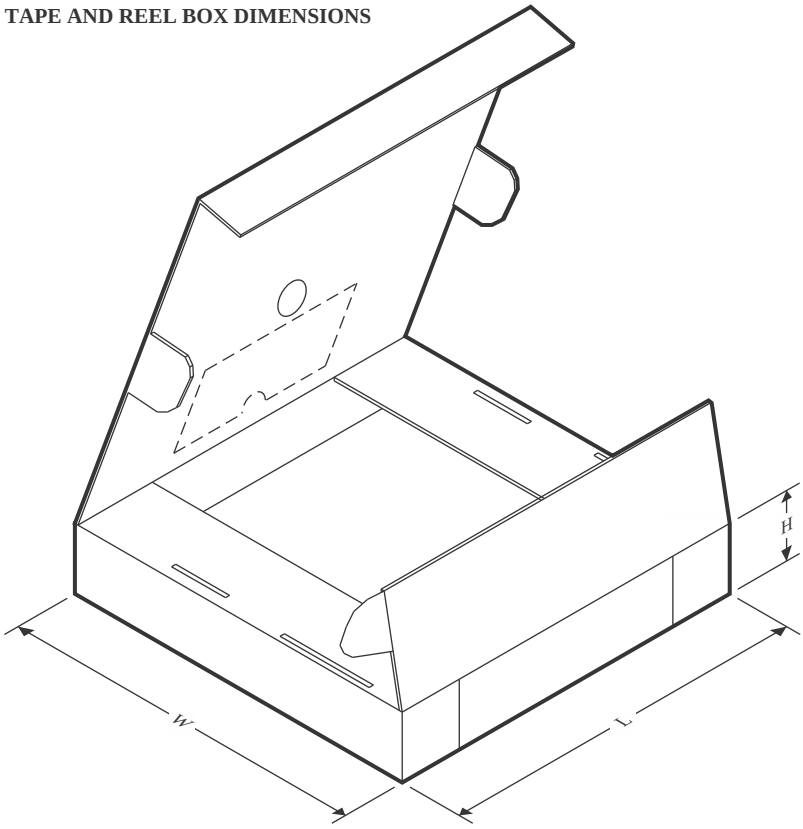
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

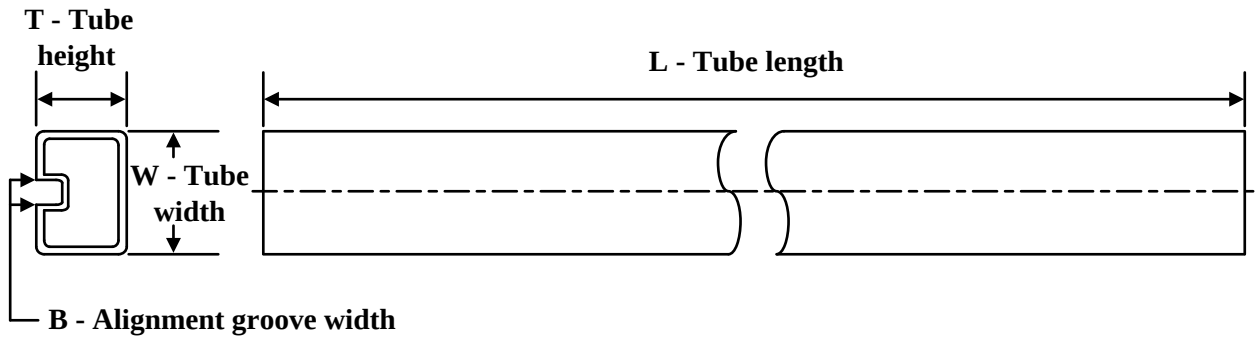
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA128U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA128U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA128UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA128UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA128UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA129U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

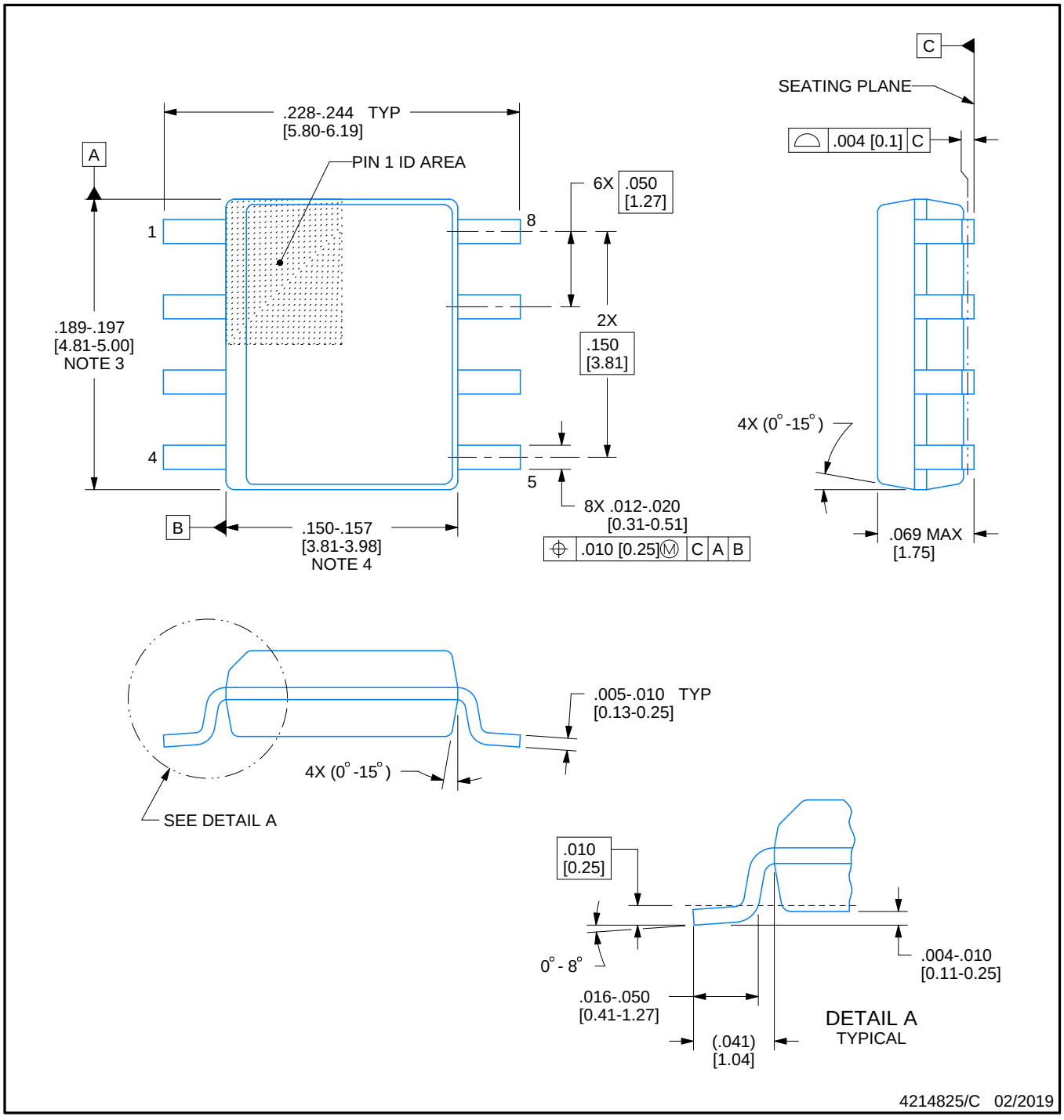
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA128P	P	PDIP	8	50	506	13.97	11230	4.32
INA128PA	P	PDIP	8	50	506	13.97	11230	4.32
INA128PG4	P	PDIP	8	50	506	13.97	11230	4.32
INA128U	D	SOIC	8	75	506.6	8	3940	4.32
INA128UA	D	SOIC	8	75	506.6	8	3940	4.32
INA128UA	D	SOIC	8	75	506.6	8	3940	4.32
INA128UG4	D	SOIC	8	75	506.6	8	3940	4.32
INA129P	P	PDIP	8	50	506	13.97	11230	4.32
INA129PA	P	PDIP	8	50	506	13.97	11230	4.32
INA129U	D	SOIC	8	75	506.6	8	3940	4.32
INA129UA	D	SOIC	8	75	506.6	8	3940	4.32
INA129UA	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

D0008A

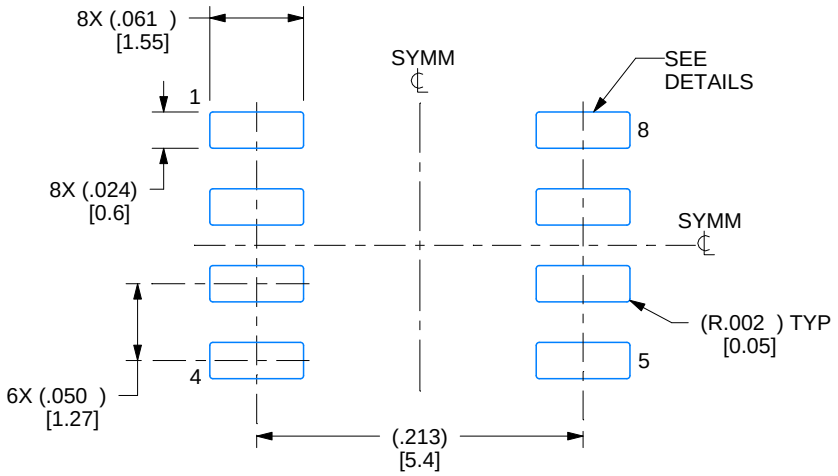
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

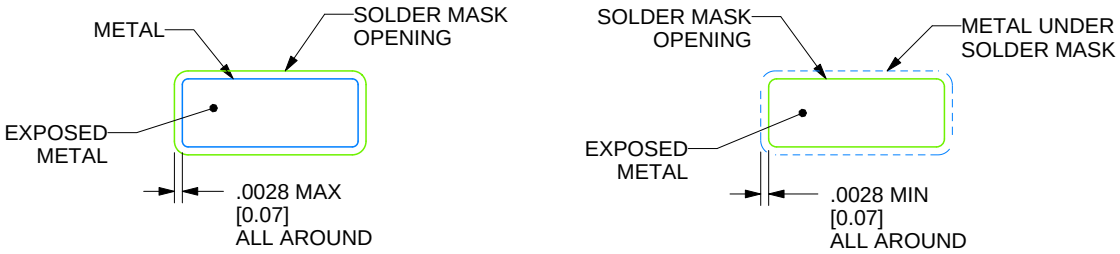


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

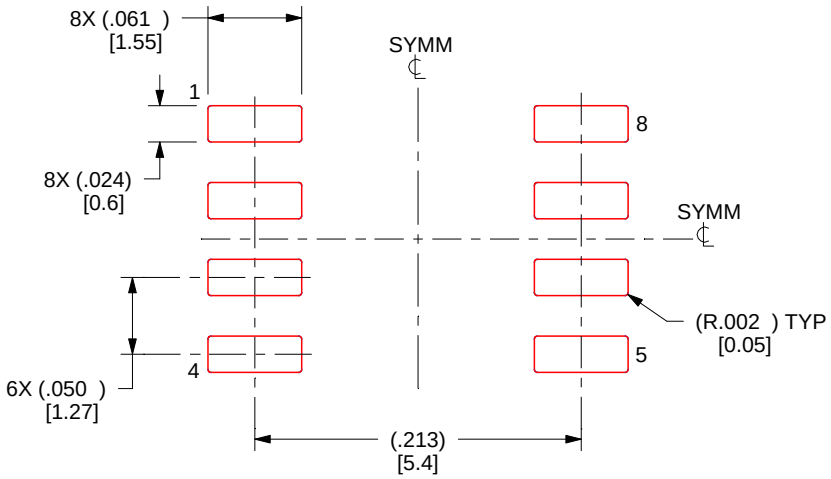
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



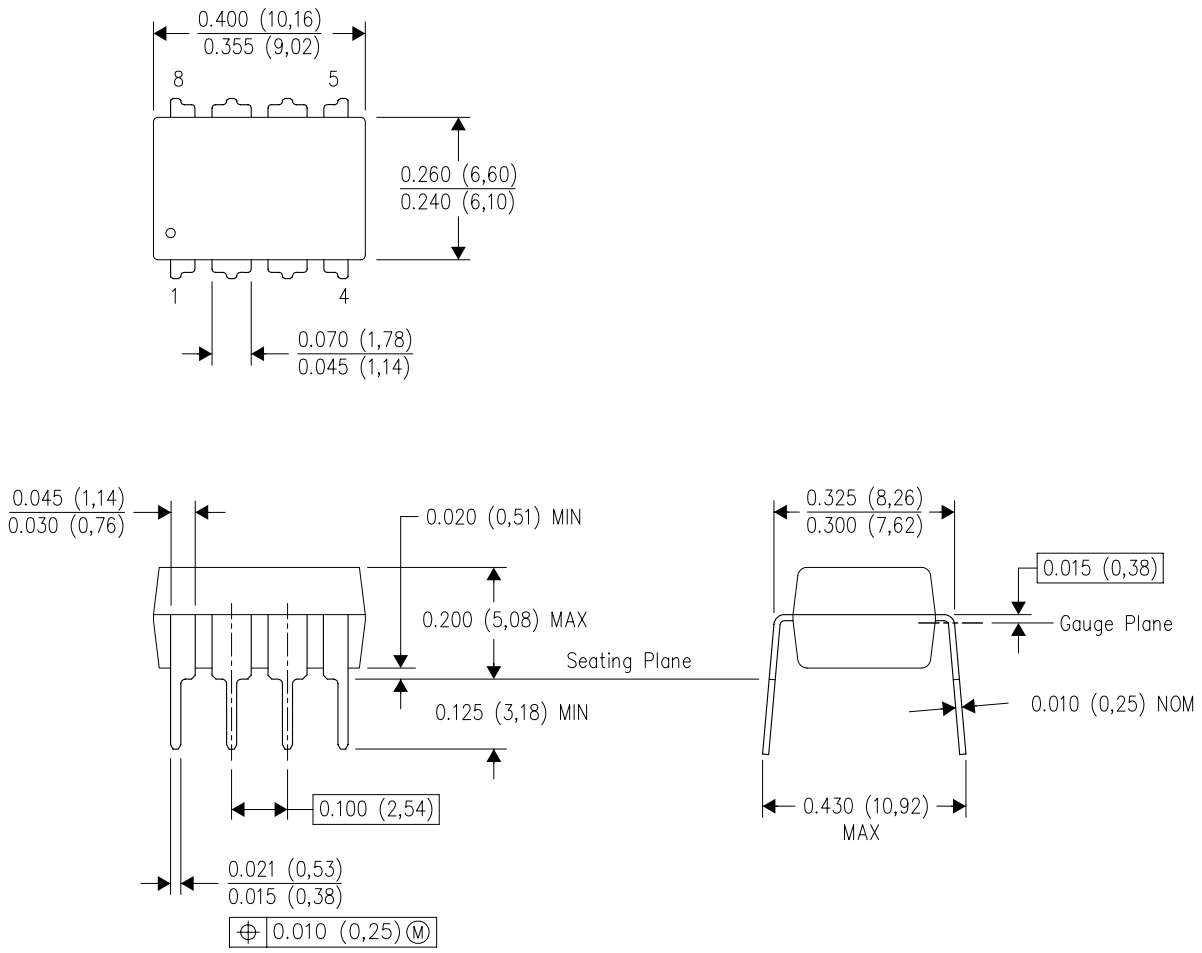
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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