TEXAS INSTRUMENTS

TLV3501, TLV3502

SBOS321E – MARCH 2005 – REVISED APRIL 2016

TLV350x 4.5-ns, Rail-to-Rail, High-Speed Comparator in Microsize Packages

1 Features

- High Speed: 4.5 ns
- Rail-to-Rail I/O
- Supply Voltage: 2.7 V to 5.5 V
- Push-Pull CMOS Output Stage
- Shutdown (TLV3501 Only)
- Micro Packages: 6-Pin SOT-23 (Single), 8-Pin SOT-23 (Dual)
- Low Supply Current: 3.2 mA

2 Applications

- Automatic Test Equipment
- Wireless Base Stations
- Threshold Detectors
- Zero-Crossing Detectors
- Window Comparators

3 Description

The TLV350x family of push-pull output comparators feature a fast 4.5-ns propagation delay and operation from 2.7 V to 5.5 V. Beyond-the-rails input common-mode range makes it an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

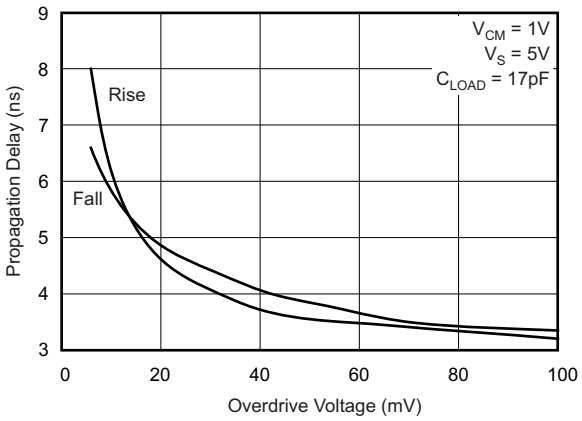
Microsize packages provide options for portable and space-restricted applications. The single (TLV3501) is available in 6-pin SOT-23 and 8-pin SO packages. The dual (TLV3502) comes in the 8-pin SOT-23 and 8-pin SO packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV3501	SOT-23 (6)	1.60 mm × 2.90 mm
	SOIC (8)	3.91 mm × 4.90 mm
TLV3502	SOT-23 (8)	1.63 mm × 2.90 mm
	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Propagation Delay vs Overdrive Voltage



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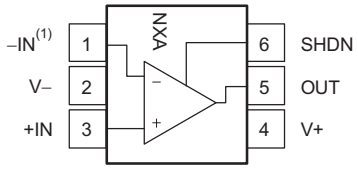
4 Revision History

Changes from Revision D (July 2005) to Revision E **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Removed Ordering Information table ... 1

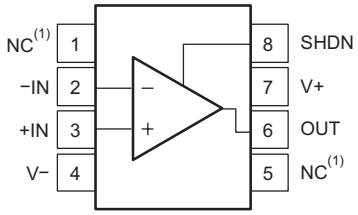
5 Pin Configuration and Functions

TLV3501: DBV Package
6-Pin SOT-23
Top View



(1) Pin 1 of the 6-pin SOT-23 is determined by orienting the package marking as indicated on the diagram.

TLV3501: D Package
8-Pin SOIC
Top View

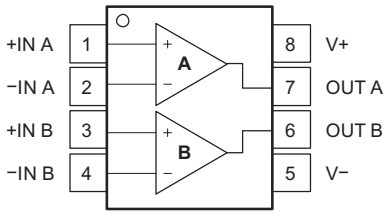


(1) NC indicates no internal connection.

Pin Functions: TLV3501

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN	2	1	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5	—	—	No internal connection (can be left floating)
OUT	6	5	O	Output
SHDN	8	6	—	Shutdown (the device is idle when this pin is not in use)
V–	4	2	—	Negative (lowest) power supply
V+	7	4	—	Positive (highest) power supply

TLV3502: DCN and D Packages
8-Pin SOT-23 and SOIC
Top View



Pin Functions: TLV3502

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	1	I	Noninverting input, channel A
–IN B	4	I	Inverting input, channel B
+IN B	3	I	Noninverting input, channel B
OUT A	7	O	Output, channel A
OUT B	6	O	Output, channel B
V–	5	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply		5.5	V
	Signal input terminal(2)	(V−) − 0.3	(V+) + 0.3	V
Current	Signal input terminal(2)		10	mA
	Output short circuit(3)		74	mA
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	2.2	2.7	5.5	V
V_{IL}	Low-level input voltage, SHDN (comparator is enabled)(1)			(V+) – 1.7	V
V_{IH}	High-level input voltage, SHDN (comparator is disabled)(1)	(V+) – 0.9			V
T_A	Operating temperature	–40		125	°C

(1) When the SHDN pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

6.4 Thermal Information: TLV3501

THERMAL METRIC(1)		TLV3501		UNIT
		DBV (SOT-23)	D (SOIC)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.2	129.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.8	75.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	69.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.3	29.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.7	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: TLV3502

THERMAL METRIC[1]		TLV3502		UNIT
		D (SOIC)	DCN (SOT-23)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	191.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.7	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57	120.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.5	14.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	118.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

At T_A = 25°C and V_S = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage[1]	V_{CM} = 0 V, I_O = 0 mA		±1	±6.5	mV
dV_{OS}/dT	Input offset voltage vs temperature	T_A = –40°C to +125°C		±5		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 5.5 V		100	400	µV/V
	Input hysteresis			6		mV
INPUT BIAS CURRENT						
I_B	Input bias current[2]	V_{CM} = V_{CC}/2		±2	±10	pA
I_{OS}	Input offset current[2][3]	V_{CM} = V_{CC}/2		±2	±10	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V−) − 0.2		(V+) − 0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = −0.2 V to (V+) + 0.2 V	57	70		dB
		V_{CM} = −0.2 V to (V+) + 0.2 V, T_A = −40°C to +125°C	55			
INPUT IMPEDANCE						
	Common-mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OH}, V_{OL}	Voltage output swing from rail	I_{OUT} = ±1 mA		30	50	mV
SHUTDOWN						
t_{OFF}	Shutdown turnoff time			30		ns
t_{ON}	Shutdown turnon time			100		ns
V_L	SHDN low threshold	Comparator is enabled[4]			(V+) − 1.7	V
V_H	SHDN high threshold	Comparator is disabled[4]	(V+) − 0.9			V
	Input bias current of shutdown pin			2		pA
I_{QSD}	Quiescent current in shutdown			2		µA
POWER SUPPLY						
V_S	Specified voltage		2.7		5.5	V
	Operating voltage range	Higher end		2.2		V
		Lower end		5.5		
I_Q	Quiescent current	V_S = 5 V, V_O = High		3.2	5	mA

(1) V_{OS} is defined as the average of the positive and the negative switching thresholds.
(2) Not production tested.
(3) The difference between I_{B+} and I_{B-}.
(4) When the shutdown pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

Electrical Characteristics (continued)

At T_A = 25°C and V_S = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified range		–40		125	°C
Operating range		–40		125	°C

6.7 Switching Characteristics

At T_A = 25°C and V_S = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$T_{(pd)}$	Propagation delay time(1)(2)	ΔV_{IN} = 100 mV, Overdrive = 20 mV	At T_A = 25°C		4.5	6.4	ns
			At T_A = −40°C to +125°C			7	ns
		ΔV_{IN} = 100 mV, Overdrive = 5 mV	At T_A = 25°C		7.5	10	ns
			At T_A = −40°C to +125°C			12	ns
$\Delta t_{(SKEW)}$	Propagation delay skew(3)	ΔV_{IN} = 100 mV, overdrive = 20 mV			0.5		ns
f_{MAX}	Maximum toggle frequency	Overdrive = 50 mV, V_S = 5 V			80		MHz
t_R	Rise time(4)				1.5		ns
t_F	Fall time(4)				1.5		ns

(1) Not production tested.
(2) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization and testing at 100-mV overdrive.
(3) The difference between the propagation delay going high and the propagation delay going low.
(4) Measured between 10% of V_S and 90% of V_S.

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, and input overdrive = 100 mV, unless otherwise noted.

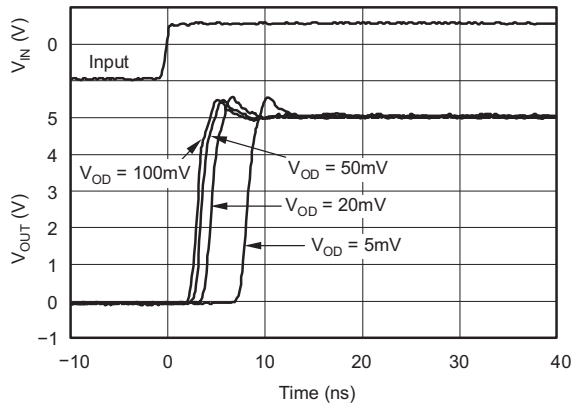


Figure 1. Output Response for Various Overdrive Voltages (Rising)

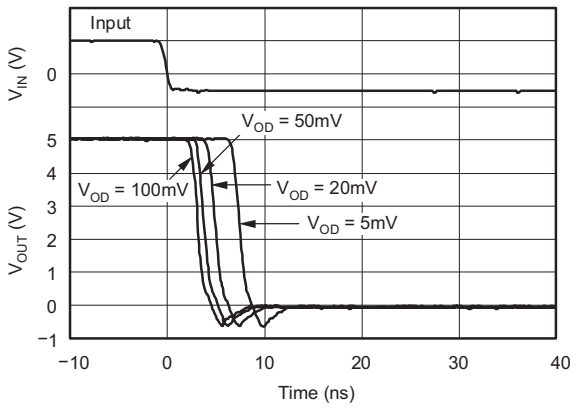
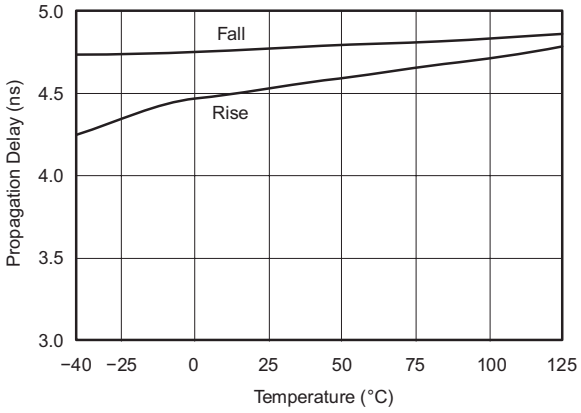
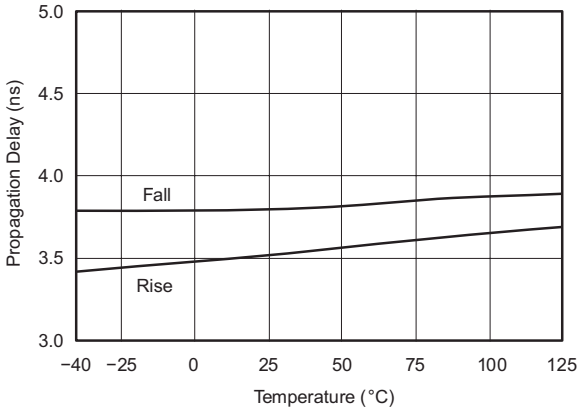


Figure 2. Output Response for Various Overdrive Voltages (Falling)



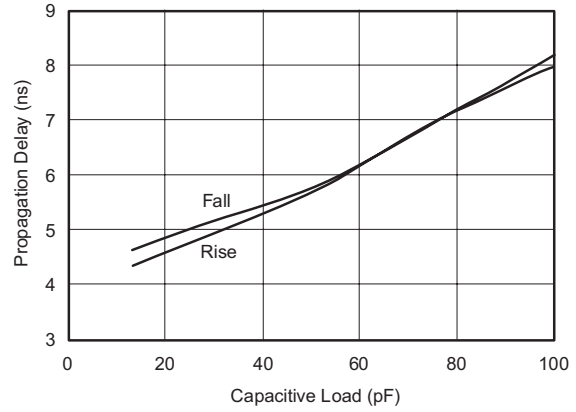
V_{OD} = 20 mV

Figure 3. Propagation Delay vs Temperature



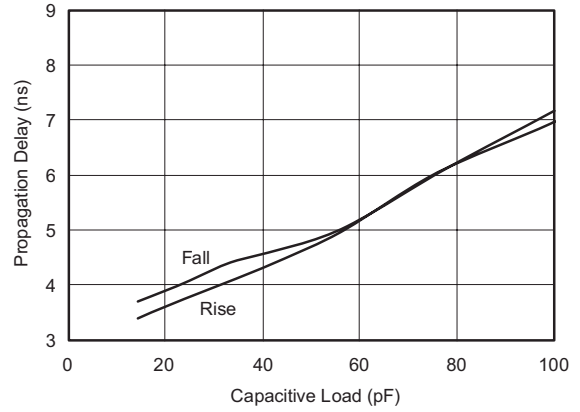
V_{OD} = 50 mV

Figure 4. Propagation Delay vs Temperature



V_{OD} = 20 mV

Figure 5. Propagation Delay vs Capacitive Load

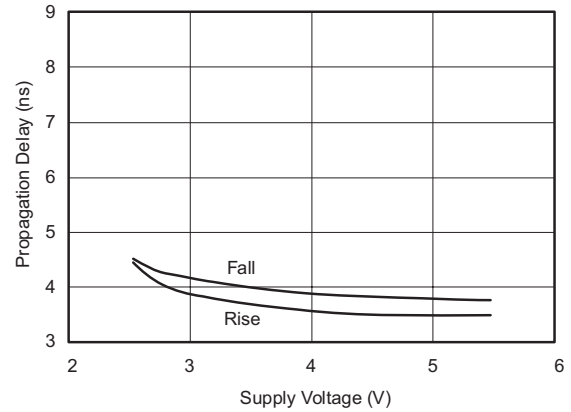


V_{OD} = 50 mV

Figure 6. Propagation Delay vs Capacitive Load

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and input overdrive = 100 mV, unless otherwise noted.



V_{CM} = 1 V V_{OD} = 20 mV

Figure 7. Propagation Delay vs Supply Voltage

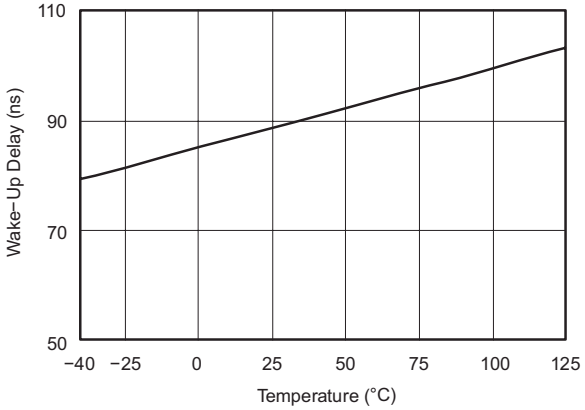
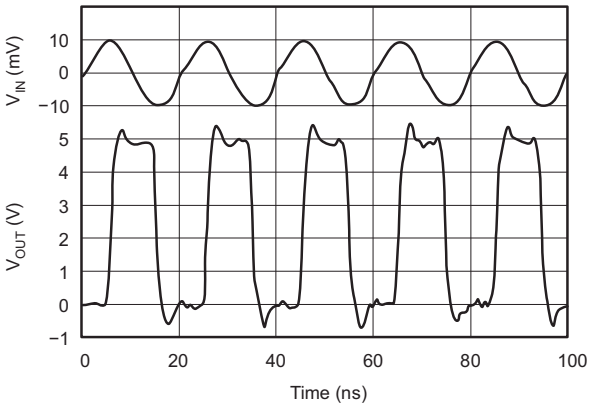


Figure 8. Wake-Up Delay vs Temperature



V_{DD} = 5 V V_{IN} = 20 mV_{PP}

Figure 9. Response to 50-MHz Sine Wave

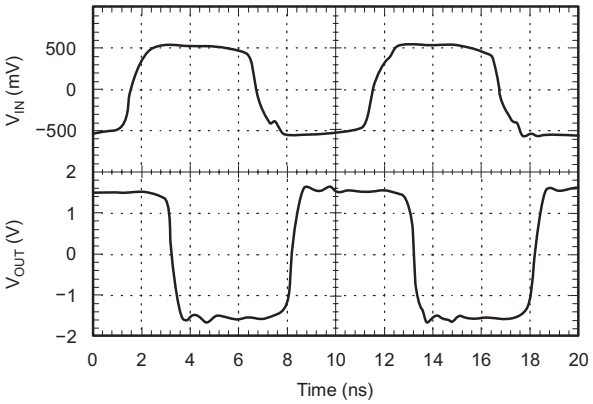


Figure 10. Response to 100-MHz Sine Wave (±2.5-V Dual Supply into 50-Ω Oscilloscope Input)

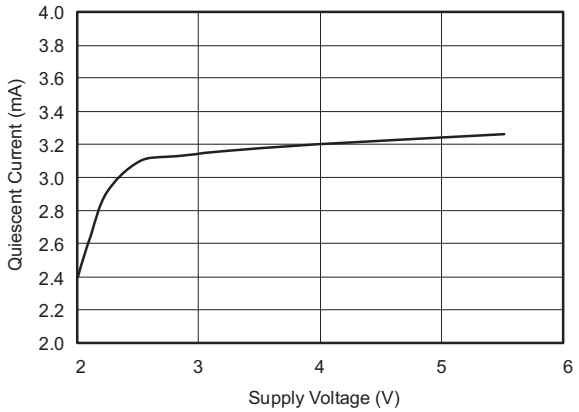


Figure 11. Quiescent Current vs Supply Voltage

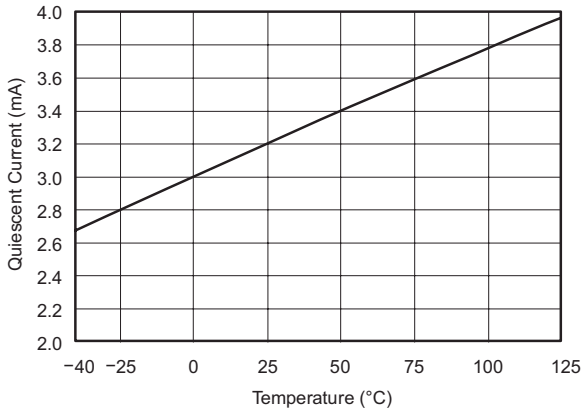


Figure 12. Quiescent Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and input overdrive = 100 mV, unless otherwise noted.

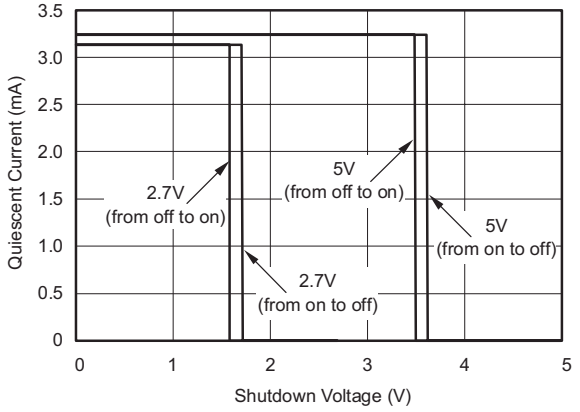


Figure 13. Quiescent Current vs Shutdown Voltage

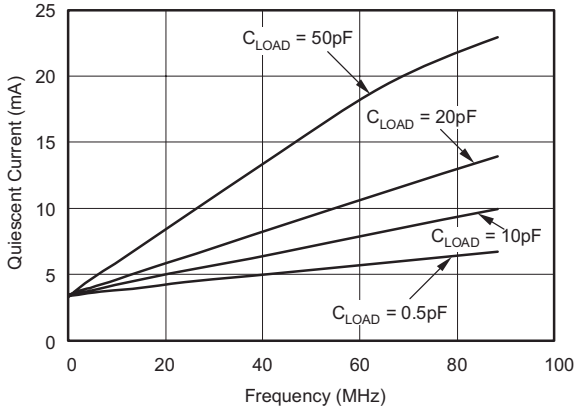


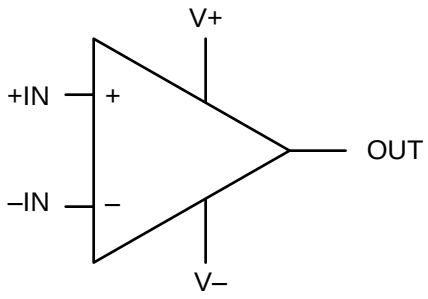
Figure 14. Quiescent Current vs Frequency

7 Detailed Description

7.1 Overview

The TLV3501 and TLV3502 devices both feature high-speed response and include 6 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV350x comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to +125°C. These devices continue to function below this range, but performance is not specified.

7.3.2 Input Overvoltage Protection

Device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in Figure 15.

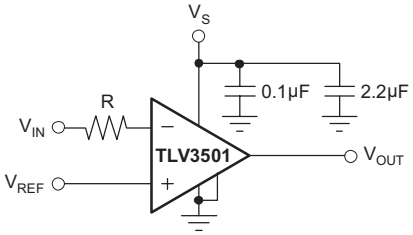


Figure 15. Input Current Protection for Voltages Exceeding the Supply Voltage

7.4 Device Functional Modes

7.4.1 Shutdown

A shutdown pin allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws approximately 2 μA, and the output goes to high impedance. When the shutdown pin is low, the TLV3501 is active. When the TLV3501 shutdown feature is not used, connect the shutdown pin to the most negative supply, as shown in Figure 16. Exiting shutdown mode requires approximately 100 ns. The TLV3502 does not have the shutdown feature.

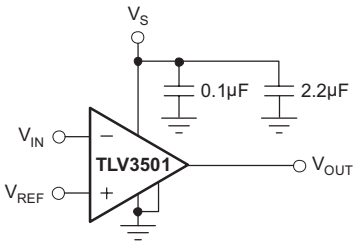


Figure 16. Basic Connections for the TLV3501

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adding External Hysteresis

The TLV350x has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of a specified offset voltage (±5 mV). For slow-moving or noisy input signals, the comparator output can cause an undesirable switch state as input signals move through the switching threshold. In such applications, the 6 mV of internal hysteresis of the TLV350x might not be sufficient. For greater noise immunity, external hysteresis can be added by connecting a small amount of feedback to the positive input. Figure 17 shows a typical topology used to introduce 25 mV of additional hysteresis, for a total of 31-mV hysteresis when operating from a single 5-V supply. Use Equation 1 to calculate the approximate total hysteresis.

$$V_{HYST} = \frac{(V+) \times R_1}{R_1 + R_2} + 6mV \quad (1)$$

The total hysteresis, V_{HYST}, sets the value of the transition voltage required to switch the comparator output, by enlarging the threshold region, thereby reducing sensitivity to noise.

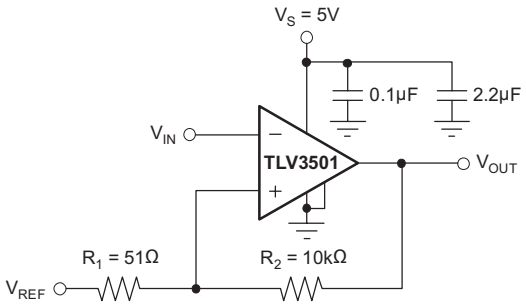


Figure 17. Adding Hysteresis to the TLV350x

8.2 Typical Application

8.2.1 Relaxation Oscillator

The TLV350x can easily be configured as a simple and inexpensive relaxation oscillator. In Figure 18, the R_2 network sets the trip threshold at 1/3 and 2/3 of the supply. Because this circuit is a high-speed circuit, the resistor values are low to minimize the effects of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+, depending on whether the output is low or high. The time to charge (or discharge) is 0.69 × R_1C. Therefore, the period is 1.38 × R_1C. For 62 pF and 1 kΩ as shown in Figure 18, the output is calculated to 10.9 MHz. An implementation of this circuit oscillated at 9.6 MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

Typical Application (continued)

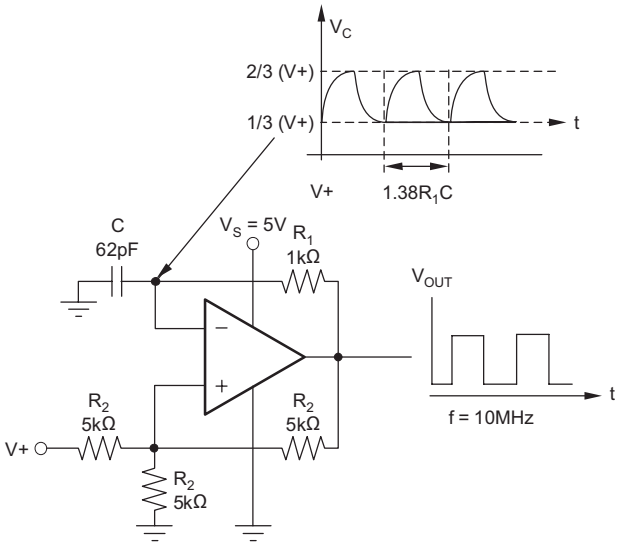


Figure 18. Relaxation Oscillator

8.2.1.1 Design Requirements

For hysteresis of 1/3 of V+ and threshold levels between 1/3 of V+ and 2/3 of V+, the resistors connected to the comparator positive input must be equal in value. The resistor value must be kept low enough so it does not create additional time constant because of the input capacitor and board parasitic capacitor. The value of the charging resistor, R_1, must be relatively low for high-frequency switching without drawing high current and affecting the output high and low level. The value of the charging capacitor must be high enough to avoid errors cause by parasitic capacitance.

8.2.1.2 Detailed Design Procedure

For the positive input, +IN = 1/3 V_{OUT} + 1/3 V+ = 1/3 V+ if V_{OUT} is low and assuming V_{OL} is very close to GND. Or, +IN = 1/3 V_{OUT} + 1/3 V+ = 1/3 V+ = 2/3 V+ if V_{OUT} is high and assuming V_{OH} is very close to V+.

For the negative input, the capacitor charges to 2/3 V+ and discharges to 1/3 V+ exponentially at the same rate with a time constant of R_1C.

8.2.1.3 Application Curve

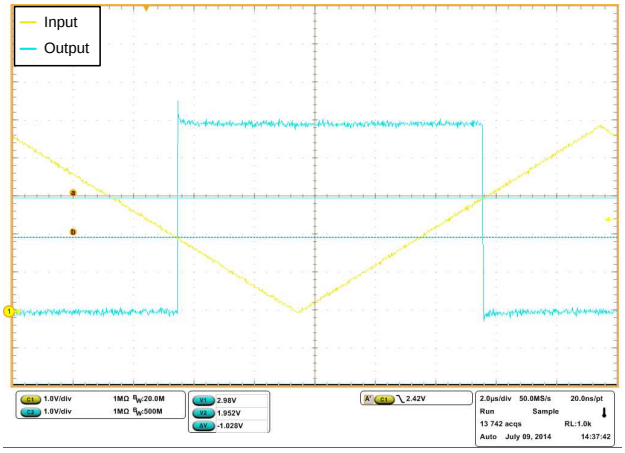


Figure 19. TLV3501 Device With Upper and Lower Thresholds With 1-V Hysteresis

Typical Application (continued)

8.2.2 High-Speed Window Comparator

A window comparator circuit determines when a signal is between two voltages. The TLV3502 can readily be used to create a high-speed window comparator. V_{HI} is the upper voltage threshold, and V_{LO} is the lower voltage threshold. When V_{IN} is between these two thresholds, the output in Figure 20 is high. Figure 21 shows a simple means of obtaining an active low output. The reference levels are connected differently between Figure 20 and Figure 21. The operating voltage range of either circuit is 2.7 V to 5.5 V.

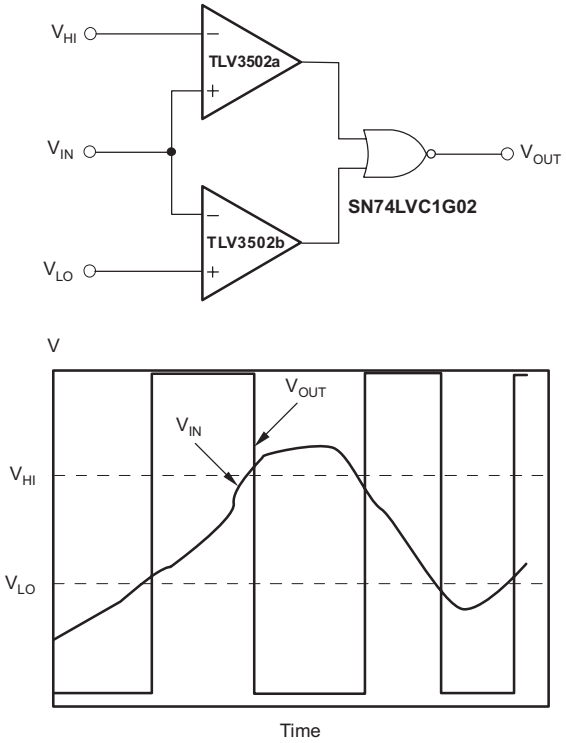


Figure 20. Window Comparator—Active High

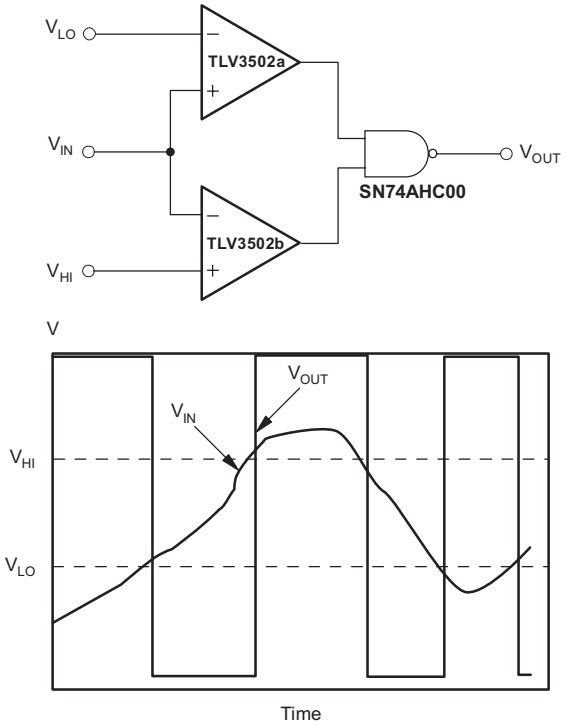


Figure 21. Window Comparator—Active Low

9 Power Supply Recommendations

The TLV350x comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to +125°C. These devices continue to function below this range, but performance is not specified.

Place bypass capacitors close to the power-supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For any high-speed comparator or amplifier, proper design and printed-circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

Minimizing resistance from the signal source to the comparator input is necessary to minimize the propagation delay of the complete circuit. The source resistance, along with input and stray capacitance, creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV350x, along with stray capacitance from an input pin to ground, results in several picofarads of capacitance.

The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2-µF tantalum capacitor does not need to be as close to the device as the 0.1-µF capacitor, and may be shared with other devices. The 2.2-µF capacitor buffers the power-supply line against ripple, and the 0.1-µF capacitor provides a charge for the comparator during high-frequency switching.

In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, use a ground plane to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias must be spaced randomly.

10.2 Layout Examples

Figure 22 shows an evaluation layout for the TLV3501 8-pin SOIC package; Figure 23 is for the 5-pin SOT-23 package. Both evaluation layouts are shown with SMA connectors that bring signals on and off the board. RT1 and RT2 are termination resistors for $+V_{IN}$ and $-V_{IN}$, respectively. C1 and C2 are power-supply bypass capacitors. Place the 0.1-µF capacitor closest to the comparator. The ground plane is not shown, but the pads connecting the resistors and capacitors are shown. Figure 24 shows a schematic of this circuit.

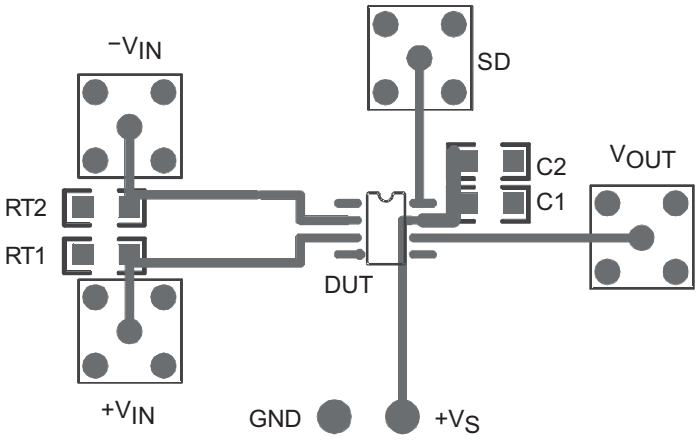


Figure 22. TLV3501D (SOIC) Sample Layout

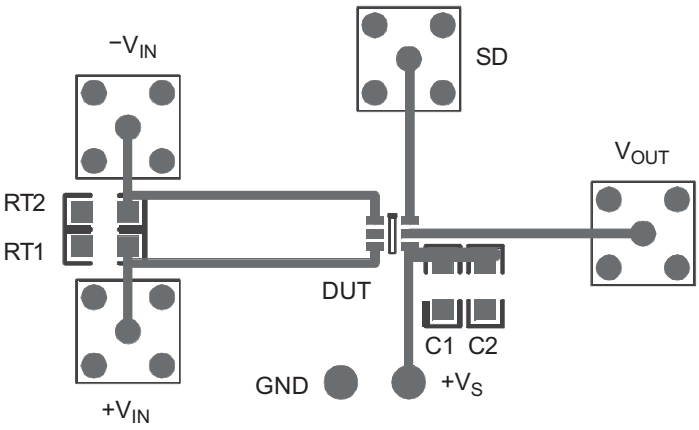


Figure 23. TLV3501DBV (SOT-23) Sample Layout

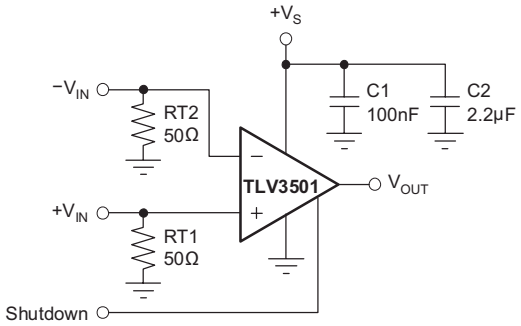


Figure 24. Layout Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the TLV350x, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *Precision Design: Analog Pulse Width Modulation*, SLAU508
- *TLV170x 2.2-V to 36-V, microPower Comparator*, SBOS589
- *TLV170x-Q1 2.2-V to 36-V, microPower Comparator*, SLOS890
- *TLV3501A-Q1 4.5ns Rail-to-Rail, High Speed Comparator in Microsized Packages*, SBOS533
- *TLV3502-Q1 4.5-ns Rail-to-Rail High-Speed Comparator*, SBOS507

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV3501	Click here	Click here	Click here	Click here	Click here
TLV3502	Click here	Click here	Click here	Click here	Click here

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3501AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3501AIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3501AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3502AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples
TLV3502AIDCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples
TLV3502AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3502 :

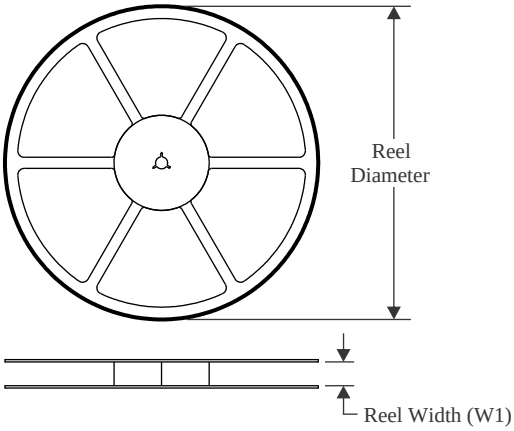
- Automotive: TLV3502-Q1

NOTE: Qualified Version Definitions:

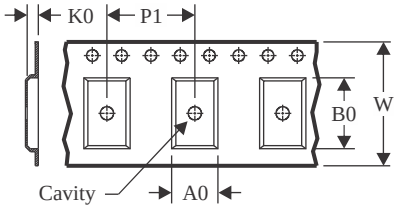
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

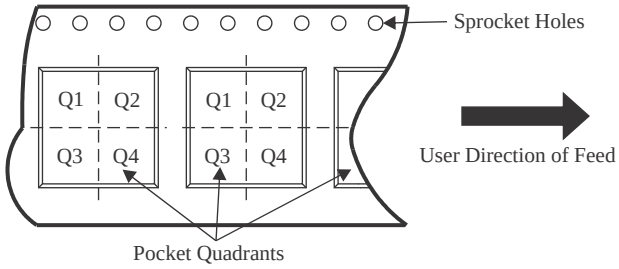


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

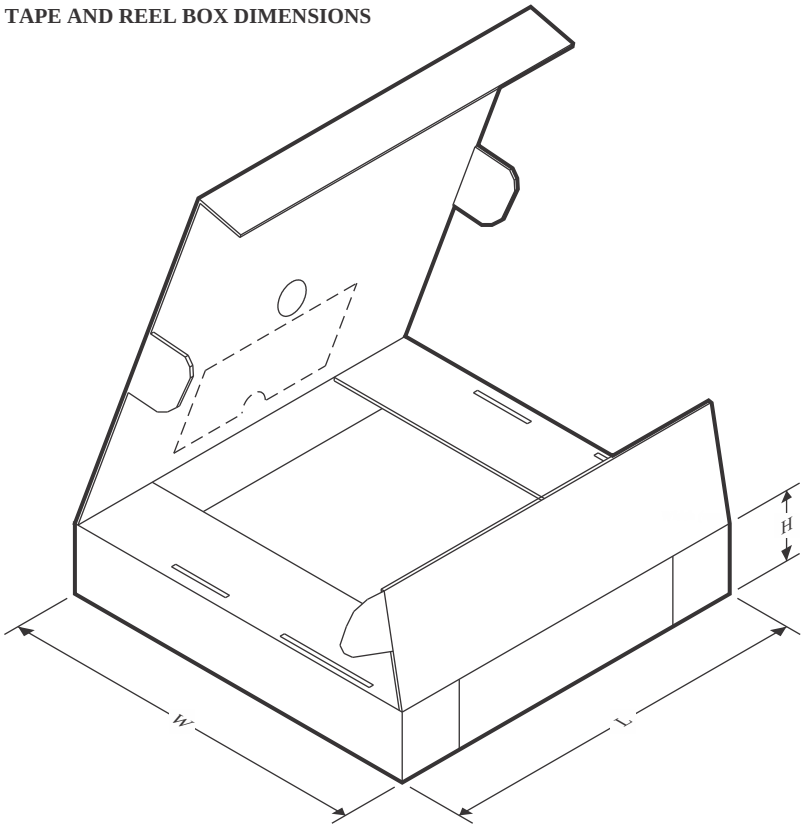
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3501AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3501AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3501AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3502AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3502AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3502AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

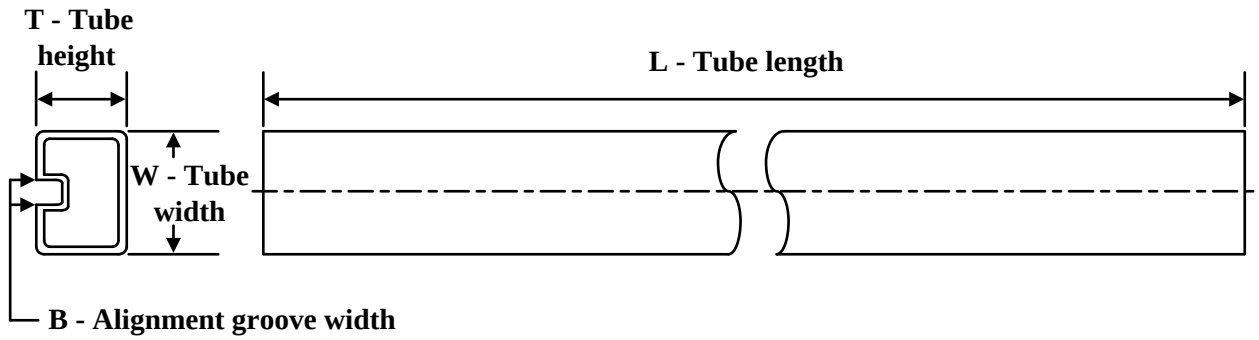
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3501AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV3501AIDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TLV3501AIDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV3502AIDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
TLV3502AIDCNT	SOT-23	DCN	8	250	213.0	191.0	35.0
TLV3502AIDR	SOIC	D	8	2500	356.0	356.0	35.0

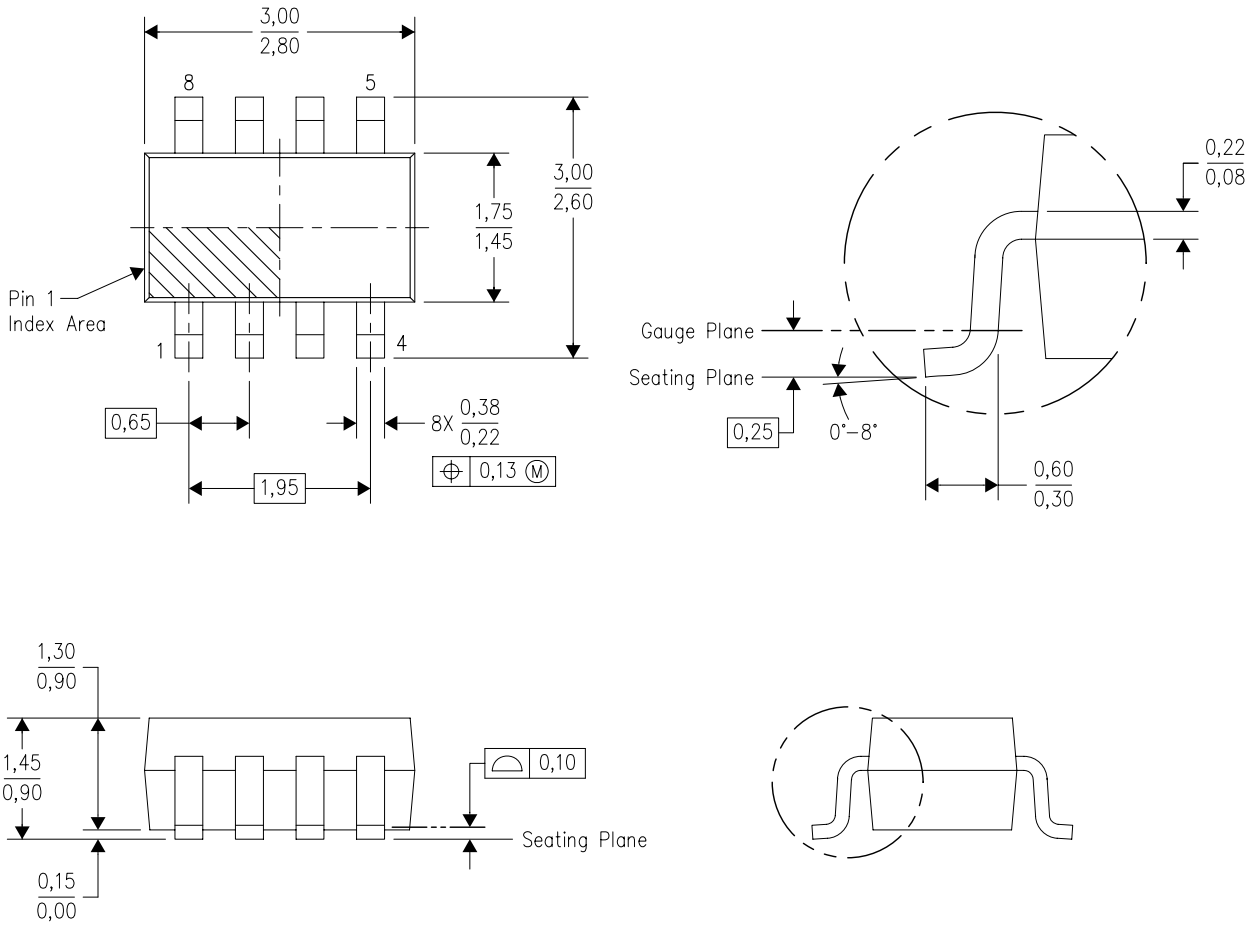
TUBE



*All dimensions are nominal

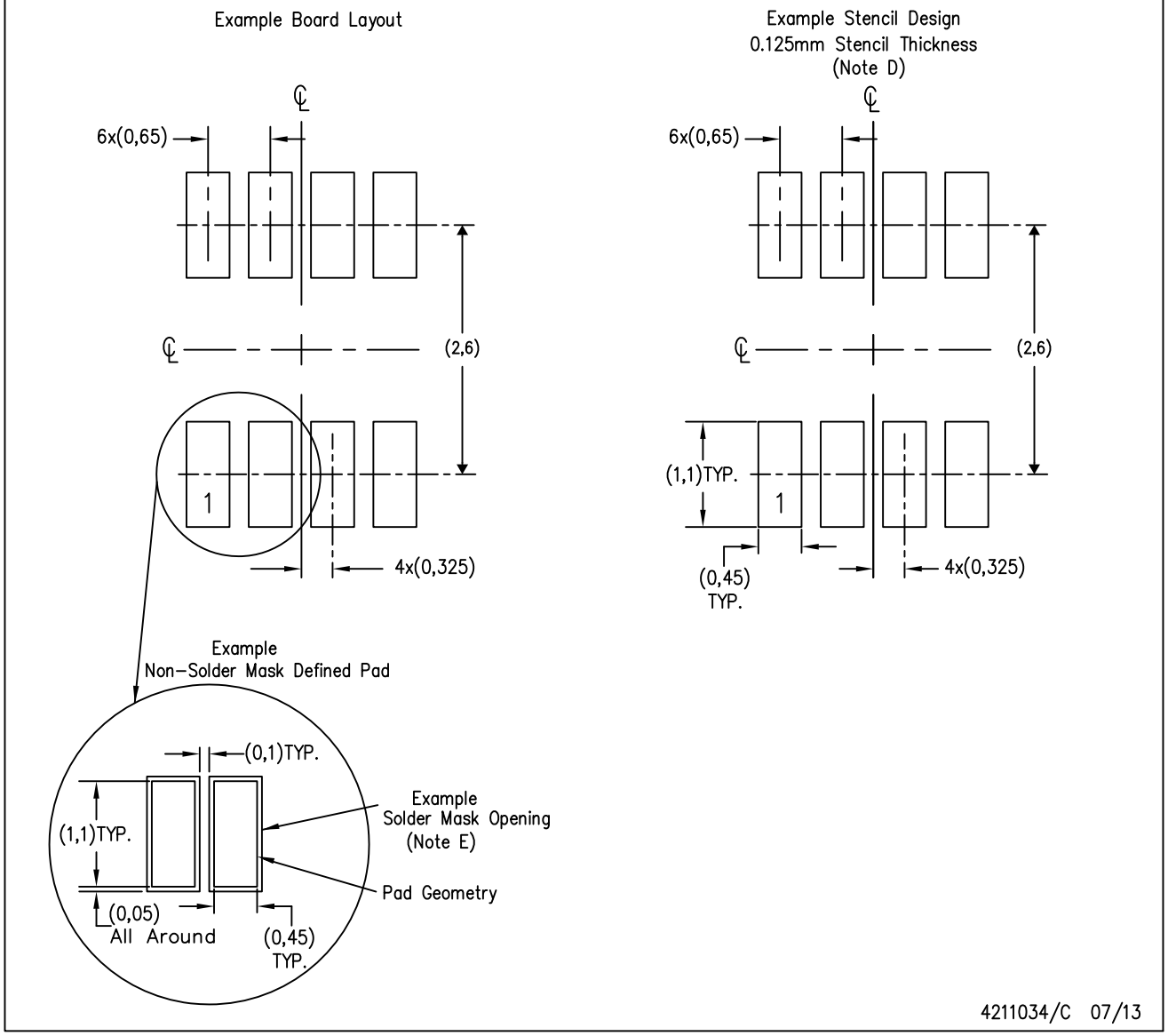
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV3501AID	D	SOIC	8	75	506.6	8	3940	4.32
TLV3501AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
TLV3502AID	D	SOIC	8	75	506.6	8	3940	4.32
TLV3502AIDG4	D	SOIC	8	75	506.6	8	3940	4.32

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



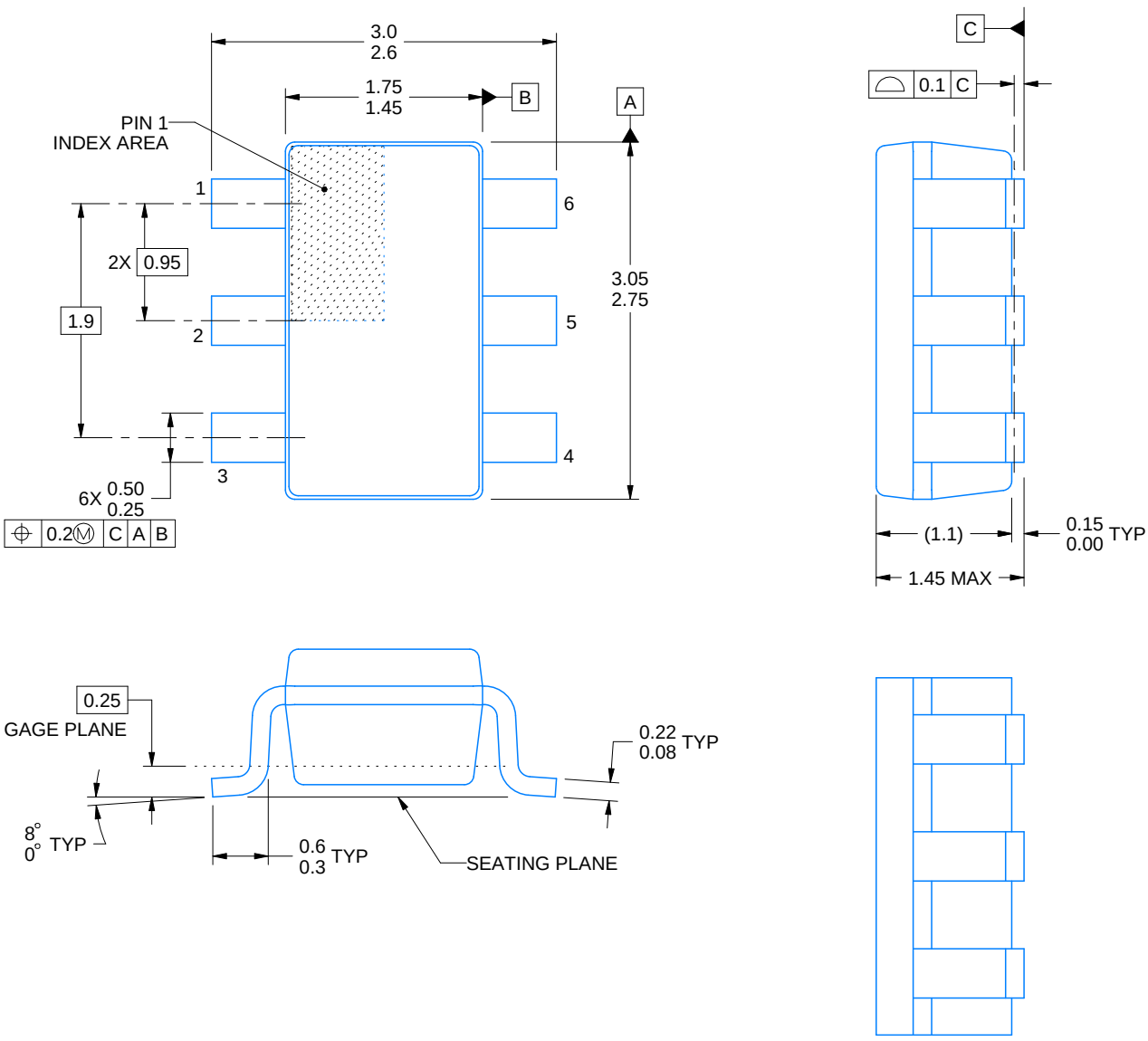
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

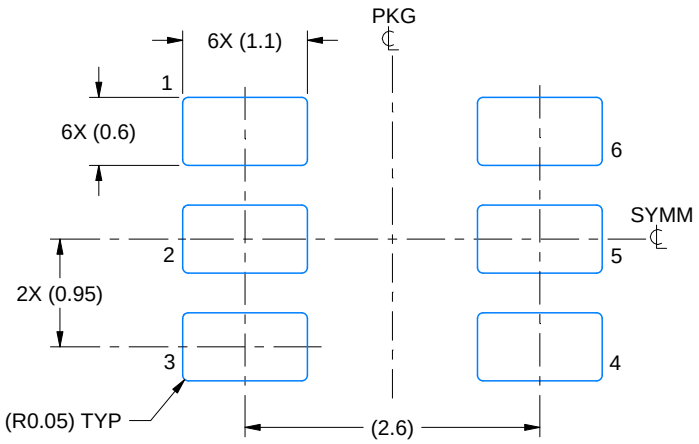


ALTERNATIVE PACKAGE SINGULATION VIEW

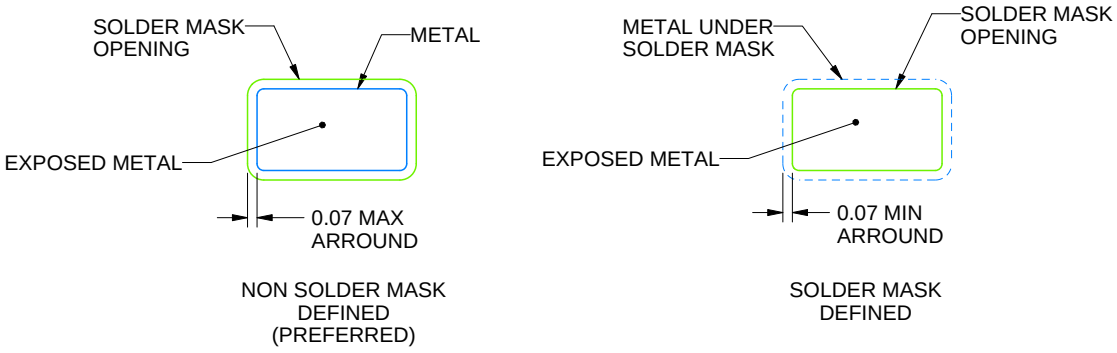
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

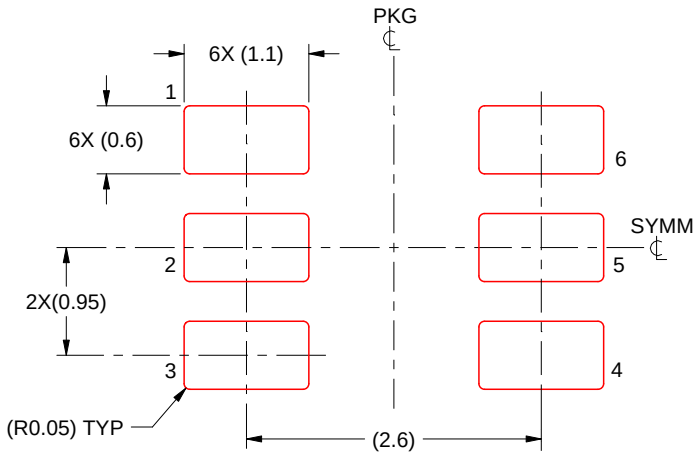


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

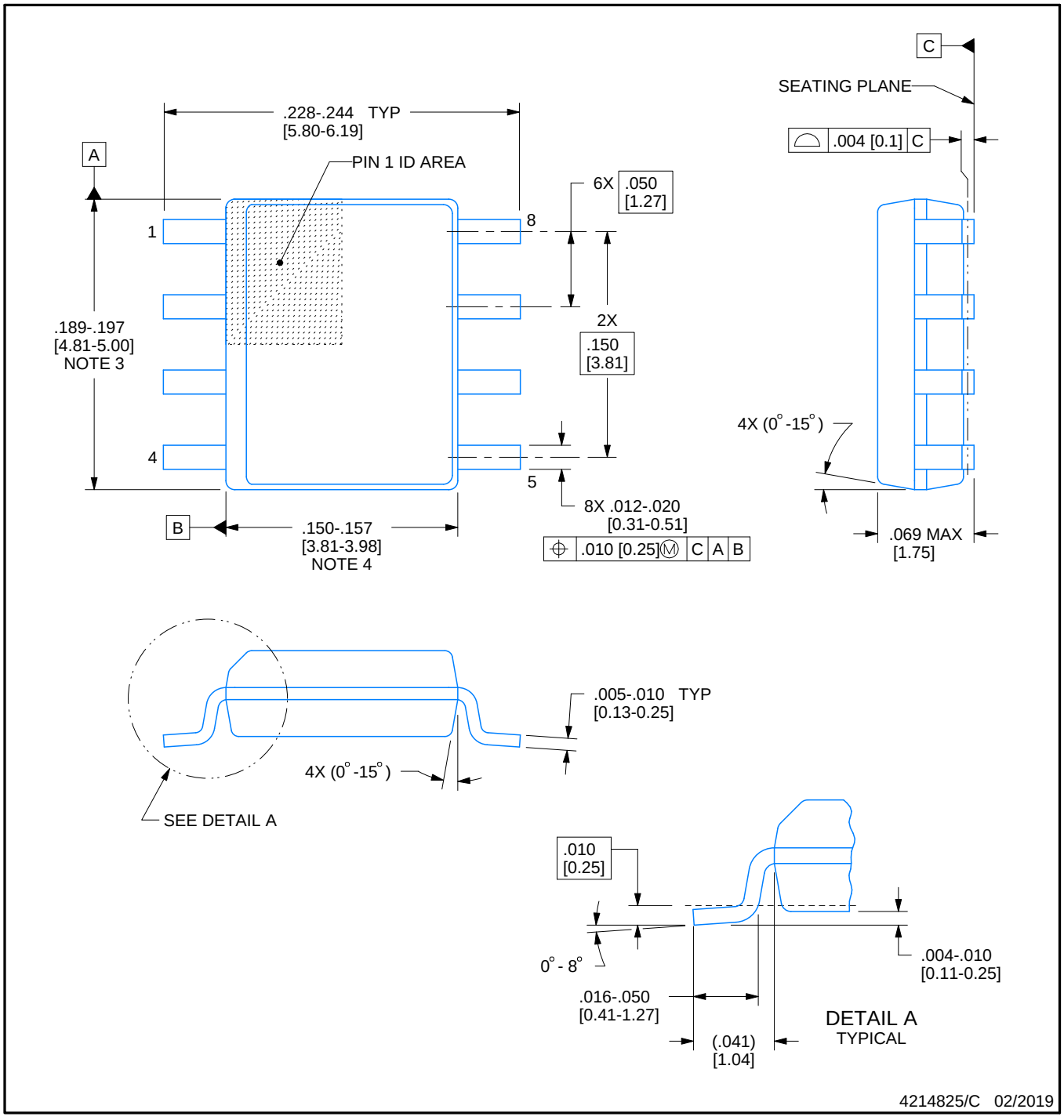
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0008A

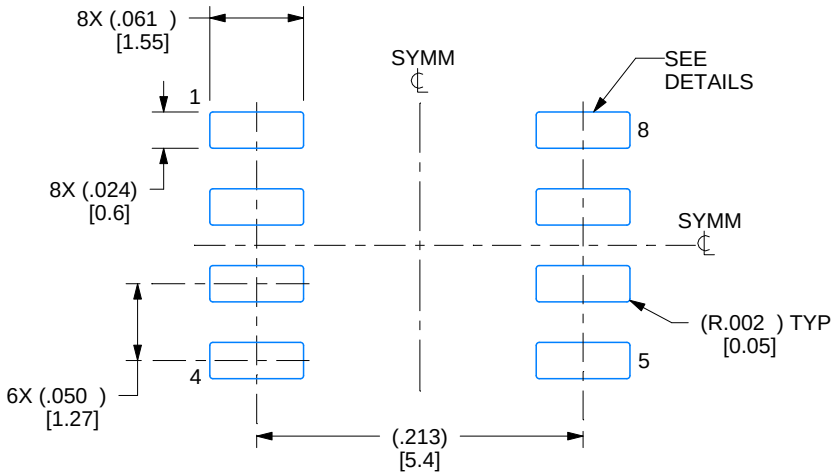
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

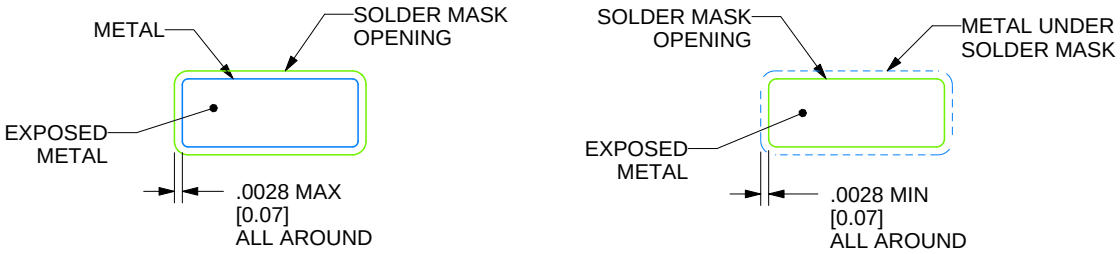


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

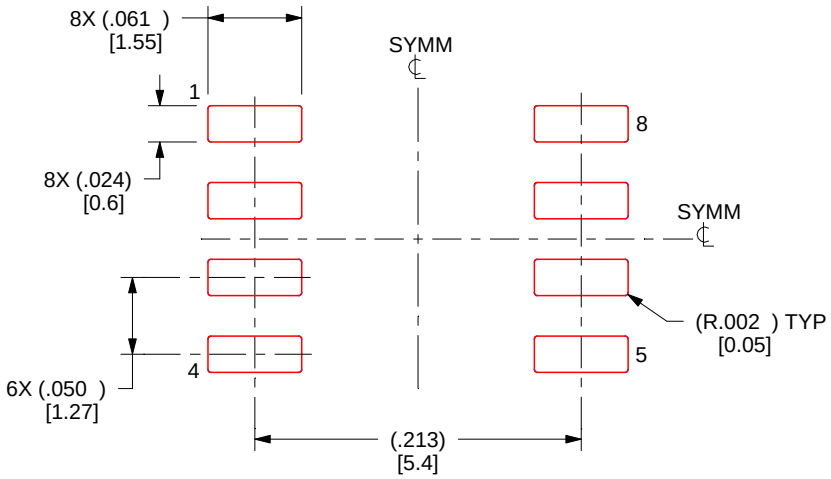
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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