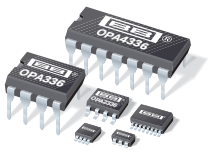


OPA336
OPA2336
OPA4336

SBOS068C – JANUARY 1997 – REVISED JANUARY 2005

SINGLE-SUPPLY, *micro*Power CMOS OPERATIONAL AMPLIFIERS
*micro*Amplifier™ Series

FEATURES

- SINGLE-SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT (within 3mV)
- *micro*POWER: I_Q = 20μA/Amplifier
- *micro*SIZE PACKAGES
- LOW OFFSET VOLTAGE: 125μV max
- SPECIFIED FROM V_S = 2.3V to 5.5V
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

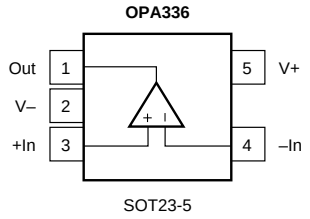
- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- HIGH-IMPEDANCE APPLICATIONS
- PHOTODIODE PRE-AMPS
- PRECISION INTEGRATORS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

DESCRIPTION

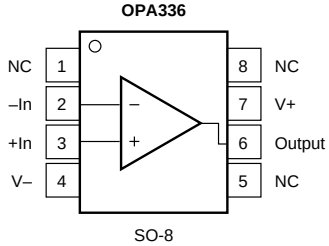
OPA336 series *micro*Power CMOS operational amplifiers are designed for battery-powered applications. They operate on a single supply with operation as low as 2.1V. The output is rail-to-rail and swings to within 3mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply—ideal for single-supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

In addition to small size and low quiescent current (20μA/amplifier), they feature low offset voltage (125μV max), low input bias current (1pA), and high open-loop gain (115dB). Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

OPA336 packages are the tiny SOT23-5 surface mount and SO-8 surface-mount. OPA2336 come in the miniature MSOP-8 surface-mount, SO-8 surface-mount, and DIP-8 packages. The OPA4336 package is the space-saving SSOP-16 surface-mount. All are specified from –40°C to +85°C and operate from –55°C to +125°C. A macromodel is available for download (at www.ti.com) for design analysis.

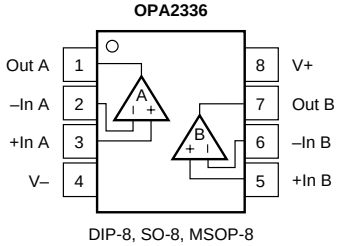


SOT23-5

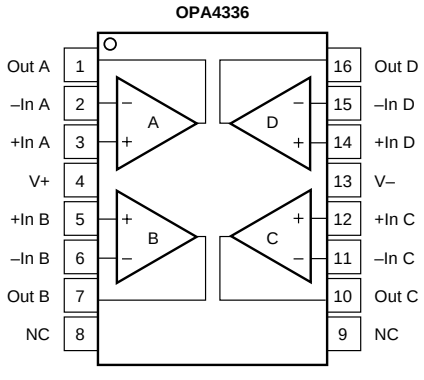


SO-8

NC = No Connection



DIP-8, SO-8, MSOP-8



SSOP-16

NC = No Connection

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DRAWING DESIGNATOR	PACKAGE MARKING
Single			
OPA336N	SOT23-5	DBV	A36[2]
OPA336NA	SOT23-5	DBV	A36[2]
OPA336NJ	SOT23-5	DBV	J36
OPA336U	SO-8 Surface-Mount	D	OPA336U
OPA336UA	SO-8 Surface-Mount	D	OPA336UA
OPA336UJ	SO-8 Surface-Mount	D	OPA336UJ
Dual			
OPA2336E	MSOP-8 Surface-Mount	DGK	B36[2]
OPA2336EA	MSOP-8 Surface-Mount	DGK	B36[2]
OPA2336P	DIP-8	P	OPA2336P
OPA2336PA	DIP-8	P	OPA2336PA
OPA2336U	SO-8 Surface-Mount	D	OPA2336U
OPA2336UA	SO-8 Surface-Mount	D	OPA2336UA
Quad			
OPA4336EA	SSOP-16 Surface-Mount	DBQ	OPA4336EA

NOTES: (1) For the most current package and ordering information, see the package option addendum at the end of this data sheet. (2) Grade will be marked on the Reel.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	7.5V
Signal Input Terminals, Voltage[2]	(V–) –0.3V to (V+) +0.3V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Rating:	
Charged Device Model, OPA336 NJ and UJ only (CDM)[4]	1000V
Human Body Model (HBM)[4]	500V
Machine Model (MM)[4]	100V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package. (4) OPA336 NJ and UJ have been tested to CDM of 1000V. All other previous package versions have been tested using HBM and MM. Results are shown.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_S = 2.3V to 5.5V

Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

PARAMETER	CONDITION	OPA336N, U OPA2336E, P, U			OPA336NA, UA OPA2336EA, PA, UA OPA4336EA			OPA336NJ, UJ			UNITS
		MIN	TYP[1]	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE											
Input Offset Voltage V_{OS}			±60	±125		*	±500		±500	±2500	µV
vs Temperature dV_{OS}/dT			**±1.5**			*			*		**µV/°C**
vs Power Supply PSRR	V_S = 2.3V to 5.5V		25	100		*	*	*	*	*	µV/V
Over Temperature	V_S = 2.3V to 5.5V			**130**			*	*		*	**µV/V**
Channel Separation, dc			0.1			*			*		µV/V
INPUT BIAS CURRENT											
Input Bias Current I_B			±1	±10		*	*		*	*	pA
Over Temperature				**±60**			*			*	**pA**
Input Offset Current I_{OS}			±1	±10		*	*		*	*	pA
NOISE											
Input Voltage Noise, f = 0.1 to 10Hz			3			*			*		µVp-p
Input Voltage Noise Density, f = 1kHz e_n			40			*			*		nV/√Hz
Current Noise Density, f = 1kHz i_n			30			*			*		fA/√Hz
INPUT VOLTAGE RANGE											
Common-Mode Voltage Range V_{CM}		–0.2		(V+) –1	*		*	*		*	V
Common-Mode Rejection Ratio CMRR	–0.2V < V_{CM} < (V+) –1V	80	90		76	86		76	86		dB
Over Temperature	–0.2V < V_{CM} < (V+) –1V	**76**			**74**			**74**			**dB**
INPUT IMPEDANCE											
Differential			10^{13} || 2			*			*		Ω || pF
Common-Mode			10^{13} || 4			*			*		Ω || pF
OPEN-LOOP GAIN											
Open-Loop Voltage Gain A_{OL}	R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	100	115		90	*		90	*		dB
Over Temperature	R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	**100**			**90**			**90**			**dB**
	R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	90	106		*	*		*	*		dB
Over Temperature	R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	**90**			*			*			**dB**
FREQUENCY RESPONSE											
Gain-Bandwidth Product GBW	V_S = 5V, G = 1		100			*			*		kHz
Slew Rate SR	V_S = 5V, G = 1		0.03			*			*		V/µs
Overload Recovery Time	V_{IN} • G = V_S		100			*			*		µs
OUTPUT											
Voltage Output Swing from Rail[2]	R_L = 100kΩ, A_{OL} ≥ 70dB		3			*			*		mV
	R_L = 25kΩ, A_{OL} ≥ 90dB		20	100		*	*		*	*	mV
Over Temperature	R_L = 25kΩ, A_{OL} ≥ 90dB			**100**			*			*	**mV**
	R_L = 5kΩ, A_{OL} ≥ 90dB		70	500		*	*		*	*	mV
Over Temperature	R_L = 5kΩ, A_{OL} ≥ 90dB			**500**			*			*	**mV**
Short-Circuit Current I_{SC}			±5			*			*		mA
Capacitive Load Drive C_{LOAD}			See Text			*			*		pF
POWER SUPPLY											
Specified Voltage Range V_S		2.3		5.5	*		*	*		*	V
Minimum Operating Voltage			2.1			*			*		V
Quiescent Current (per amplifier) I_Q	I_O = 0		20	32		*	*		23	38	µA
Over Temperature	I_O = 0			**36**			*			**42**	**µA**
TEMPERATURE RANGE											
Specified Range		–40		+85	*		*	*		*	°C
Operating Range		–55		+125	*		*	*		*	°C
Storage Range		–55		+125	*		*	*		*	°C
Thermal Resistance θ_{JA}											
SOT-23-5 Surface-Mount			200			*			*		°C/W
MSOP-8 Surface-Mount			150			*					°C/W
SO-8 Surface-Mount			150			*			*		°C/W
DIP-8			100			*					°C/W
SSOP-16 Surface-Mount			100			*					°C/W
DIP-14			80			*					°C/W

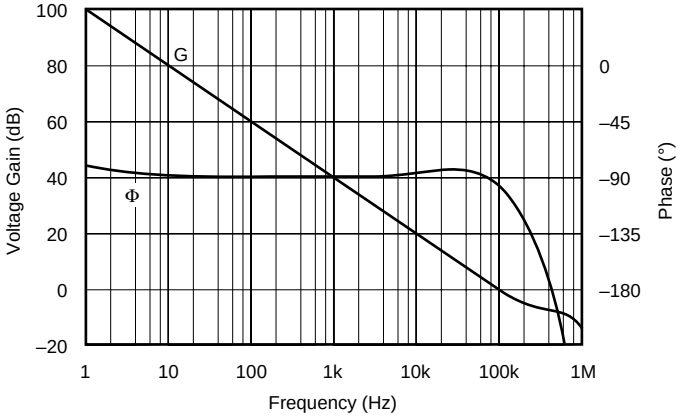
*Specifications same as OPA2336E, P, U.

NOTES: (1) V_S = +5V. (2) Output voltage swings are measured between the output and positive and negative power-supply rails.

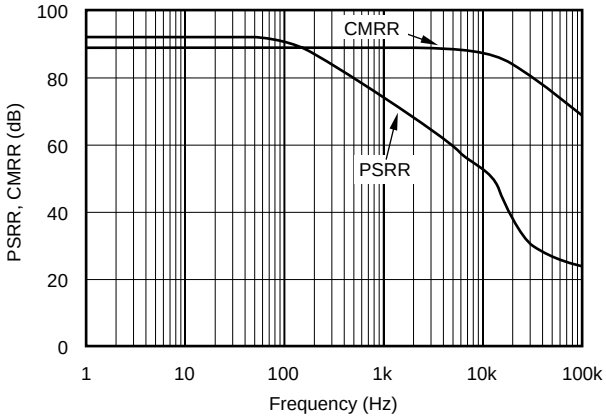
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

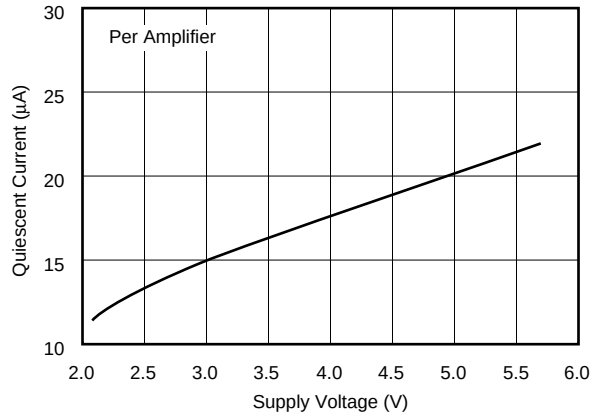
OPEN-LOOP GAIN/PHASE vs FREQUENCY



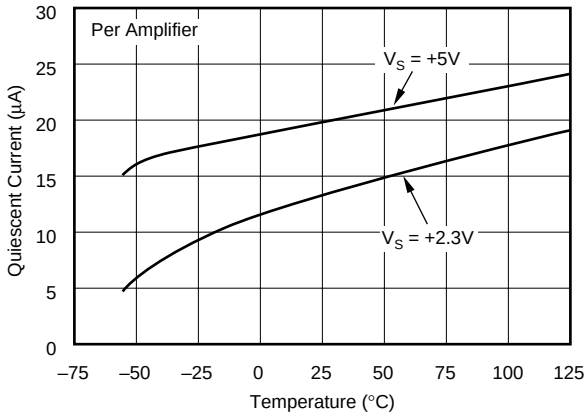
POWER-SUPPLY and COMMON-MODE REJECTION RATIO vs FREQUENCY



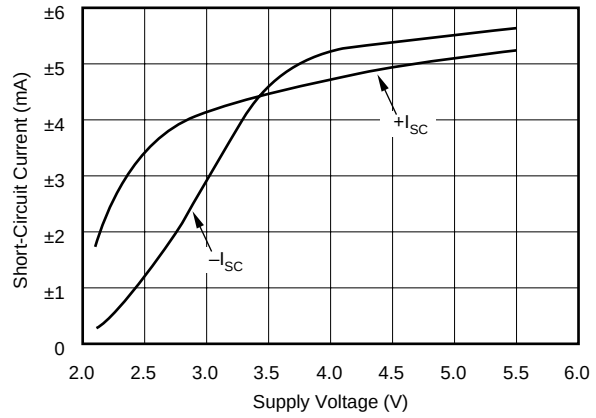
QUIESCENT CURRENT vs SUPPLY VOLTAGE



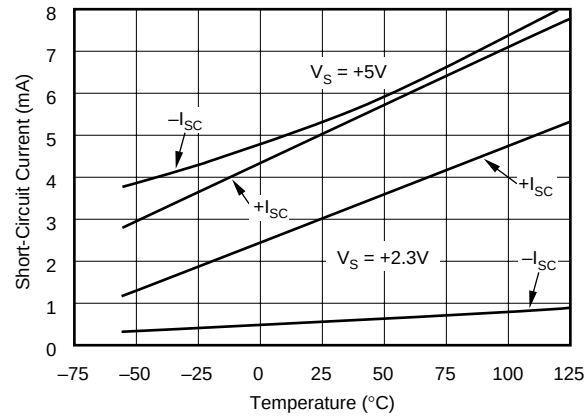
QUIESCENT CURRENT vs TEMPERATURE



SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



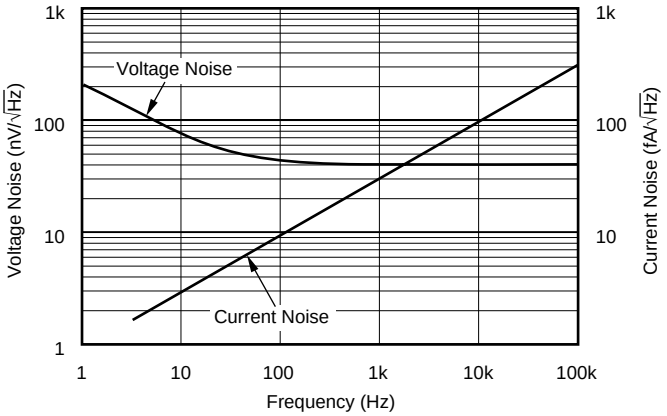
SHORT-CIRCUIT CURRENT vs TEMPERATURE



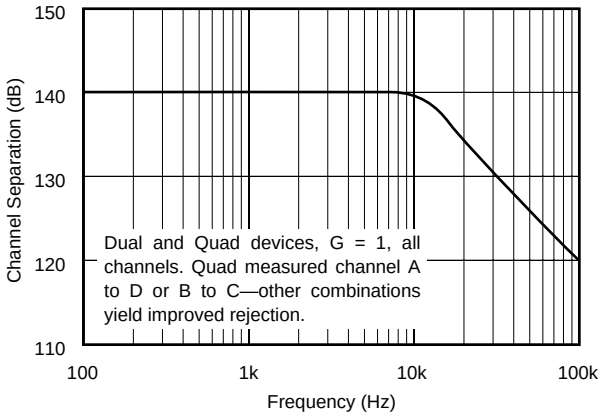
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

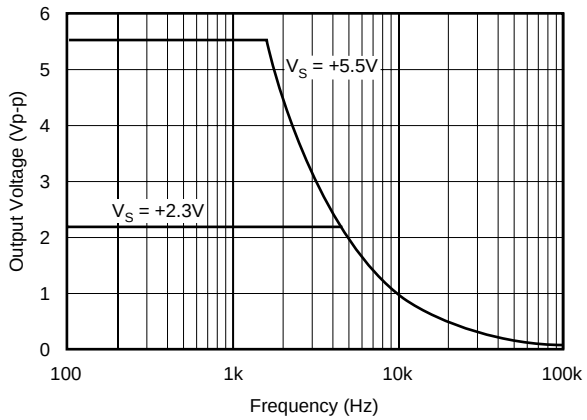
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



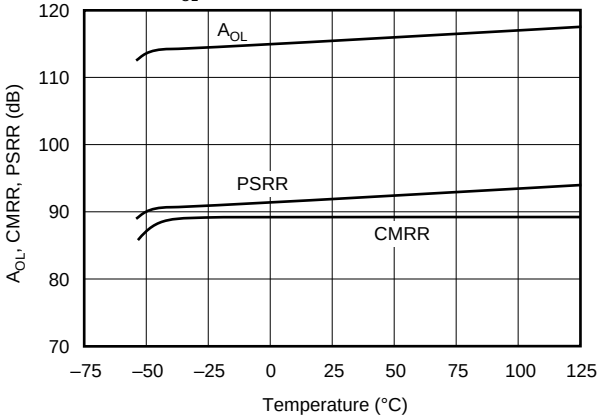
CHANNEL SEPARATION vs FREQUENCY



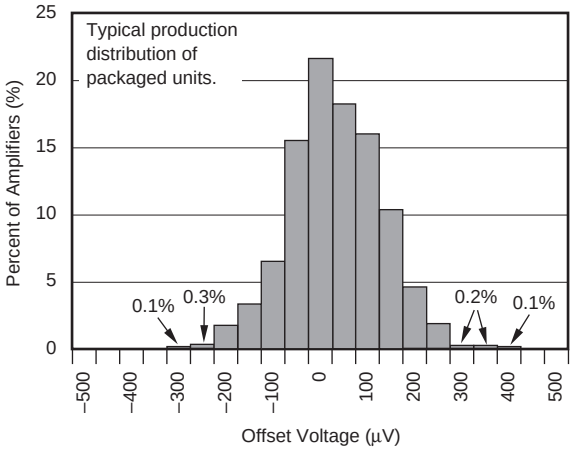
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



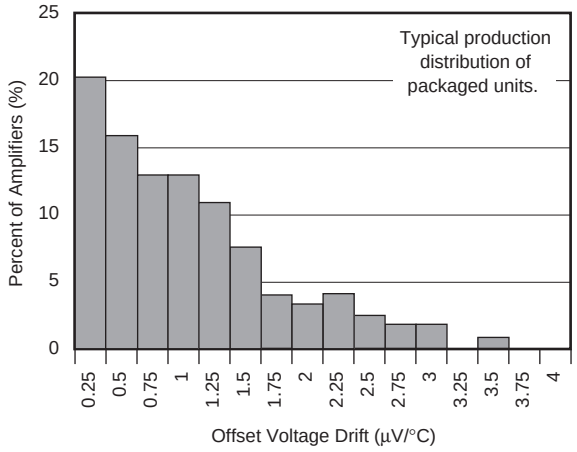
A_{OL}, CMRR, PSRR vs TEMPERATURE



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



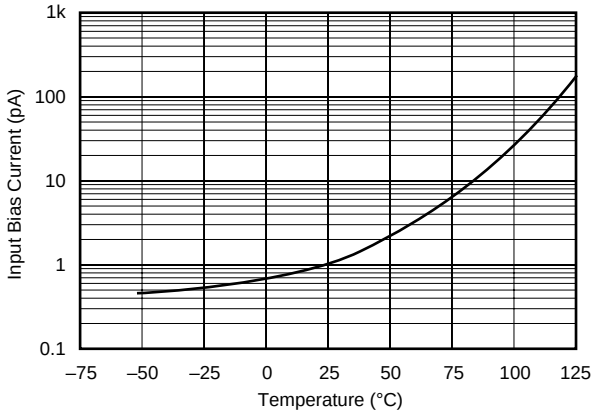
OFFSET VOLTAGE DRIFT MAGNITUDE PRODUCTION DISTRIBUTION



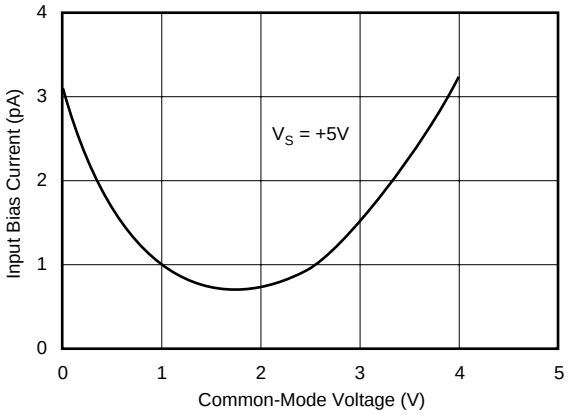
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

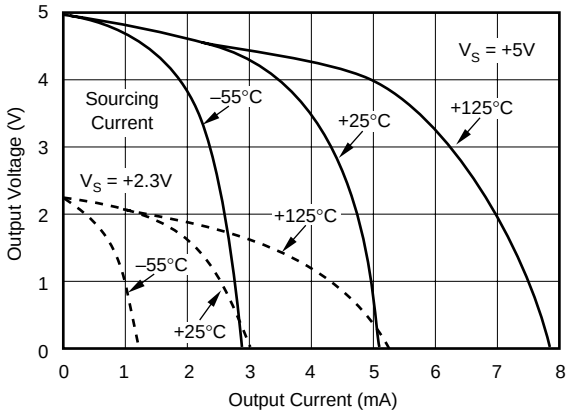
INPUT BIAS CURRENT vs TEMPERATURE



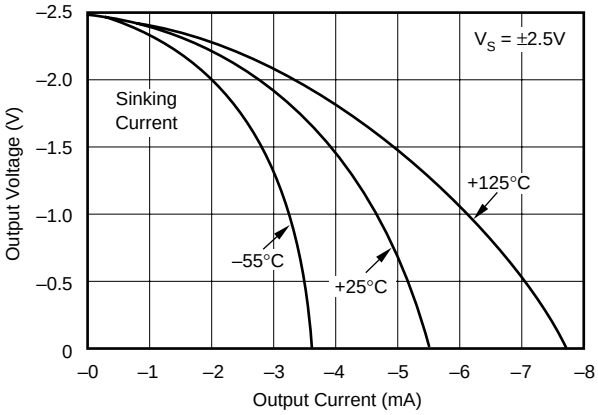
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



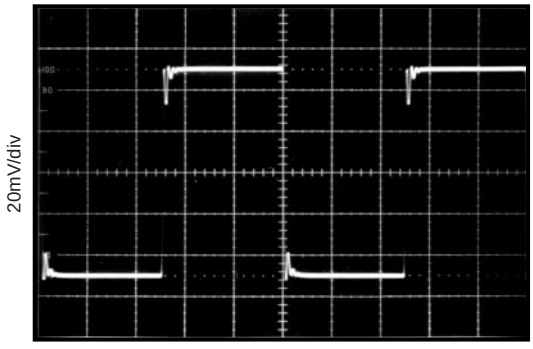
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



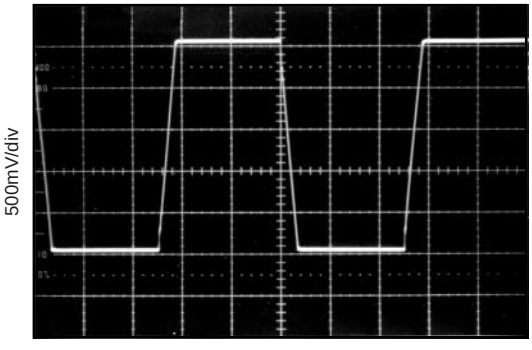
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 200pF, V_S = +5V



LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 620pF, V_S = +5V



APPLICATIONS INFORMATION

OPA336 series op amps are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 0.01µF ceramic capacitors. OPA336 series op amps are protected against reverse battery voltages.

OPERATING VOLTAGE

OPA336 series op amps can operate from a +2.1V to +5.5V single supply with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical characteristics. OPA336 series op amps are fully specified for operation from +2.3V to +5.5V; a single limit applies over the supply range. In addition, many parameters are ensured over the specified temperature range, –40°C to +85°C.

INPUT VOLTAGE

The input common-mode range of OPA336 series op amps extends from (V–) – 0.2V to (V+) – 1V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 300mV beyond the supplies. Thus, inputs greater than the input common-mode range but less than maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, the inputs may go beyond the power supplies without phase inversion, as shown in Figure 1, unlike some other op amps.

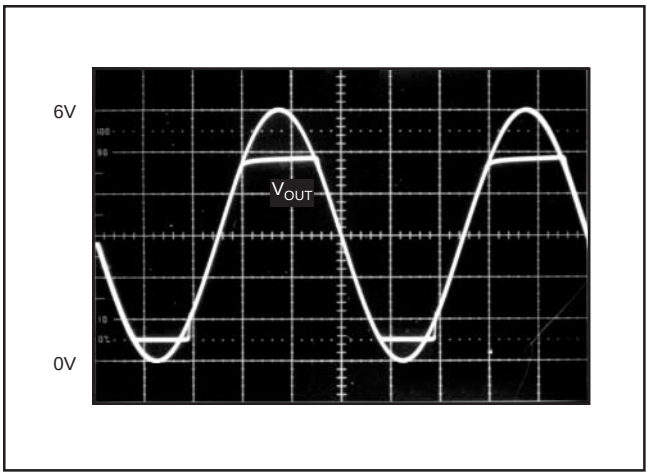


FIGURE 1. No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

Normally, input bias current is approximately 1pA. However, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated as long as the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 2.

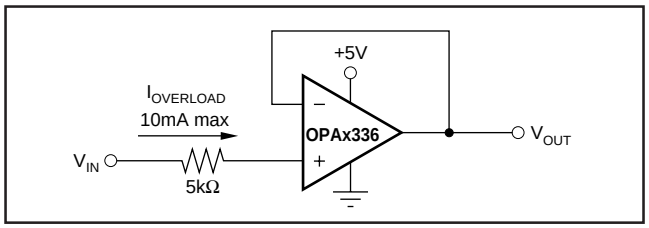


FIGURE 2. Input Current Protection for Voltages Exceeding the Supply Voltage.

CAPACITIVE LOAD AND STABILITY

OPA336 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op-amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

When properly configured, OPA336 series op amps can drive approximately 10,000pF. An op amp in unity-gain configuration is the most vulnerable to capacitive load. The capacitive load reacts with the op amp's output resistance, along with any additional load resistance, to create a pole in the response which degrades the phase margin. In unity gain, OPA336 series op amps perform well with a pure capacitive load up to about 300pF. Increasing gain enhances the amplifier's ability to drive loads beyond this level.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 50Ω to 100Ω resistor inside the feedback loop, as shown in Figure 3. This reduces ringing with large capacitive loads while maintaining DC

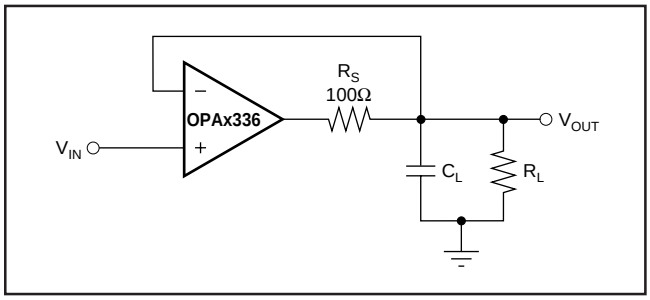


FIGURE 3. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

accuracy. For example, with R_L = 25kΩ, OPA336 series op amps perform well with capacitive loads in excess of 1000pF, as shown in Figure 4. Without R_S, capacitive load drive is typically 350pF for these conditions, as shown in Figure 5.

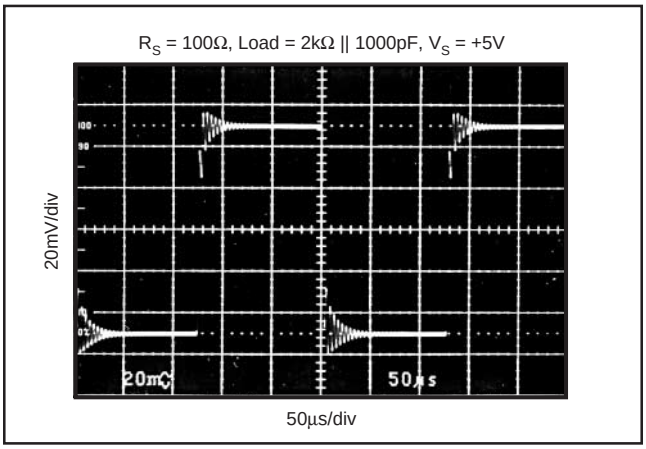


FIGURE 4. Small-Signal Step Response Using Series Resistor to Improve Capacitive Load Drive.

Alternatively, the resistor may be connected in series with the output outside of the feedback loop. However, if there is a resistive load parallel to the capacitive load, it and the series resistor create a voltage divider. This introduces a Direct Current (DC) error at the output; however, this error may be insignificant. For instance, with R_L = 100kΩ and R_S = 100Ω, there is only about a 0.1% error at the output.

Figure 5 shows the recommended operating regions for the OPA336. Decreasing the load resistance generally improves capacitive load drive. Figure 5 also illustrates how stability differs depending on where the resistive load is connected. With G = +1 and R_L = 10kΩ connected to V_S/2, the OPA336 can typically drive 500pF. Connecting the same load to ground improves capacitive load drive to 1000pF.

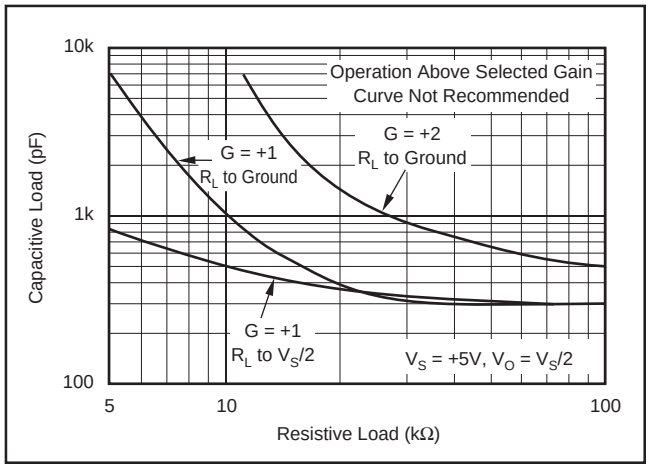


FIGURE 5. Stability—Capacitive Load vs Resistive Load.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2336E/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336E/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA336N/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/3KG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA336NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NJ/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336NJ/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA336UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA4336EA/250	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/250G4	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/2K5	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA336 :

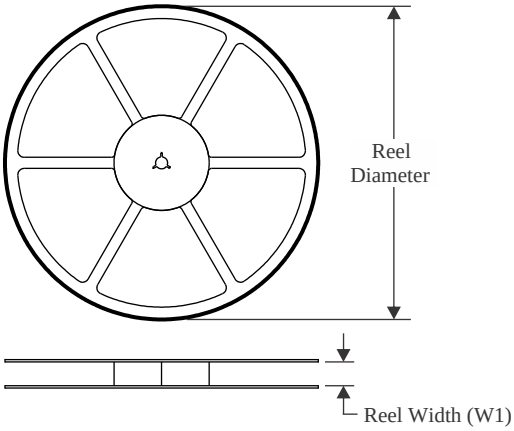
- Enhanced Product : OPA336-EP

NOTE: Qualified Version Definitions:

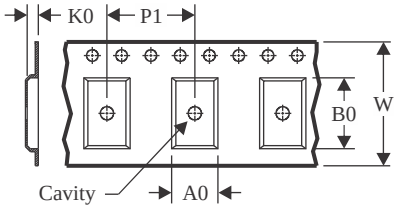
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

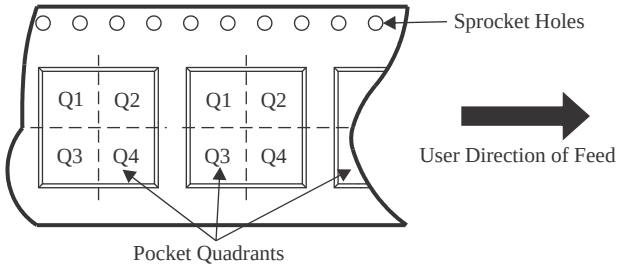


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

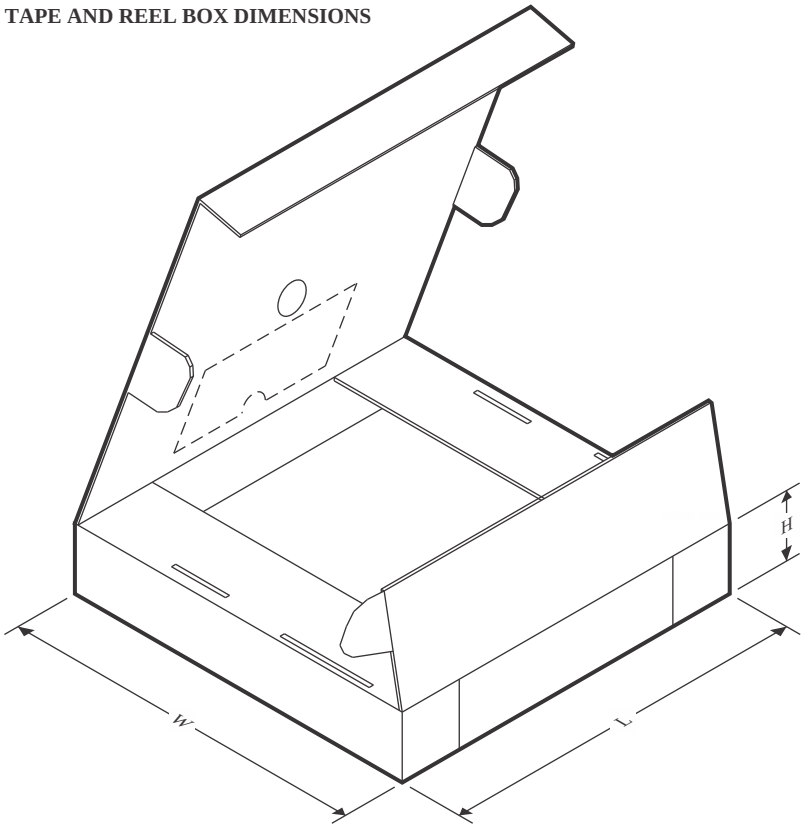
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2336U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2336UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA336N/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336N/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336N/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA336NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336NJ/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA336NJ/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336NJ/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA336UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4336EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4336EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

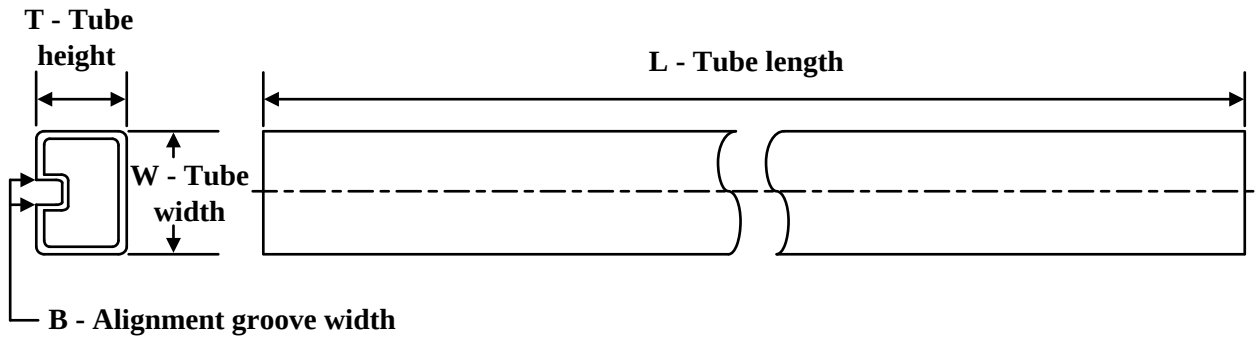
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2336U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2336UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA336N/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336N/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
OPA336N/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336NA/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
OPA336NJ/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336NJ/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336NJ/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA336UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4336EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4336EA/2K5	SSOP	DBQ	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

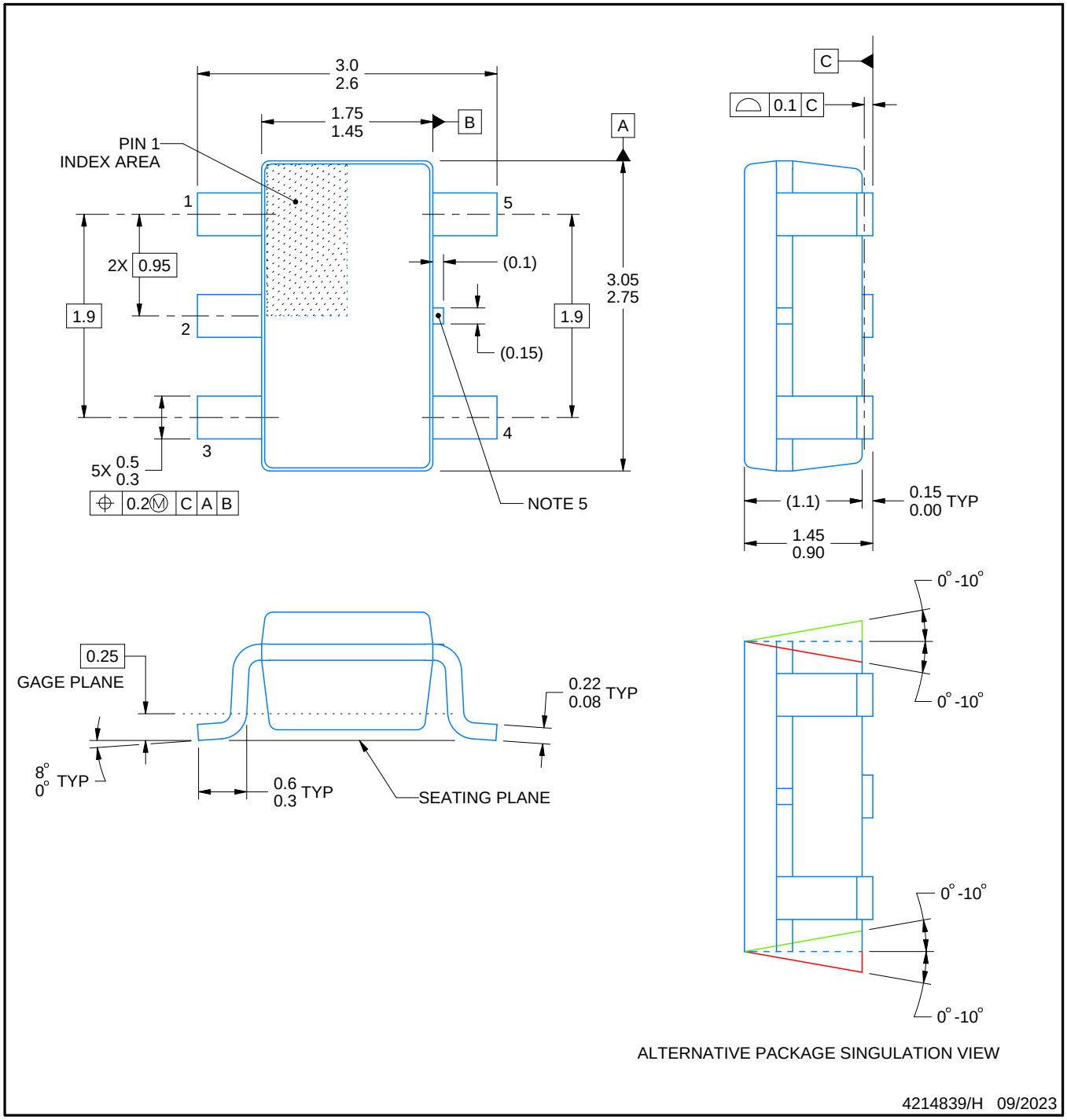
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2336U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2336UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2336UG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA336U	D	SOIC	8	75	506.6	8	3940	4.32
OPA336UA	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

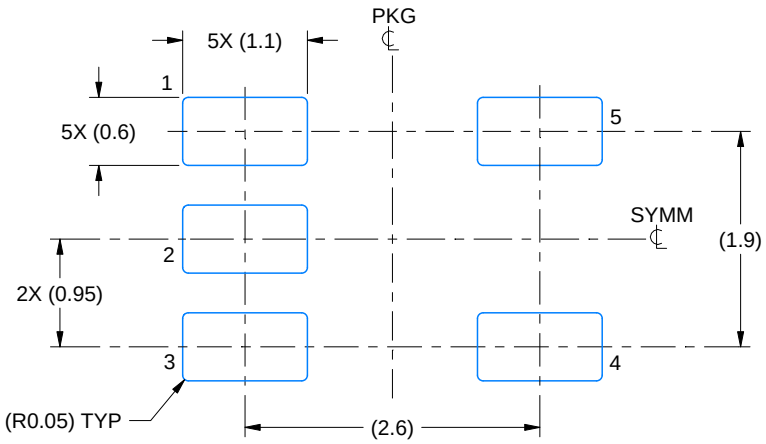


ALTERNATIVE PACKAGE SINGULATION VIEW

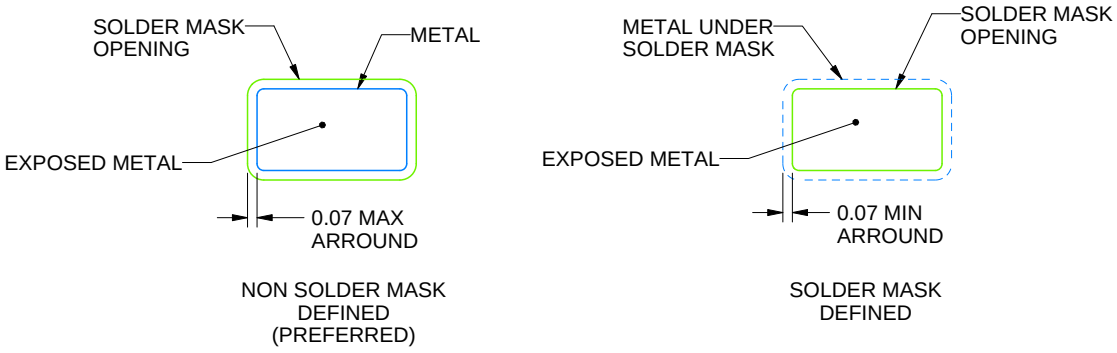
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

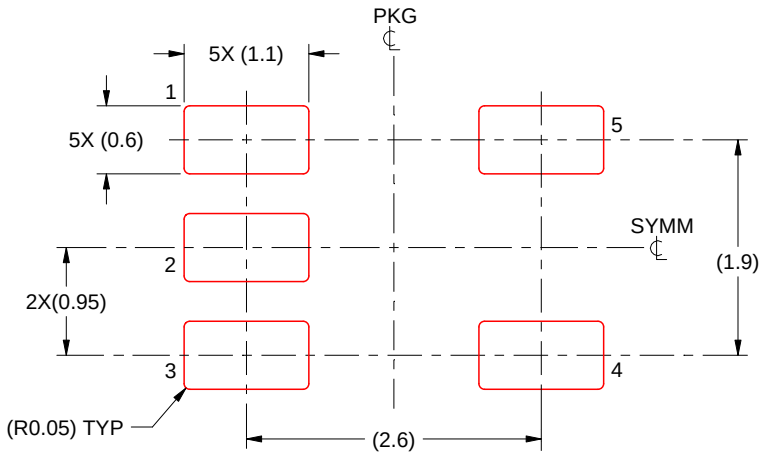


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

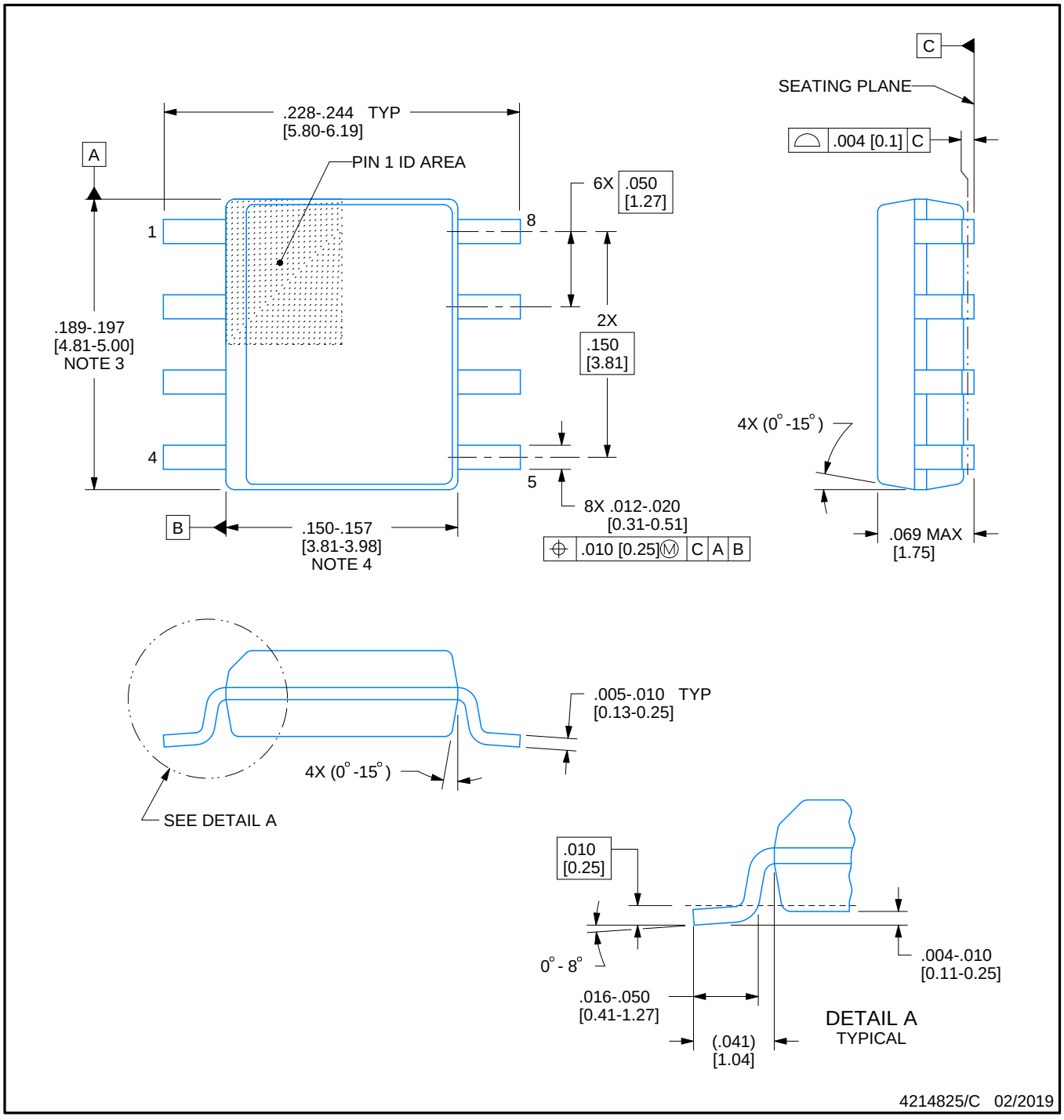
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0008A

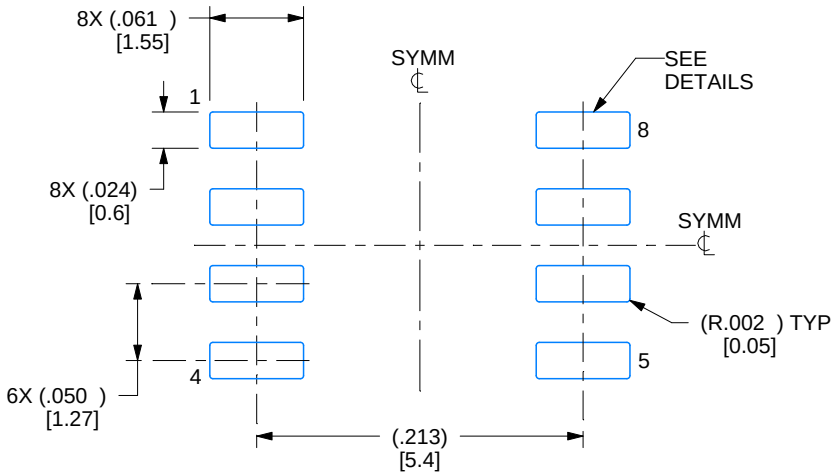
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

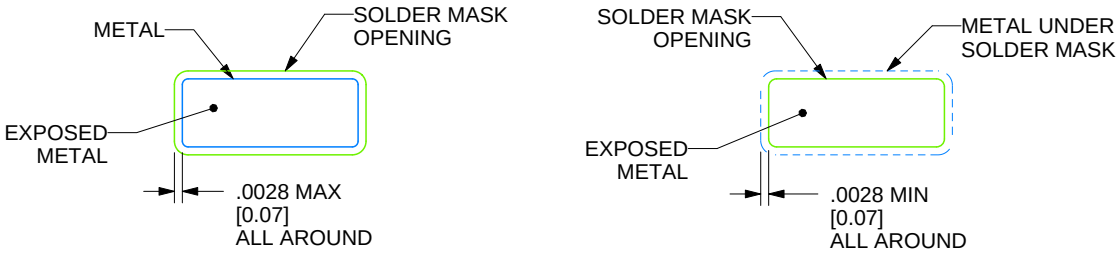


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

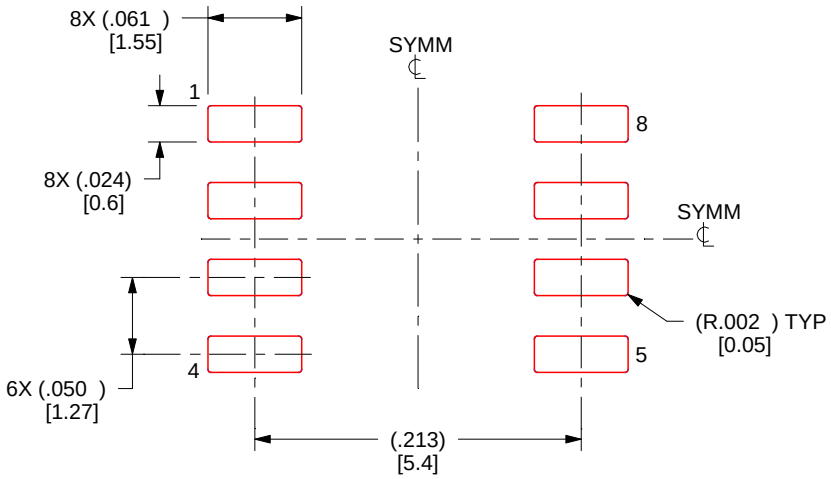
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

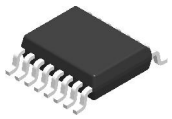


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

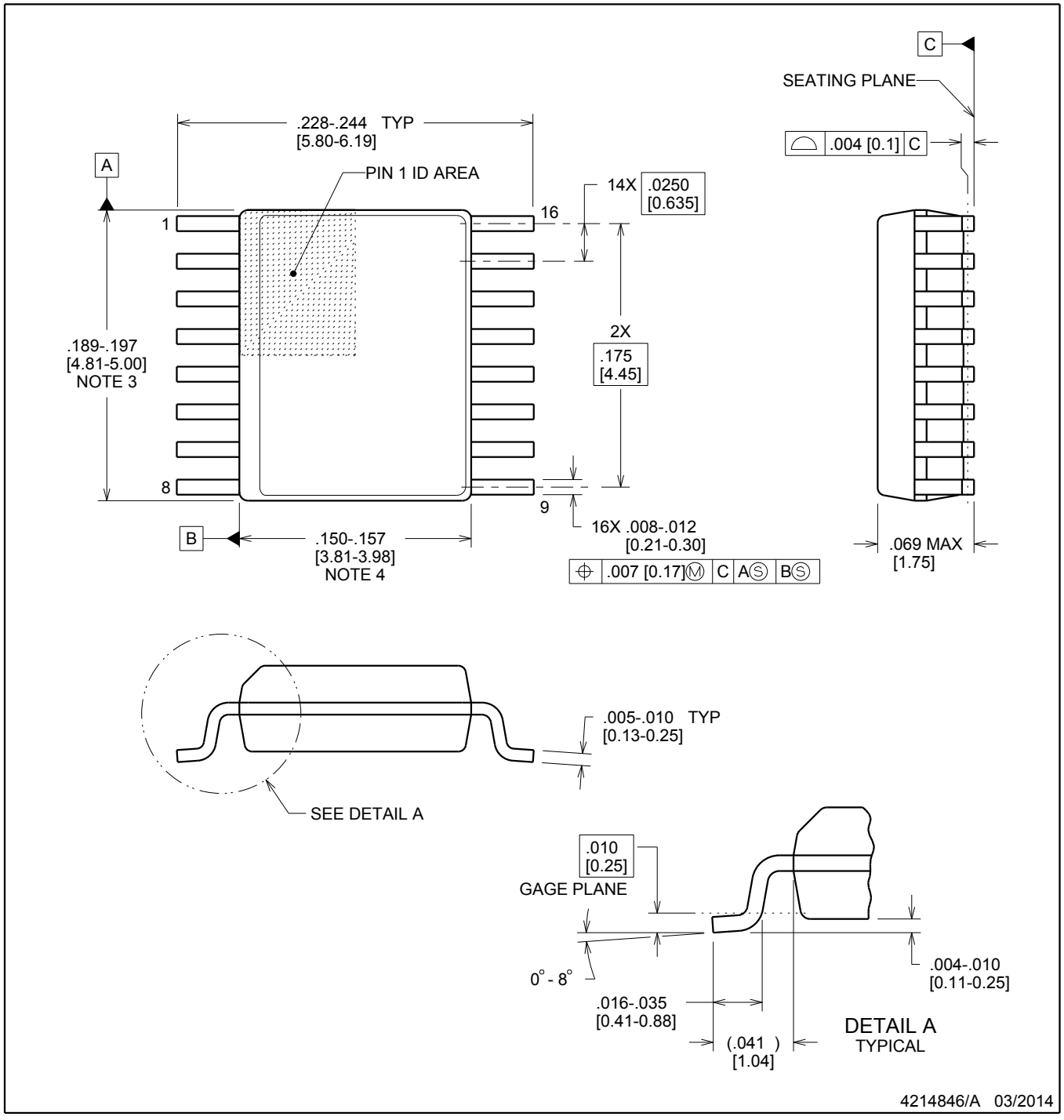


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

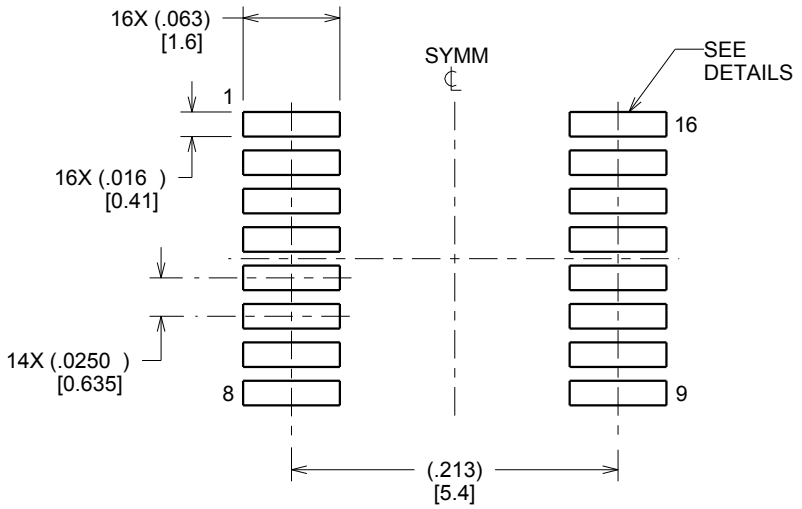
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

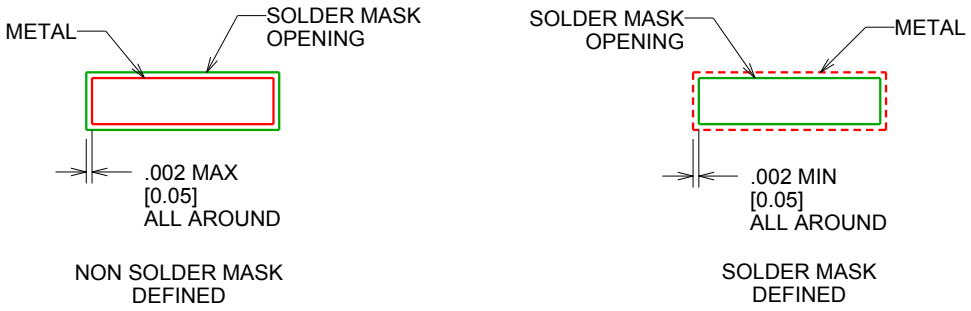
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

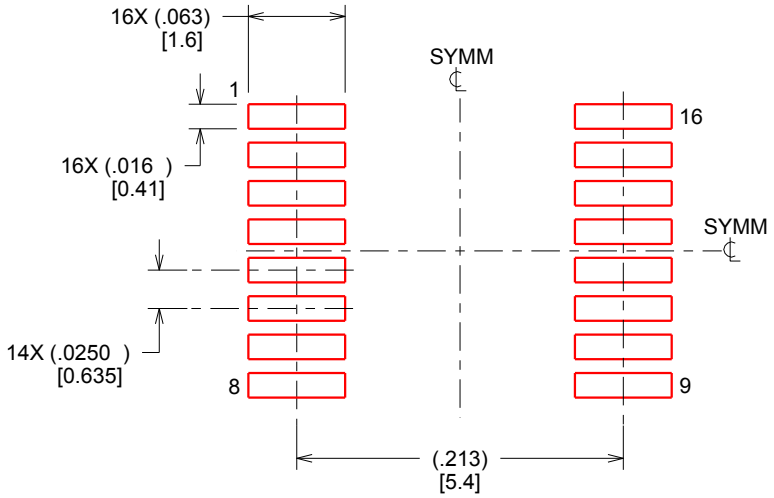
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



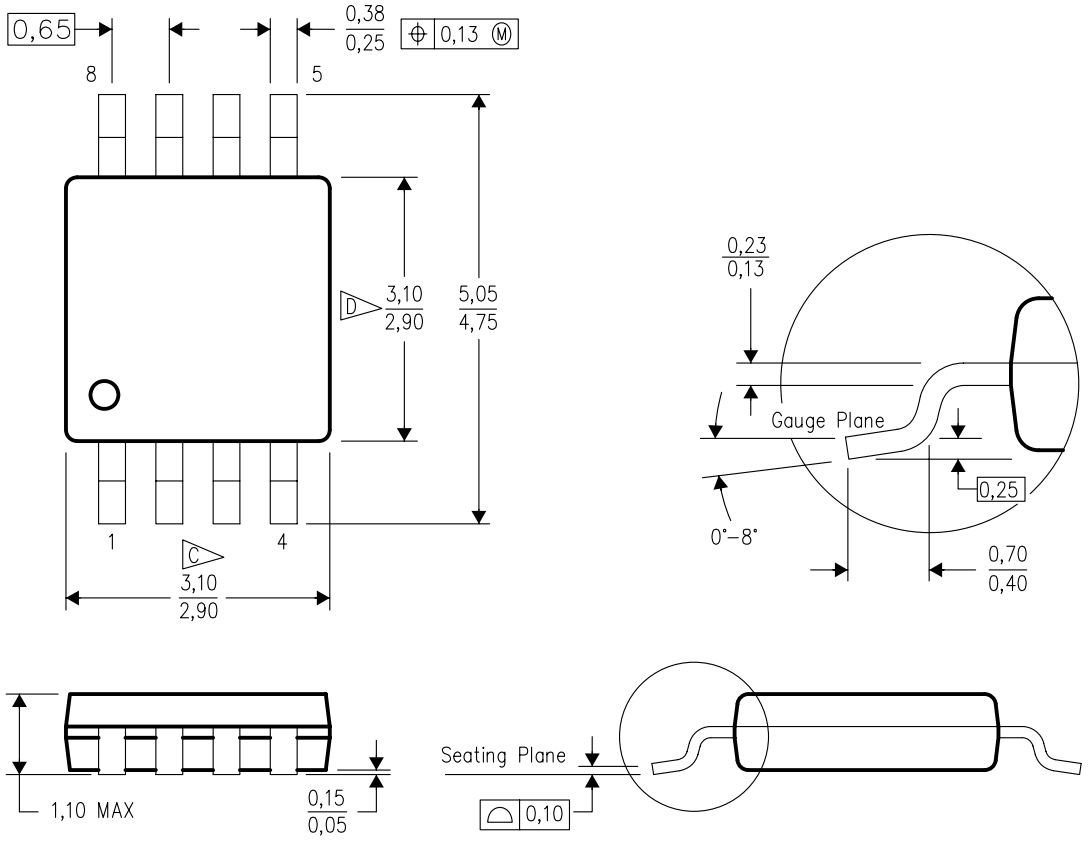
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

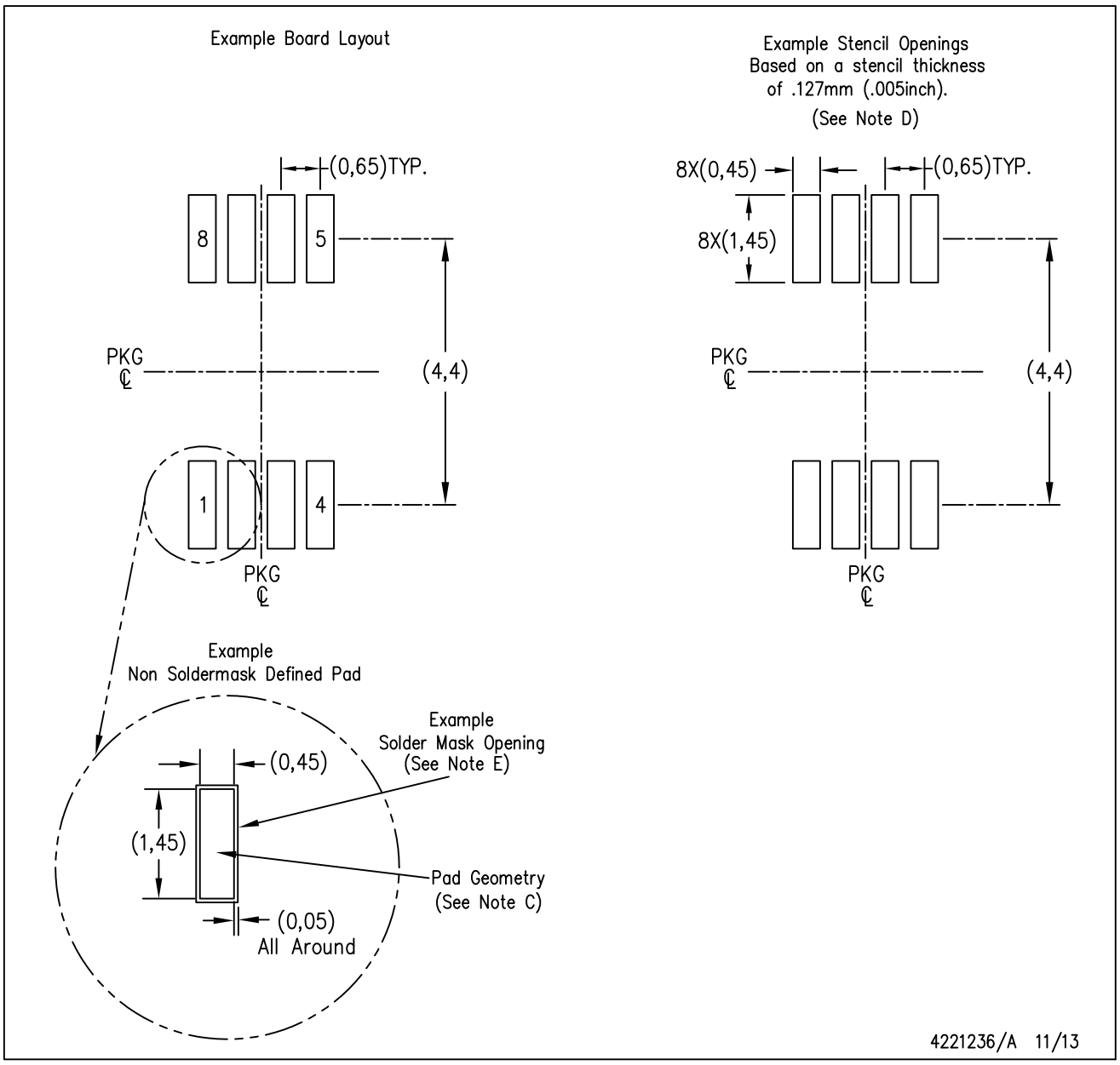
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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