具有 ±15kV IEC ESD 保护功能的 AM26LV32E 低电压高速四路差分线路接收器

1 特性

- 达到或超出 TIA/EIA-422-B 和 ITU Recommendation V.11 标准的要求
- 由 3.3V 单电源供电运行
- 开关频率高达 32MHz
- RS422 总线引脚的 ESD 保护（参阅 *ESD 等级*）
- 低功率损耗：27mW（典型值）
- 开路失效防护
- 具有 ±200mV 灵敏度的 ±7V 共模输入电压范围
- 接受 5V 逻辑输入及 3.3V 电源（使能输入）
- 输入迟滞：35 mV（典型值）
- 与 AM26C32、AM26LS32 引脚兼容
- I_{off} 支持局部断电模式运行

2 应用

- 高可靠性汽车应用
- 配置控制和打印支持
- ATM 和点钞机
- 智能电网
- 交流和伺服电机驱动器

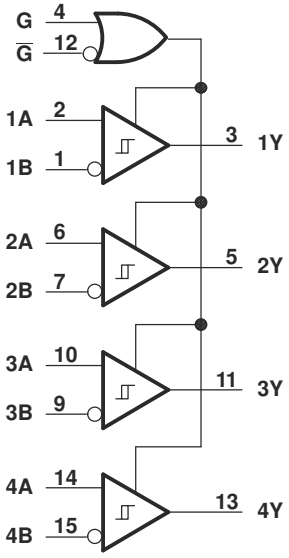
3 说明

AM26LV32E 器件由四个差分线路接收器组成，且具有三态输出。该器件旨在以较小的电源电压满足 TIA/EIA-422-B 和 ITU Recommendation V.11 驱动器的要求。这款器件经过优化，可在高达 32MHz 的开关速率下实现平衡总线传输。通过三态输出，该器件可直接连接至总线组织式系统。AM26LV32E 具有失效防护电路，该电路可防止该器件在接收器输出端放置未知电压信号。在开路失效防护中，会在相应的输出端产生高电平状态。该器件支持使用 I_{off} 的局部断电应用。I_{off} 电路可禁用输出，以防在器件断电时电流回流对器件造成损坏。

封装信息

器件型号	封装(1)	封装尺寸(2)
AM26LV32E	SO (16)	10.2mm × 7.8mm
	SOIC (16)	9.9mm x 6mm
	VQFN (16)	4mm x 3.5mm
	TSSOP (16)	5mm x 6.4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (December 2020) to Revision E (August 2023) — **Page**

- 将“器件信息”表更改为*封装信息* 表 1
- Changed the *Thermal Information* 5
- Changed the *Typical Characteristics* 6

Changes from Revision C (July 2018) to Revision D (December 2020) — **Page**

- 将“特性”从*开路、短路及终止失效防护* 更改为*开路失效防护* 1
- 删除了“说明”中的文本：*短路失效防护和终止失效防护* , 更改为*开路失效防护* 1
- Deleted text from the last paragraph in Input Fail-Safe Circuitry: *terminated or short* 8
- Deleted text from 表 8-1: *shorted, or terminated* 9

Changes from Revision B (July 2015) to Revision C (July 2018) — **Page**

- Changed the pinout image appearance 3
- Changed the A and B Input signals on the waveform of 图 7-1 7

Changes from Revision A (May 2008) to Revision B (July 2015) — **Page**

- 添加了*“引脚配置和功能”部分、“ESD 等级”表、“特性说明”部分、“器件功能模式”、“应用和实施”部分、“电源相关建议”部分、“布局”部分、“器件和文档支持”部分以及“机械、封装和可订购信息”部分* 1

5 Pin Configuration and Functions

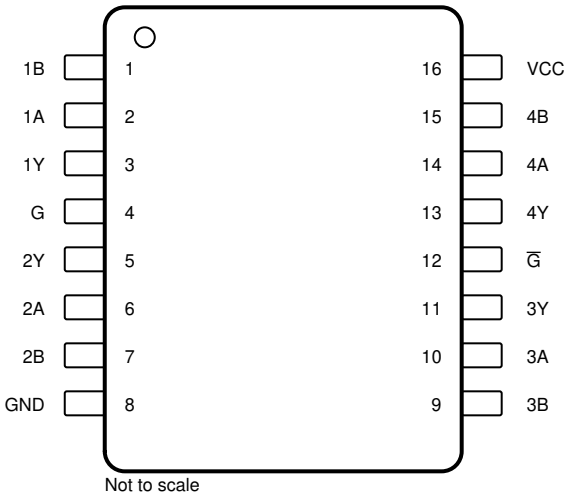


图 5-1. D, NS, or PW Package, 16-Pin SOIC, SO, or TSSOP (Top View)

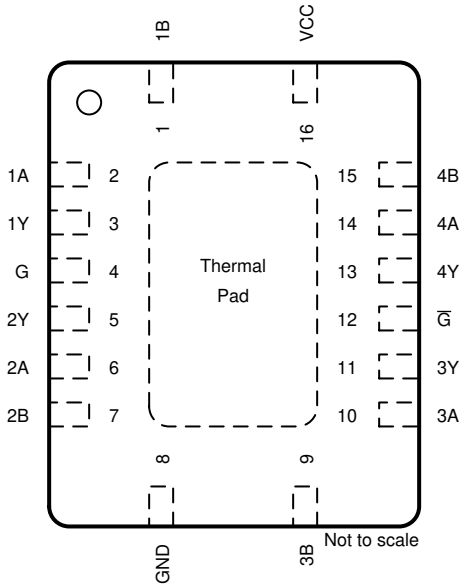


图 5-2. RGY Package 16-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	2	I	RS422/RS485 differential input (noninverting)
1B	1	I	RS422/RS485 differential input (inverting)
1Y	3	O	Logic level output
2A	6	I	RS422/RS485 differential input (noninverting)
2B	7	I	RS422/RS485 differential input (inverting)
2Y	5	O	Logic level output
3A	10	I	RS422/RS485 differential input (noninverting)
3B	9	I	RS422/RS485 differential input (inverting)
3Y	11	O	Logic level output
4A	14	I	RS422/RS485 differential input (noninverting)
4B	15	I	RS422/RS485 differential input (inverting)
4Y	13	O	Logic level output
G	4	I	Active-high select
$\overline{G}$	12	I	Active-low select
GND	8	—	Ground
V_{CC}	16	—	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		-0.5	6	V
V_I	Input voltage	A or B inputs	–14	14	V
		G or $\overline{G}$ inputs	–0.5	6	
V_{ID}	Differential input voltage(4)		–14	14	V
V_O	Output voltage		–0.5	6	V
I_O	Output current			±20	mA
I_{IK}	Input clamp current	$V_I < 0$		-20	mA
I_{OK}	Output clamp current	$V_O < 0$		-20	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.
(3) This device is designed to meet TIA/EIA-422-B and ITU.
(4) Differential input voltage is measured at the non-inverting input with respect to the corresponding inverting input.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		IEC61000-4-2, Contact Gap Discharge	±8000	
		IEC61000-4-2, Air Gap Discharge	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±15000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IC}	Common-mode input voltage	–7		7	V
V_{ID}	Differential input voltage	–7		7	V
I_{OH}	High-level output current			–5	mA
I_{OL}	Low-level output current			5	mA
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		AM26LV32E								UNIT
		D (SOIC)	DR (SOIC-Reel)	PW (TSSOP)	PWR (TSSOP-Reel)	NS (SOP)	NSR (SOP-Reel)	RGY (VQFN)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.1	84.6	109	107.5	69	88.5	92	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	43.5	34	38.4	34	46.2	40	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	43.2	N/A	53.7	N/A	50.7	N/A	24.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	10.4	N/A	3.2	N/A	13.5	N/A	2.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	42.8	N/A	53.1	N/A	50.3	N/A	24.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	N/A	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended ranges of common-mode input, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input					0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input			−0.2			V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)				35		mV
V_{IK}	Input clamp voltage, G and $\overline{G}$	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −5 mA		2.4	3.2		V
		V_{ID} = 200 mV, I_{OH} = −100 μA		V_{CC} − 0.1			
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 5 mA			0.17	0.5	V
		V_{ID} = −200 mV, I_{OL} = 100 μA				0.1	
I_{OZ}	High-impedance state output current	V_O = V_{CC} or GND				±50	μA
I_{off}	Output current with power off	V_{CC} = 0 V, V_O = 0 or 5.5 V				±100	μA
I_I	Line input current	Other input at 0 V	V_I = 10 V			1.5	mA
			V_I = −10 V			−2.5	
I_I	Enable input current, G and $\overline{G}$	V_I = V_{CC} or GND				±1	μA
r_i	Input resistance	V_{IC} = −7 V to 7 V, Other input at 0 V		4	17		kΩ
I_{CC}	Supply current (total package)	G, $\overline{G}$ = V_{CC} or GND, No load, Line inputs open			8	17	mA
C_{pd}	Power dissipation capacitance	One channel			150		pF

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 图 7-1	8	16	26	ns
t_{PHL}	Propagation delay time, high- to low-level output		8	16	26	ns
t_t	Transition time	See 图 7-1		5		ns
t_{PZH}	Output-enable time to high-level	See 图 7-2		17	40	ns
t_{PZL}	Output-enable time to low-level	See 图 7-2		10	40	ns
t_{PHZ}	Output-disable time from high-level	See 图 7-2		20	40	ns
t_{PLZ}	Output-disable time from low-level	See 图 7-2		16	40	ns
$t_{sk(p)}$	Pulse skew	See 图 7-1 图 7-2		4	6	ns
$t_{sk(o)}$	Pulse skew	See 图 7-1 图 7-2		4	6	ns
$t_{sk(pp)}$	Pulse skew (device to device)	See 图 7-1 图 7-2		6	9	ns
$f_{(max)}$	Maximum operating frequency	See 图 7-1		32		MHz

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.7 Typical Characteristics

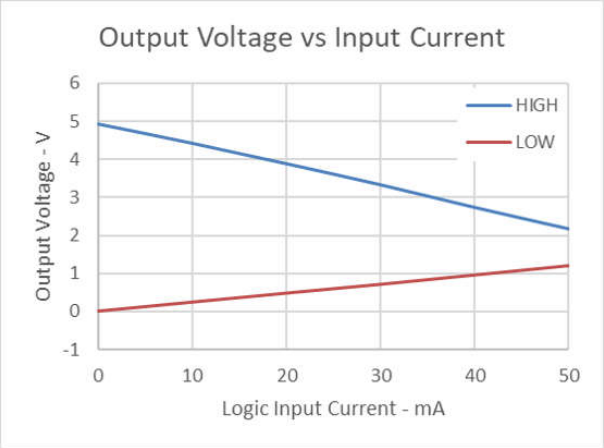
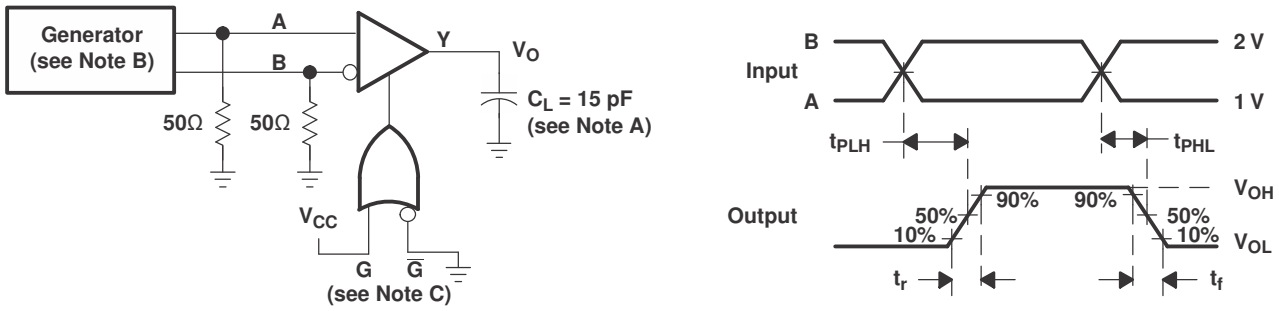


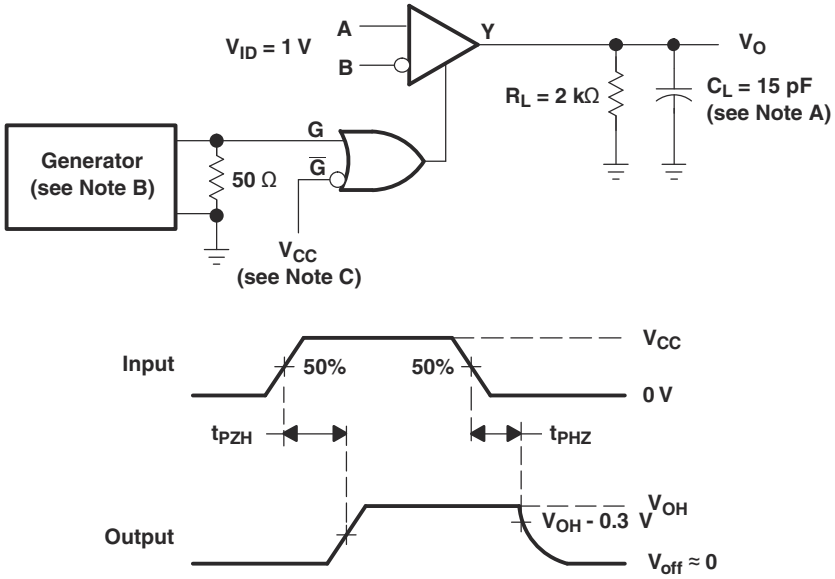
图 6-1. Output Voltage vs Input Current

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

图 7-1. Switching Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ⩽ 50%, $t_r = t_f = 6$ ns.

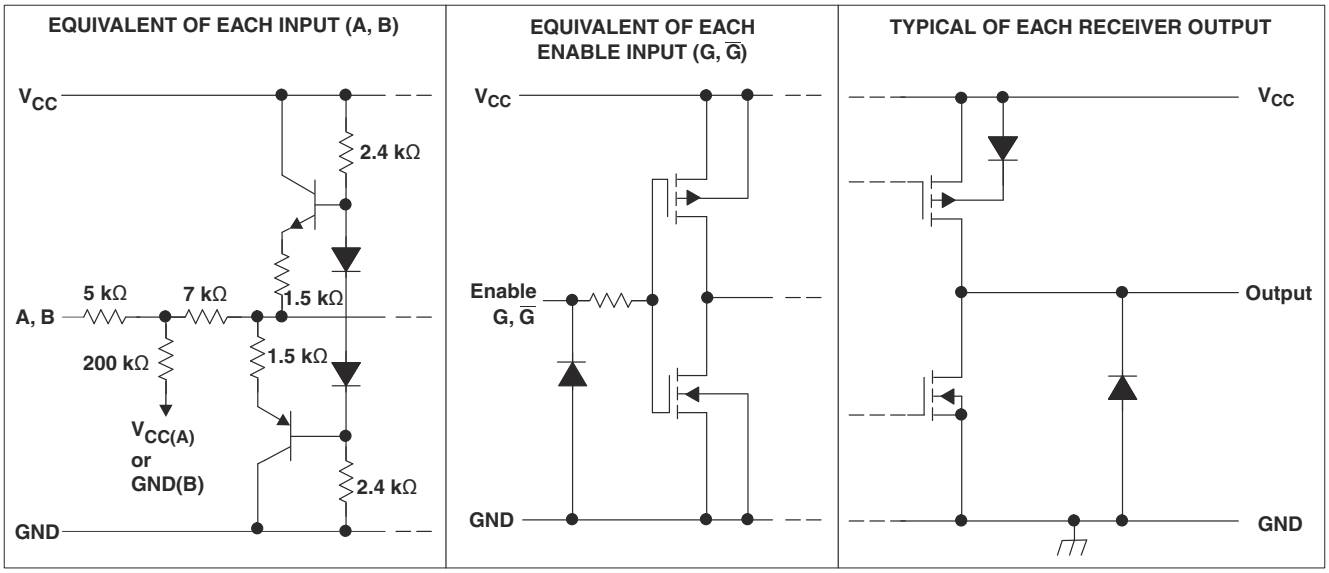
图 7-2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

8 Detailed Description

8.1 Overview

The AM26LV32E is a low-voltage, quadruple-differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low power or low voltage MCU to interface with heavy machinery, subsystems and other devices through long wires of up to 1000 m, giving any design a reliable and easy to use connection. As with any RS422 interface, the AM26LV32E works in a differential voltage range, which enables very good signal integrity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ±7-V Common-Mode Range With ±200-mV Sensitivity

For a common-mode voltage varying from –7 V to 7 V, the input voltage is acceptable in low ranges greater than 200 mV as a standard.

8.3.2 Input Fail-Safe Circuitry

RS-485 specifies that the receiver output state should be logic high for differential input voltages of $V_{AB} \geq +200$ mV and logic low for $V_{AB} \leq -200$ mV. For input voltages in between these limits, a receiver's output state is not defined and can randomly assume high or low. Removing the uncertainty of random output states, modern transceiver designs include internal biasing circuits that put the receiver output into a defined state (typically high) in the absence of a valid input signal. A loss of input signal can be caused by:

- an open circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus
- a short circuit due to an insulation fault, connecting both conductors of a differential pair to one another
- an idle bus when none of the bus transceivers are active.

An open circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus. The AM26LV32E has an internal circuit that ensures functionality during an open failure.

8.3.3 Active-High and Active-Low

The device can be configure using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin, allows the device to operate on an active-high and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

表 8-1. Function Table (Each Driver)

DIFFERENTIAL INPUT	ENABLES(1)		OUTPUT
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
Open	H	X	H
	X	L	H
X	L	H	Z

(1) H = high-level, L = low-level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

9 Application Information Disclaimer

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, ac termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and, indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31E and AM26LV32E, respectively, were tested at room temperature with a 3.3-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

9.2 Typical Application

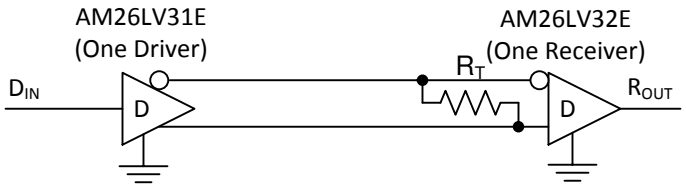


图 9-1. Differential Terminated Configuration

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, R_{OUT} , of the cable and can vary from about 80 Ω to 120 Ω.

9.2.2 Detailed Design Procedure

图 9-1 shows a configuration with R_T as termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS-422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

9.2.3 Application Curve

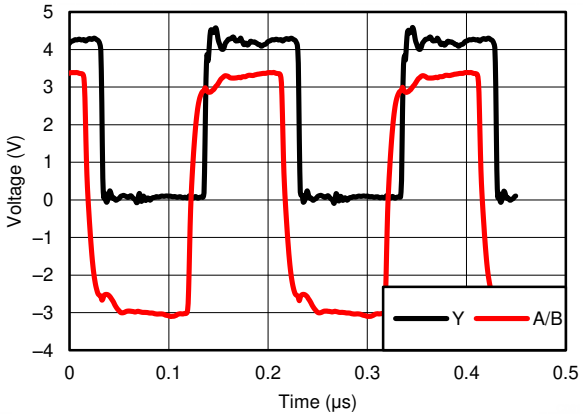


图 9-2. Differential 120-Ω Terminated Output Waveforms (CAT 5E Cable)

10 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- µ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

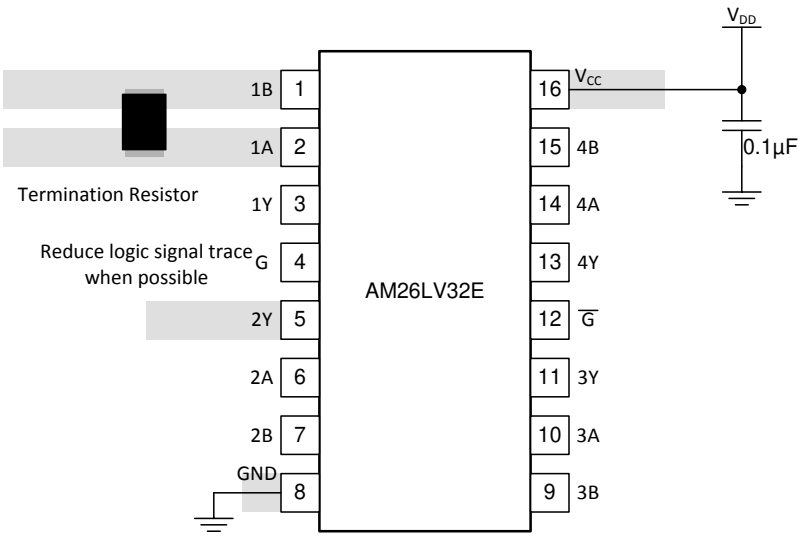


图 11-1. Trace Layout on PCB and Recommendations

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV32EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32EI	Samples
AM26LV32EIDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32EI	Samples
AM26LV32EINSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32EI	Samples
AM26LV32EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32	Samples
AM26LV32EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB32	Samples
AM26LV32EIRGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SB32	Samples
AM26LV32EIRGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SB32	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM26LV32E :

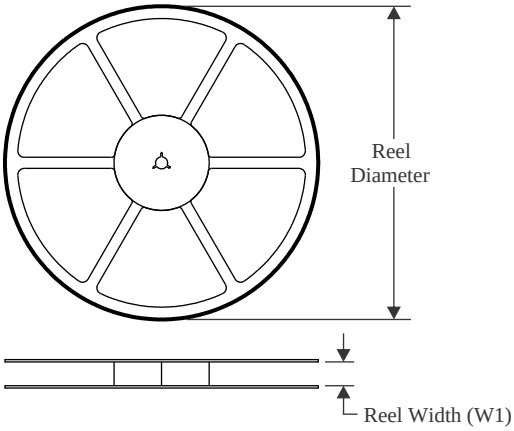
- Enhanced Product : AM26LV32E-EP

NOTE: Qualified Version Definitions:

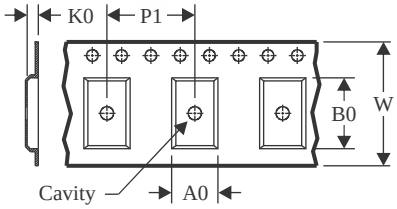
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

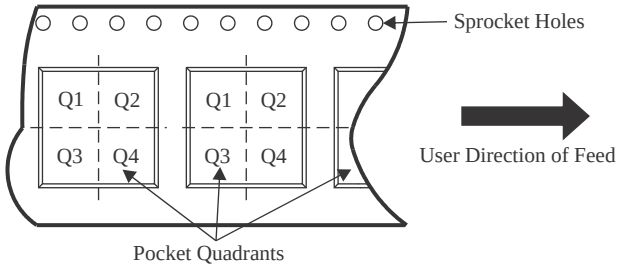


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

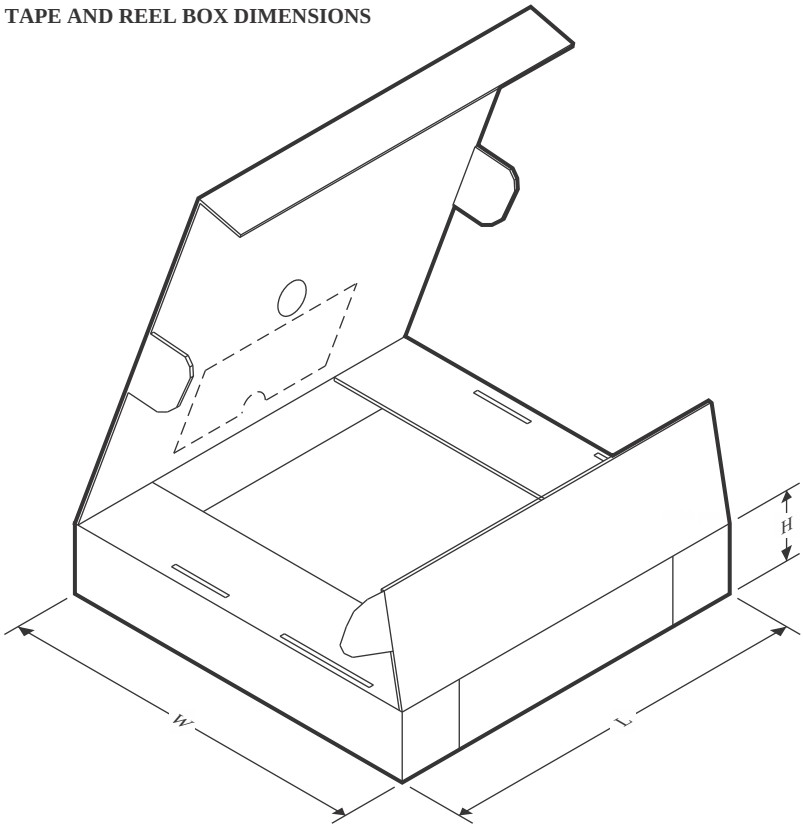
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV32EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32EINSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV32EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV32EIRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

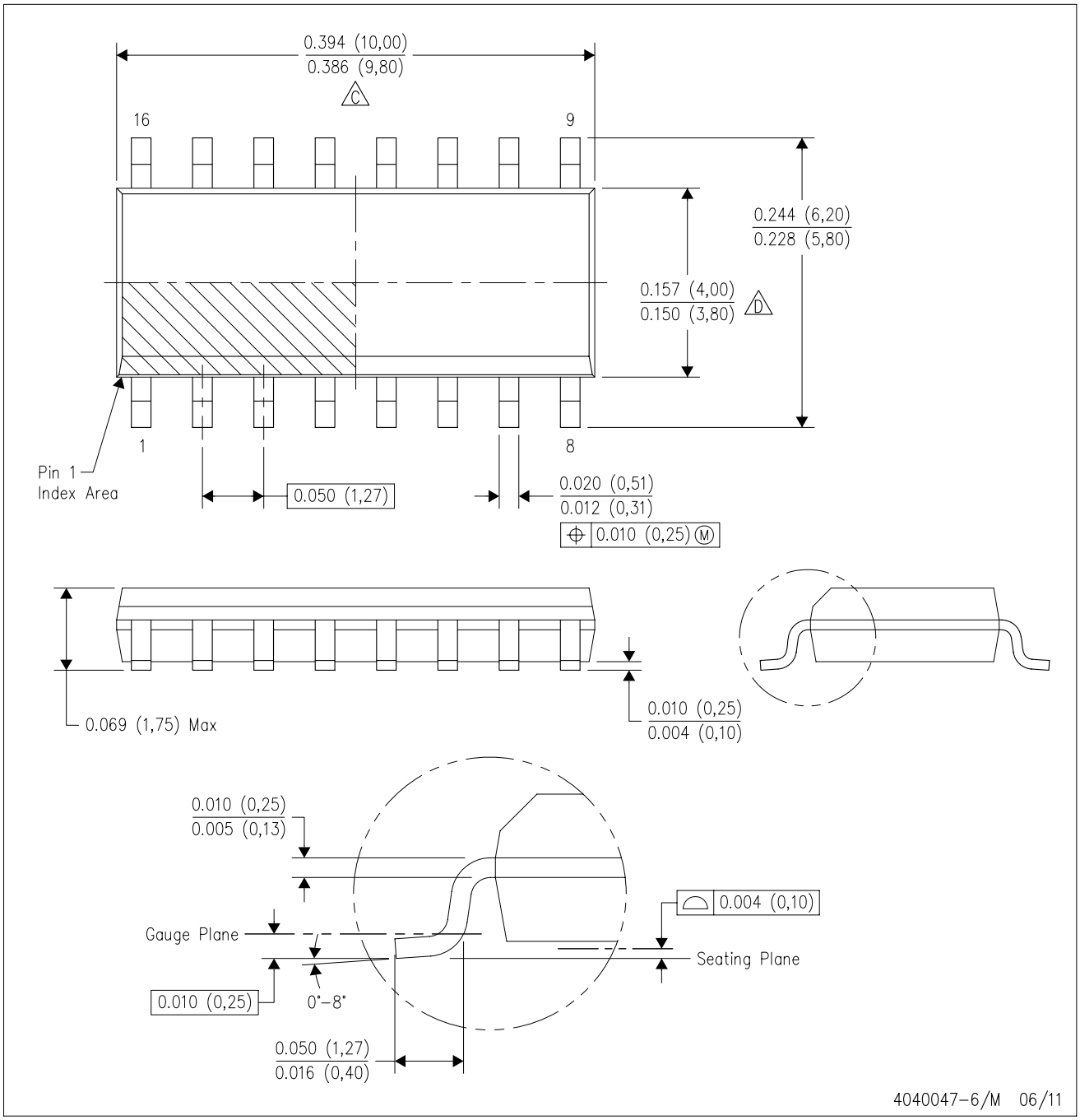
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV32EIDR	SOIC	D	16	2500	356.0	356.0	35.0
AM26LV32EINSR	SO	NS	16	2000	356.0	356.0	35.0
AM26LV32EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26LV32EIRGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



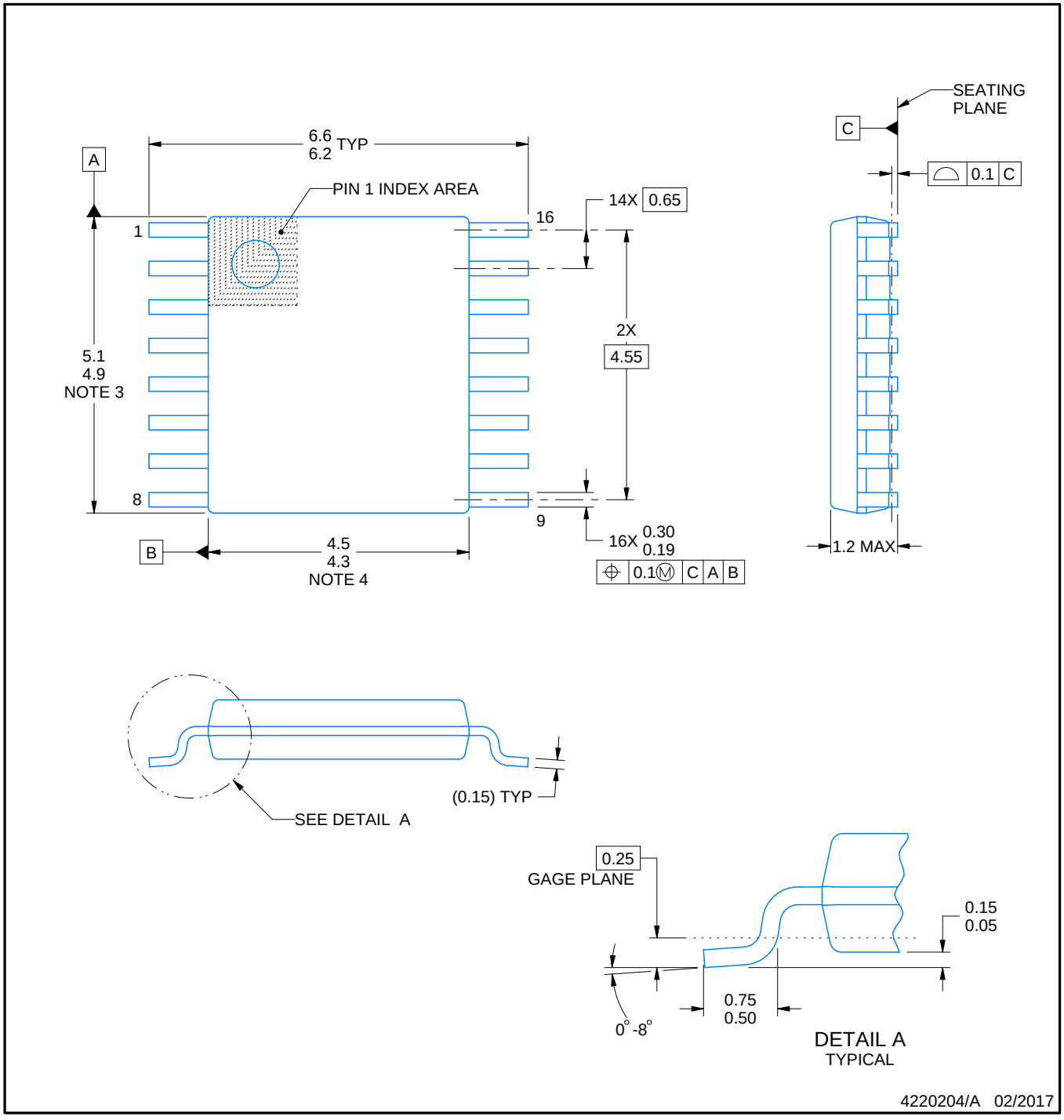
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

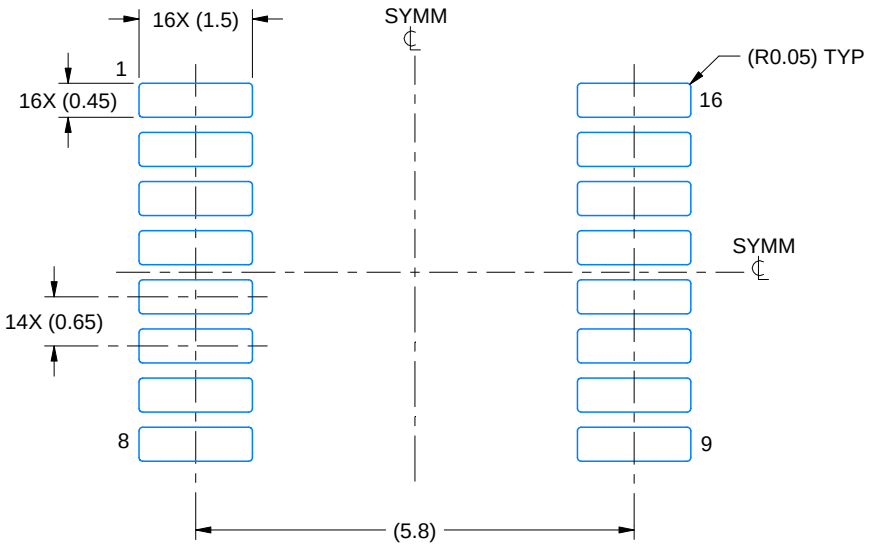
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

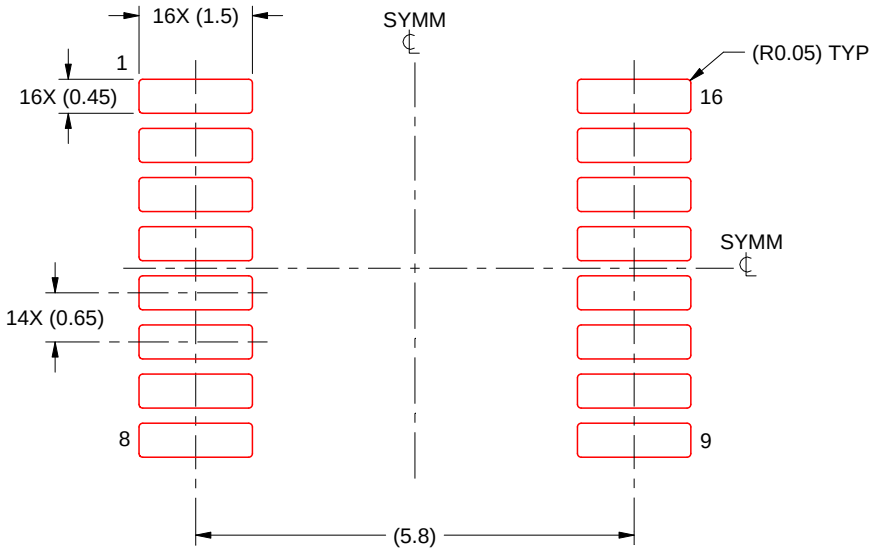
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

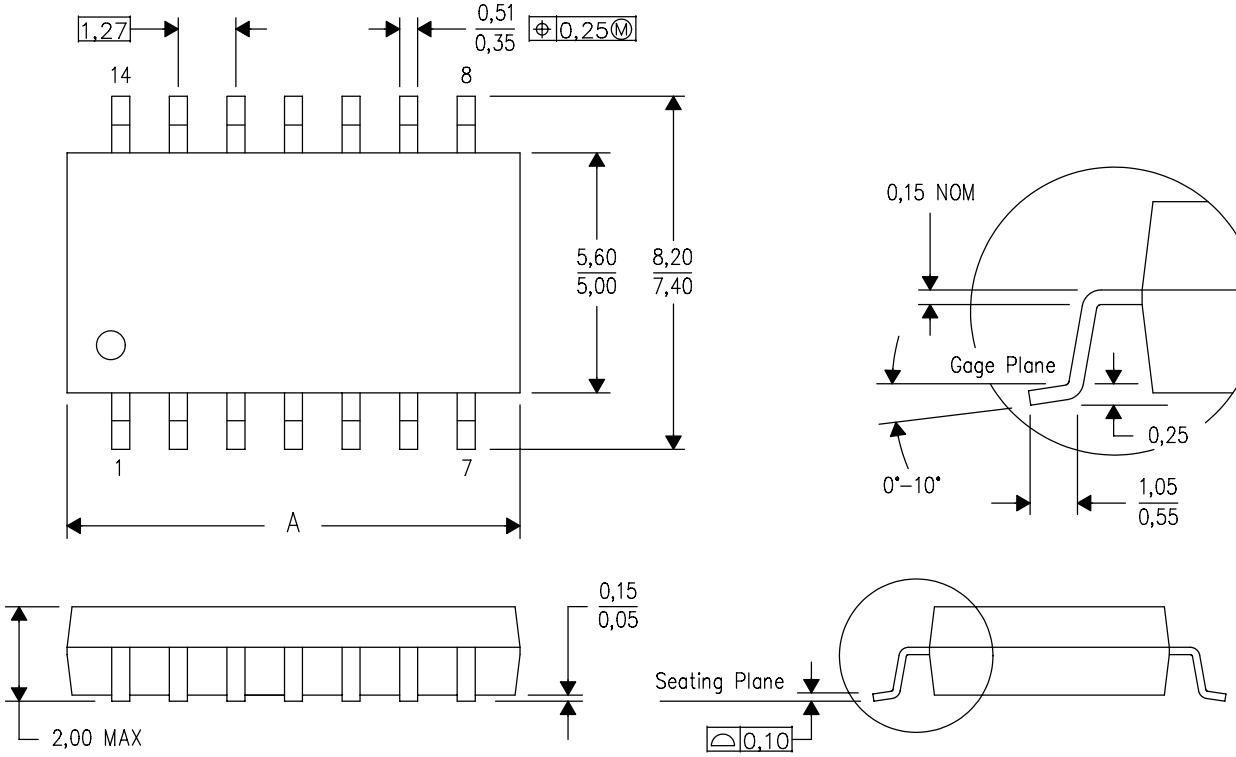
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

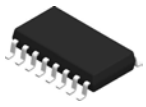
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

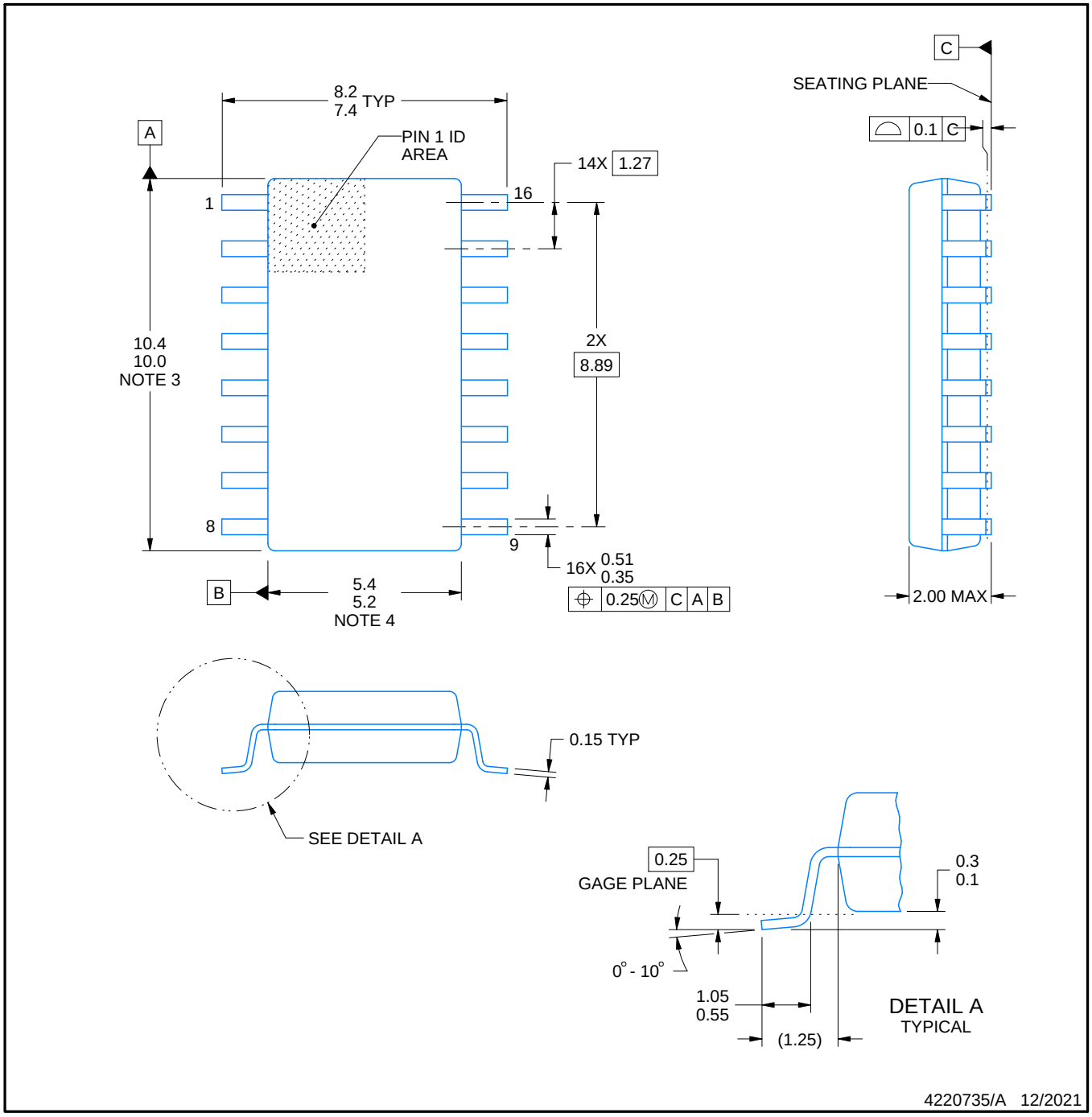


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

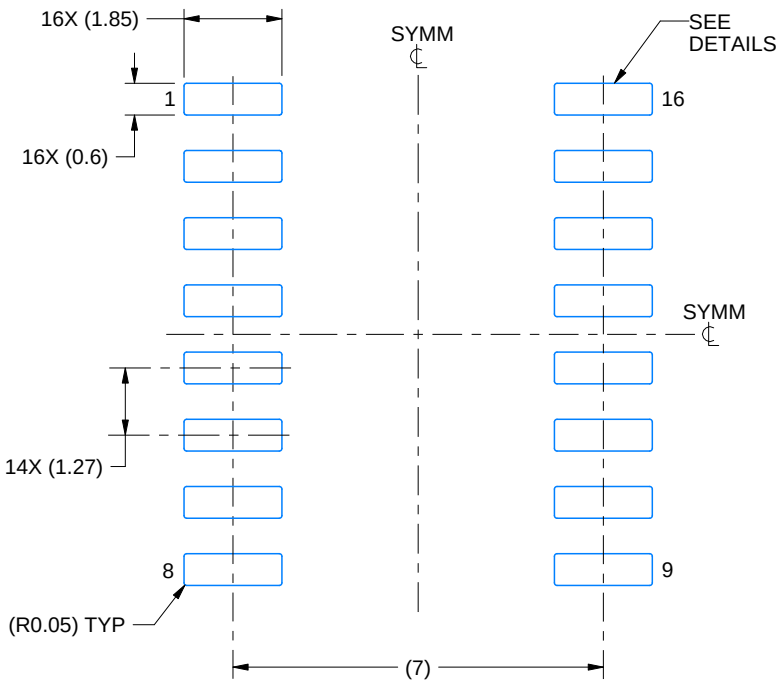
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

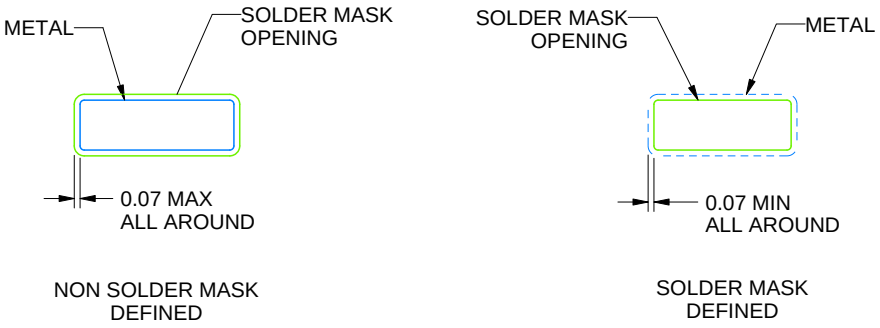
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

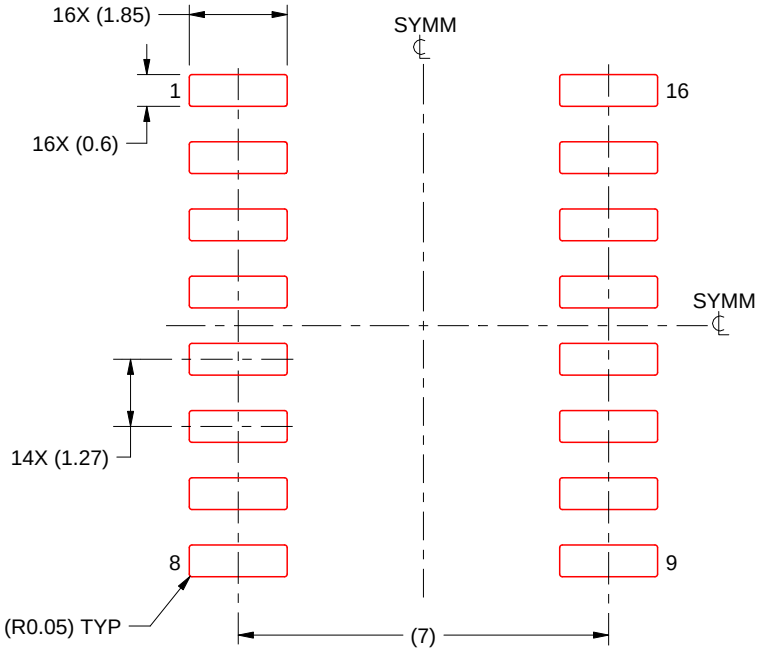
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



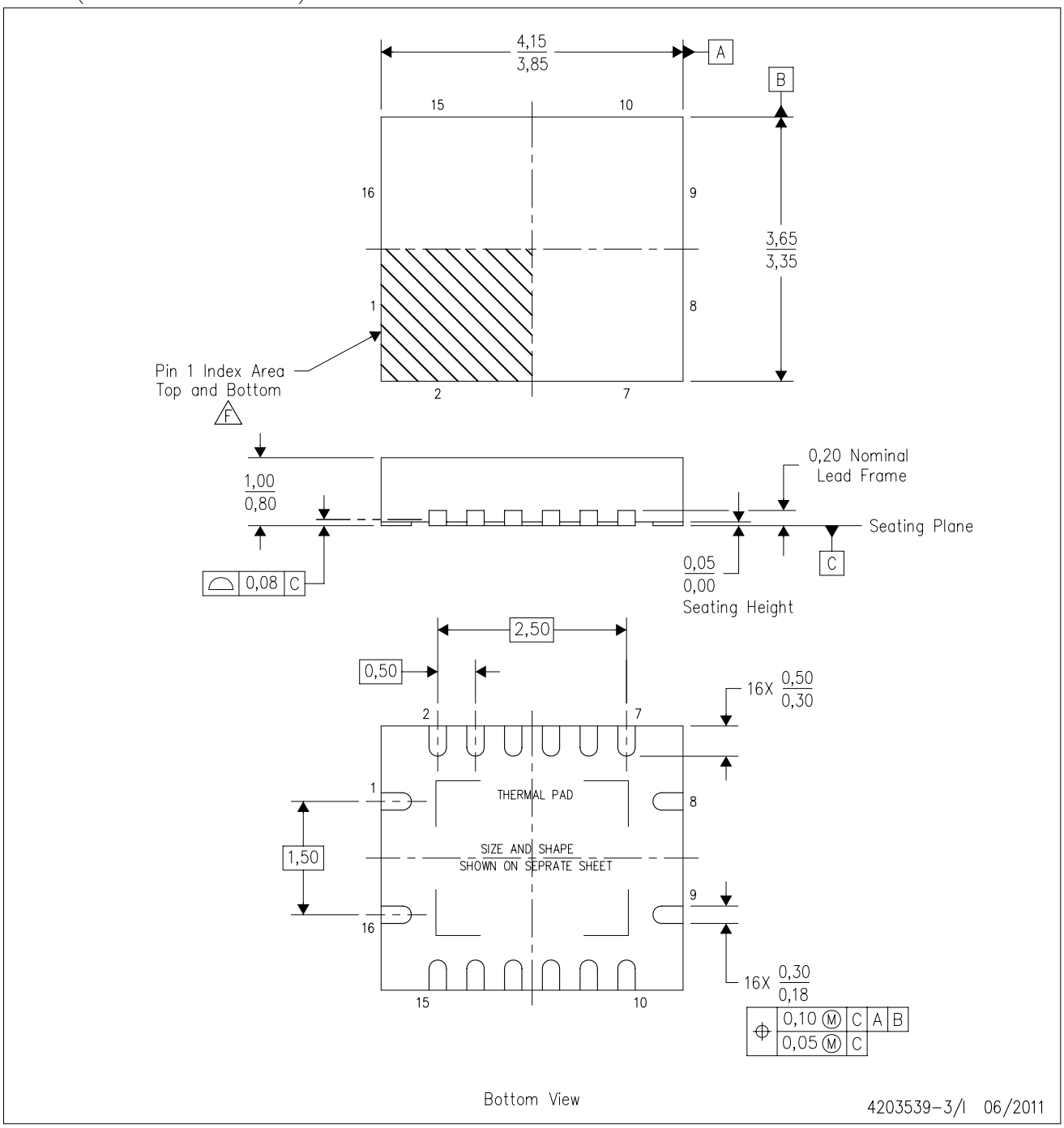
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

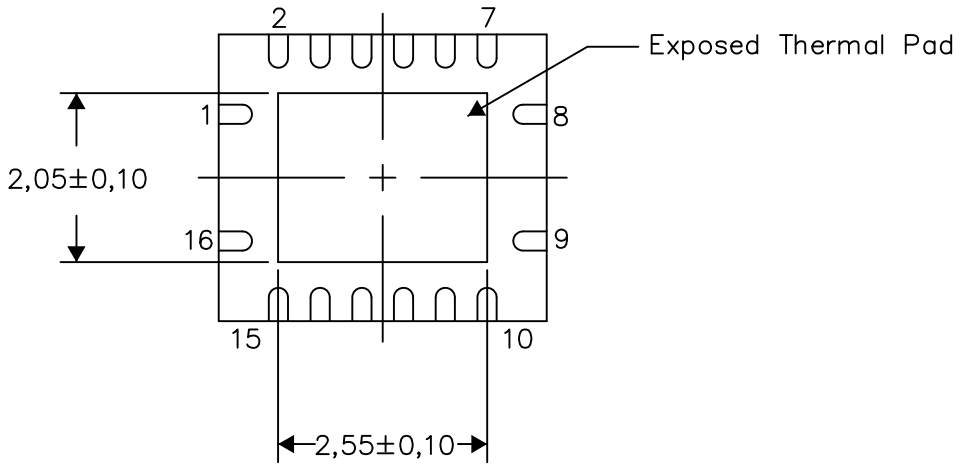
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



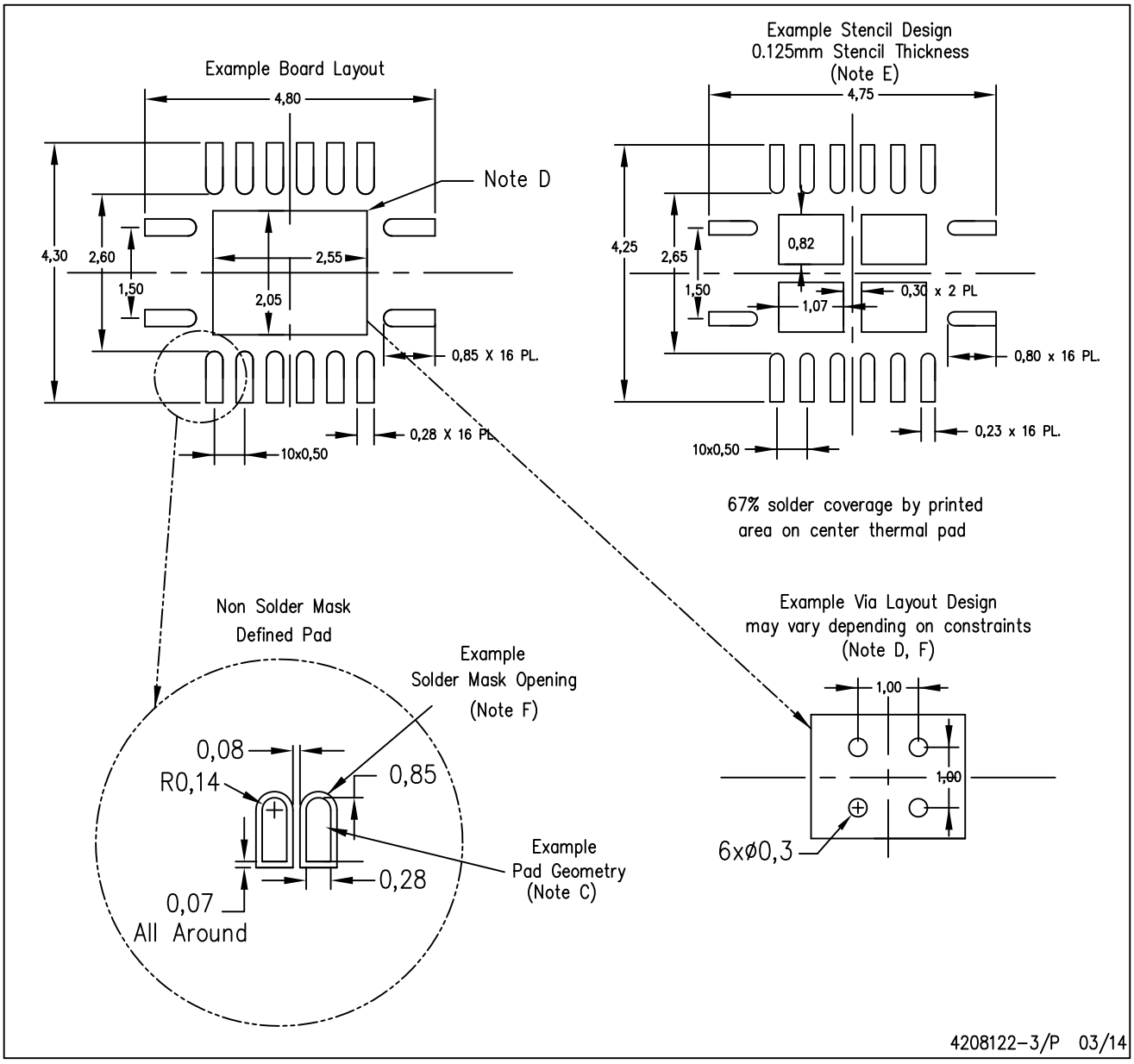
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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