TPS92515x 集成有 N 沟道 FET、高侧电流感测和分流 FET PWM 调光功能的 2A 降压 LED 驱动器

1 特性

- 符合 AEC-Q100 1 级标准
- 集成 290mΩ（典型值）内部 N 沟道场效应晶体管 (FET)
- 输入电压范围：
  - TPS92515x：5.5V 至 42V
  - TPS92515HVx：5.5V 至 65V
  - 启动后工作电压低至 5.15V
- 低偏移高侧峰值电流比较器
- 高达 2A 的恒定平均电流
- 固有逐周期电流限制
- 多种调光方法
  - 10,000:1 分流脉宽调制 (PWM) 调光范围
  - 1000:1 PWM 调光范围
  - 200:1 模拟调光范围
- 简单的恒定关断时间控制
  - 无环路补偿
  - 快速瞬态响应
- 散热增强型 HVSSOP 封装
- 集成热保护

2 应用

- 汽车照明：LED 开关矩阵 AFS 头灯，DRL，远光灯/近光灯，雾灯，尾灯，转向信号灯，轮廓灯，售后市场
- 工业照明：工厂自动化、飞行时间 (TOF)、电器、零售照明、机器视觉检测、紧急出口和/或安全照明、医用照明、舞台和场地照明
- 农业、航海和重工业照明
- 高对比度分流 FET 调光

3 说明

TPS92515 系列器件是集成了低电阻 N 沟道金属氧化物半导体场效应晶体管 (MOSFET) 的紧凑型单片开关稳压器。该系列器件适用于 注重 高效率、高带宽、PWM 和/或模拟调光以及小尺寸的高亮度 LED 照明应用。

该稳压器利用恒定关断时间和峰值电流控制功能来运行。工作原理十分简单：在基于输出电压的一段关断时间后，即开始导通时间。达到电感峰值电流阈值后，导通时间立即结束。TPS92515 器件可配置为在分流 FET 调光周期的导通和关断时间内保持恒定的纹波峰峰值。这非常适合在整个分流 FET 调光范围内保持线性响应。

稳态精度是在低偏移高侧比较器的支持下得到保证。可单独使用模拟或 PWM 调光技术来调制 LED 电流，也可同时使用这两种技术来调制 LED 电流。其他 特性包括欠压闭锁 (UVLO)、宽输入电压操作、固有 LED 开路操作和热关断功能，其工作温度范围较宽。

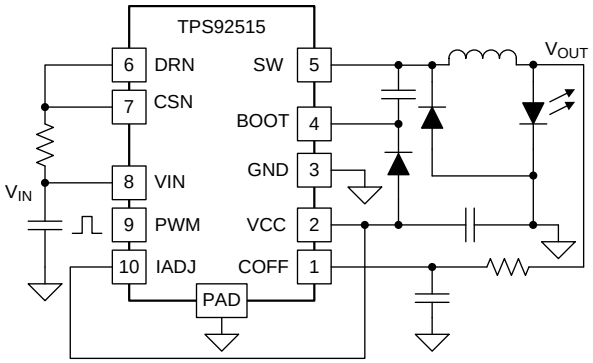
TPS92515 和 TPS92515-Q1 器件的工作输入电压范围高达 42V。TPS92515HV 和 TPS92515HV-Q1 提供输入范围高达 65V 的高电压选项。所有器件均采用散热增强型 10 引脚 HVSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS92515	HVSSOP (10)	3mm x 3mm
TPS92515-Q1		
TPS92515HV		
TPS92515HV-Q1		

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化的降压 LED 驱动器应用



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4 修订历史记录

Changes from Original (April 2016) to Revision A **Page**

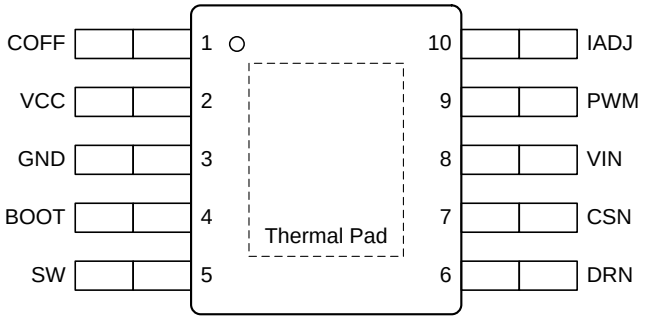
- 已将数据表状态由*产品预览*更改为*量产数据* 1

5 Device Comparison Table

DEVICE	MAXIMUM VOLTAGE (V)	CONTROL METHOD	AUTOMOTIVE QUALIFIED
TPS92515HV-Q1	65	Internal N-channel FET, constant OFF-time	Y
TPS92515-Q1	42		Y
TPS92515HV	65		N
TPS92515	42		N
LM3409HV-Q1	75	External P-channel FET, constant OFF-time	Y
LM3409-Q1	42		Y
LM3409HV	75	External P-channel FET, constant OFF-time	N
LM3409	42		N
LM3406HV-Q1	75	Internal N-channel FET, controlled ON-time	Y
LM3406-Q1	42		Y
LM3406HV	75		N
LM3406	42		N

6 Pin Configuration and Functions

DGQ Package
HVSSOP 10-Pin with PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	4	I	Connect a ceramic capacitor between BOOT and SW and a diode from VCC to BOOT to power the high-side FET drive circuitry.
COFF	1	I	Connect a resistor from V_{OUT}, and a capacitor to GND to set the OFF-time.
CSN	7	I	Current sense negative input. Connect current sense resistor from VIN to CSN for high-side current sense control.
DRN	6	I	Internal FET drain. Connect to CSN node
GND	3	G	Ground
IADJ	10	I	Output current adjust. Connect to an external divider, reference or tie to VCC.
PWM	9	I	PWM dimming input. Connect to PWM control signal. Output current is pulse-width modulated (PWM) dimmed from the maximum analog controlled level. Connect to VCC if not used.
SW	5	O	Internal FET Source. Connect to output inductor
VCC	2	O	5-V Regulator Output. Use a decoupling capacitor from VCC to ground. See section on VCC capacitor selection.
VIN	8	I	Connect to input voltage. VIN is also the current sense positive input.
Thermal pad		—	Connect to ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VIN, DRN, SW, CSN to GND	TPS92515, TPS92515-Q1	–0.3	45.0	V
	TPS92515HV, TPS92515HV-Q1	–0.3	65.0	
DRN to SW	TPS92515, TPS92515-Q1	–0.3	45.0	
	TPS92515HV, TPS92515HV-Q1	–0.3	65.0	
BOOT to GND	TPS92515, TPS92515-Q1	–0.3	50.5	
	TPS92515HV, TPS92515HV-Q1	–0.3	70.5	
COFF, IADJ, PWM to GND		–0.3	5.5	
BOOT to SW		–0.3	5.5	
VCC to GND		-0.3	5.5	
VIN to CSN		–0.3	0.3	
SW to GND, 10-ns transient (2)		–2.0		
Storage temperature, T_{stg}		-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DRN to SW. Absolute maximum not to be exceeded.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	TPS92515, TPS92515-Q1	5.5		42	V
		TPS92515HV, TPS92515HV-Q1	5.5		65	
T_A	Operating ambient temperature				125	°C
T_J	Operating junction temperature				150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS92515 HVSSOP 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and device Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 40 V, –40°C ≤ T_J ≤ 150°C, V_{BOOT} is referenced to SW pin, unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PEAK CURRENT COMPARATOR						
V_{CST}	V_{IN}– V_{CSN} peak current threshold	V_{IADJ} = VCC	224	240	251	mV
		V_{IADJ} = 2.2 V	211.5	220	223.5	mV
A_{ADJ}	V_{IADJ} to V_{IN} – V_{CSN} threshold gain	0.1 ≤ V_{IADJ} ≤ 2.2 V		0.1		V/V
I_{CSN}	Current sense pin, input bias current		–5		0	µA
t_{DEL}	CSN pin falling delay	CSN fall to SW fall		75	130	ns
t_{LEB}	Minimum ON-time	Minimum pulse width	75	195	275	ns
SYSTEM CURRENTS						
I_{cq}	Operating current	Not switching, V_{IADJ} = V_{VCC}		0.85	1.5	mA
INTEGRATED N-Channel MOSFET AND DRIVER						
$R_{DS(on)}$	FET ON-resistance	I_{DRN-SW} = 200mA, V_{BOOT} = 5 V, T_J = 25°C		290	500	mΩ
		I_{DRN-SW} = 200mA, V_{BOOT} = 5 V, T_J = 150°C		290	600	
		I_{DRN-SW} = 200mA, V_{BOOT} = 3.5 V, T_J = 25°C		310	500	
		I_{DRN-SW} = 200mA, V_{BOOT} = 3.5 V, T_J = 150°C		310	650	
$I_{DRN-SW(off)}$	FET leakage current	V_{DRN-SW} = 6 V, V_{SW} = 0 V		10		µA
$V_{BOOT-UVLO}$	Voltage where gate drive is disabled	V_{BOOT} falling	2.0	2.8	3.5	V
$V_{BOOT-UVLO(hys)}$	BOOT pin UVLO Hysteresis			125		mV
$I_{PD(PWM/UVLO)}$	Pull down from SW when PWM low.	PWM low, V_{BOOT} = 5 V , V_{SW} = 8 V		100	130	µA
$I_{PD(BOOT)}$	Pull down from SW when V_{BOOT} reaches $V_{BOOT-UVLO}$	PWM high, V_{BOOT} < BOOT-UVLO, V_{SW} = 8 V		5	7	mA
I_{BOOT_Q}	BOOT pin quiescent current	V_{BOOT} = 5.5 V, 0 V ≤ V_{SW} ≤ 65 V		60	90	µA
VCC/REFERENCE REGULATOR						
VCC	Regulated pin voltage	$I_{VCC(ext)}$ ≤ 500 µA	4.8	5.0	5.2	V
VCC_{DO}	Drop out voltage	$I_{VCC(ext)}$ ≤ 500 µA		0.1	0.2	V
VCC_{UVLO}	VCC undervoltage lockout	Falling threshold, V_{IN} = 10 V	4.0	4.2	4.4	V
VCC_{UVLO_hys}	VCC undervoltage lockout hysteresis			0.22		V
$I_{VCC(ILIM)}$	VCC regulator current limit	VCC shorted to GND	14	19	23	mA
VIN_{UVLO}	VIN UVLO Falling Threshold		4.65	4.90	5.15	V
VIN_{UVLO_hys}	VIN UVLO Hysteresis		150	190	225	mV
OFF-TIMER						
V_{OFT}	OFF-time threshold		0.95	1.00	1.05	V
$t_{D(off)}$	C_{OFF} threshold	C_{OFF} to SW rising delay		68	120	ns
$t_{OFF(max)}$	Maximum OFF-time			230		µs
PWM/UVLO (Enable)						
$I_{PWM(uvlo)}$	PWM/UVLO pin current	$V_{PWM(uvlo)}$ = 5.5 V		10		nA
$V_{PWM(uvlo)}$	PWM/UVLO pin threshold	PWM pin rising	0.95	1.0	1.05	V
$V_{PWM(uvlo-hys)}$	PWM/UVLO pin hysteresis	Difference between rising and falling threshold	50	100	150	mV
$t_{PWM(uvlo)}$	PWM/UVLO pin delay	PWM pin rising to SW pin rising		75	130	ns
		PWM pin falling to SW pin falling		100	170	ns
$I_{PWM(uvlo-hys)}$	PWM/UVLO hysteresis current	$V_{PWM(uvlo)}$ = 2 V	–25	–20	–15	µA

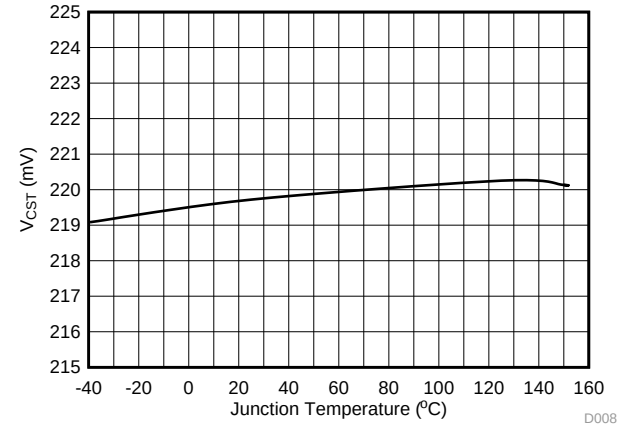
Electrical Characteristics (continued)

V_{IN} = 40 V, –40°C ≤ T_J ≤ 150°C, V_{BOOT} is referenced to SW pin, unless otherwise specified.

THERMAL SHUTDOWN				
T_{SD}	Thermal shutdown temperature		175	°C
$T_{SD(hyst)}$	Thermal shutdown hysteresis		10	

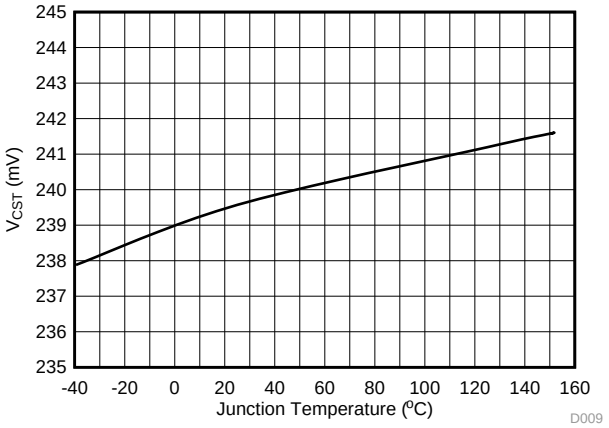
7.6 Typical Characteristics

$T_J = T_A = 25°C$ unless otherwise specified. Characteristics are identical for TPS92515x and TPS92515HVx. V_{IN} >42 V curves apply to TPS92515HVx only.



V_{IADJ} = 2.2 V V_{IN} = 40 V

Figure 1. V_{CST} vs. Junction Temperature



V_{IADJ} = VCC V_{IN} = 40 V

Figure 2. V_{CST} vs. Junction Temperature

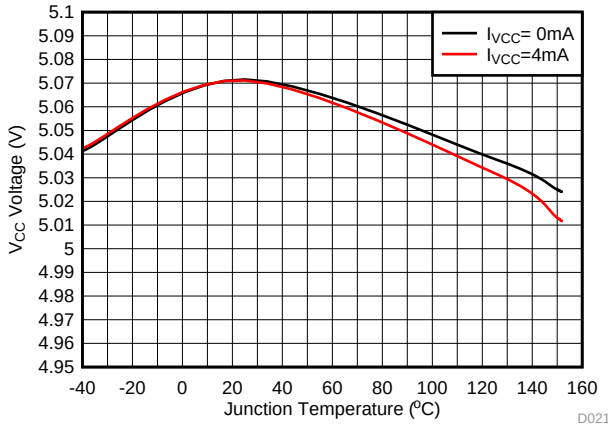


Figure 3. V_{CC} vs. Junction Temperature

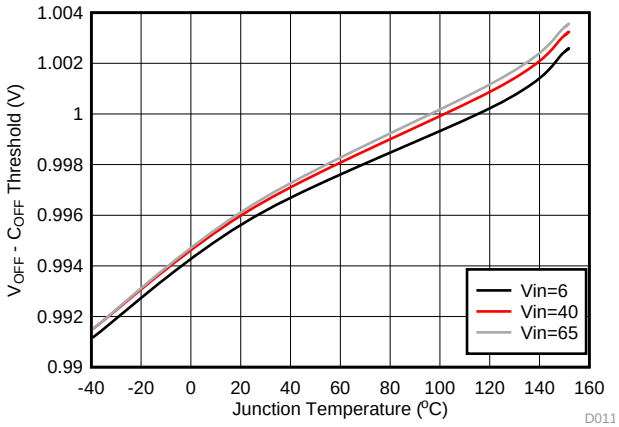
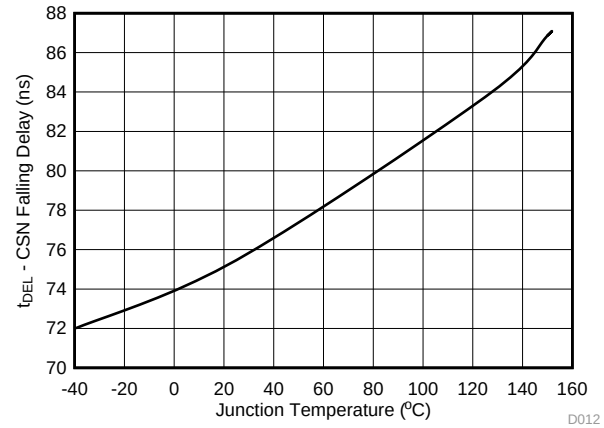
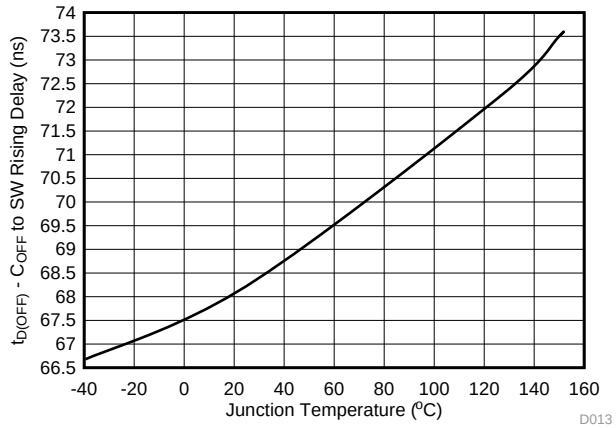


Figure 4. V_{OFF} vs. Junction Temperature



V_{IN} = 6 V

Figure 5. CSN Pin Falling Delay Time vs. Junction Temperature



V_{IN} = 40 V

Figure 6. Off-Time Delay vs. Junction Temperature

Typical Characteristics (continued)

$T_J = T_A = 25°C$ unless otherwise specified. Characteristics are identical for TPS92515x and TPS92515HVx. V_{IN} >42 V curves apply to TPS92515HVx only.

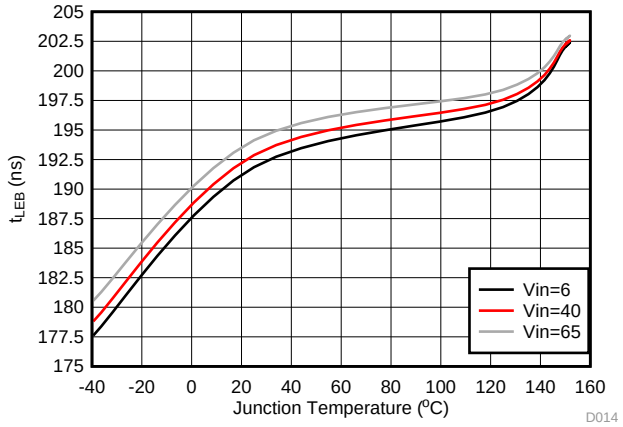
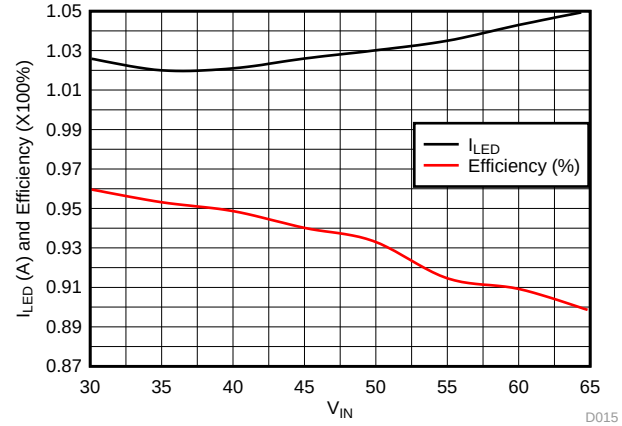
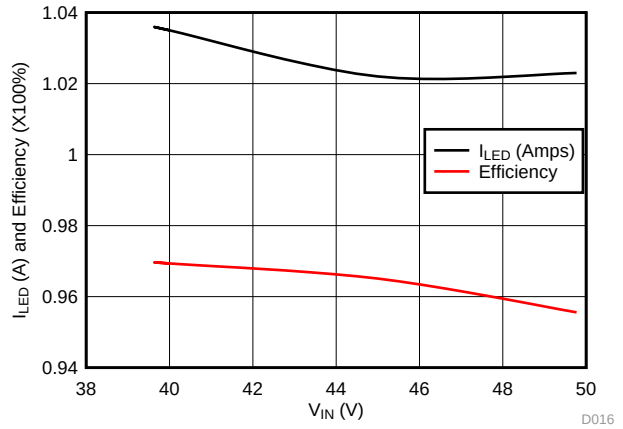


Figure 7. Leading-Edge Blanking Time vs. Junction Temperature



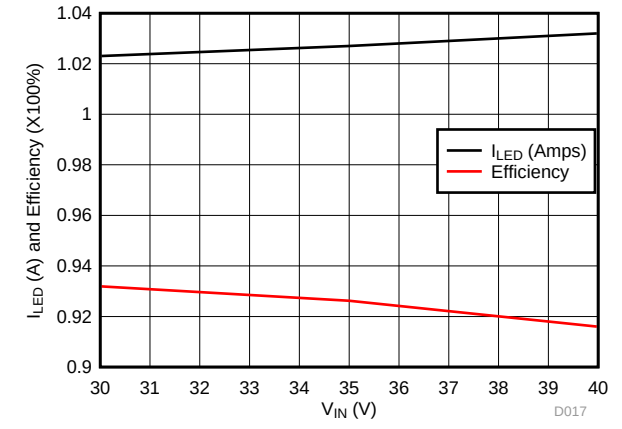
V_{LED} = 22 V V_{IADJ}=2.4 V R_{SENSE} = 0.196 Ω

Figure 8. EVM Configuration Result



V_{LED} = 35 V V_{IADJ}=2.4 V R_{SENSE} = 0.196 Ω

Figure 9. EVM Configuration Result



V_{LED} = 13 V V_{IADJ}=2.4 V R_{SENSE} = 0.196 Ω

Figure 10. EVM Configuration Result

8 Detailed Description

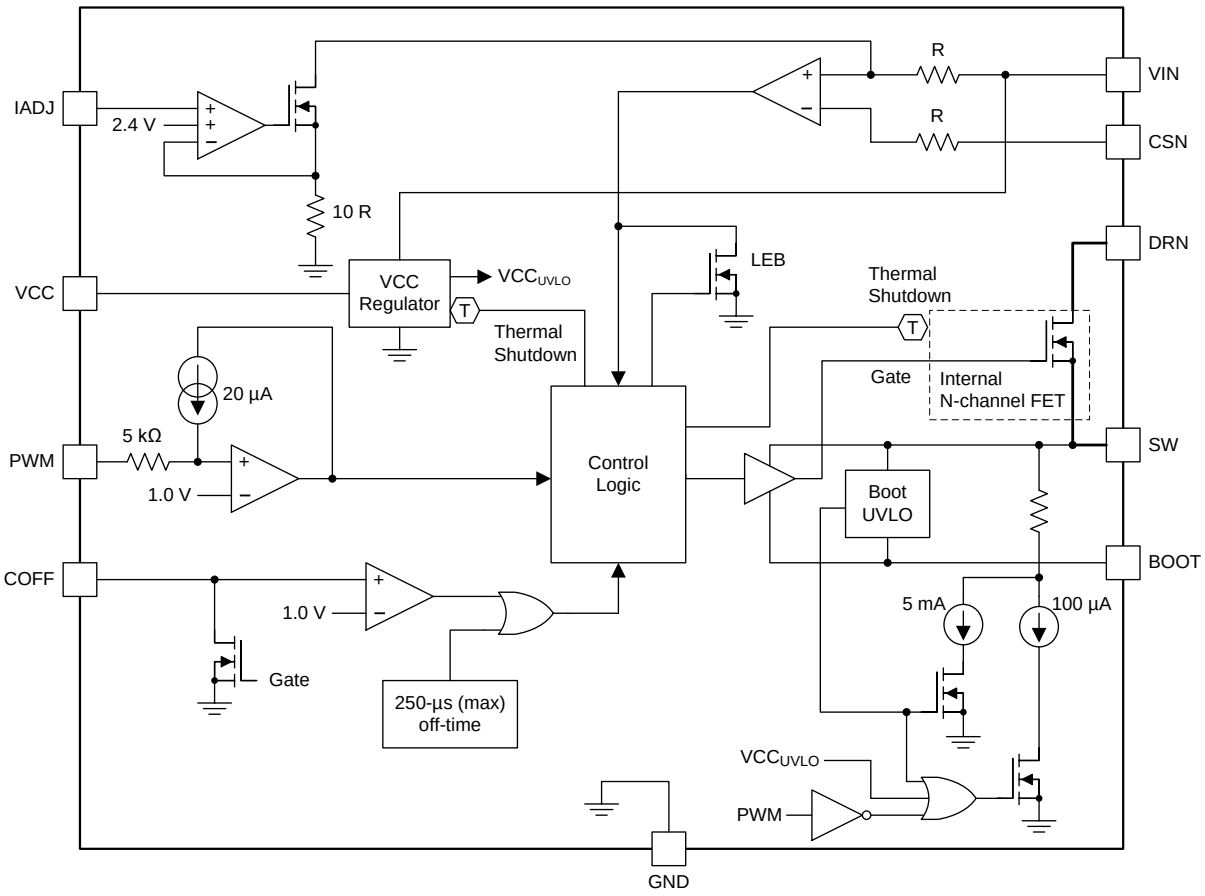
8.1 Overview

The TPS92515 is an internal N-channel MOSFET (monolithic NFET) hysteric control, buck regulator. Hysteretic operation allows a high control bandwidth and is ideal for shunt FET and LED matrix applications (series LED switched network). The high-side differential current sense with low adjustable threshold voltage via a 10:1 divider, provides an excellent method for regulating output current while maintaining high system efficiency. The device uses a controlled OFF-time (COFT) architecture to allow the converter to operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with no external control loop compensation, and provides an inherent cycle-by-cycle current limit.

The adjustable current sense threshold provides the capability for analog dimming the LED current over the full range and the PWM dimming input allows for high-frequency PWM dimming control requiring no external components. Configuration options allow for easy implementation of external shunt FET dimming. See also the *OFF-Timer, Shunt FET Dimming or Shunted Output Condition* section.

The device does not internally limit the maximum attainable average LED current. It does have a thermal limit based on the maximum junction temperature. The maximum junction temperature is a function of the system operating points (efficiency, ambient temperature, thermal management), component choices, and switching frequency. This functionality allows the device to provide constant currents up to 1 A in a wide variety of applications and up to 2 A in a smaller sub-set of applications. This simple regulator contains all the features necessary to implement a high-efficiency, versatile, high-performance LED driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 General Operation

The TPS92515 operates using a peak-current, constant OFF-time as described in Figure 11. Two states dictate the high-side FET control. The switch turns on and stays on until the programmed peak current is reached. The peak current is controlled by monitoring the voltage across the sense resistor. When the voltage drop is higher than the programmed threshold, the peak current is reached, and the switch is turned OFF, which initiates the OFF-time period. A capacitor on the COFF pin is then charged through a resistor connected to the output. When the COFF pin voltage reaches the 1-V (typical) threshold, the OFF-time ends. The COFF pin capacitor resets and the main switch turns ON, and the next cycle begins.

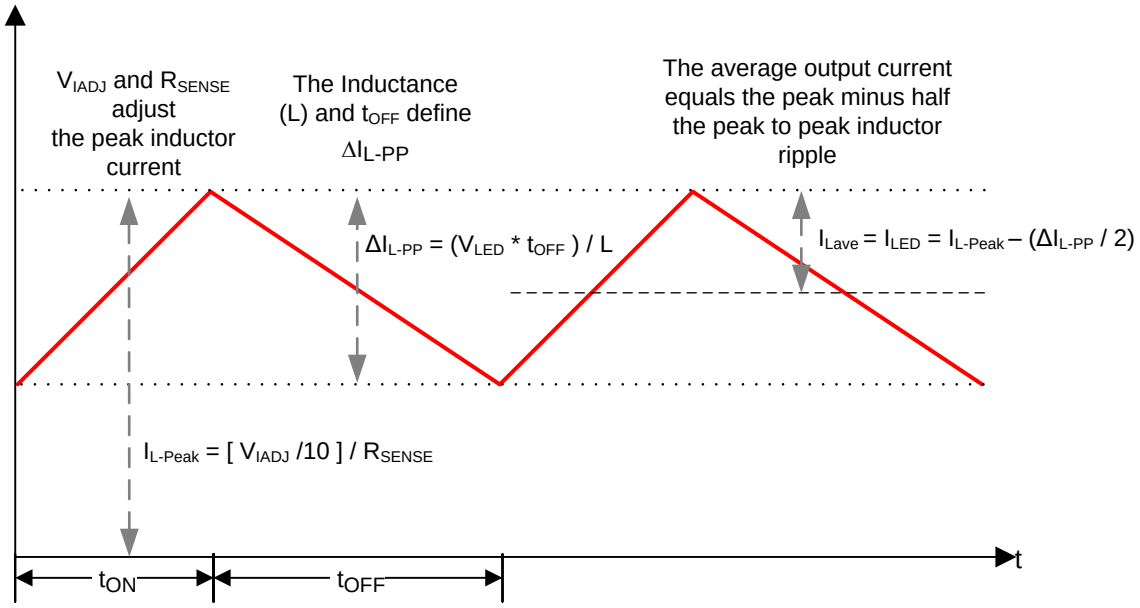


Figure 11. Hysteretic Operation

Although commonly referred to as *constant OFF-time*, the OFF-time control voltage is normally derived from the output voltage. This connection ensures constant peak-to-peak ripple. To maintain a constant ripple over various input and output voltages, the converter OFF-time becomes shorter or longer resulting in a change in frequency. If the input voltage and output voltage are relatively constant, the frequency also remains constant. If either the input voltage or the output voltage changes, the frequency changes. For a fixed input voltage, the device operates at the maximum frequency at 50% duty cycle and the frequency reduces as the duty cycle becomes shorter or longer. A graphical representation is shown in Figure 12. For a fixed output voltage (V_{LED}), the frequency is always the maximum at the highest input voltage as shown in Figure 13.

Feature Description (continued)

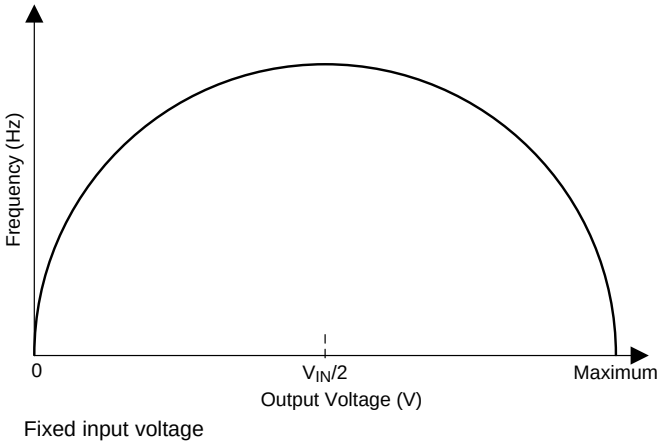


Figure 12. Frequency vs LED Output Voltage

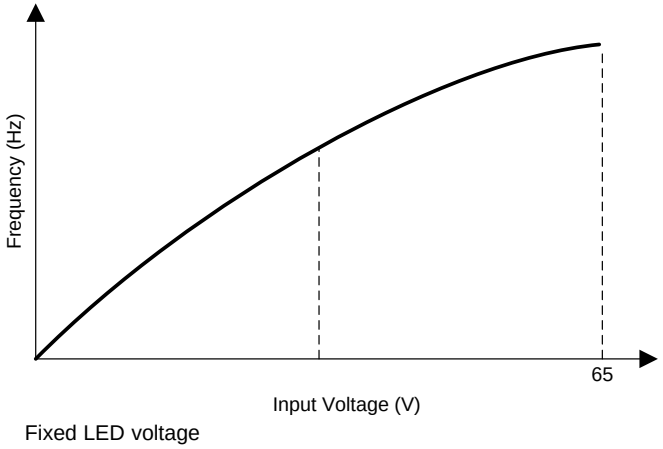


Figure 13. Frequency vs Input Voltage (V_{IN})

By making the OFF-time proportional to the output voltage, it is possible to illustrate how V_{LED} can be removed from the output current equation. When V_{LED} >> V_{OFT} , the output ripple can be defined as shown in Equation 1.

$$\Delta I_{L\text{-}PP} = (V_{LED} \times dt)/L \quad (1)$$

where

- dt is defined by the OFF-timer

$$dt = \frac{Cdv}{i} = \frac{C_{OFF}(1V)}{\left[\frac{V_{LED}}{R_{OFF}}\right]} = \frac{C_{OFF}R_{OFF}(1V)}{V_{LED}} \quad (2)$$

Substitute dt in Equation 1 to create Equation 3.

$$\Delta I_{L-PP} = \frac{Vdt}{L} = \frac{V_{LED}dt}{L} = \frac{V_{LED}\left[\frac{C_{OFF}R_{OFF}(1V)}{V_{LED}}\right]}{L} = \frac{C_{OFF}R_{OFF}(1V)}{L} \quad (3)$$

$$I_{LED} = \frac{\frac{V_{IADJ}}{10}}{R_{SENSE}} - \frac{C_{OFF}R_{OFF}(1V)}{2L} \quad (4)$$

When V_{LED} >≈ 10 V, use the I_{LED} calculation Equation 4. The *Detailed Design Procedure* section describes a design example that uses the more detailed equation. A V_{LED} > 10 V ensures a linear charging ramp below 1 V. If V_{LED} <≈10 V, use Equation 5 that considers the exponential charging characteristic.

$$I_{LED} = \left[\frac{\frac{V_{IADJ}}{10}}{R_{SENSE}}\right] - \left[\frac{V_{LED}\left[-R_{OFF}C_{OFF}\left[\ln\left[1-\frac{V_{OFT}}{V_{LED}}\right]\right]\right]}{2L}\right] \quad (5)$$

Because the control method relies on thresholds to control the main switch, offsets and delays must also be considered when examining the output accuracy. The I_{LED} equation can be expanded to include these error sources as shown in Equation 6. I_{LED} equations include several passive components, so it is important to consider the tolerance of each component. The V_{CST_Offset} parameter is the variation in the V_{CST} threshold between the typical and maximum or minimum values as defined in the Electrical Characteristics table.

Feature Description (continued)

$$I_{LED} = \left[\frac{\frac{V_{IADJ}}{10} \pm \left(V_{CST\_Offset}\right)}{R_{SENSE}} + \frac{(V_{IN} - V_{LED})(t_{DEL})}{L} \right] - \left[\frac{V_{LED}\left[-R_{OFF}C_{OFF}\left[\ln\left[1 - \frac{V_{OFT}}{V_{LED}} \right] \right] \right] + t_{D(OFF)}}{2L} \right] \quad (6)$$

8.3.2 Current Sense Comparator

A comparator, two resistors and a current source create a peak current detection circuit block. See the Functional Block Diagram for details. A current source controlled by V_{IADJ} draws a current across a resistor in series with a comparator, forcing a proportional offset. The resistor in the current source (10 R) and in series with the comparator (R) are sized with a 10:1 ratio. This ratio allows for a practical voltage range of operation for the IADJ pin and maintains a small current sense voltage for low losses and less impact on efficiency.

The ON cycle begins with the offset in place via IADJ across the resistor R at the VIN pin. When the current rises enough to create a voltage across the sense resistor to match the offset, the comparator trips. The end of the ON-time period starts an OFF-time cycle.

Trace resistance can have an impact on accuracy, so care should be used when routing the traces to VIN and CSN from the sense resistor. Because the sense resistor value is typically in milli-ohms, use a short kelvin connection to CSN and place the sense resistor as close as possible to VIN.

8.3.3 OFF Timer

The converter OFF-time is controlled via the COFF pin. The output voltage charges a capacitor to 1 V through a resistor creating a delay. Deriving the OFF-time from the output voltage creates a ramp representing the inductor current. If the output voltage cannot be used, another voltage fixed source may be implemented to create a truly constant OFF-time. However, this configuration reduces output current accuracy. When the device is first enabled (when VCC rises above the VCC undervoltage lockout threshold) the pull-down on the COFF pin is disabled, allowing a voltage to build up on the COFF capacitor. At the same time, the maximum off timer begins. If the voltage source is sufficiently above the 1-V threshold, the ramp becomes linear and approximates the inductor current. If the 1-V nominal COFF threshold is reached, or the COFF capacitor charge time duration is greater than $t_{OFF(max)}$ (maximum OFF-time timer expires), a switching cycle starts.

The timer reaches the maximum OFF-time during start-up when the output is completely discharged or when shunt FET dimming and the shunt FET shunts the output for the required period.

Equation 7 calculates R_{OFF} for a desired OFF-time.

$$R_{OFF} = \frac{t_{OFF}}{-C_{OFF}\left[\ln\left[1 - \frac{V_{OFT}}{V_{LED}} \right] \right]} \quad (7)$$

8.3.4 OFF-Timer, Shunt FET Dimming or Shunted Output Condition

The OFF-time is derived from the output voltage to create a constant inductor ripple. A constant inductor ripple ensures linearity when dimming. When the dimming method selected requires the output to be shorted, (shunt FET or Switched Matrix approach) it is necessary to derive the OFF-time ramp from an alternate source. When the output is shunted, the output voltage becomes very low and possibly less than the 1 V OFF-timer threshold voltage. If this occurs, the off timer is not able to trip and the OFF-time reaches the maximum OFF-time before the switch is turned on again. The system is able to operate in this mode, but constant inductor current ripple and linear shunt-FET dimming is not possible. To avoid this situation, VCC can be used as a parallel source to charge the COFF capacitor and maintain a constant ripple even when the output is shorted. This ensures precise dimming linearity. Refer to Figure 14 for connection information.

It is not recommended to apply power to the OFF-timer circuitry while the VIN pin is not powered. The device includes an internal diode between the COFF pin and the VCC pin. If the COFF pin receives power with no input voltage (V_{IN}) applied, VCC pin voltage could inadvertently be pulled up and cause the device to attempt operation. This attempt could negatively affect the application if this operation is not desired.

Feature Description (continued)

Selecting the value for R_{OFF2} is a two-step process.

The first step is to compute the OFF-time required when the output is shunted ($t_{OFF-Shunt}$).

$$t_{OFF-Shunt} = \frac{\Delta I_{Lpk-pk} \times L}{V_{SHUNT} + (0.7)}$$

where

- V_{SHUNT} is the output voltage when the shunt device or LED Matrix device is ON (8)

The second steps is to compute R_{OFF2} using ($t_{OFF-Shunt}$).

$$R_{OFF2} = \frac{-t_{OFF-Shunt}}{C_{OFF} \times \ln\left[1 - \left[\frac{1}{V_{CC}}\right]\right]} \quad (9)$$

The value of R_{OFF1} becomes the previously calculated value of R_{OFF}.

The result of these calculations produce an inductor current that maintains the same DC value when shunted or when not shunted as shown in Figure 15.

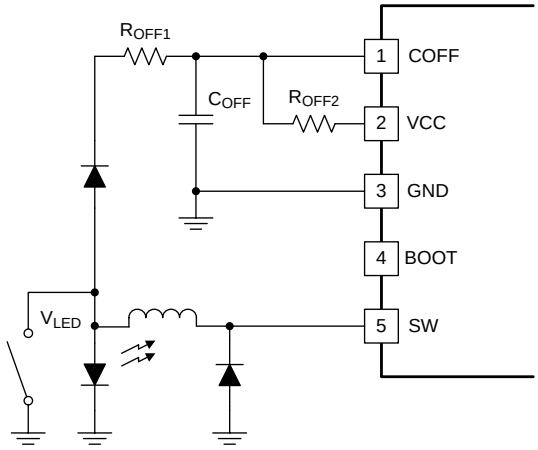
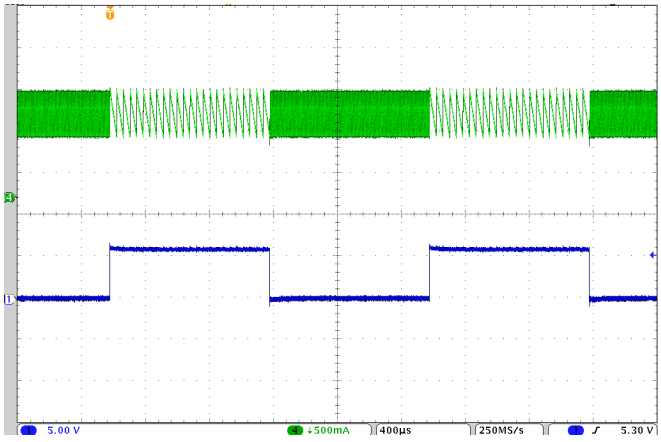


Figure 14. Shunt Dimming COFF Connection



Ch1: PWM Signal Time: 400 µs/div

Ch4: Inductor current No Output Capacitor

Figure 15. Shunt FET Dimming with Optimized Inductor Current

8.3.5 Internal N-channel MOSFET

Integrated in the TPS92515 is a low on-resistance ($R_{DS(on)}$) N-channel MOSFET. The resistance specified in the *Electrical Characteristics* table for the drive voltage and temperature is important to consider because the actual on-resistance for a given operating point affects efficiency and the transition point into drop-out when operating at high currents. A sensing element for thermal shutdown circuitry has been located close to the internal FET to better assist in part protection.

8.3.5.1 Drop-Out

The TPS92515 can operate safely even when the input voltage enters the drop-out region. As V_{IN} approaches V_{LED}, ΔI_{L-PP} falls to a level much lower than during normal operation. Because the average output current is based on Equation 10, as ΔI_{L-PP} becomes smaller, the average current tends to increase. The amount of increase depends on the value of ΔI_{L-PP} used in the design. If drop-out performance is a concern, performance can be improved by lowering the ΔI_{L-PP} design parameter.

$$I_{LED} = IL_{PEAK} - (\Delta I_{L-PP}/2) \quad (10)$$

Feature Description (continued)

8.3.6 VCC Internal Regulator and Undervoltage Lockout (UVLO)

The device incorporates a linear regulator to generate the 5-V (typ) V_{CC} voltage. The V_{CC} output voltage is monitored to implement undervoltage lockout (UVLO) protection. The UVLO thresholds are fixed and cannot be adjusted. The device has been designed to supply current for the device operation as well as additional power for external circuitry. If a 5-V rail is required in an application, the device can allow up to 500 µA to be drawn in addition to the device load. A capacitance of 1 µF or ≥ 10× the BOOT capacitance to a maximum of 10 µF is recommended.

The device requires adequate input decoupling in order to lower ΔV_{IN-PP} ripple for the best V_{CC} supply voltage performance. ΔV_{IN-PP} must not exceed 10% of the input voltage V_{IN} or 2 V, whichever is lower.

8.3.7 Analog Adjust Input

The analog adjust pin (IADJ) provides the reference for the peak current trip point. Through the use of an internal 10:1 divider, a wider range and finer control of the peak current sense threshold is created. For example, applying 2.2 V to the IADJ pin creates a 220-mV, peak-current-sense trip point. The lower sense voltage also lowers the power (V^2/R) losses at the sense resistor. There is a practical lower limit to the IADJ pin voltage choice due to circuit non-idealities. For example, using V_{IADJ} = 0.5 V results in a sense voltage of 50 mV, which does not allow accurate operation.

8.3.7.1 IADJ Pin Clamp

The IADJ pin incorporates an internal 2.4-V clamp. An area of inaccuracy in the clamp knee point voltage requires the designer to consider how to mitigate this situation when selecting an IADJ pin voltage. The most accurate method is to apply 2.2 V to the IADJ pin, which allows it to remain below the clamp *knee-point voltage* area. If an accurate, external, 2.2-V (or lower) reference is not available, use the next most accurate control method which is the internal clamp. The least accurate method uses a resistor divider on the VCC pin. The *Analog and PWM Dimming - Normalized Results and Comparison* section includes measured analog dimming results.

Feature Description (continued)

8.3.7.2 IADJ Pin Clamp Characteristic

Figure 16 shows the clamping characterization. Figure 28 shows an application measurement. The translation is straightforward, with the exception of the knee-point voltage area. For voltages ≤2.2 V, the internal VIN to CSN peak current sense voltage equals V_{IADJ}/10. For voltages ≥ 2.4 V the voltage equals 240 mV. For the area 2.2 ≤ V_{IADJ}≤ 2.4 the voltage approximates V_{IADJ}/10, but varies slightly more than the other regions of operation.

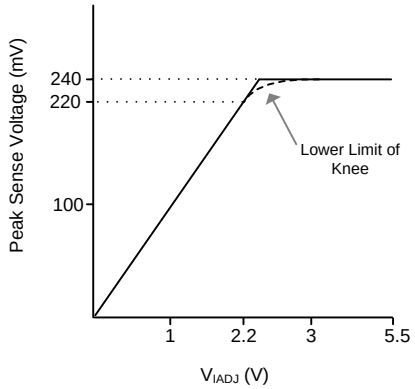


Figure 16. IADJ Pin Internal Clamp Characteristic

Feature Description (continued)

8.3.7.3 Analog Adjust (IADJ Pin) Control Methods

This section describes several analog adjust (IADJ) control methods configurations.

Table 1. IADJ Pin Connection Schematics

FIGURE	IADJ PIN CONNECTION
Figure 17	IADJ pin tied directly to the VCC pin using the internal 2.4-V clamp.
Figure 18	IADJ pin tied through a voltage divider to the VCC pin allowing a lower peak current sense voltage
Figure 19	IADJ pin tied through a resistor and thermistor divider, implementing thermal foldback function.
Figure 20	IADJ pin is connected to a micro controller. A GPI/GPIO is connected to a filter to create an analog adjust voltage.
Figure 21	IADJ pin connection to implement a soft-start sequence
Figure 22	IADJ pin is connected to a precision reference. This configuration yields the highest accuracy.

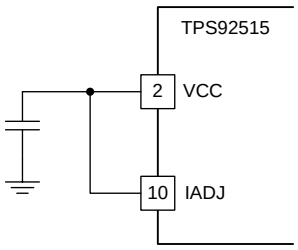


Figure 17.

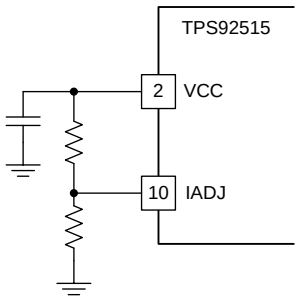


Figure 18.

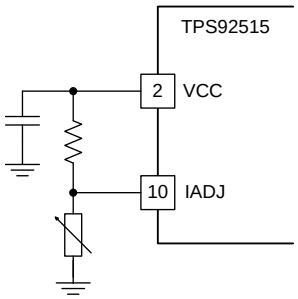


Figure 19.

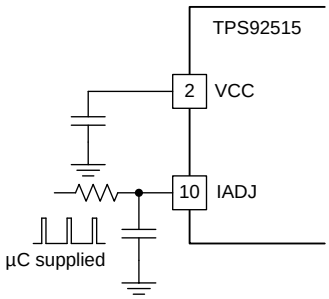


Figure 20.

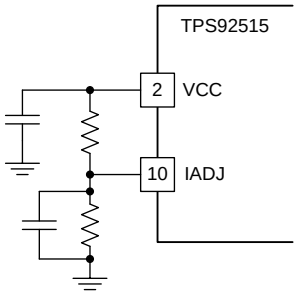


Figure 21.

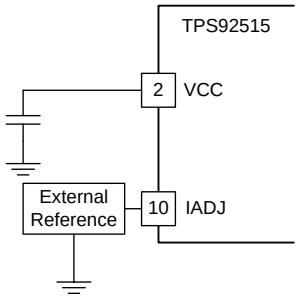


Figure 22.

8.3.7.4 IADJ Control Method Notes

- Connecting the IADJ pin directly to VCC is simple and is the most accurate stand-alone implementation.
- Using a resistor divider circuit can lower the sense voltage and improve efficiency if the converter output currents are high. The trade-off is an increased variation in the peak trip voltage. Note that there are also practical limitations to how low the sense voltage can be and maintain a reasonable accuracy.

- The simple thermal foldback method sizes the divider to set the IADJ voltage above 2.4 V. This method uses the internal clamp when thermal foldback is not required and sets the IADJ voltage below 2.4 V when foldback is required. Match the temperature characteristic of the thermistor to the second resistor in the divider. As an alternative, use a positive temperature coefficient (PTC) thermistor as the upper resistor in the divider.
- By using a micro-controller to control the timing output, the duty cycle can be controlled and the voltage can be filtered and connected to the IADJ pin. Use a filter pole of 1/10th the micro-controller control pin output switching frequency, or use R ≈ 1 kΩ and C ≈ 4.7 µF as a starting point.
- Simply add a capacitor to the IADJ pin and size the R-C constant to produce the desired soft-start time. Consider the maximum current is reached when V_{IADJ} = 2.4 V.
- To achieve the highest accuracy, use an external, high-precision reference and power it from the TPS92515 VCC if required. A 1% or 2% Zener diode, TL431 device, or an existing precision reference circuit can be used.

8.3.8 Thermal Protection

The TPS92515 device incorporates thermal protection circuitry. If the TPS92515 thermal pad is not soldered, or not soldered correctly, the device reaches the thermal shutdown temperature prematurely. Use X-ray inspection or some other means to verify the device thermal pad soldering to ensure correct assembly.

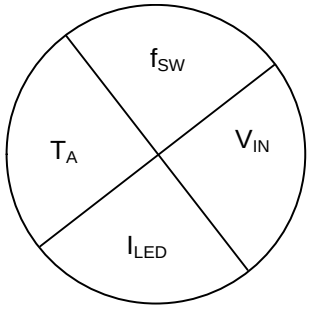
Two internal sensing elements ensure proper temperature measurement across the die. One sensing element is located near the internal FET. The other sensing element is located near the V_{CC} regulator. Power dissipation the FET and internal regulator contribute the most to device temperature rise.

When the device temperature reaches the thermal shut-down level at the FET sense point, the high-side FET and internal regulator become disabled and switching stops. When thermal shut-down temperature is reached at the regulator sense point, the V_{CC} regulator becomes disabled, and switching stops when V_{CC} falls below the VCC_{UVLO} level. In both cases, after the device lowers 10°C (typical) from the trip temperature, normal operation resumes.

8.3.8.1 Maximum Output Current and Junction Temperature

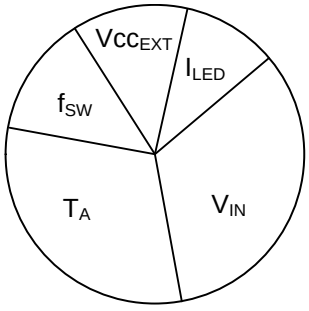
As with all power converter controllers and regulators, practical limits to specification maximums must be considered for each application. For example, it is not possible to operate the TPS92515 with a switching frequency of 1 MHz, output current of 2 A, at an ambient temperature of 125°C and stay within operating limits. Conversion factors and environment must be considered. This section describes two conversion scenarios with different operating conditions that would result in approximately the same junction temperature. In each case all of the power loss factors combine to develop the device junction temperature.

Figure 24 describes a design with half the output current and a lower switching frequency compared to that shown in Figure 23. However, the design shown in Figure 24 has a higher ambient temperature, higher V_{IN} and an additional external V_{CC} load, resulting in similar junction temperature. Table 2 lists trade-offs and impact on temperature. In general, applications requiring high current (2 A) or a high switching frequency (> 1 MHz) provide reduced maximum ambient temperature levels.



I_{LED} = 1 A
f_{SW} = 500 kHz
V_{IN} = 14 V
T_A = 85°C

Figure 23. Power Balanced



I_{LED} = 500 mA
f_{SW} = 300 kHz
V_{IN} = 60 V
T_A = 125°C
External V_{CC} load = 500 µA

Figure 24. Power Unbalanced

Table 2. Device Junction Temperature Factors

FACTOR		AFFECT ON TEMPERATURE AND TRADE-OFFS
T_A	Ambient temperature	An increase in the ambient temperatre will increase the junction temperature by the same amount.
V_{IN}	Input voltage	A higher input voltage results in more power developed across the internal regulator resulting in higher internal losses. A higher voltage often yields a larger step-down conversion and lower efficiency.
I_{LED}	LED current	A higher LED output current results in higher power (I^2R) losses in current carrying elements like the internal MOSFET.
$I_{VCC(ext)}$	External V_{CC} current	Current used to supply additional loads external to the TPS92515 device draw from the internal regulator. More external current results in an increased junction temperature. When an external source supplies the BOOT current internal power dissipation decreases.
f_{SW}	Switching frequency	Each time the internal FET is turned ON and OFF, current must flow from VCC to the gate driver. The current drawn by a switching gate approximately equals the gate charge times the switching frequency. Power loss associated with the switching edge transitions also increase with frequency.
η	Efficiency	Switching conversions requiring difficult conversions (small duty cycles) have higher overall losses. These losses increase the overall temperature of the application and the device temperature.

8.3.9 Junction Temperature Relative Estimation

The dominant power loss factors predict the junction temperature. These equations offer an estimate of device temperature for the use of considering different conversion scenarios. By adding the losses and using the device thermal impedance, a temperature can be predicted. In this case we consider losses internal to the device: Conduction loss in the MOSFET, an estimate of switching losses and I_{cq} losses.

$$T_{J-Estimate} = \left[P_{LOSS_{COND}} + P_{LOSS_{SW}} + (I_{Gate} + I_{cq}) * V_{IN} \right] * \Theta_{JA} + T_A \tag{11}$$

By expanding the terms an estimate can be calculated using Equation 12

$$T_{J-Estimate} = \left[\left[\left[I_{LED}{}^2 x\ 0.6\ x\ \frac{V_{LED}}{V_{IN}} \right] + \left[\left(0.5\ x\ V_{IN}\ x\ I_{LED}\ x\ 60E^{-9} x\ f_{SW} \right) x\ 1.2 \right] + \left[(3E^{-9} x\ f_{SW} + 1E^{-3}) * V_{IN} \right] \right] x\ 56.2 \right] + T_{Ambient} \tag{12}$$

8.3.10 BOOT and BOOT UVLO

The TPS92515 contains circuitry to ensure proper operation of the internal MOSFET. Typically a capacitor tied to the switchnode (SW pin) and a diode connected to the VCC supply powers the BOOT pin. Each time the diode conducts current, a path is created from the VCC pin to charge the BOOT capacitor. The connection allows the BOOT capacitor to float with the switch-node voltage and internal FET source. Anytime the main switching diode conducts current, the switch-node falls to a diode drop below ground. This creates a path for the boot capacitor to be charged in approximately 150 ns or less. A typical BOOT capacitance of 0.1 µF can maintain the ON-state of the FET for approximately 5 ms. This timing allows conversion duty-cycles of >> 99%. Anytime the BOOT voltage reaches a level that does not allow proper FET turn-on, the high-side FET will be turned off.

Although the internal VCC regulator typically supplies power to the BOOT drive circuitry, that power can be supplied by a suitable external source. Use this configuration to save power dissipation in the device and to lower the junction temperature. Ensure the external source does not exceed 5 V and that it can supply an adequate average current equal to or greater than $3 \times 10^{-9} \times f_{SW}$.

8.3.10.1 Start-Up, BOOT-UVLO and Pre-Charged Condition

If a pre-charge condition occurs (a voltage exists on the output at turn-on) a resulting undervoltage lockout of the BOOT pin activates an internal, 5-mA (typical) pulldown. The pulldown reduces the time required to bring the output voltage low enough to charge the BOOT capacitor and begin operation. The device activates this strong pulldown any time undervoltage lockout of the BOOT pin occurs. However, in most situations the diode turn-on does most of the work to lower the switch node voltage. The pulldown will not act as a synchronous FET.

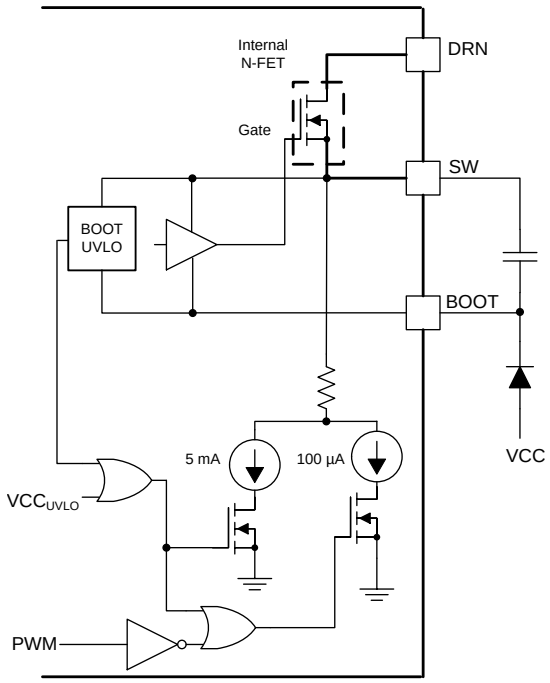


Figure 25. BOOT and PWM Pull-Downs

8.3.11 PWM (UVLO and Enable)

If PWM dimming or ON/OFF control is not needed in the application, the pin should be tied to VCC. The pin must be tied above 1 V if operation is desired.

PWM dimming can be achieved using the PWM pin. A signal above 1 V (typical) and below 900 mV (typical) when measured at the PWM pin should be used. Standard PWM frequency ranges can also be used (100 Hz to 2 kHz). When using higher frequencies the delays from PWM to gate turn ON and turn OFF can begin to limit the achievable duty cycle.

For example, the PWM to gate delay (turn on + turn off ≈ 100 ns) and the time to slew the switchnode up and down (approximately 100 ns) total approximately 200 ns.

For example, if a 10 kHz PWM frequency is desired having a period of 100 µs, the minimum duty cycle is 200 ns/100 µs = 0.2%. This is sometimes referred to as "500:1 dimming". As the PWM signal width becomes smaller, the converter ON and OFF time are eventually controlled by the PWM input signal directly. For example, if the PWM ON-time is shorter than the converter natural demanded ON-time, the PWM signal itself becomes the control signal for the high-side switch. The PWM pin activates a weak pulldown, as shown in Figure 25. Because the PWM pin is also UVLO (undervoltage lockout and device enable), when pulled low it is necessary to ensure the output is 100% OFF. The high-side FET driver has a small leakage path to the output. Although very small (<<100µA), theLEDs could glow if the current was not eliminated. The 100-µA (typical) pulldown is activated and held ON while PWM is low and ensures no light output.

8.3.11.1 Using PWM for UVLO (Undervoltage Lockout) Protection

When the PWM pin exceeds the 1-V (typical) threshold, the device activates a 100-mV (typical) fixed hysteresis and an adjustable hysteresis based on an internal current source ($I_{PWM(uvlo-hys)}$). This functionality provides noise immunity to the PWM control and adjustability to the UVLO hysteresis. The two thresholds can be designed as described in the *UVLO Programming Resistors* section.

8.3.11.1.1 UVLO Programming Resistors

The value of resistors R2 and R3 establish the undervoltage lockout level as shown in Figure 26. Include a small level of capacitance (approximately 0.1 µF) at the UVLO pin for noise immunity. If the application does not require drop-out operation (operation when V_{IN} approximates V_{LED}) program a UVLO level allows no switching to occur until there is adequate input voltage available.

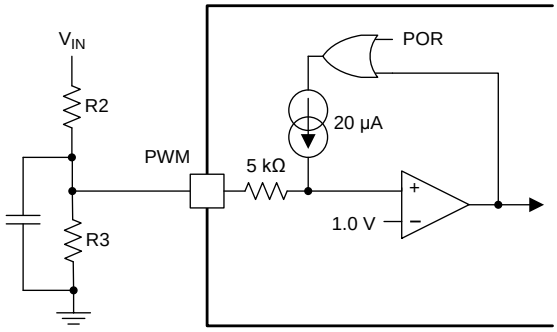


Figure 26. UVLO Programming Resistors

Select the desired amount of voltage hysteresis and the desired turn-ON threshold ($V_{IN\text{-}RISE\_THRESHOLD}$). Because of the small amount of fixed-voltage hysteresis and fixed-hysteresis current, some combinations of turn-ON and turn-OFF thresholds are not possible. If the calculation results in values that are zero or negative, the combinations selected are not possible. After selecting a turn-ON point and desired amount of voltage hysteresis (V_{HYST}) use Equation 13 and Equation 14 to calculate R3 and R2.

$$R_3 = \frac{V_{HYST} - \left[0.1 \text{ x } V_{IN-RISE\_THRESHOLD}\right]}{20\mu A \text{ x } \left[V_{IN-RISE\_THRESHOLD} - 1\right]} \quad (13)$$

$$R_2 = \left[V_{IN-RISE\_THRESHOLD} - 1\right] \text{x } R_3 \quad (14)$$

8.3.11.2 Using PWM for Digitally Controlled Enable

If using the PWM pin as to provide and enable function, ensure the signal edge rate is adequate (< 100 ns) when measured at the device PWM pin to prevent the device from turning ON and turning OFF when the level transitions through the 1-V threshold region. If the edge is too slow or if the high level is not adequately above the 1-V threshold, a small capacitor may be required on the PWM pin to avoid multiple turn-ON and turn-OFF cycles when passing through this region.

8.3.11.3 UVLO: VIN, VCC and BOOT UVLO

The TPS92515 contains 3 internal under voltage lock-outs which must be satisfied for the device to operate: VIN UVLO ensures adequate voltage to power the high-side comparator. VCC UVLO ensures internal rails are adequate for the device to function, and BOOT UVLO ensures proper high-side FET operation and smooth dropout operation. All of the UVLO's operate independently and automatically. Under normal operation they do not require any specific user attention.

8.3.11.4 Analog and PWM Dimming - Normalized Results and Comparison

When the PWM applied signal is less than the switching cycle period and falls during an OFF-time it has no impact on the current for that cycle as the switch is already OFF. This situation can be avoided by increasing the switching frequency. Shunt FET PWM dimming avoids this issue. Current adjustment that maintains a constant ripple when shunted (see the *OFF-Timer, Shunt FET Dimming or Shunted Output Condition* section), creates a linear relation to the PWM shunt FET duty cycle and the average output current. Shunt FET PWM dimming can out-perform PWM dimming as characterized in Figure 27 through Figure 29, but is more complicated to implement.

Another impact on linearity can occur when using the analog dimming function. Discontinuous conduction mode (DCM) occurs when the inductor current reaches 0 A during each cycle,. When the device enters DCM, the output current is no longer the peak current minus half the ripple. The linear range can be extended by lowering the ripple, $\Delta I_{L\text{-}PP}$. If the system is being digitally controlled, the applied IADJ pin voltage can be adjusted when it is known the DCM operation occurs. In either case, a lower limit is eventually reached when the measured peak threshold voltage is approximately < 50 mV. At this point, the offset error becomes a significant portion of the peak current trip point voltage being measured.

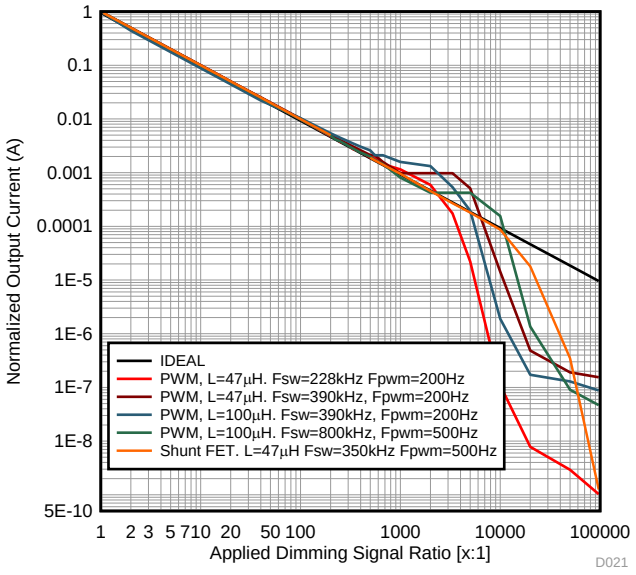
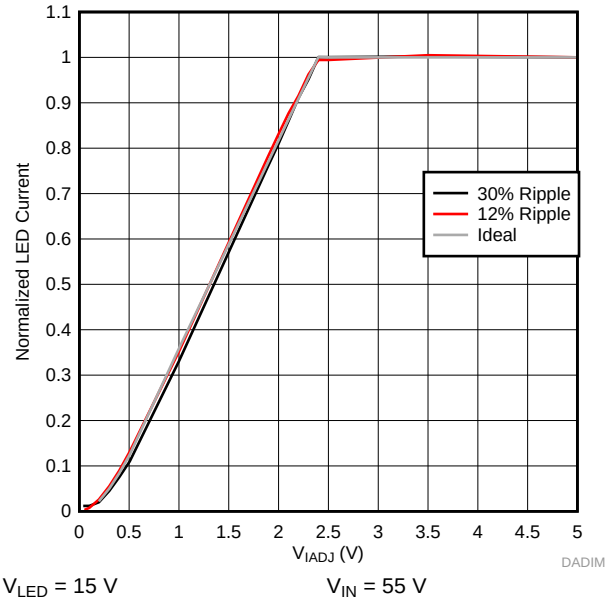
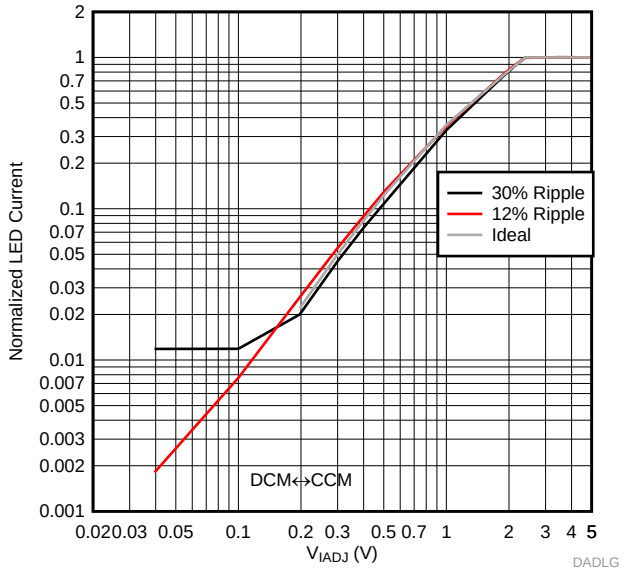


Figure 27. PWM Dimming Performance with Shunt Dim Comparison



V_{LED} = 15 V V_{IN} = 55 V

Figure 28. Analog Dimming Performance



V_{LED} = 15 V V_{IN} = 55 V

Figure 29. Analog Dimming Performance (Log Scale)

8.4 Device Functional Modes

This device has no additional functional modes.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS92515 buck current regulator is suitable for implementing step-down LED drivers. This section presents a simplified design process for an LED driver with the following specifications:

- Buck converter topology
- Input voltage: 65 V
- Output voltage: 22 V (7 LEDs)
- Output current 1 A

Use the following design procedure to select component values for this and similar buck applications.

9.2 Typical Application

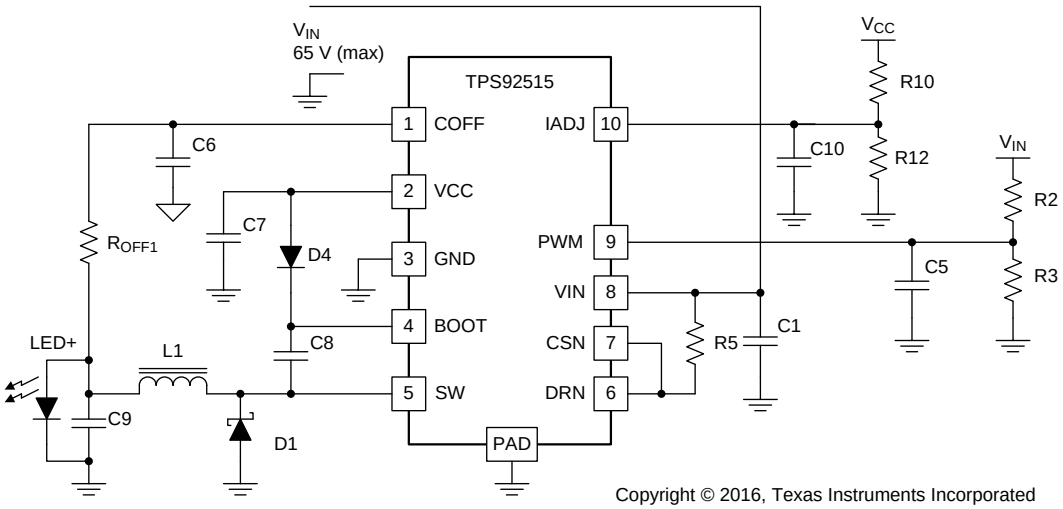


Figure 30. TPS92515 BUCK LED Driver

9.2.1 General Design Procedure

This procedure includes the fundamental design equations required for a TPS92515 buck converter design.

9.2.1.1 Calculating Duty Cycle

Start with an efficiency of n estimation of 0.9.

$$D = \frac{V_{LED}}{V_{IN} \times n}$$

where

- $V_{OUT} = V_{LED}$ (15)

9.2.1.2 Calculate OFF-Time Estimate

Equation 16 uses the switching period T to derive the OFF-time (t_{OFF}) .

Typical Application (continued)

$$t_{OFF} = \frac{1}{f_{SW}} x\left[1-D\right]$$

derived from:

- $T = [t_{OFF} + t_{ON}] = [t_{OFF} + (D \times T)]$ and
- $T = 1/f_{SW}$ (16)

9.2.1.3 Calculate OFF-Time Resistor R_{OFF}

Select a C_{OFF} between 100 pF and 1 nF. The preferred value is 470 pF. The EC table specifies the OFF-time threshold (V_{OFT}) at 1 V.

$$R_{OFF} = \frac{t_{OFF}}{-C_{OFF}\left[\ln\left[1-\frac{V_{OFT}}{V_{LED}}\right]\right]} \quad (17)$$

9.2.1.4 Calculate the Minimum Inductance Value

Where ΔI_{L-PP} is in Amperes. For example, a 1-A solution with 20% inductor ripple: set ΔI_{L-PP} = 0.2A

$$L = \frac{V_{LED} \text{ x } t_{OFF}}{\Delta I_{L-PP}} \quad (18)$$

When selecting the inductor, ensure the ratings for both peak and average current are adequate. Equation 19 calculates the peak inductor current.

$$IL_{PEAK=} \frac{\left[\frac{V_{IADJ}}{10}\right]}{R_{SENSE}} \quad (19)$$

9.2.1.5 Calculate the Sense Resistance

Always use the highest V_{IADJ} voltage the application allows without exceeding 5.5 V. The device clamps any higher value to a level 2.4 V. See also the *Analog Adjust Input* for details.

$$R_{SENSE} = \frac{\left[\frac{V_{IADJ}}{10}\right]}{I_{LED} + \frac{\left[\Delta I_{L-PP}\right]}{2}} \quad (20)$$

9.2.1.6 Calculate Input Capacitance

NOTE

Input voltage ripple (ΔV_{IN-PP}) must not exceed 10% of the input voltage (V_{IN}) or 2 V, whichever is lower.

For example, V_{IN} = 50 V, 50 x 0.1 = 5 V; the maximum ΔV_{IN-PP} remains 2 V.

$$C_{IN-MIN} = \frac{I_{LED} \text{ x } \left[\frac{1}{f_{SW}} - t_{OFF}\right]}{\Delta V_{IN-PP}} \quad (21)$$

9.2.1.7 Calculate Output Capacitance

Because current is being regulated and is continuous, no output capacitance is required to supply the load and maintain output voltage. This regulation helps when designing a high-frequency PWM dimming on the LED load. When no output capacitor is used, the same design calculations for ΔI_{L-PP} also apply to ΔI_{LED-PP}.

Typical Application (continued)

A capacitor placed in parallel with the LED load can be used to reduce ΔI_{LED-PP} while keeping the same average current through both the inductor and the LED load. With an output capacitor, the inductance can be lowered, making the magnetic smaller and less expensive. Alternatively, the circuit can be run at lower frequency with the same inductor value, improving the efficiency and increasing the maximum allowable average output voltage. A parallel output capacitor is also useful in applications where the inductor or input voltage tolerance is poor. Adding a capacitor that reduces ΔI_{LED-PP} to well below the target provides headroom for changes in inductance or V_{IN} that might otherwise push the maximum ΔI_{LED-PP} too high.

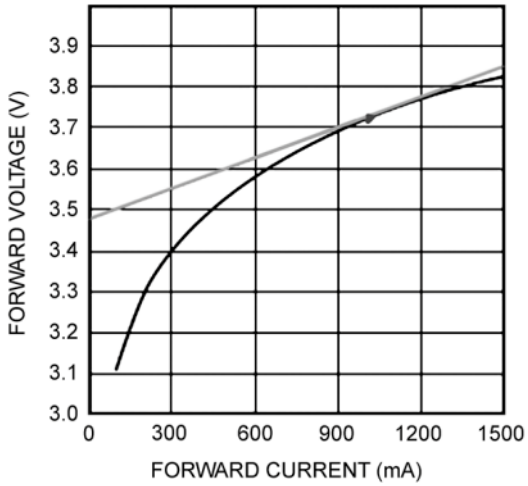


Figure 31. Calculating Dynamic Resistance r_D from LED Characteristics.

Determine the output capacitance by establishing the desired ΔI_{LED-PP} and the LED dynamic resistance, r_D. Calculate the dynamic resistance as the slope of the LED exponential DC characteristic at the nominal operating point as shown in Figure 31. Simply dividing the forward voltage by the forward current at the nominal operating point results in an incorrect value that is between 5 times and 10 times too high. Calculate total dynamic resistance for a string of n LEDs connected in series as the dynamic resistance of one device multiplied by n. Use Equation 22 and Equation 23 to estimate ΔI_{LED-PP} when using a parallel capacitor:

$$\Delta I_{LED-PP} = \frac{\Delta I_{L-PP}}{1 + \frac{r_D}{Z_C}} \quad \text{and} \quad Z_C = \frac{1}{2\pi f_{SW} C_O} \tag{22}$$

$$C_O = \frac{\left[\Delta I_{L-PP} - \Delta I_{LED-PP}\right]}{\Delta I_{LED-PP}\left[2\pi f_{SW}\right] r_D} \tag{23}$$

Typical Application (continued)

9.2.2 Design Requirements

Table 3 shows the design parameters for an example Buck LED driver application.

Table 3. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		30	65	65	V
V_{ULVO}	Input UVLO setting				29	V
$V_{UVLO-HYST}$	Input UVLO hysteresis			4		
OUTPUT CHARACTERISTICS						
V_{FLED}	LED forward voltage			3.14159		V
n	Number of LEDs in series			7		
V_{LED}	Output voltage	LED+ to LED–		22		V
I_{LED}	Output current			1000		mA
P_{MAX}	Maximum output power			22	25	W
SYSTEMS CHARACTERISTICS						
$\Delta I_{LEDpk-pk}$	LED current ripple			10%		
ΔI_{Lpk-pk}	Inductor current ripple			45%		
ΔV_{IN-PP}	Input voltage ripple			2		V
f_{SW}	Switching frequency			580		kHz

9.2.3 Detailed Design Procedure

This procedure describes the fundamental component selections for the design specifications noted in Equation 17.

9.2.3.1 Calculating Duty Cycle

Solve for D: $V_{OUT} = V_{LED}$. Assume a target efficiency of 90%. ($\eta = 0.9$)

$$D = \frac{V_{LED}}{V_{IN} \text{ x } n} = \frac{22}{65 \text{ x } 0.9} = 0.37 = 37\% \tag{24}$$

9.2.3.2 Calculate OFF-Time Estimate

Equation 25 uses the switching period T to derive the OFF-time (t_{OFF}) .

$$t_{OFF} = \frac{1}{f_{SW}} x\left[1-D\right] = \frac{1}{580kHz} x\left[1-.376\right] = 1.076\,\mu s$$

where

- $T = t_{OFF} + t_{ON}$
- $t_{OFF} + (D \text{ x } T)$, and $T = 1/f_{SW}$ (25)

9.2.3.3 Calculate OFF-Time Resistor R_{OFF}

Select a C_{OFF} between 100 pF and 1 nF. The preferred value is 470 pF. The EC table specifies the OFF-time threshold (V_{OFT}) at 1 V.

$$R_{OFF} = \frac{t_{OFF}}{-C_{OFF}\left[\ln\left[1-\frac{V_{OFT}}{V_{LED}}\right]\right]} = \frac{1.076\mu}{-470p\left[\ln\left[1-\frac{1}{22}\right]\right]} = 49212\Omega \tag{26}$$

9.2.3.4 Calculate the Inductance Value

this example uses a 1-A solution with 45% inductor ripple. Set $\Delta I_{L-PP} = 0.45A$

$$L = \frac{V_{LED} \text{ x } t_{OFF}}{\Delta I_{L-PP}} = \frac{22 \text{ x } 1.076\mu}{1.0 \text{ x } .45} = 52\mu H$$

where

- $\Delta I_{L\text{-}PP}$ is in A

(27)

When selecting an inductor ensure the ratings for both peak and average current are adequate. Typically an inductance value of at least the calculated value or higher would be selected. For example, most cases use 56 µH or 68 µH given the 52 µH calculation. However, in this example size and efficiency are a concern and the application allows for the use of an output capacitor. Because a value of 52 µH not close to any common values, and output capacitance is allowed, 47 µH is selected. 47 µH has a lower winding resistance (DCR) for the same case size.

9.2.3.5 Calculate the Sense Resistance

Always use the highest V_{IADJ} voltage that the application allows. Do not exceed 5.5 V. A value higher than 2.4 V is clamped to 2.4 V. Refer back to Analog Adjust Input for details.

$$R_{SENSE} = \frac{\left[\frac{V_{IADJ}}{10}\right]}{I_{LED} + \frac{\left[\Delta I_{L-PP}\right]}{2}} = \frac{\left[\frac{2.4}{10}\right]}{1.0 + \frac{\left[0.45\right]}{2}} = 0.196\Omega$$

(28)

9.2.3.6 Calculate Input Capacitance

NOTE

Inductor ripple current ($\Delta V_{IN\text{-}PP}$) must not exceed 10% of the input voltage (V_{IN}) or 2 V, whichever is lower.

For example, V_{IN} = 65 V, 65 x 0.1 = 6.5 V; the maximum $\Delta V_{IN\text{-}PP}$ remains 2 V.

$$C_{IN-MIN} \geq \frac{I_{LED} \text{ x } \left[\frac{1}{f_{SW}} - t_{OFF}\right]}{\Delta V_{IN-PP}} \geq \frac{1 \text{ x } \left[\frac{1}{580k} - 1.076\mu\right]}{2} \geq 324nF$$

(29)

9.2.3.7 Verify Peak Current for Inductor Selection

When selecting in inductor consider these three specifications.

- the required inductance
- the average current rating
- the peak current rating

Equation 30calculates the peak current rating

$$IL_{PEAK=} \frac{\left[\frac{V_{IADJ}}{10}\right]}{R_{SENSE}} = \frac{\left[\frac{2.4}{10}\right]}{.196\Omega} = 1.22A$$

(30)

9.2.3.8 Calculate Output Capacitance

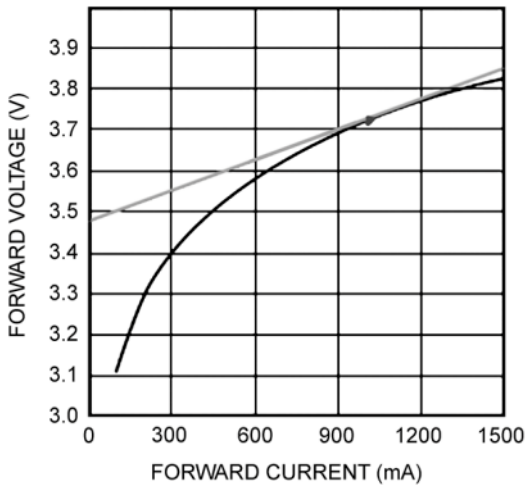


Figure 32. Calculating Dynamic Resistance r_D from LED Specifications

Solve for r_D, using the slope of the tangent line, then multiply by the number of LEDs.

$$r_D = \frac{3.83 - 3.63}{1.5 - 0.6} = .0222\Omega \text{ x } 7 = 1.55\Omega \quad (31)$$

Substitute the value of r_D with other parameters to solve for the required minimum output capacitor to meet the required LED ripple current level:

$$C_{O=} \frac{\left[\Delta I_{L-PP} - \Delta I_{LED-PP}\right]}{\Delta I_{LED-PP}\left[2\pi\ f_{SW}\right] r_D} = \frac{\left[0.45 - 0.15\right]}{0.15\left[2\pi\ 580k\right] 1.55} \geq 354\ nF \quad (32)$$

9.2.3.9 Calculate UVLO Resistance Values

Consider the rising threshold of VIN to be 29 V and the hysteresis to be 4 V, calculate R2 and R3 to create the desired operation:

$$R_3 = \frac{V_{HYST} - \left[0.1 \text{ x } V_{IN-RISE\_THRESHOLD}\right]}{20\mu A \text{ x } \left[V_{IN-RISE\_THRESHOLD} - 1\right]} = \frac{4 - \left[0.1 \text{ x } 29\right]}{20\mu A \text{ x } \left[29 - 1\right]} = 1964\Omega \quad (33)$$

$$R_2 = \left[V_{IN-RISE\_THRESHOLD} - 1\right] \text{x } R_3 = \left[29 - 1\right] \text{x } 1964 = 54.9k\Omega \quad (34)$$

The final schematic is shown in Figure 33 and performance curves in Application Curves:

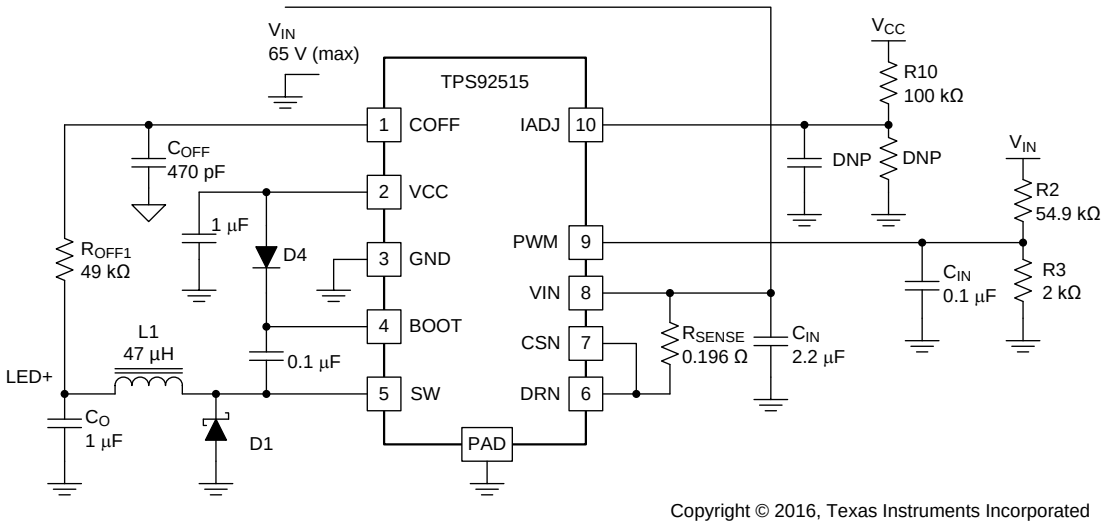
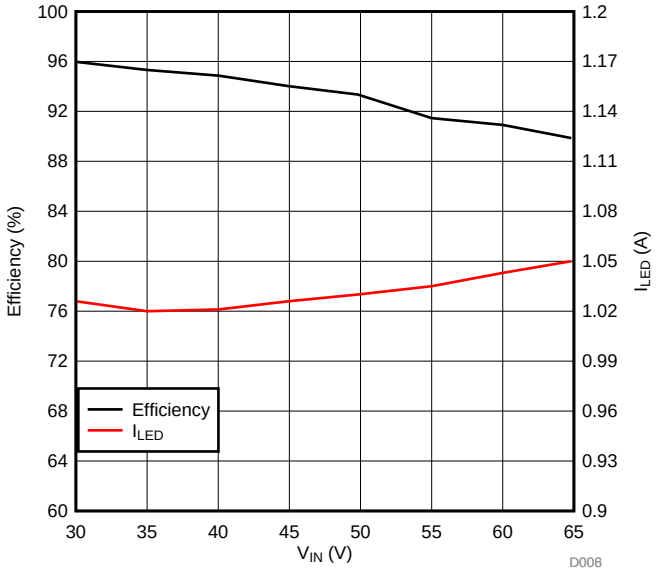


Figure 33. Application Schematic

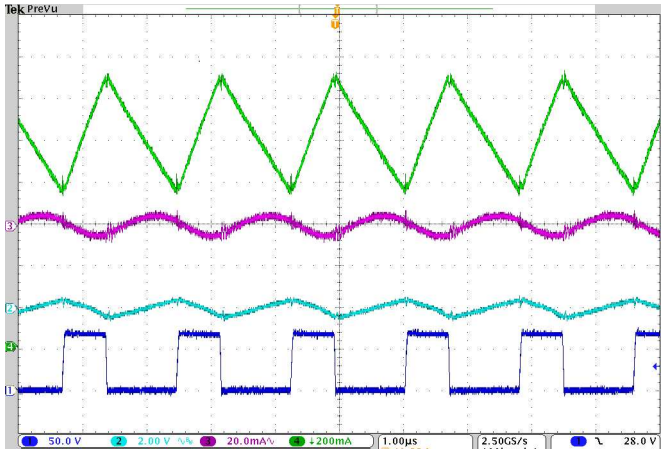
9.2.4 Application Curves

Buck LED driver example: V_{OUT} = 22 V (7 LEDs), I_{OUT} = 1 A



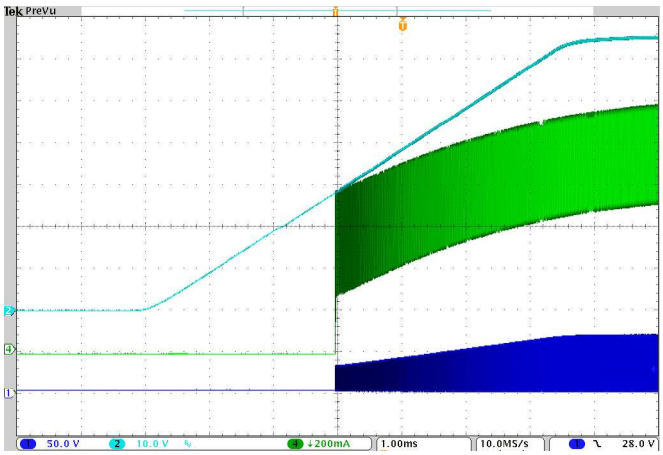
V_{LED} = 22 V I_{OUT} = 1.0 A

Figure 34. Efficiency and Output Current vs. Input Voltage



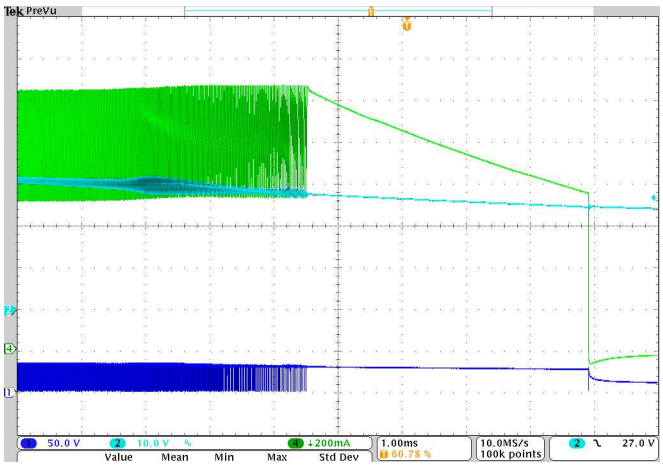
Ch1: SW Voltage; Ch2: VIN Ripple Voltage (AC Coupled);
Ch3: I_{LED-PP}; Ch4: Inductor current;
Time: 1 µs/div

Figure 35. Normal Operation



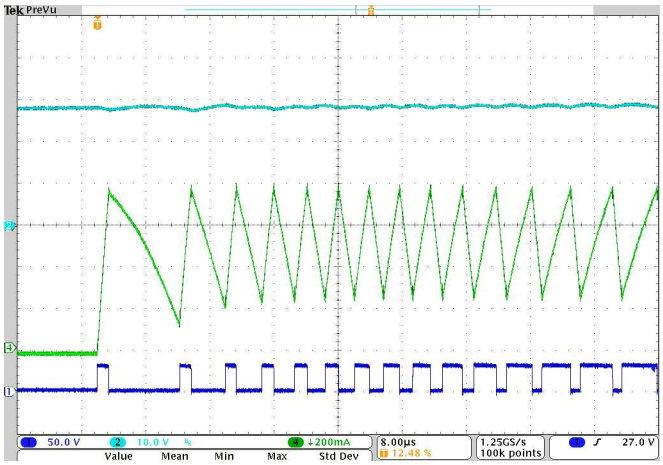
Ch1: SW Voltage; Ch2: VIN (DC Coupled);
Ch4: Inductor current; UVLO designed limit attained.
Time: 1 ms/div

Figure 36. Startup Transient



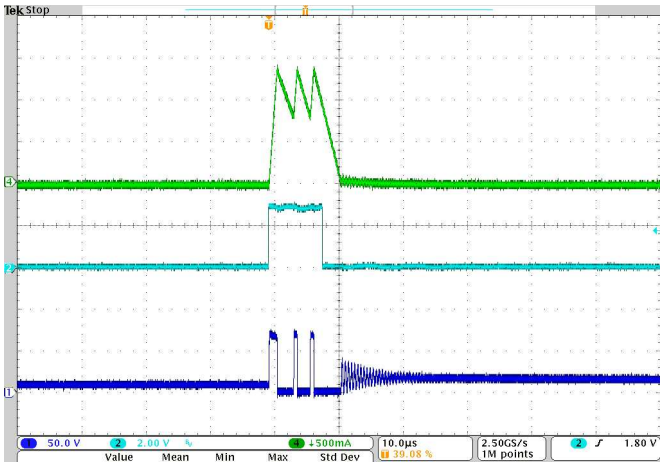
Ch1: SW Voltage; Ch2: VIN (DC Coupled);
Ch4: Inductor current; UVLO designed limit attained.
Time: 1 ms/div

Figure 37. Shut-Down Transient



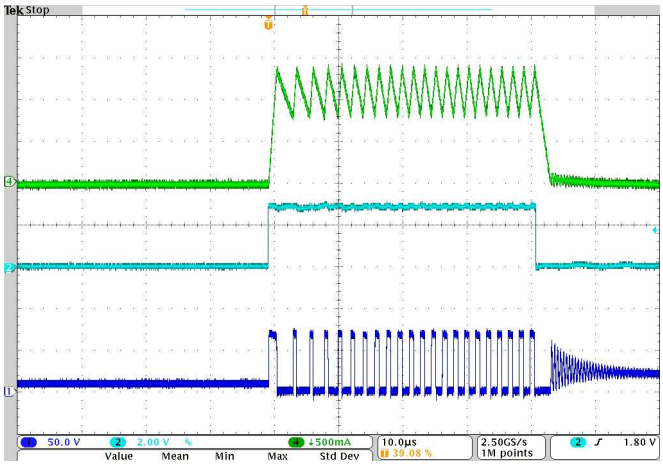
Ch1: SW Voltage; Ch2: VIN (DC Coupled);
Ch4: Inductor current;
Time: 8 µs/div

Figure 38. First 15 SW Node Pulses at Turn-On



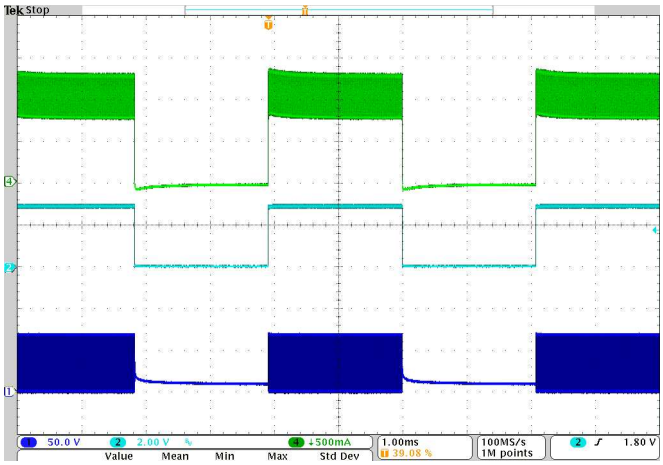
Ch1: SW Voltage; Ch2: PWM pin;
Ch4: Inductor current;
Time: 10 µs/div

Figure 39. PWM Dimming: 250Hz, 0.25% Duty Cycle



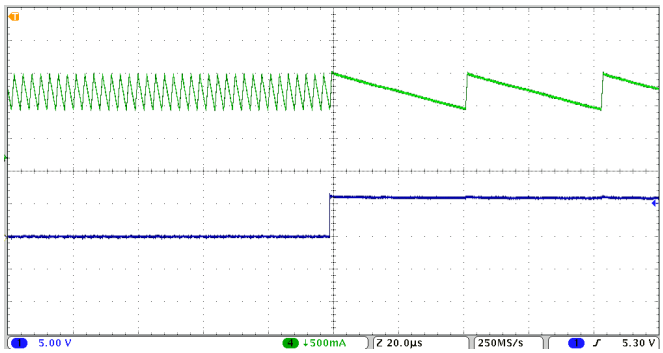
Ch1: SW Voltage; Ch2: PWM pin;
Ch4: Inductor current;
Time: 10 µs/div

Figure 40. PWM Dimming: 250Hz, 1% Duty Cycle



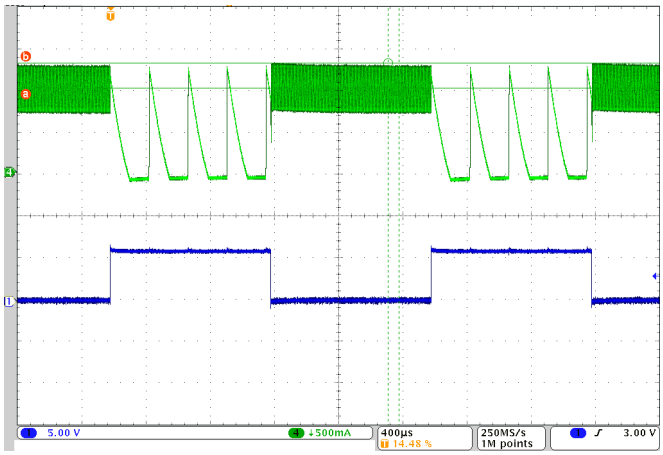
Ch1: SW Voltage; Ch2: PWM pin;
Ch4: Inductor current;
Time: 1 ms/div

Figure 41. PWM Dimming: 250Hz, 50% Duty Cycle



Ch1: PWM Signal
Ch4: Inductor current; $\Delta I_{L\text{-}PP}$ Maintained
Time: 20 µs/div

Figure 42. Shunt FET Dimming - Optimized Inductor Current Waveform



Ch1: PWM Signal
Ch4: Inductor current; OFF-time reaching Maximum OFF-Time
Time: 400 µs/div

Figure 43. Shunt FET Dimming - Non-Optimized Inductor Current

9.3 Dos and Don'ts

Dos	Don'ts
Check soldering of thermal pad in production	
Check device case and junction temperature during and after prototyping of any solution.	

10 Power Supply Recommendations

The TPS92515 was designed with the consideration of two main input source possibilities; direct from battery or from the output of a boost stage. For either application, ensure input voltage ripple requirements are met. The input ripple must go no higher than 10% of the input voltage to a maximum of 2 V.

10.1 Input Source Direct from Battery

Operation direct from battery has been considered when designing the TPS92515. The device ratings are such that load dump and other battery voltage excursions should not exceed the ratings of the device. When the battery voltage drops, the device's ability to run in to drop-out and various UVLO controls ensure a controlled recovery and no device damage. The BOOT UVLO protection allows duty cycles over 99%.

10.2 Input Source from a Boost Stage

The TPS92515 maximum input voltage of 65 V makes it a suitable second stage buck regulator for a variety of applications and LED output configurations. For an average LED forward voltage of 3.5 V, and allowing for some headroom below the 65-V maximum input, the TPS92515 can successfully control up to 17 LEDs connected in series.

11 Layout

11.1 Layout Guidelines

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines maximizes noise rejection and minimizes the generation of EMI within the circuit.

Figure 44 shows a sample layout and the associated current loops.

- Discontinuous currents are the type of current most likely to generate EMI, therefore care should be taken when routing these paths.
  - The main path for discontinuous current contains the input capacitor (C_{IN}), the recirculating diode (D1), the internal MOSFET (DRN pin to SW pin), and the sense resistor (R_{SENSE}) shown as LOOP2. Make LOOP2 as small as possible.
  - Make the connections between all three components short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and the SW pin connect, shown as LOOP1) should be only large enough to connect the components without excessive heating from the current it carries.
- The IADJ, COFF, CSN and VIN pins are all high-impedance control inputs, therefore minimize the loops containing these high impedance nodes. The most sensitive loop contains the sense resistor (R_{SENSE}) Place the sense resistor as close as possible to the CSN and VIN pins to maximize noise rejection.
- Place the OFF-time capacitor (connected from the COFF pin to ground) close to the COFF and GND pins to maximize noise rejection.
- If external resistors are used to bias the IADJ pin, they should also be placed close to the IADJ and GND pins and could be decoupled with a small capacitor.
- In some applications the LED load can be far away (several inches or more) from the device, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED load is large or separated from the main converter, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

11.2 Layout Example

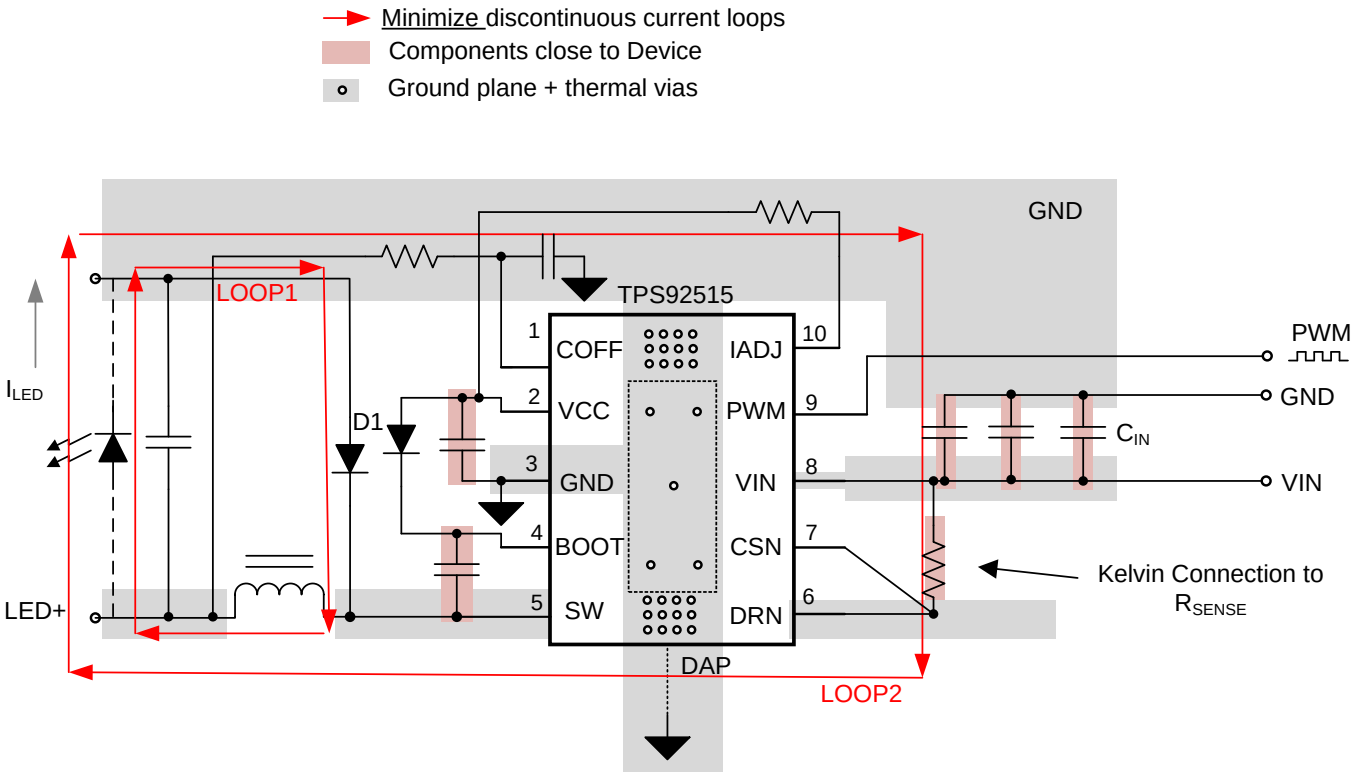


Figure 44. TPS92515 Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

12.1.1.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS92515	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS92515-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS92515HV	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS92515HV-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92515DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15NX	Samples
TPS92515DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15NX	Samples
TPS92515HVDGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15PX	Samples
TPS92515HVDGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15PX	Samples
TPS92515HVQDGQRQ1	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15QX	Samples
TPS92515HVQDGQTQ1	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15QX	Samples
TPS92515QDGQRQ1	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15OX	Samples
TPS92515QDGQTQ1	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15OX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

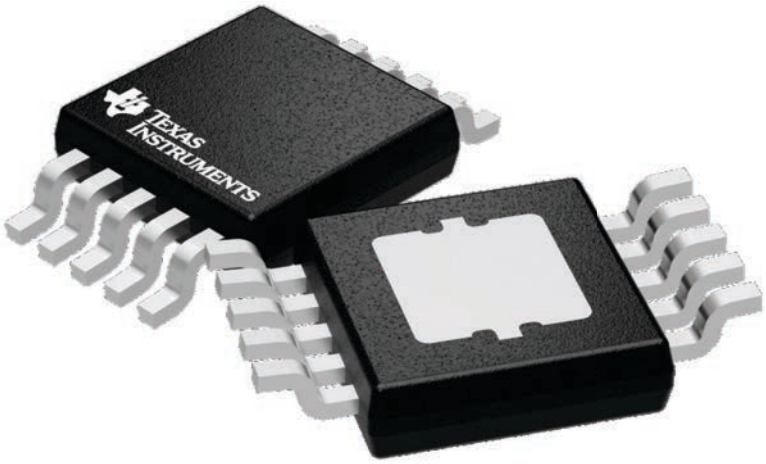
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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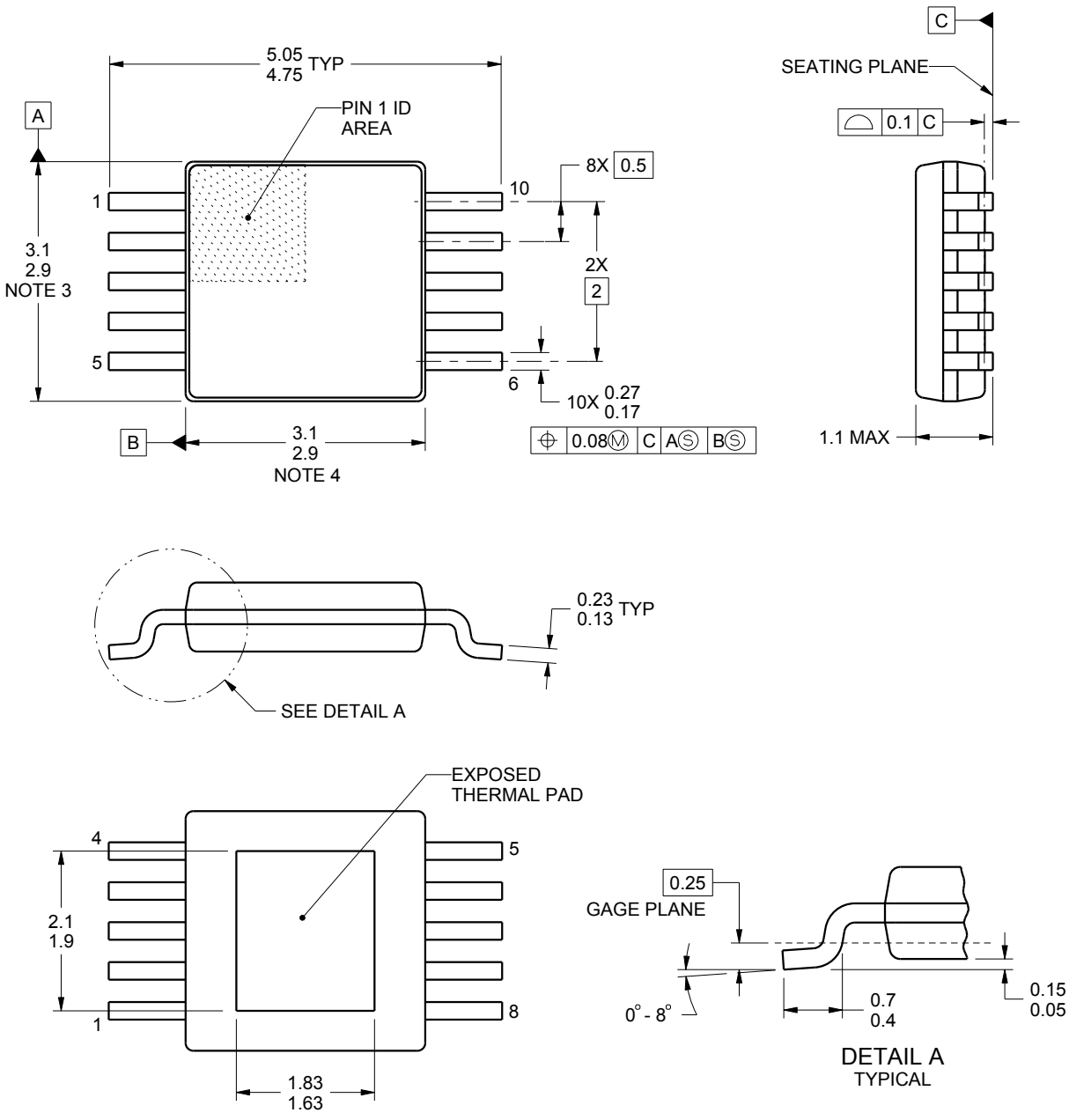
PACKAGE OUTLINE

DGQ0010E

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



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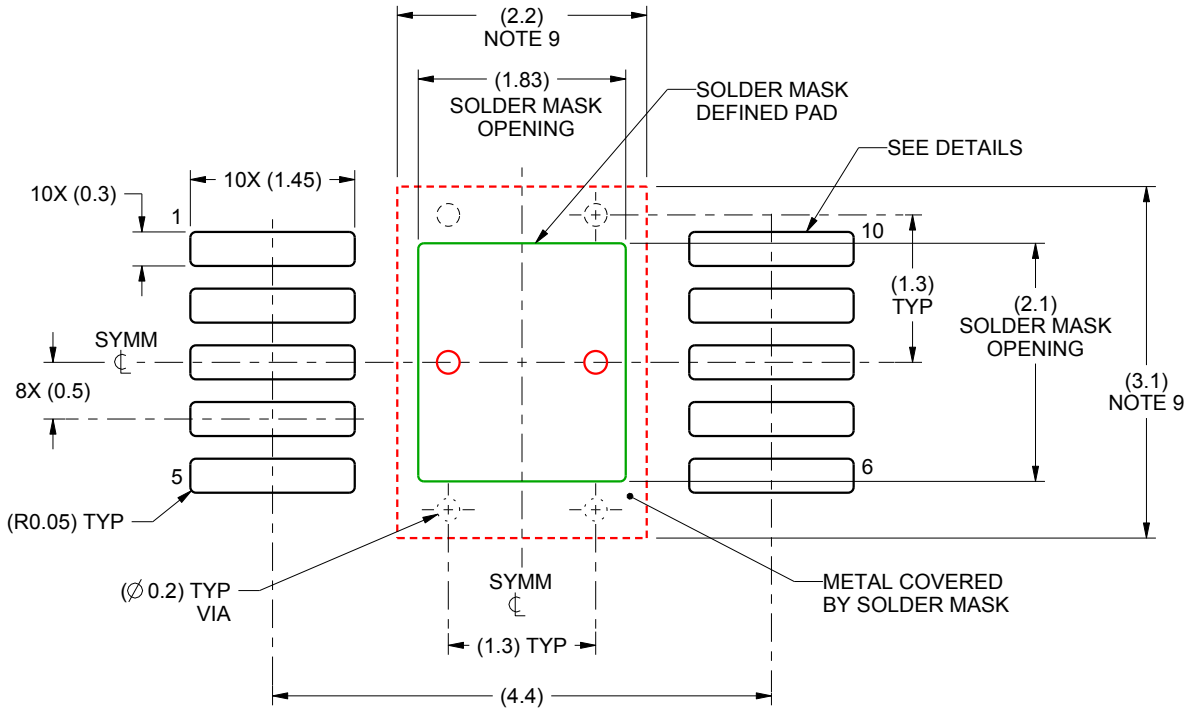
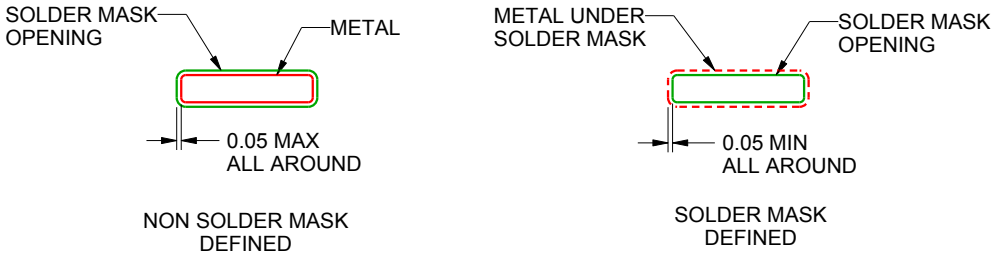
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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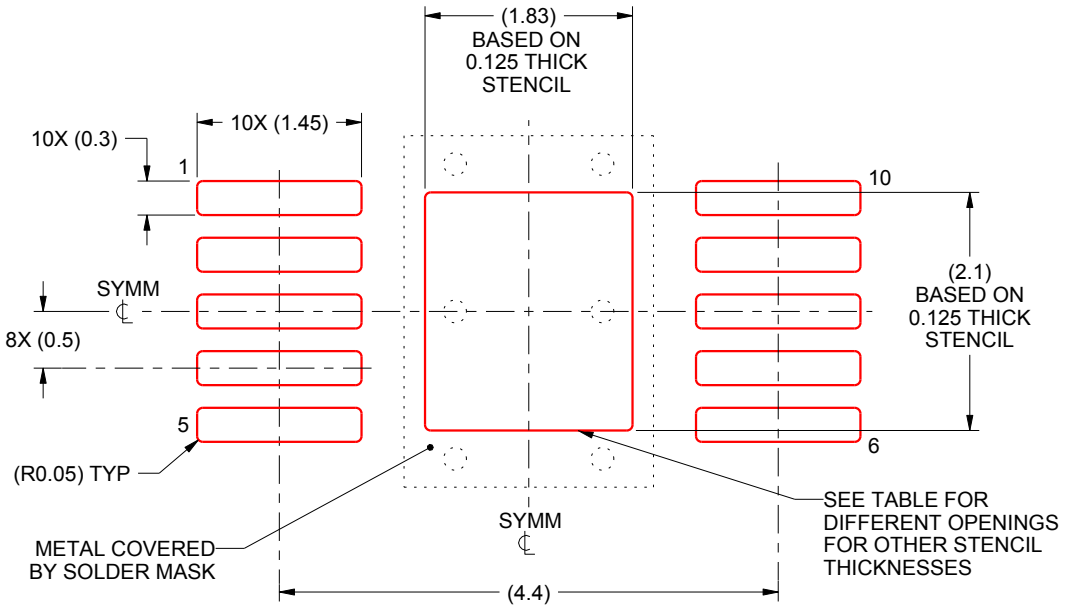
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.35
0.125	1.83 X 2.1 (SHOWN)
0.150	1.67 X 1.92
0.175	1.55 X 1.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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>>TI(德州仪器)